Neoway 有方

Neo_M660 GPRS Module Hardware User Guide

Version 3.4



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V3.1	Modified the sensitivity indicator.	2013-11
V3.2	Modified the open resources and block diagram	2013-11
V3.3	 Updated the logo of neoway Added the description about storage temperature Modified the description of the model 	2014-02
V3.4	 Simplified the description of power-on procedure Modified the requirements of digital IO input 	2014-04

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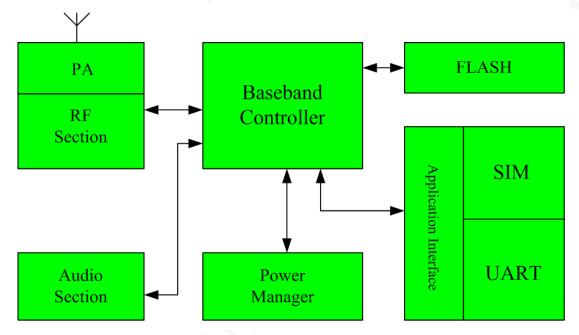
1 Overview

M660 is a compact wireless GSM/GPRS module that supports downlink EDGE. It can provide functions of high-quality voice, SMS, and data services and is widely used in industrial and civil fields.

This document defines the features, indicators, and test standards of the M660 module and provides reference for the hardware design of each interface.

2 Block Diagram

The M660 module consists of baseband controller, Flash ROM, RF section, application interfaces, etc. All sections coordinate with each other to provide such communication functions as GPRS data and voice.



3 Specifications

Table 3-1 M660 specifications

Specifications	Description	
Frequency	GSM850/900/1800/1900 MHz/quad-band	
Sensitivity	<-106dBm	
Transmit power	850/900 Class4(2W)	
	1800/1900 Class1(1W)	
Protocol	Compatible with GSM/GPRS Phase 2/2+	
AT	GSM07.07	
	Extended AT commands	
Audio	FR, EFR, HR, AMR	
SMS	TEXT/PDU	
	Point-to-point/cell broadcast	
Packet data	GPRS CLASS 12	
Circuit Switch Data	CSD data service	
	USSD	

Supplementary service	Call forwarding (CFB, CFNA, CFU)	
	Call waiting	
	Three-way calling	
CPU	ARM7-EJ@260MHz, 32MB SRAM,16 to 32MB Nor Flash	
Operating temperature	-40°C to +85°C	
Storage temperature	-40°C to +85°C	
Operating voltage	3.5 V to 4.3 V (3.9 V is recommended)	
Peak current	Max 1.8A	
Operating current	< 250 mA	
Current in sleep mode	< 2.2 mA	

4 Model, Encapsulation and Pins

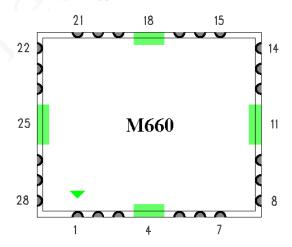
4.1 Model

Model	Function	Frequency
M660	850/900/1800/1900MHz, standard module	Quad-frequency

4.2 Specifications and Encapsulation

Specifications	M660
Dimensions	22 mm x 18.4 mm x 2.7 mm (H x W x D)
Weight	2.2 g
Packaging	28-pin LCC

Figure 4-1 Appearance of the M660 module



The maximum input voltage at all IO ports (including peak signal current) cannot exceed 3.1 V because the module uses a 2.8 V IO power system. In the application of the module, the IO output voltage from the 3.3 V power supply system of the external circuit might greatly overshoot 3.1 V due to the signal integrity design. In this situation, the IO pins of the module might be damaged if the IO signals are connected to the

IO port on the 2.8-V system. To rectify this issue, take measures to match the level. For details, see the Section 5.2.



The level at the interfaces of the M660 module is 2.8 V.

4.3 Pin Definition

Table 4-1 M660 pin definition

Pin	Signal	I/O	Function	Remarks
1	VSIM		SIMpower supply	1.8/3.0V compatible.
2	SIM_CLK	DO	SIM clock output	
3	SIM_DATA	DIO	SIM data I/O	5KΩ internal pull-up
4	GND	PWR	GND	
5	SIM_RST	DO	SIM reset output	
6	MICP	ΑI	MIC+	Vi≤200mVpp
7	MICN	AI	MIC-	Vi≤200mVpp
8	EAR-L	AO	Earpiece output L	Signal Ended Output. Can drive a $16\Omega/32\Omega$ earpiece directly.
9	EAR-R	AO	Earpiece output R	Signal Ended Output. Can drive a $16\Omega/32\Omega$ earpiece directly.
10	DTR	DI	Data Terminal Ready	Can be used to control sleep mode.
11	GND	PWR	GND	
12	RING	DO	Incoming call or SMSRING indicator	Can be used to indicate an incoming voice call or SMS.
13	VCCIO	PWR	2.8V power output	Can be used to power the level translators. Imax=5mA
14	Reserved		Reserved	
15	Reserved		Reserved	
16	URXD	DI	Serial data input of module	V.24: TXD
17	UTXD	DO	Serial data output of module	V.24: RXD
18	GND	PWR	GND	
19	RESET	DI	Reset input	Active low >60mS
20	BACK_LIG	DO	Status LED	2.8V/4mA output
	HT			High level can drive a LED directly
21	ON/OFF	DI	Switch the module on/off	Low level pulse triggered
22	ANT	I/O	Antenna interface	A 50ohm antenna expected
23	GND	PWR	GND	
24	Reserved		Reserved	
25	GND	PWR	GND	
26	VBAT	PWR	Main power supply	3.5V~4.3V (typical 3.9V)
27	VBAT	PWR	Main power supply	
28	GND	PWR	GND	



PWR: indicates power supply pins Reserved: indicates reserved pins DI: indicates digital signal input pins

DO: indicates digital signal output pins

AI: indicates analogy signal input pins

AO: indicates analogy signal output pins

4.4 PCB Foot Print

LCC packaging is adopted to package the pins of the M660 module. Figure 4-2 shows the recommended PCB foot print. (unit: mm)

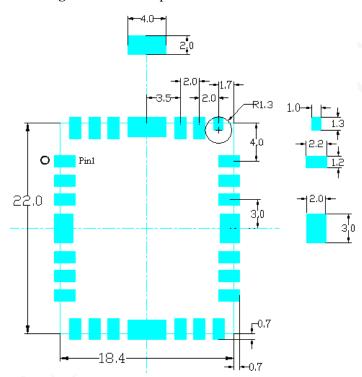


Figure 4-2 PCB foot print recommended for M660



CAUTION

- Every other pitch not specified is 2.0mm.
- The circle on the top-right with a 1.0mm radius, defines a keep-out region, under which any copper or wire is inhibited, due to the RF test point here needs to be surrounded by restricted area filled with air.
- There may be some masks on the bottom of the module PCB, created by hollowing the solder resist layer, causing reveal of copper. To avoid short circuits, it is recommended to cover the application PCB with a silkscreen block at the area under the module, but excluding soldering area. For details about the layout requirements, see 5.7 RF Interface and PCB Layout

5 Interface Design

5.1 Power Supply and Switch Interface

I/O Signal **Function** Remarks VCCIO **PWR** 2.8 V power supply output Loading capability < 50 mA Reset at low level RESET DI Module reset input ON/OFF DI On/Off input Low level pulse can change the On/Off state. **PWR** Main power supply input **VBAT** 3.5 V to 4.3 V (3.9 recommended)

Table 5-1 Power supply and switch interface

5.1.1 Design Requirements

VBAT is the main power supply of the module. Its input voltage ranges from 3.5 V to 4.3 V and the preferable value is 3.9V.In addition to digital signals and analog signals, it supplies power for RF power amplifier.

The performance of the VBAT power supply is a critical path to module's performance and stability. The peak input current at the VBAT pin can be up to 1.8A. Therefore, a large bypass tantalum capacitor or aluminum capacitor is expected to reduce voltage drops during bursts. Meanwhile, the power supply should not have great internal resistance and should ensure the rated 1.5A current.

It is recommended that you add 0.1 uF, 100 pF, and 33 pF filter capacitors to enhance the stability of the power supply. Figure 5-1shows how the capacitors help to improve the peak current performance.

Current test point Power VBAT **GPRS** source I_max module C2 C1 C3 C1 I_max 10 uF 1.8 A 100 uF 1.1 A Close to module 470 uF A8.0 C2: filters common digital noise 1000 uF 0.6AC3: filters RF noise

Figure 5-1 Capacitors used for the power supply

Results may vary depending on the ESR of capacitors, and the impedance of power source. A low ESR 1000 uF aluminum capacitor can be selected for C1. As an alternative, a 470 uF tantalum capacitor is also suit. In case of Li-ion cell battery used, 220uF or even 100uF tantalum capacitor may be applicable because of the battery's low internal impedance and the ability to provide high transient current.

Figure 5-2 shows how the GSM bursts and voltage drops.

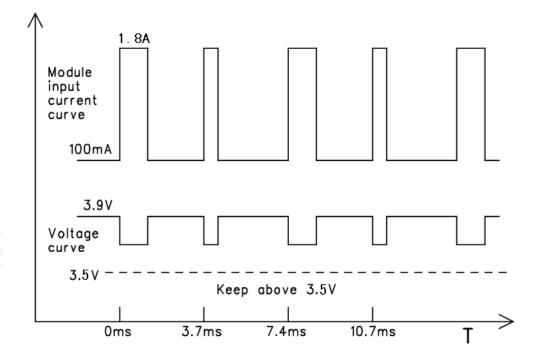


Figure 5-2 Current peaks and voltage drops

For the VBAT design, you must ensure that the voltage is not lower than 3.5 V during the operating, otherwise the module cannot work properly. The voltage should not exceed 4.3 V. Otherwise the

over-voltage can even damage the module permanently. You need to provide protection for the main power supply of the module in case of over-voltage.

A controllable power supply is preferable if used in harsh conditions. The module might fail to reset in remote or unattended applications, or in an environment with great electromagnetic interference (EMI). You can use the enable pin on the LDO or DC/DC chipset to control the switch of the power supply as shown in Figure 5-3.

MIC29302 in the following figure is an LDO.

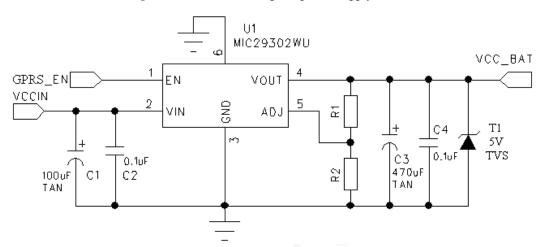


Figure 5-3 Reference design of power supply control

The alternative way is to use a p-MOSFET to control the module's power, as shown in Figure 5-4. When the external MCU detects the exceptions such as no response from the module or the disconnection of GPRS, power off/on can rectify the module exceptions.In Figure 5-4, the module is powered on when GPRS_EN is set to high level.

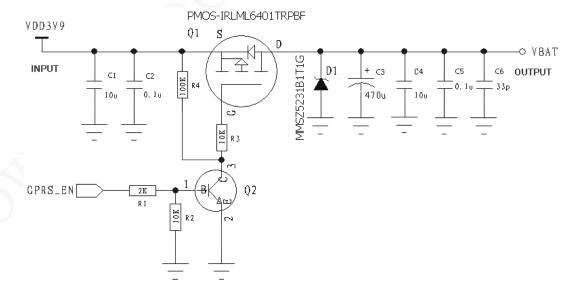


Figure 5-4 Reference design of power supply controlled by p-MOSFET

NOTE

Q2 is added to eliminate the need for a high enough voltage level of the host GPIO. In case that the GPIO can output a high voltage greater than VDD3V9 - $|V_{GS(th)}|$, where $V_{GS(th)}$ is the Gate Threshold Voltage, Q2 is not needed.

Reference components:

- Q1 can be IRML6401 or Rds(on) p-MOSFET which has higher withstand voltage and drain current.
- Q2: a common NPN transistor, e.g. MMBT3904; or a digital NPN transistor, e.g. DTC123.If digital transistor is used, delete R1 and R2.
- C4: 470 uF tantalum capacitor rated at 6.3V; or 1000 uF aluminum capacitor. If lithium battery is used to supply power, C4 can be 220 uF tantalum capacitor.

Power Supply Protection

It is strongly recommended that you addzener diodes for the VBAT power supply to decrease the power supply overshoot. MMSZ5231B1T1G from ONSEMI and PZ3D4V2 from Prisemi are options.

Trace

The trace width of primary loop lines for VBAT on PCB must be able to support the safe transmission of 2A current and ensure no obvious loop voltage decrease. Therefore, the trace width of VBATloop line is required 2 mm and the ground level should be as complete as possible.

Power Separating

As shown in Figure 5-2, the GPRS device works in burst mode that generates voltage drops on power supply. And furthermore this results in a 217Hz TDD noise through power (One of the way generating noise. Another way is through RF radiation). Analog parts, especially the audio circuits, are subjected to this noise, known as a "buzz noise" in GSM systems. To prevent other parts from being affected, it's better to use separated power supplies. The module shall be supplied by an independent power, like a DC/DC or LDO. See Figure 5-5.

DC/DC or LDO should output rated peak current larger than 1.5 A.

Reference design (a)

The inductor used in Reference Design (b), should be a power inductor and have a very low resistance. The value of 10 uH, with average current ability greater than 1.2A and low DC resistance, is recommended.

Other Other C-DC/LDC DC-DC/LDC circuits circuits Power Power input input 10uH GPRS GPRS DC-DC/LDC Module Module

Figure 5-5 Reference designs of separated power supply

Reference design (b)



CAUTION

Never use a diode to make the drop voltage between a higher input and module power. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, due to the forward voltage of diode will vary greatly in different temperature and current.

EMC Considerations for Power Supply

Place transient overvoltage protection components like TVS diode on power supply, to absorb the power surges. SMAJ5.0A/C could be a choice.

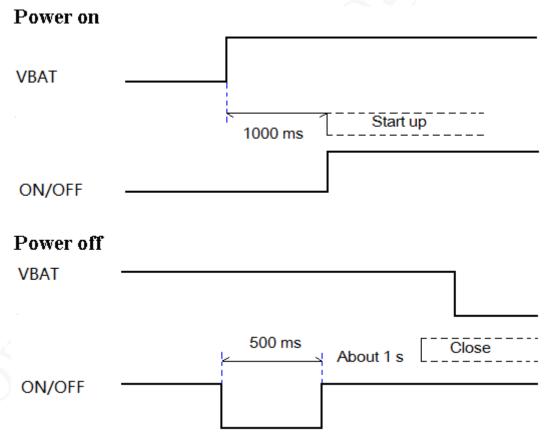
5.1.2 Power on Procedure

Prior to turning on the module, power on the host MCU and complete the UART initialization. Otherwise conflictions may occur during initialization, due to unstable conditions.

5.1.3 ON/OFF Procedure

ON/OFF is a low level pulse active input, used to turn on or off the module.

Figure 5-6 Turning on/off the module using ON/OFF



Turning on the Module

While the module is off, drive the ON/OFF pin to ground for at least **1 second** and then release, the module will start. An unsolicited message (+EIND: 1) will be sent to host through UART port, indicating that the module is powered on and can respond to the AT commands.

When you design your program, you can use the unsolicited message +EIND: 1 to check whether the module is started and +EIND: 128 to check whether the module is reset properly.

It's recommended that you drive the ON/OFF pin to low before supplying power toVBAT. One second later after the VBATis supplied power, release the ON/OFF pin. Then the module starts up. After the module is operating, keep ON/OFF being high level.

Turning off the Module

While the module is on, drive the ON/OFF pin to low level for at least 1 second and then release, the module will try to detach to network and normally 2 seconds later it will shut down. Another approach to turn off the module is using AT commands.

Figure 5-7 shows a reference circuit for ON/OFF control with inverted control logic.

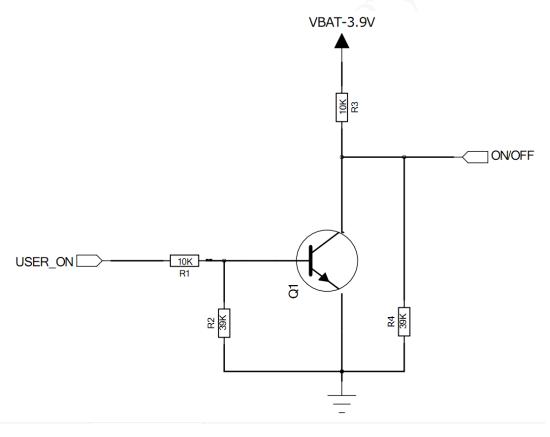


Figure 5-7 Reference circuit for ON/OFF control

In the above figure, high level takes effect for ON/OFF on the user side (USER_ON).

R1 and R2 can be adjusted according to the driving capability of the USER_ON pin.

Q1: a common NPN transistor, e.g. MMBT3904; or a digital NPN transistor, e.g. DTC123.If digital transistor is used, delete R1 and R2.The combination of R3 and R4 should limit the high voltage of ON/OFF less than 3.1 V.



CAUTION

- Level abnormalities at interfaces connected to the external MCU, especially the UART port, might affect the power on procedure of the module. For example, when a module is turned on, the IO ports of the MCU are still in output status because they have not been initialized completely. The module might fails to start if the UTXD signal (output pin) is forced to pull up or down.
- Some abnormal status on IO ports might affect the power-on of the module if there is input voltage on IO ports before turning on the module.
- The better way to rescue the module from abnormal condition, is to apply a power OFF-ON procedure, rather than using the ON/OFF control signal. In fact ON/OFF signal is software-dependent.

5.1.4 RESET

Pull the RESET signal to low level for more than 100 ms to reset the module. A pull-up resistor is internally included. Reset pin can be left disconnected if not used.

5.1.5 VCCIO

It is recommended that VCCIO is only used for interface level transformation. VMC can output 2.8 V and 50 mA. It stops output after the module is shut down.

5.2 UART

Table 5-2 UART

Signal	I/O	Function Description	Remarks
URXD	DI	UART data receive	
UTXD	DO	UART data transmit	

UART is used for AT commands, data sending/receiving, firmware updating, etc.

Figure 5-8shows the signal connection between the module (DCE) and the terminal (DTE).

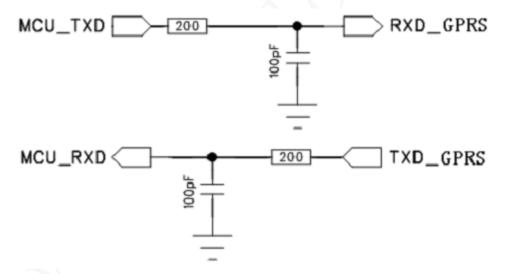
DCE TXD TXD RXD

Figure 5-8 Signal connection between DCE and DTE

The UART of M660works at **2.8 V**CMOS logic level. The voltages for input high level should **not** exceed 3.1 V. Supported baud rates are 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 bit/s, and the default rate is **115200 bit/s**.

If the UART is interfacing with a MCU that has 3.3V logic levels, 200 Ω or 330 Ω resistors should be connected in series with the signals.

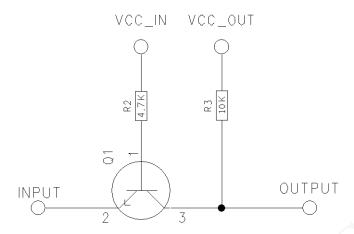
Figure 5-9 Recommended circuit for the communication between 3.3V MCU and UART



In Figure 5-9, 100 pF or 220 pF filter capacitor should be placed near the receive pin of the module. Resistance ($200\,\Omega$ to $470\,\Omega$) and capacity ($100\,\mathrm{pF}$ to $470\,\mathrm{pF}$) can be selected based on the tested signal wave. Great serial resistance and filter capacity will decrease the signal level, resulting in great signal wave distortion and the low adaptable UART communication baudrate.

When the external device IO voltage is 5 V, level transformation is required for both UART receive and transmit. Figure 5-10shows a reference circuit.

Figure 5-10 Recommended circuit for the communication between 5V MCU and UART



INPUT is connected to Transmit of the MCU and VCC_IN is connected to the 5 V power supply of the external device. OUTPUT is connected to Receive of the module and VCC_OUT is connected to VCCIOof the module (2.8 V).

The pull-up resistor R3 ranges from 4.7 K to 10 K; R2 ranges from 2 K to 10 K.Resistors are selected based on the voltage of the power supply and UARTbaudrate. You can select resistors with great resistance to reduce the power supply when the power supply has great voltage or the baudrate is low. But, the resistance will affect the quality of the square wave. In addition, the circuit performance is affected by the signal traces during PCB layout.

It is recommended that you choose a high-speed NPN transistor because the Q1 switch rate will affect the wave quality after transformation. For example, MMBT3904, or MMBT2222.



CAUTION

Avoid data produced at UART when the module is turned on. You are advised to send data to the UART2 seconds after the module is turned on so that the module would not respond wrongly.

5.3 DTR and RING

Table 5-3 DTR and RING pins

Signal	I/O	Function	Remarks
DTR	DI	Signal for controlling sleep mode	
RING	DO	Ring output	

5.3.1 DTR Pin

Generally DTR is used for sleep mode control. For details, see *M660AT Commands Set*.Based on the setting of the selected mode, pulling DTR low will bring the module into relevant power saving mode. Working in this mode, the power consumption is around 2 mA, depending on the DRX setting of network.

In sleep mode, the module can also respond to the incoming call, SMS, and GPRS data. The host MCU can also control the module to exit sleep mode by controlling DTR.

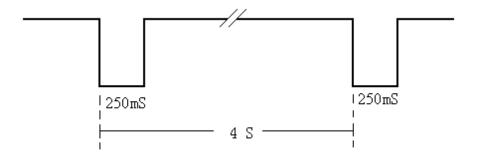
Process of entering the sleep mode:

- 1. Keep DTR high in normal working mode. Activate the sleep mode by using the AT command.
- 2. Pull DTR low, and the module will enter sleep mode, but only after process and pending data are finished.
- In sleep mode, the module can be woken up by the events of incoming voice call, received data, or SMS. Meanwhile the module will send out the unsolicited messages by the interface of RING orUART.
 - Upon receipt of the unsolicited messages, the host MCU should pull DTR high firstly, otherwise the module will resume sleep mode shortly. And then the host MCU can process the voice call, received data, or SMS. After processing is finished, pull DTR low again to put the module into sleep mode.
- 4. Pull DTR high, the module will exit from sleep mode actively, and furthermore enable the UART. Thus the voice call, received data, or SMS can be processed through UART. After processing finished pull it low again, to take the module back to sleep mode.

5.3.2 RING Signal Indicator

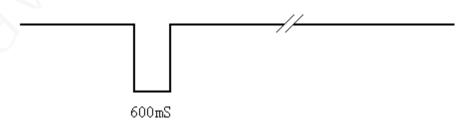
• Calling: Once a voice call is coming, UART output "ring" character strings and meanwhile the RING pin outputs 250 ms low pulses at 4seconds period. After the call is answered, the high level restores.

Figure 5-11 RING indicator for incoming call



• SMS: Upon receipt of SMS, the module outputs one 600mS low pulse.

Figure 5-12 RING indicator for SMS

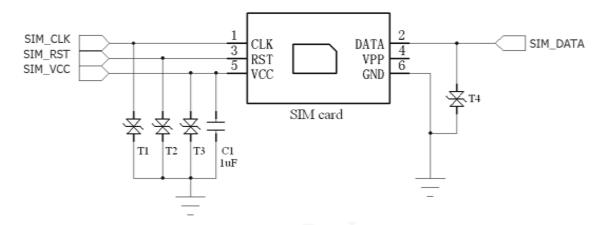


5.4 SIM Card Interface

Signal I/O **Function Description** Remarks VSIM **PWR** SIM card power supply output 1.8/3.0V SIM CLK DO SIM card clock output SIM_RST DO SIM card reset output SIM_DATA SIM card data IO DIO Internal pull up

Table 5-4 SIM Card Interface

Figure 5-13 Reference design of SIM card interface



M660 supports 3.0 V and 1.8 V SIM cards. VSIM supplies power for SIM card with 30mA.

SIM_DATA is internally pulled up with a 5Kresistor. External pull-up resistor is not needed.

SIM_CLK can work at several frequencies and at hundreds KHz to several MHz.

ESD protectors, such as ESD diodes or ESDVaristors, are recommended on the SIM signals, especially in applications with badly ESD. The total equivalent capacitance on any SIM signal, include the junction capacitance of the ESD diode and the distributed capacitance of PCB trace cannot be higher than 100pF.

If the SIM card is installed in a closed case without human touch or ESD, 22~33pFMLCC capacitors can replace the ESD diodes for cost down.

SIM card is sensitive to GSMTDD noise and RF interference. So, the PCB design should meet the following requirements:

- The antenna should be installed a long distance away from the SIM card and SIM card traces, especially to the build-in antenna.
- The PCB traces of SIM should be as short as possible and shielded with GND copper.



CAUTION

Small capacitors and the junction capacitance of the ESD diode are to avoid the interference from/to antenna, ensuring the correct SIM access and good RF performance.

5.5 Running LED Indicator

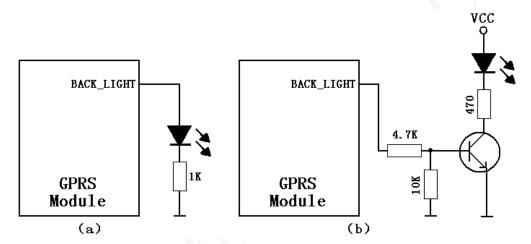
Table 5-5 LED indicator

Signal	I/O	Function	Remarks
BACK_LIGHT	DO	Indicates running status	High level drives the LED indicator

When the module is running, the LED indicator is driven by the BACK_LIGHT to indicate different module status with its various blink behaviors.

It can output a 4 mA current and 2.8 V voltage, therefore the LED can be directly connected to this pin with a resistor in series. For better luminance, drive the LED with a transistor instead.

Figure 5-14 LED indicator



5.6 Audio Interface

Table 5-6 Audio interface

Signal	I/O	Function	Remarks
MICP	AI	MIC+ input	$Vpp \le 200mV$
MICN	AI	MIC- input	$Vpp \le 200mV$
EAR-L	AO	Earpiece output L	Can drive a $16\Omega/32\Omega$ earpiece directly
EAR-R	AO	Earpiece output R	Can drive a $16\Omega/32\Omega$ earpiece directly

Figure 5-17 shows a reference audio interface. The peak voltage routed to MICP/MICN should not exceed 200 mV AC. The module can meet the requirements of common handsets with AGC and volume control.

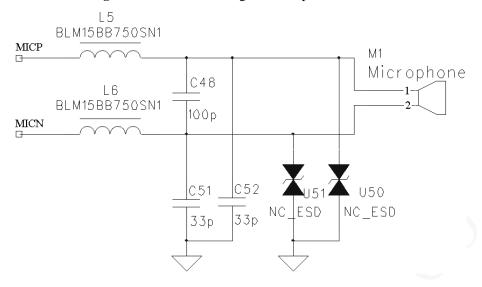


Figure 5-15 Reference design of microphone interface

In Figure 5-16, a bias voltage for microphone is provided through MICP and MICN.But if an amplifier is used between the microphone and module, capacitors like C1 and C2, should be placed between the outputs of amplifier and module, to block the bias voltage.

For a peak voltage greater than 200 mV AC, an attenuation circuit comprised of R1-R4 should be used.

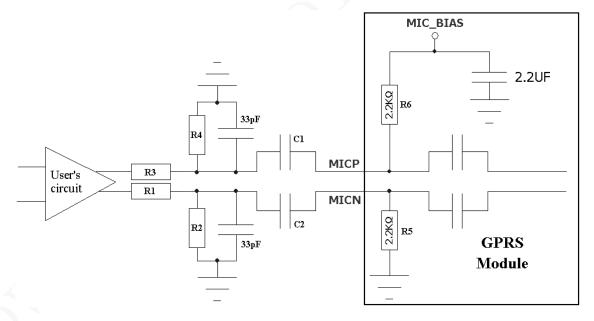


Figure 5-16 Reference design for MIC interface

In Figure 5-15 and Figure 5-16, the audio input circuits are designed to meet the requirements for small audio signal, far away from interference source and masking PCB routing by ground.

BLM18BD252SN1

BLM18BD252SN1

BLM18BD252SN1

BLM18BD252SN1

Figure 5-17 Reference design for earphone output

Figure 5-17 shows a reference design for the earphone interface, through which a $16/32 \Omega$ earphone can be driven directly. You are advised to use large capacitors for C1 and C2 to ensure the low frequency response of the audio signals.

If an external amplifier is used for driving the speakers, coupling capacitors of 1 uF to 4.7 uF should be used to block the DC voltage, as shown in Figure 5-18.

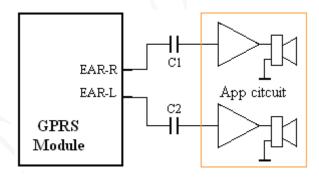


Figure 5-18 Coupling capacitor interfacing

You can remove the ESD diode or resistor in the above figures if microphone, earphone, or speaker is installed inside the product shell, they are far away pickup hole in structure, or there is no pickup hole.

5.7 RF Interface and PCB Layout

A 50 Ω antenna is required. VSWR< 1.5. The antenna should be well matched to achieve best performance. It should be installed far away from high speed logic circuits, DC/DC power, or any other strong disturbing sources.

ESD protection is built in module. For special ESD protection, anESD diode can be placed close to the antenna. But ensure to use a low junction capacitance one. The junction capacitance should be less than 0.5 pF, otherwise the RF signal will be attenuated. RCLAMP0521P from Semtech, or ESD5V3U1U from Infineon, can be used here. SeeFigure 5-19.

The trace between the antenna pad of module and the antenna connector, should have a 50 Ω characteristic impedance, and be as short as possible. The trace should be surrounded by ground copper. Place plenty of holes to connect this ground copper to main ground plane, at the copper edge.

If the trace between the module and connector has to be longer, or built-in antenna is used, a π -type matching circuit should be needed, as shown in Figure 5-19. The types and values of C1, L1, and L2 should be verified by testing using network analyzer instrument. If the characteristic impedance is well matched, and VSWR requirement is met, just use a 50 Ω resistor for C1 and leave L1, L2 un-installed.

Avoid any other traces crossing the antenna trace on neighboring layer.

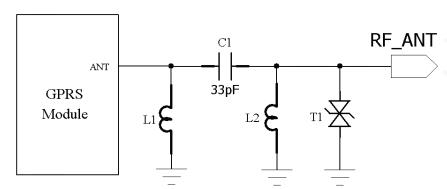


Figure 5-19 Reference design for antenna interface

On two-layer boards which cannot control resistance properly, the RF route should be as short and smooth as possible and at a width of 0.8 to 1.0mm; the RF is 1mm away from the ground. If the PCB is thinner than 1.5 mm, ensure no trace on the back of the RF by emptying it.

Figure 5-20 shows a two-layer board application. The RF is connected to GSCRF connector through traces on PCB, which is connected to the antenna via cable.

The RF testing point is at the PCB projection area, where the copper is removed (diameter: 1.0 mm). Around the area, drill enough ground holes. For multiple-layer PCB, ensure no traces or copper on the top layer around this area and put copper on the second layer to mask other signals. In this manner, you can lay out traces on other layers.

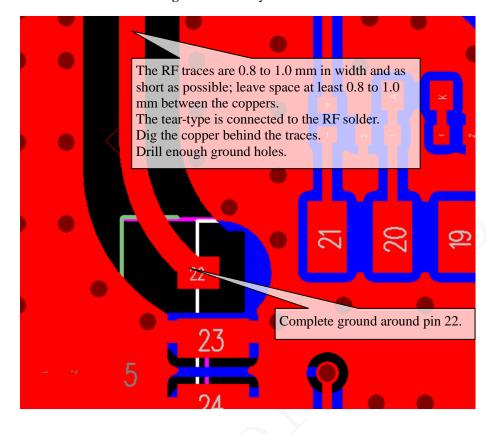


Figure 5-20 RF layout reference



CAUTION

On the PCB, keep the RF signals and RF components away from high-speed circuits, power supplies, transformers, great inductors, the clock circuit of single-chip host, etc.

6 Mounting the Module onto the Application Board

M660 is compatible with industrial standard reflow profile for lead-free SMT process.

The reflow profile is process dependent, so the following recommendation is just a start point guideline:

- Only one flow is supported.
- Quality of the solder joint depends on the solder volume. Minimum of 0.15mm stencil thickness is recommended.
- Use bigger aperture size of the stencil than actual pad size.
- Use a low-residue, no-clean type solder paste.

7 Package

M660modules are packaged in sealed bags on delivery to guarantee a long shelf life. Package the modules again in case of opening for any reasons.

If exposed in air for more than 48 hours at conditions not worse than 30°C/60% RH, a baking procedure should be done before SMT. Or, if the indication card shows humidity greater than 20%, the baking procedure is also required.

The baking should last for at least 24 hours at 90° C.

8 Abbreviations

ADC	Analog-Digital Converter		
AFC	Automatic Frequency Control		
AGC	Automatic Gain Control		
AMR	Acknowledged multirate (speech coder)		
CSD	Circuit Switched Data		
CPU	Central Processing Unit		
DAI	Digital Audio interface		
DAC	Digital-to-Analog Converter		
DCE	Data Communication Equipment		
DSP	Digital Signal Processor		
DTE	Data Terminal Equipment		
DTMF	Dual Tone Multi-Frequency		
DTR	Data Terminal Ready		
EFR	Enhanced Full Rate		
EGSM	Enhanced GSM		
EMC	Electromagnetic Compatibility		
EMI	Electro Magnetic Interference		
ESD	Electronic Static Discharge		
ETS	European Telecommunication Standard		
FDMA	Frequency Division Multiple Access		
FR	Full Rate		
GPRS	General Packet Radio Service		
GSM	Global Standard for Mobile Communications		
HR	Half Rate		
IC	Integrated Circuit		
IMEI	International Mobile Equipment Identity		
LCD	Liquid Crystal Display		
LED	Light Emitting Diode		
MS	Mobile Station		
PCB	Printed Circuit Board		
PCS	Personal Communication System		
RAM	Random Access Memory		
RF	Radio Frequency		
ROM	Read-only Memory		
RMS	Root Mean Square		
RTC	Real Time Clock		
SIM	Subscriber Identification Module		
SMS	Short Message Service		
SRAM	Static Random Access Memory		
TA	Terminal adapter		
TDMA	Time Division Multiple Access		
UART	Universal asynchronous receiver-transmitter		
VSWR	Voltage Standing Wave Ratio		