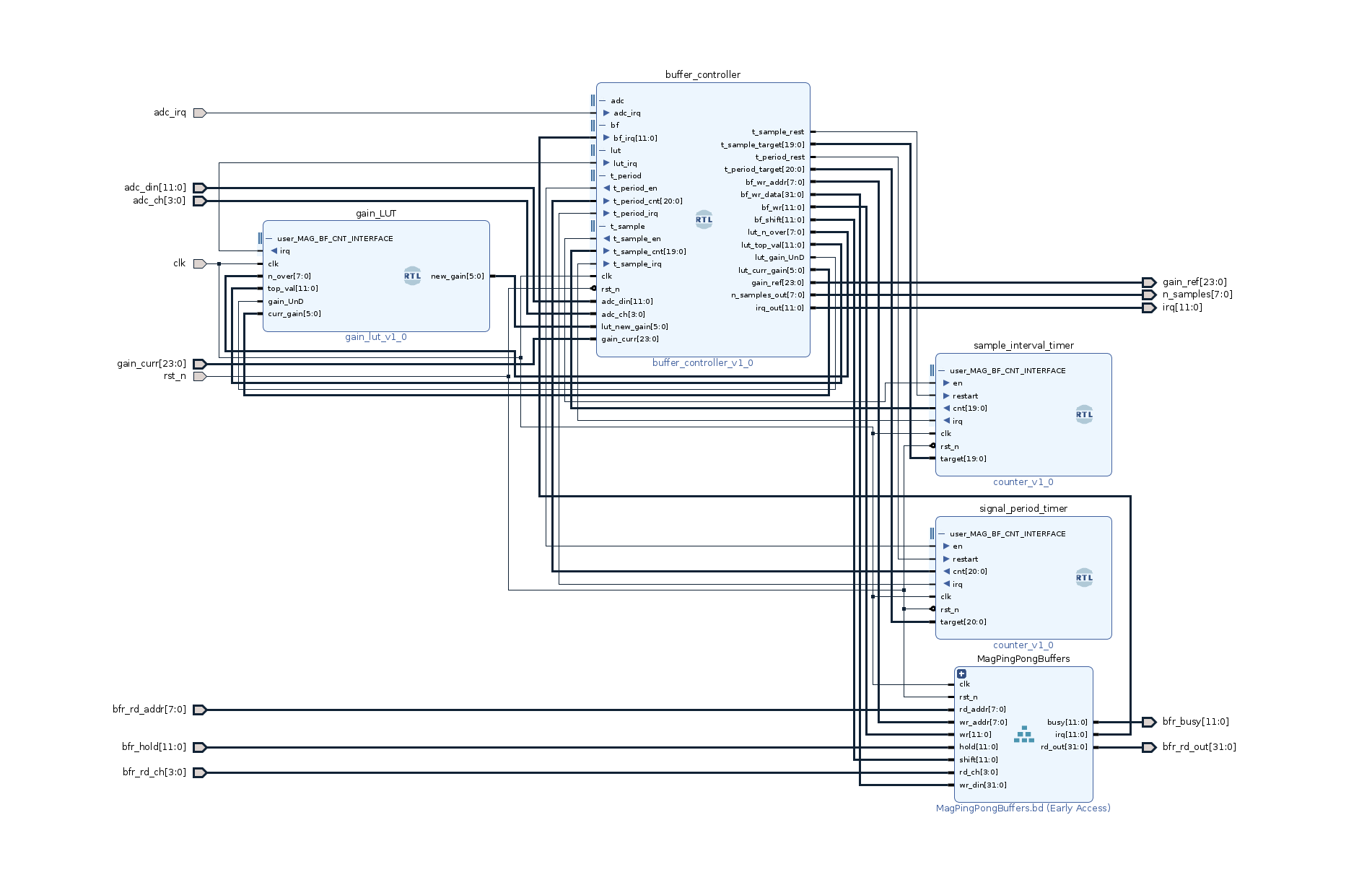
# Tests of **BufferFlowControl** Submodule Functionality

The aim is to verify that the submodule is working as expected. The tests are divided into simulation tests and physical tests.

## Intended Functionality



The intended functionality of the BufferFlowControl submodule is

1. To receive samples sequentially from the channels in order 0-3-6-9-1-4-7-10-2-5-8-11 and to push the samples to the pingpong buffers
2. After having sampled the channels once, wait until irq of the sample time counter to start sampling again, stop sampling upon irq of the signal period counter
3. While sampling a signal period, count for each channel the number of occurrences of the signal above the threshold and note the maximum signal value for adjustment of the gain
4. Determine upon the end of sampling one signal period which magnetometers should change the gain and if it should be up or down
5. Fetch gain change from a lookup table
6. After having decided the gain change options, initiate the shift of the pingpong buffers for which the corresponding magnetometer should not change gain and initiate the gain change for the correct magnetometers while the pingpong buffers are shifting
7. Keep track of which pingpong buffers have shifted and issue irq for the accepted channels when the pingpong buffers have shifted
8. Start sampling again when all gain changes have been processed

## Simulation

Simulation tests are carried out to test the functionality above.

### Simulation 1

This test tests a single pingpong\_buffer to verify the intended functionality.

### Simulation 2

This test tests the MagPingPongBuffers hierarchy to verify the intended functionality.

### Simulation 3

This test the full BufferFlowControl hierarchy for functionality point 1.

### Simulation **4**

This test the full BufferFlowControl hierarchy for functionality point 2.

### Simulation 5

This test the full BufferFlowControl hierarchy for functionality point 3.

### Simulation **6**

This test the full BufferFlowControl hierarchy for functionality point 4.

### Simulation **7**

This test the full BufferFlowControl hierarchy for functionality point 5.

### Simulation **8**

This test the full BufferFlowControl hierarchy for functionality point 6.

### Simulation **9**

This test the full BufferFlowControl hierarchy for functionality point 7.

### Simulation **10**

This test the full BufferFlowControl hierarchy for functionality point 8.