# Gain Settle Test

The purpose of the test is to determine the settling time of the signal propagating through the amplifier when the input signal is changed. This is the case when the ADC shifts between two axes. This information will be used to determine how fast the system can shift from sampling one axis to sampling the next axis on a given gain level.

## Setup

The test is performed by monitoring the following signal:

* The mag ch0 signal *a0*
* The mag ch1 signal *a1*
* The output of the amplifier *o*
* An output of the FPGA indicating the currently read channel from the ADC *s*

Only one magnetometer is sampled continuously. The gain can be adjusted from the terminal through a program written for the u96 to set the gain in the FPGA. Similarly, the axis can be chosen.

The gain is set to the condition for the test. The axis is changed from 0 to 1. An oscilloscope trigers on rising edge of *s*. All the signals are recorded.

The test is repeated for 3 different positions of the magnetometer, for 3 different currents, for 16 different gain steps