# Software Defined Radio Receiver Project

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KONRAD MCCLURE

06/08/2020

ENGR 357

# Design Criteria

The design criteria given to us by Dr. Frohne were:

1. Minimum discernible signal less than 1 uV.
2. Good image rejection.
3. Low noise figure.
4. Inexpensive to construct.

We choose to build our circuit to operate in the (5.000-10.000 MHz) band, centered around the “40-meter” Amateur Radio band.

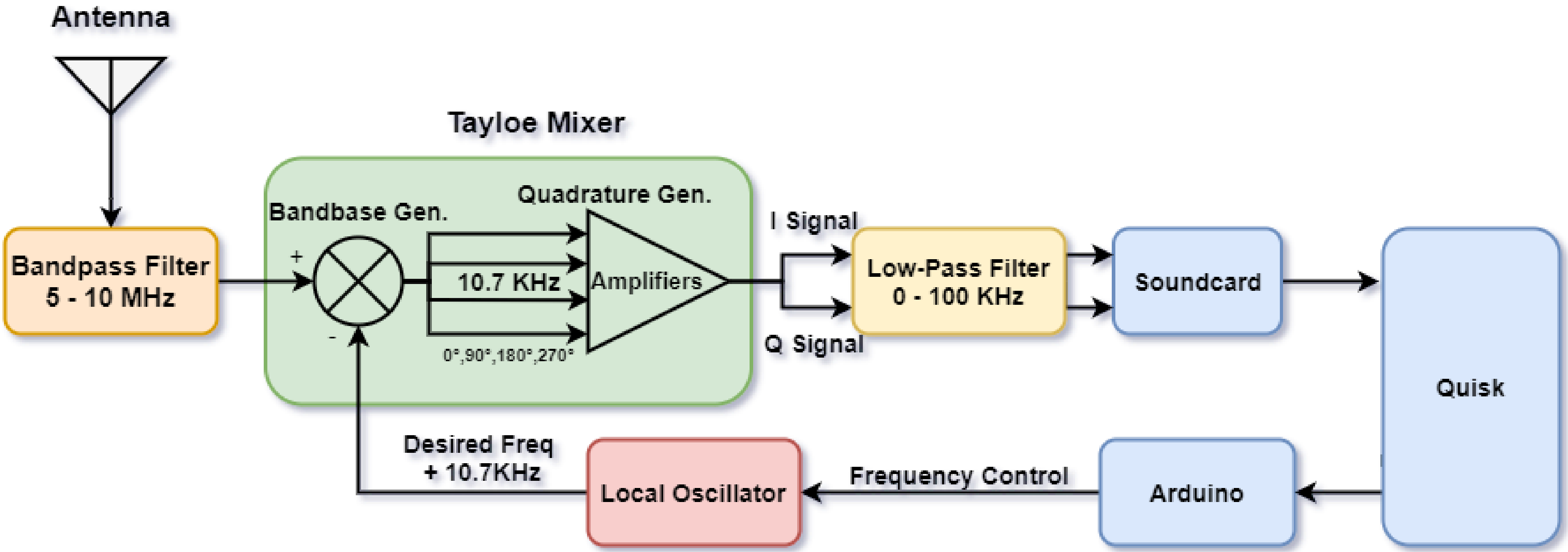
Our IF frequency we chose to be 10.7 kHz.

# Other Design Objectives

We set some of our own design objectives as well:

1. Simplicity of Design
   - Avoid using transformers
   - Utilize a Tayloe Mixer
2. Ease + Quality of Amplification
   - Instrumentation Amps
3. Ease of Construction
   - Primarily through-hole parts

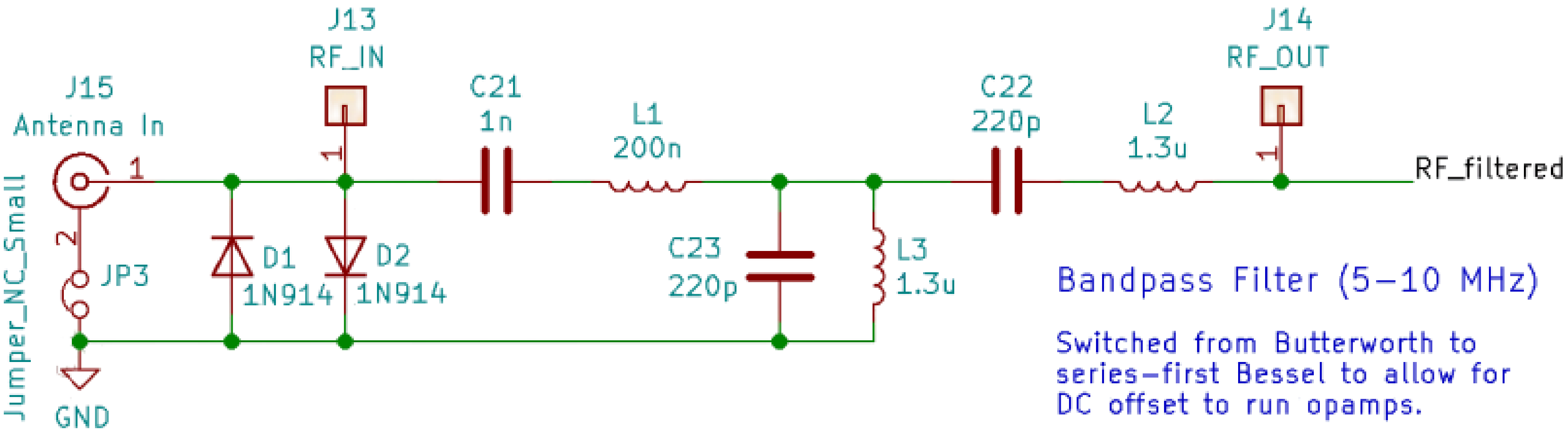
# Block Diagram



# Bandpass Filter Design (5-10) MHz

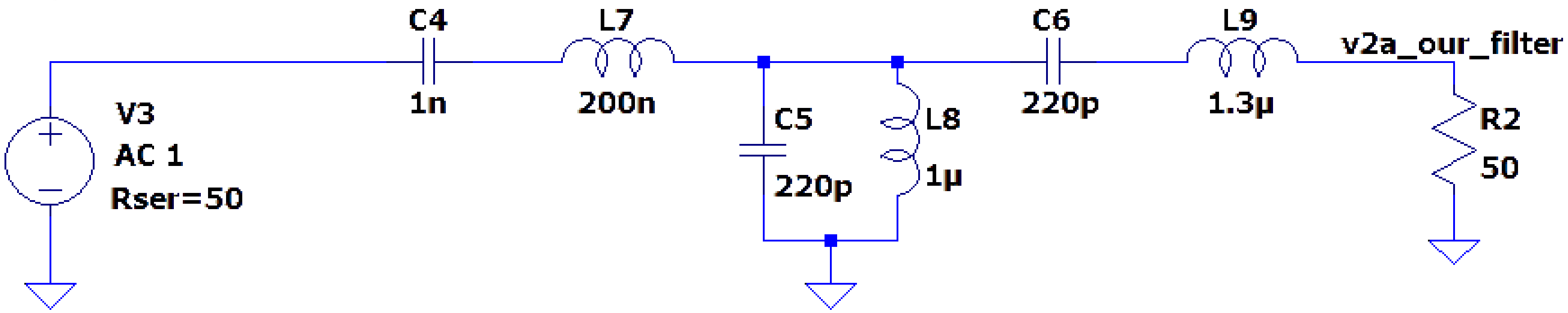
Designing a series-first Bessel filter allowed us to give our RF signal a DC offset so that we could run our op amps on single supply

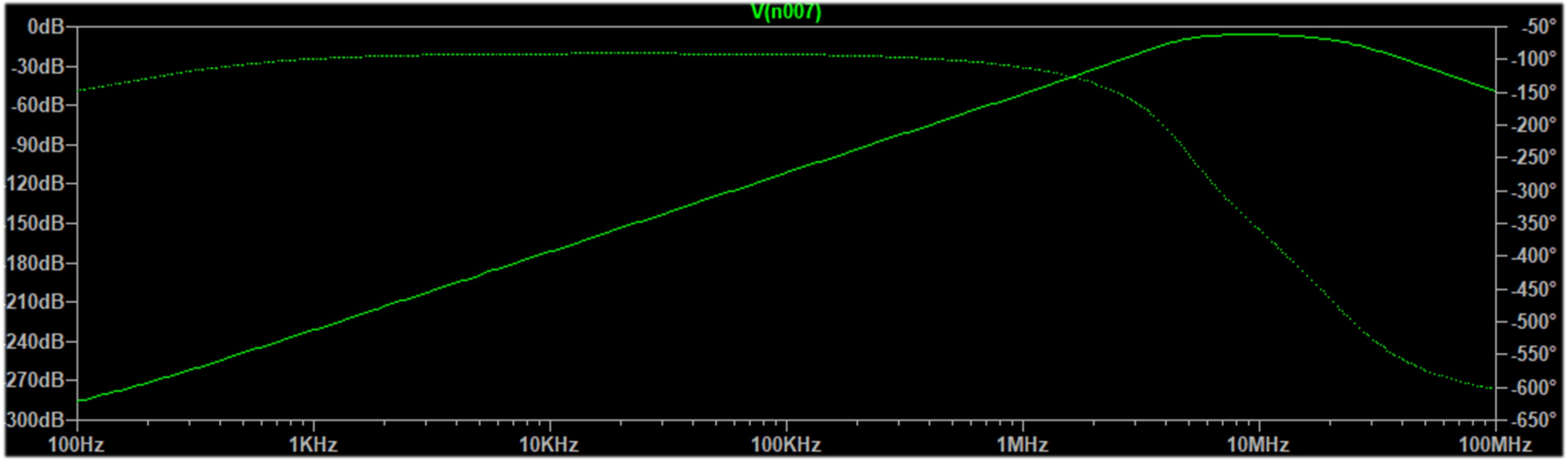
Keeping it a 3rd order kept the cost low.



# Bandpass Filter

(5-10 MHz)



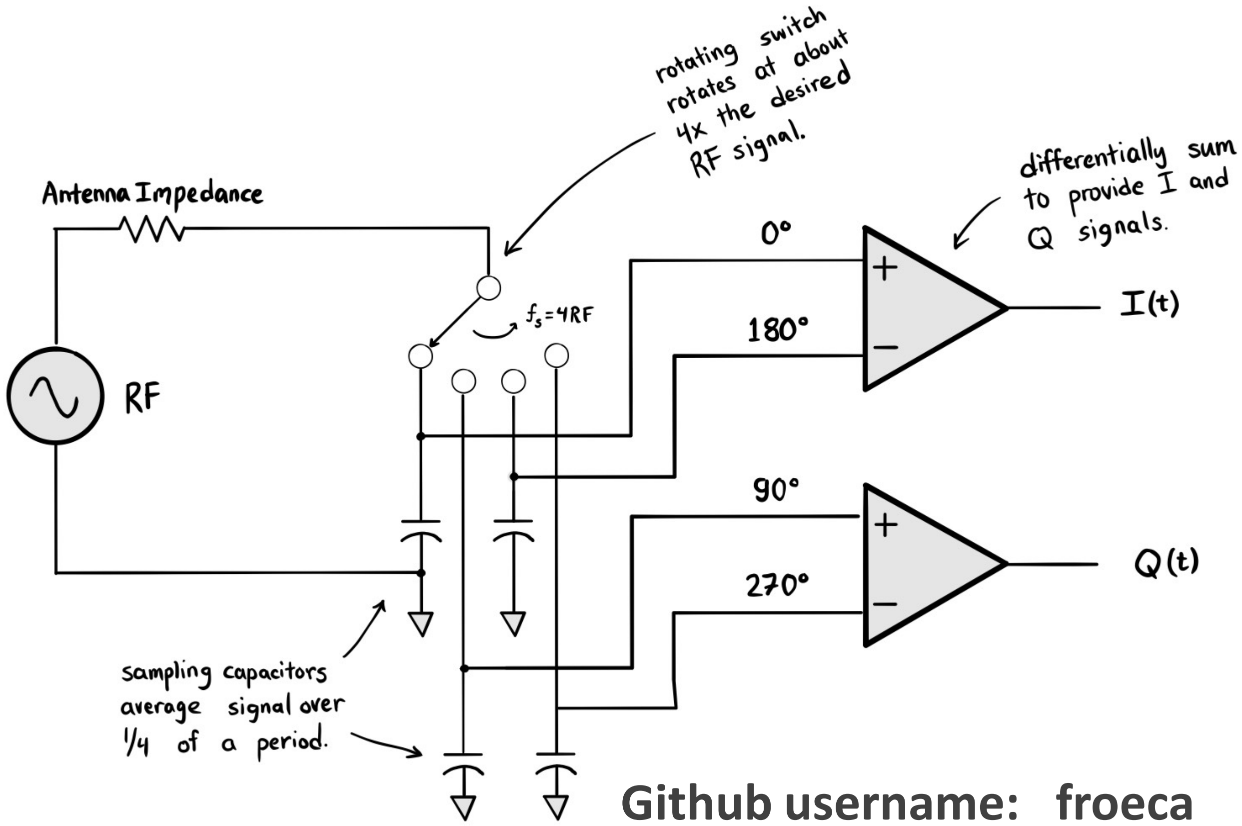



# Tayloe Mixer Functionality

A four-position switch that cycles at the local oscillator frequency. Sampling capacitors are placed such that the signal is sampled four times each period of the RF. Differentially summing the outputs produces the I and Q signals.

$$f_{LO} = f_{RF} - 1/4\ f_{LO}$$

“Ultra Low Noise, High Performance, Zero IF Quadrature Product Detector and Preamplifier.” – Dan Tayloe

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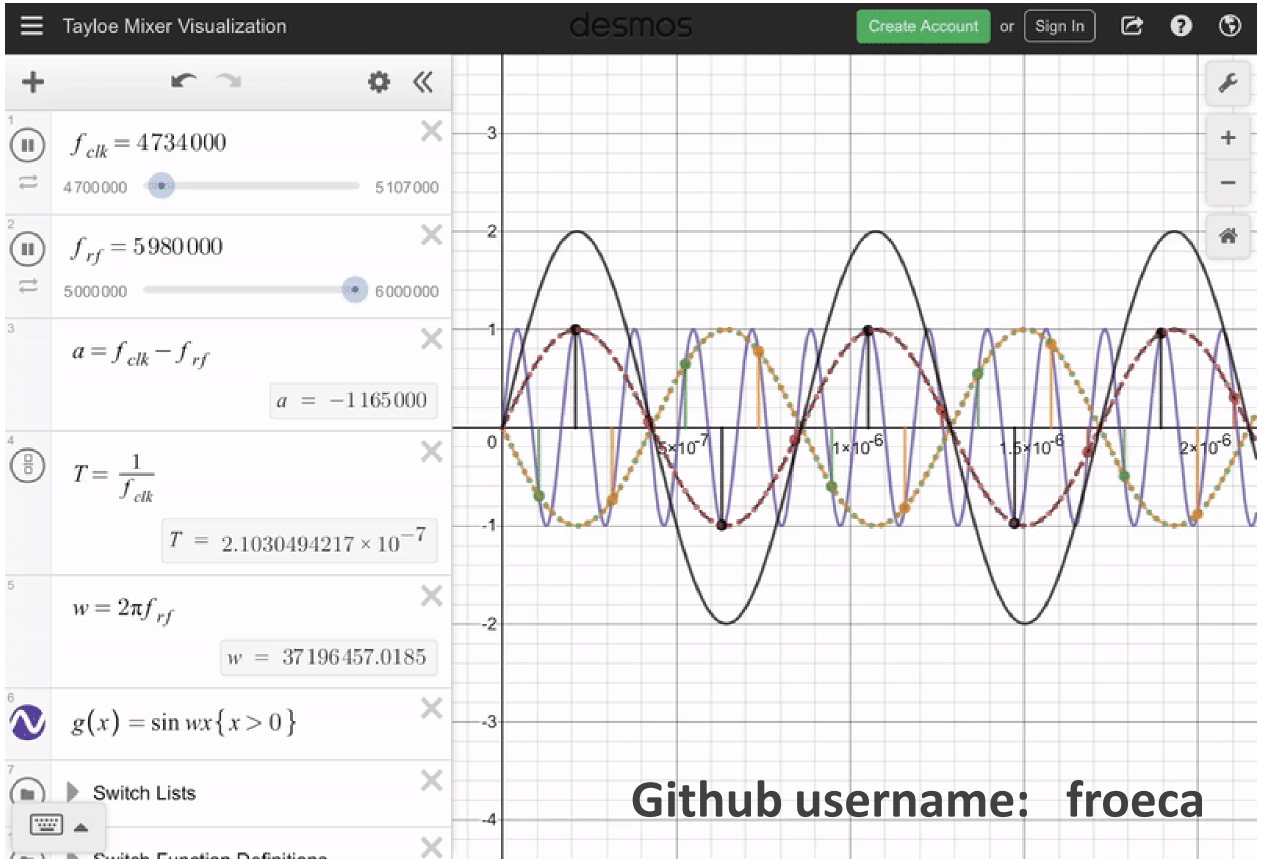


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# Tayloe Mixer

**From our design goals:**

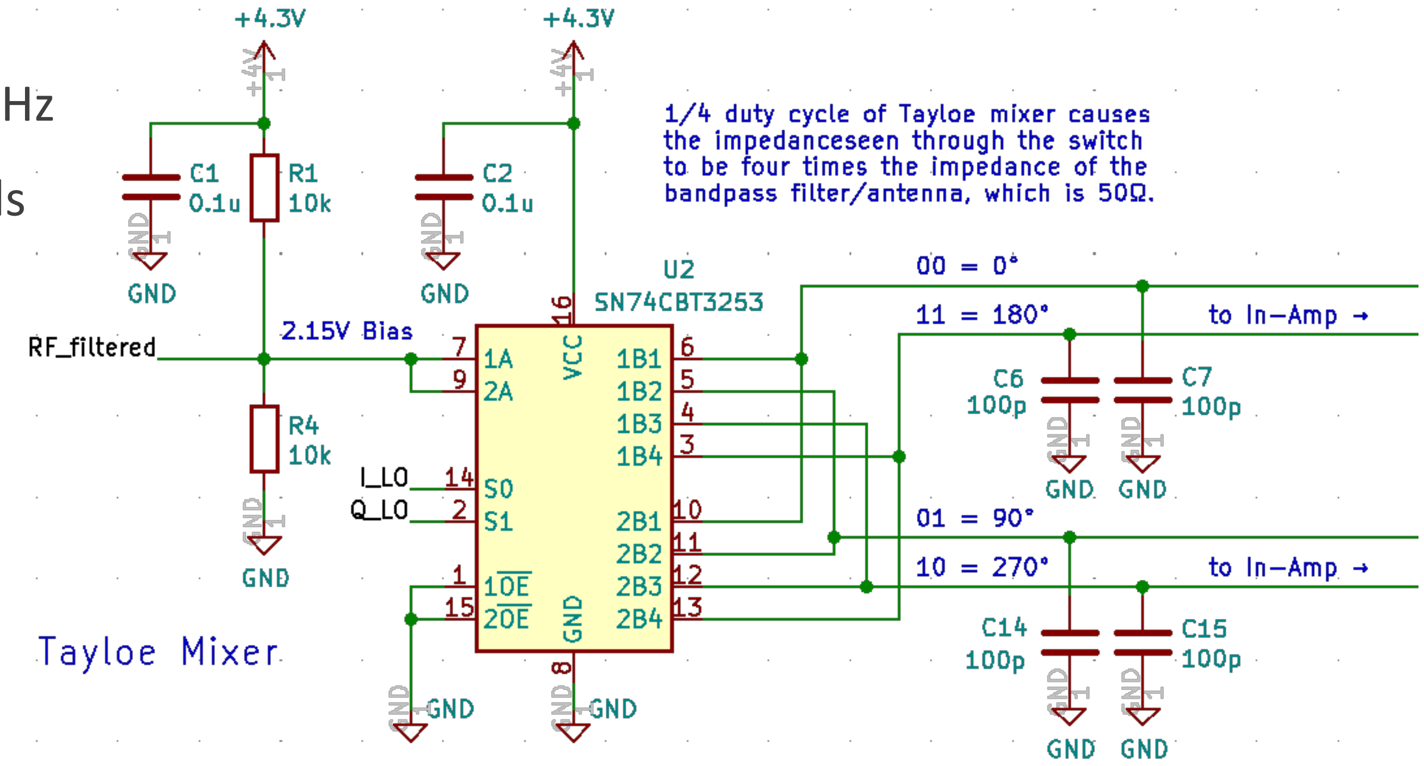
$f_{IF}$ = 10.7kHz, 5 MHz < $f_{RF}$ < 10 MHz

The LO freq, $f_{LO}$, would be upwards of 40 MHz.

Thus, the period of the local oscillator is: 25 ns.

**IC Selection:** SN74CBT3253

**Reasons:**
Fast switching speed ($t_{pd}$ = 6.6 ns),
Low on-state resistance ($r_{on}$ = 7 Ω),
Cheap price ($0.58).



# Digital Section – (Johnson Counter)

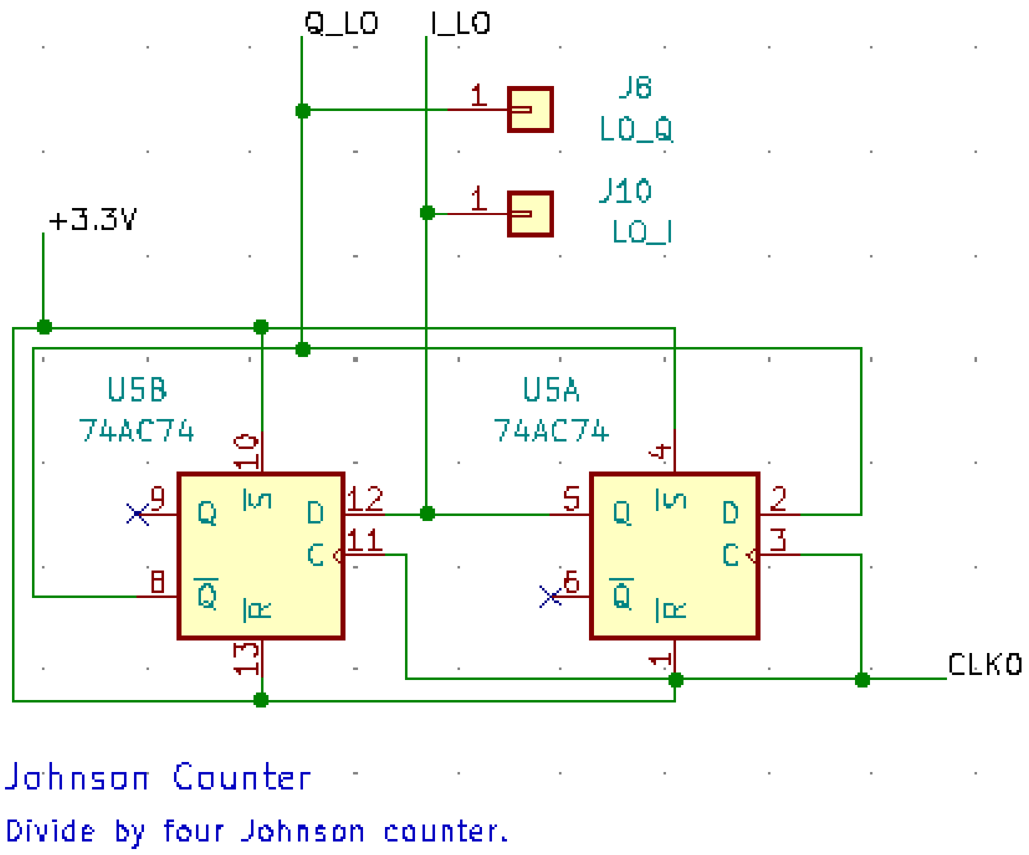
Since we must sample four times each period of the RF signal, the frequency of our local oscillator must be four times the frequency of the RF.

$$f_{LO} = 4f_{RF}$$

A simple divide by four Johnson counter was used to control the select lines of the mux.

**IC selection:** 74AC74

**Reason:** Fast switching speed, through hole package option, cheap price ($0.55).



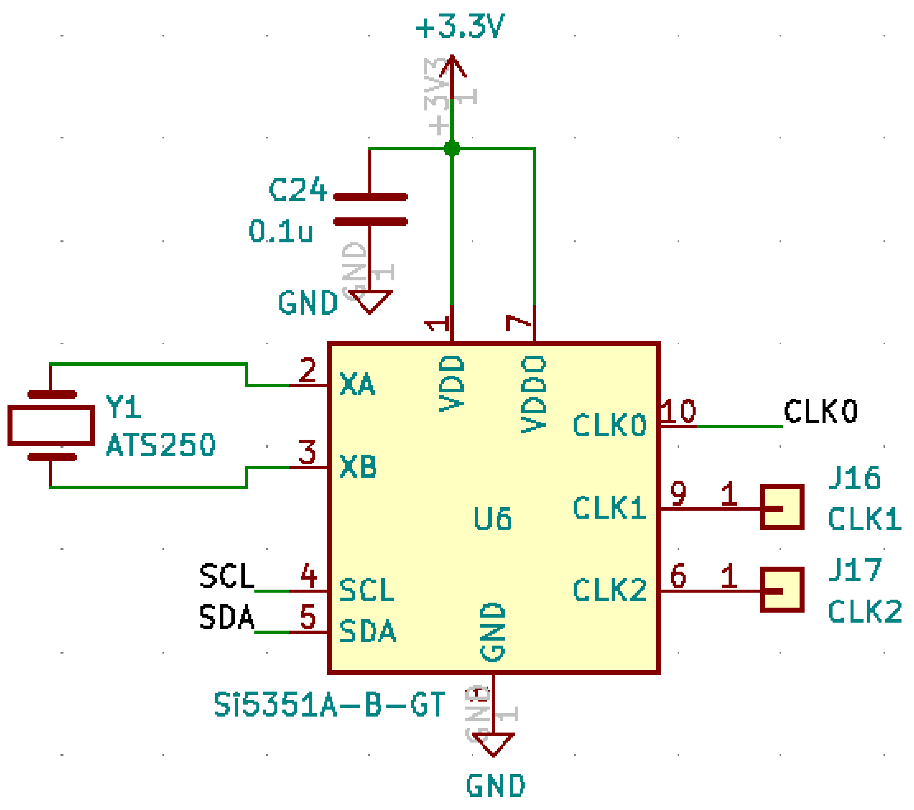
# Digital Section – (Clk Gen and Arduino)

The Arduino Nano v3 controls the clock generator via the SDA and SCL signals.

The ATS250 crystal is needed to drive the SI5351. As mentioned previously, the clk gen runs at 4x the frequency of the desired RF signal.

**IC selection:** SI5351

**Reason:** Compatibility with Arduino code, reasonable price ($0.92)



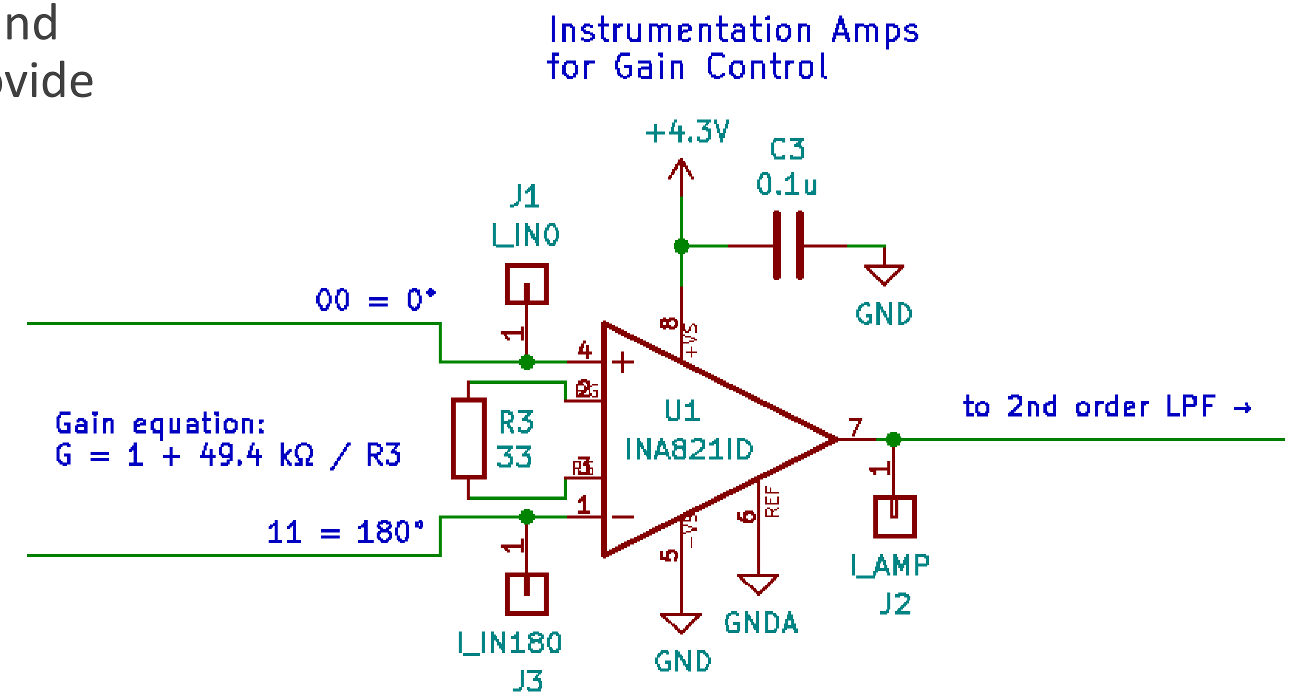
# Instrumentation Amps

The 0° and 180° capacitors differentially sum to provide the in-phase (I) signal and the 90° and 270° capacitors sum to provide the quadrature (Q) signal. We used instrumentation amps to:

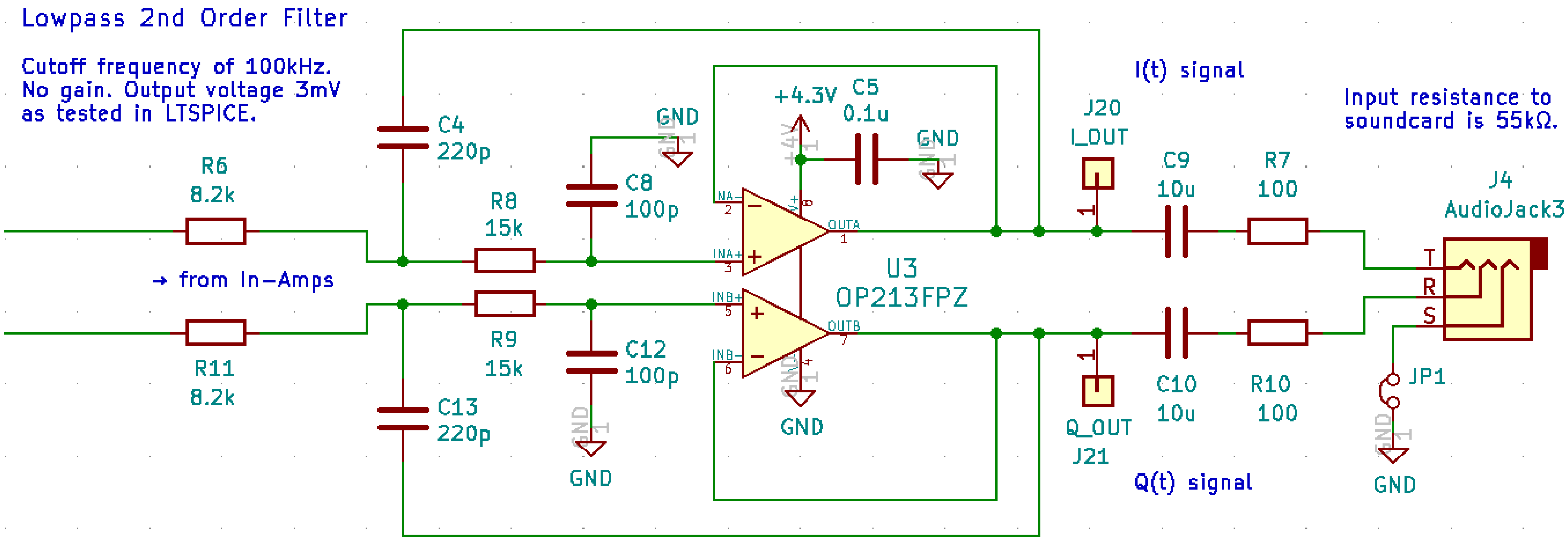
- Eliminate gain variance.
- Have more control over the gain.
- Lower noise.
- Reduce common-mode gain.

**IC selection:** INA821ID

**Reason:** Low-noise (7 $nV/\sqrt{Hz}$), single supply, cheapest we could find ($5.15).

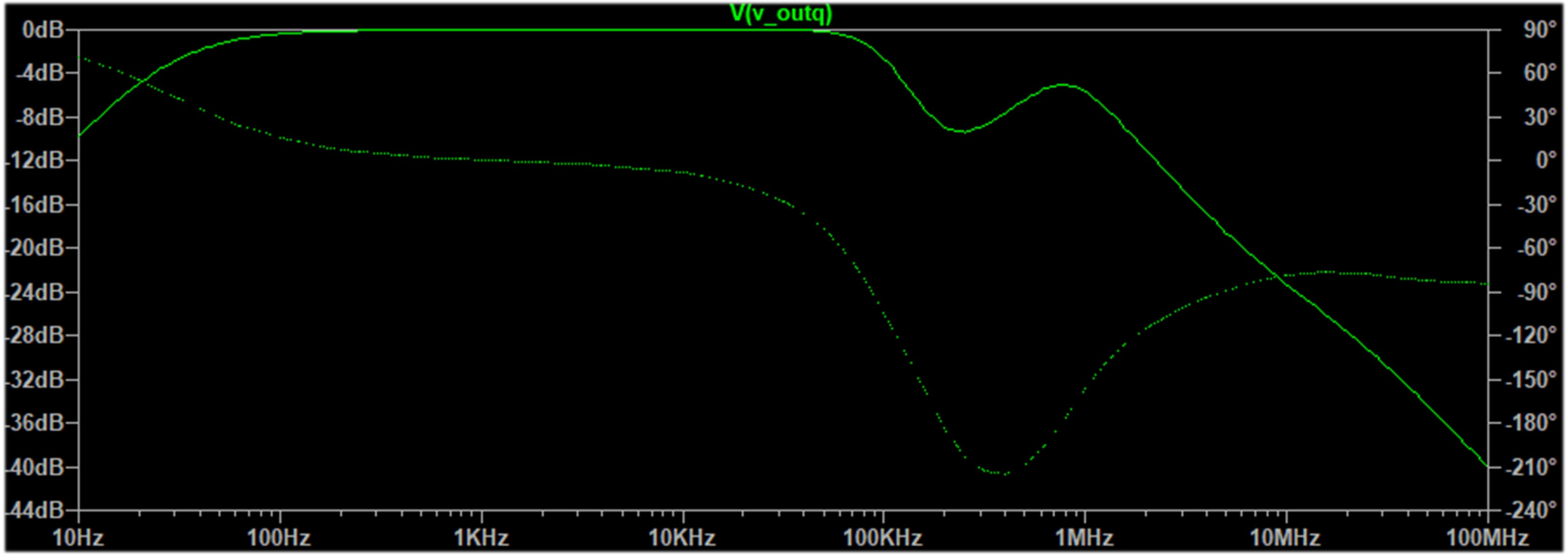


# $2^{nd}$ Order Low-Pass Filter




**IC selection:** OP213FPZ **Reason:** Low-noise ($4.7\ nV/\sqrt{Hz}$), single supply, through hole package.

# $2^{nd}$ Order Low-Pass Filter Response

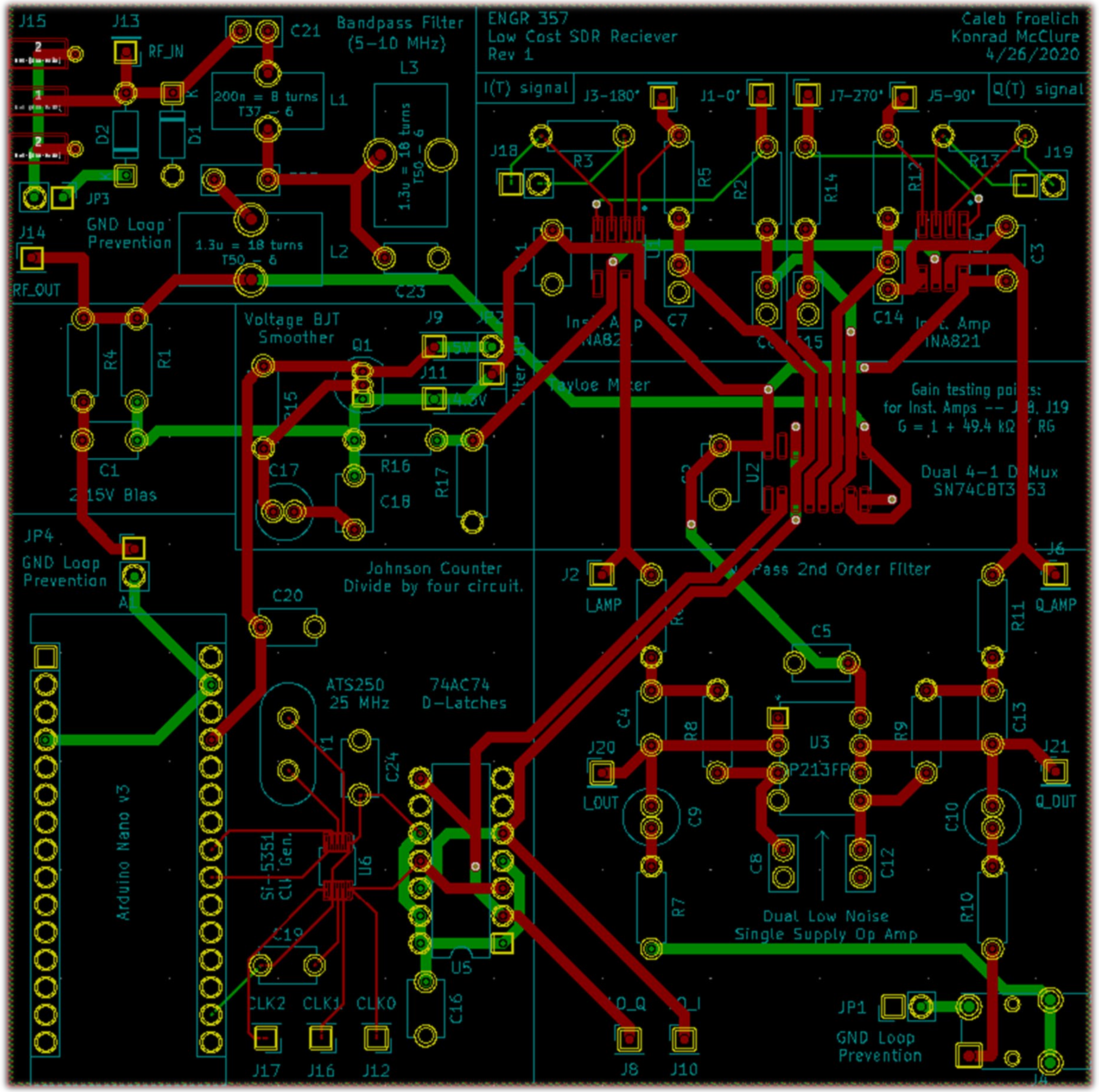


# Component Price List

| | value: | qty: | price: |
|---|---|---|---|
| **Resistors:** | 15k | 2 | obtained from lab |
| | 10k | 4 | |
| | 8.2k | 2 | |
| | 1k | 1 | |
| | 100 | 2 | |
| | 50 | 4 | |
| | 33 | 2 | |
| **Capacitors:** | 10u | 3 | $0.10 |
| | 0.1u | 10 | $0.14 |
| | 1n | 1 | $0.18 |
| | 220p | 4 | $0.19 |
| | 100p | 6 | $0.22 |
| **Inductors:** | 1.3u | 2 | supplied by |
| | 200n | 1 | Dr. Frohne |

| | value: | qty: | price: |
|---|---|---|---|
| **Diodes:** | 1N914 | 2 | $0.10 |
| **Transistor:** | PN2222ATF | 1 | $0.24 |
| **Crystal:** | ATS250 | 1 | $0.37 |
| **IC's:** | 74AC74 | 1 | $0.55 |
| | Si5351A-B-GT | 1 | $0.92 |
| | SN74CBT3253 | 1 | $0.58 |
| | INA821ID | 2 | $5.15 |
| | OP213FPZ | 1 | $7.47 |
| **PCB board:** | | 5 | $2.00 |

| **Total** | **$ 26.54** |
|---|---|

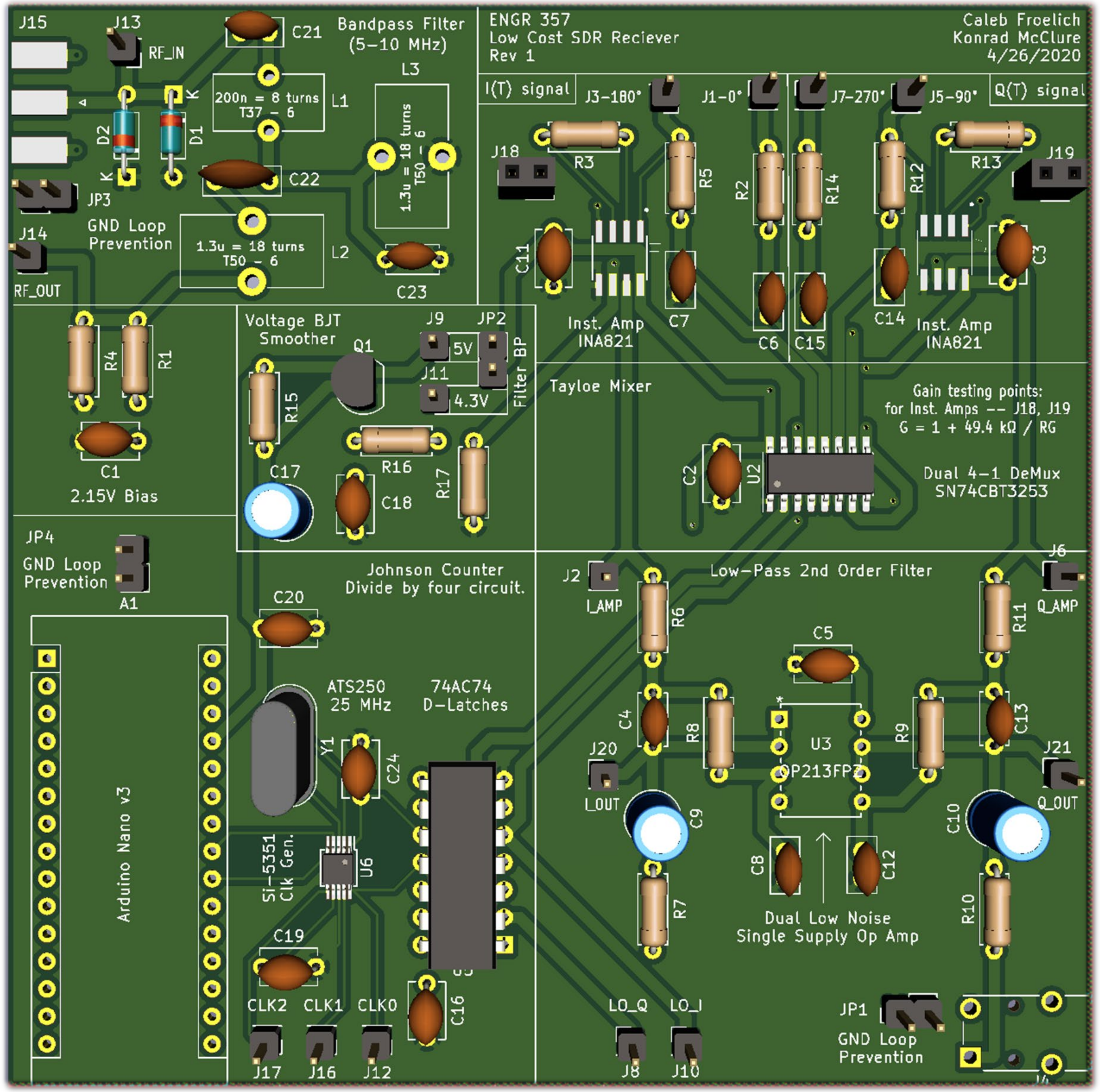



# PCB Board Design

To keep the input/output impedance of devices as close to 50Ω as possible, the trace width was calculated to be:

1.064 mm

The digital section need not have the same trace width. For convenience, we used 0.250 mm.

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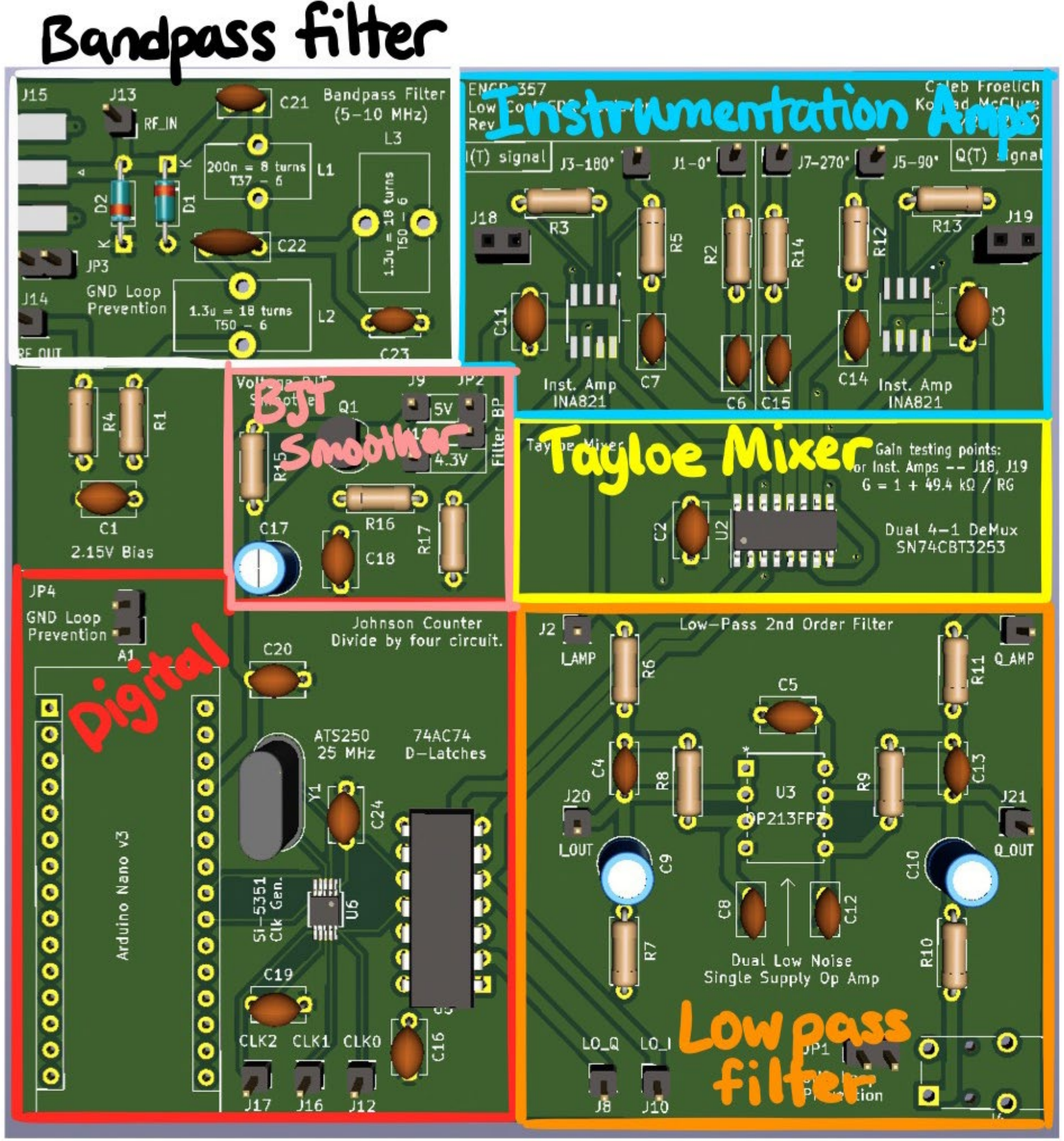


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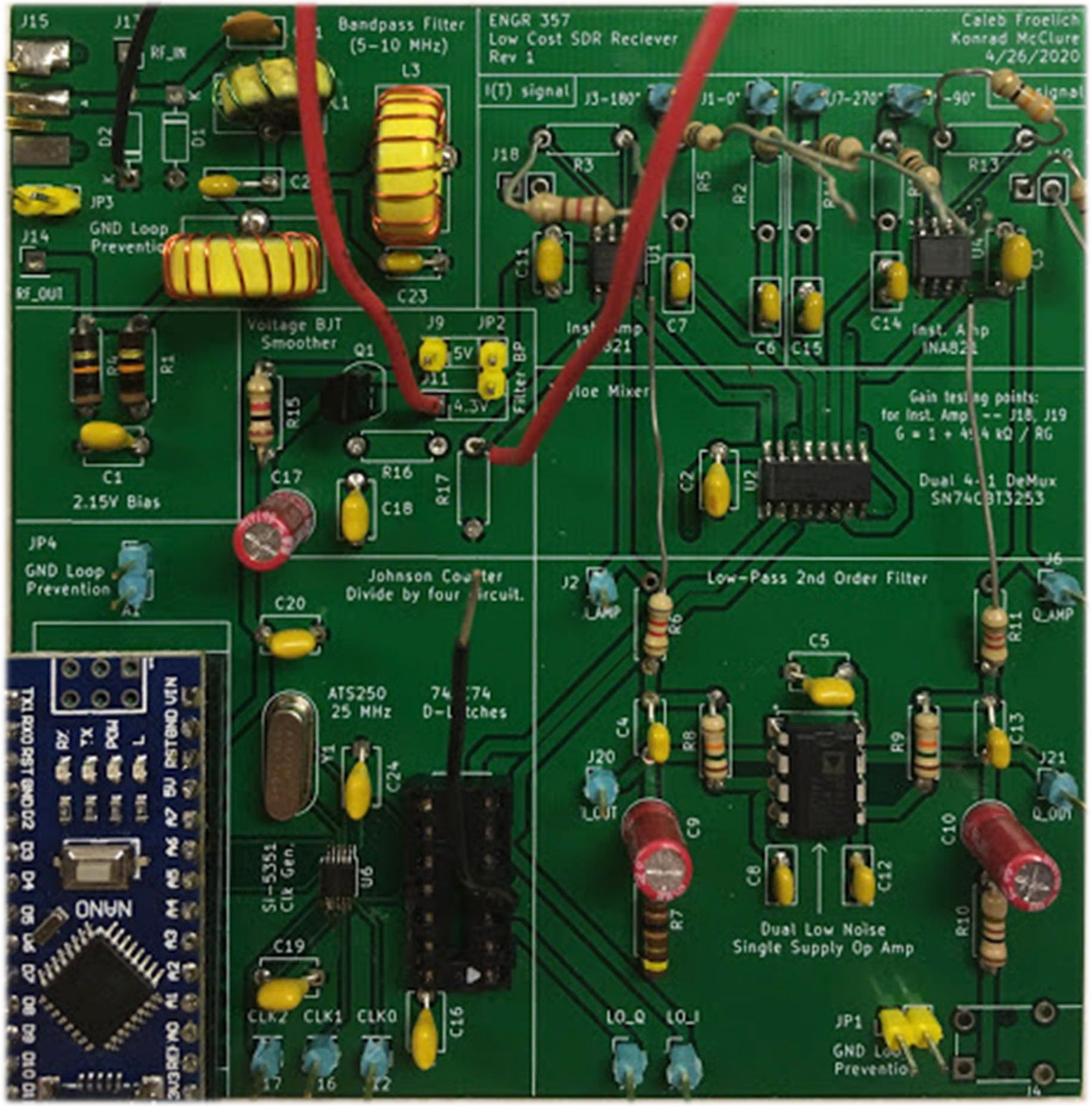



# Board Construction

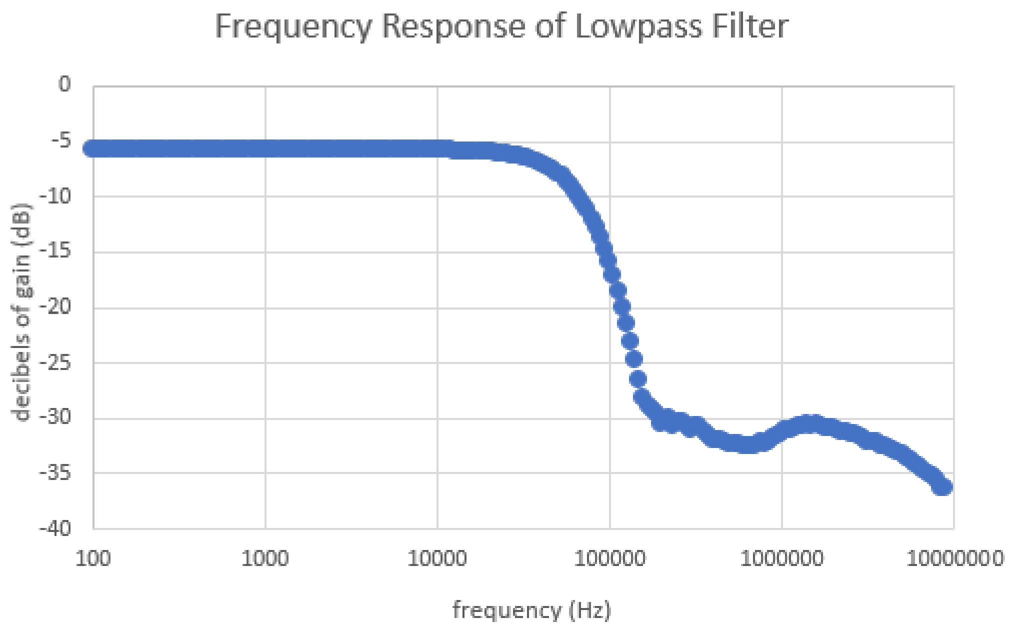
To allow for testing, we constructed the board in phases, isolating each section.

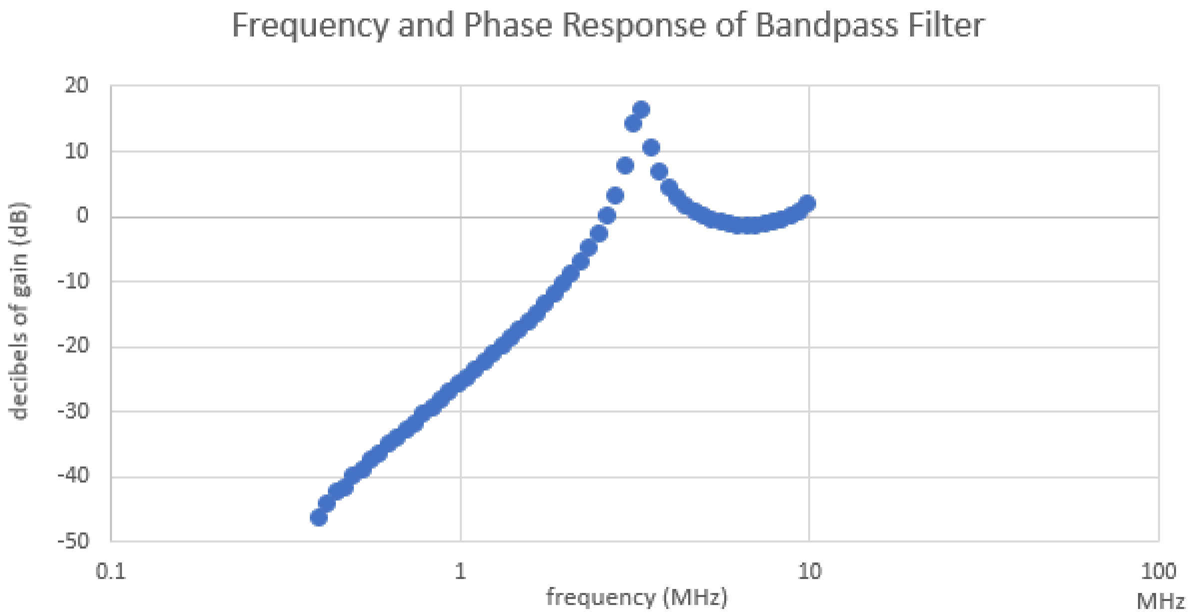
We tested components in the following order:

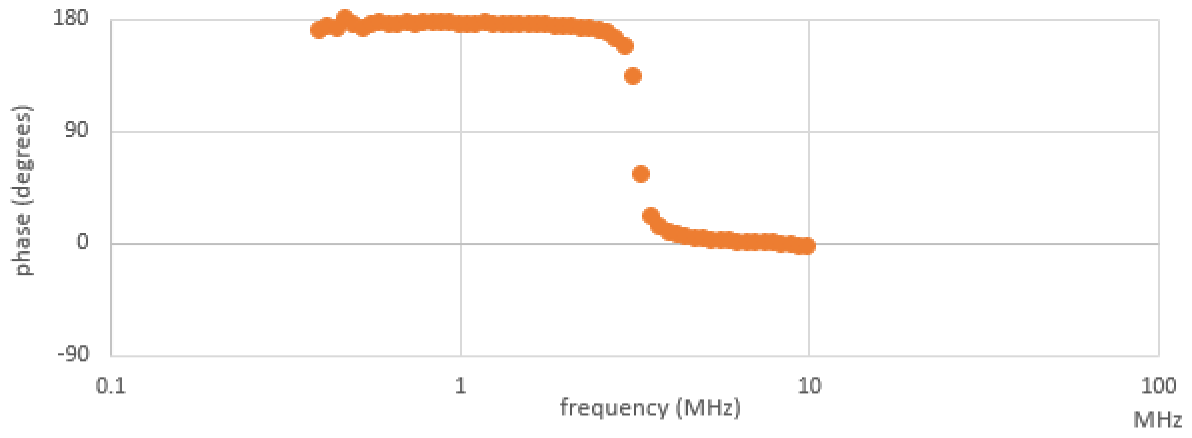
1. Bandpass filter
2. Lowpass filter
3. Instrumentation Amplifiers
4. Voltage Smoother
5. Digital section.
6. Multiplexer / Whole circuit.

# Testing Results
(filters)

Data obtained from Caleb's circuit.

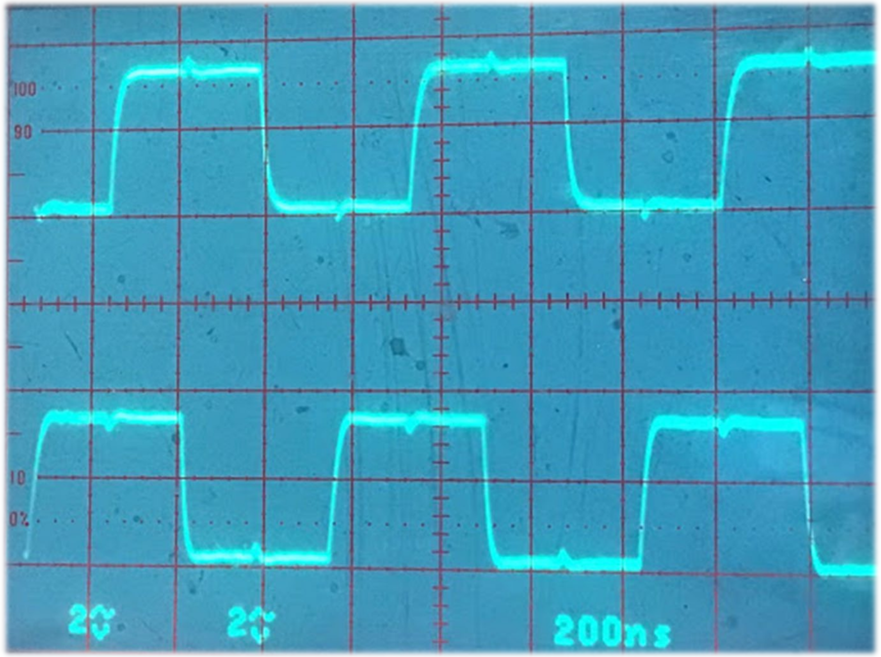


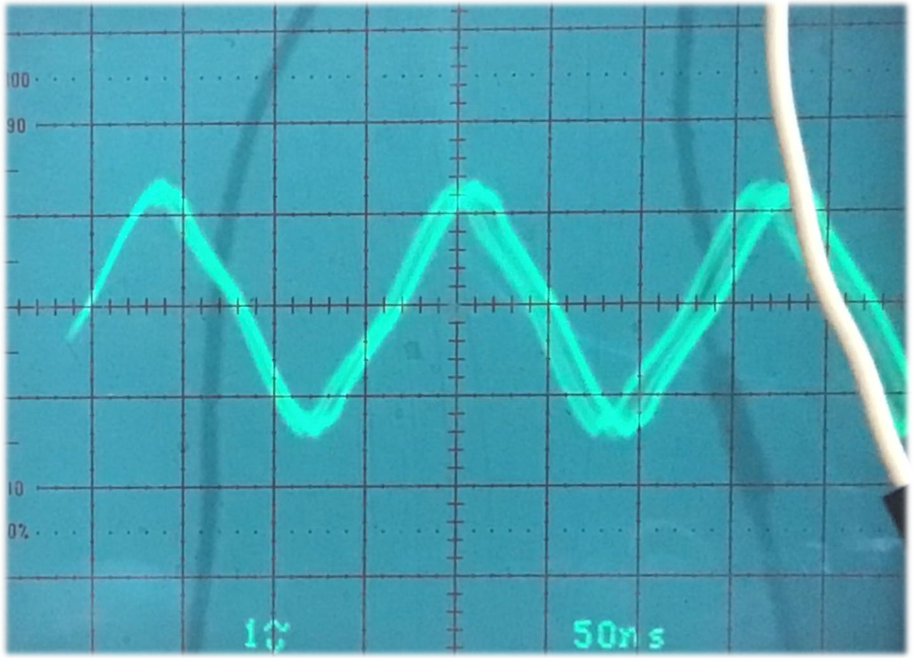



# Testing Results
## (clk gen and Johnson counter)

Results obtained from Caleb's circuit.



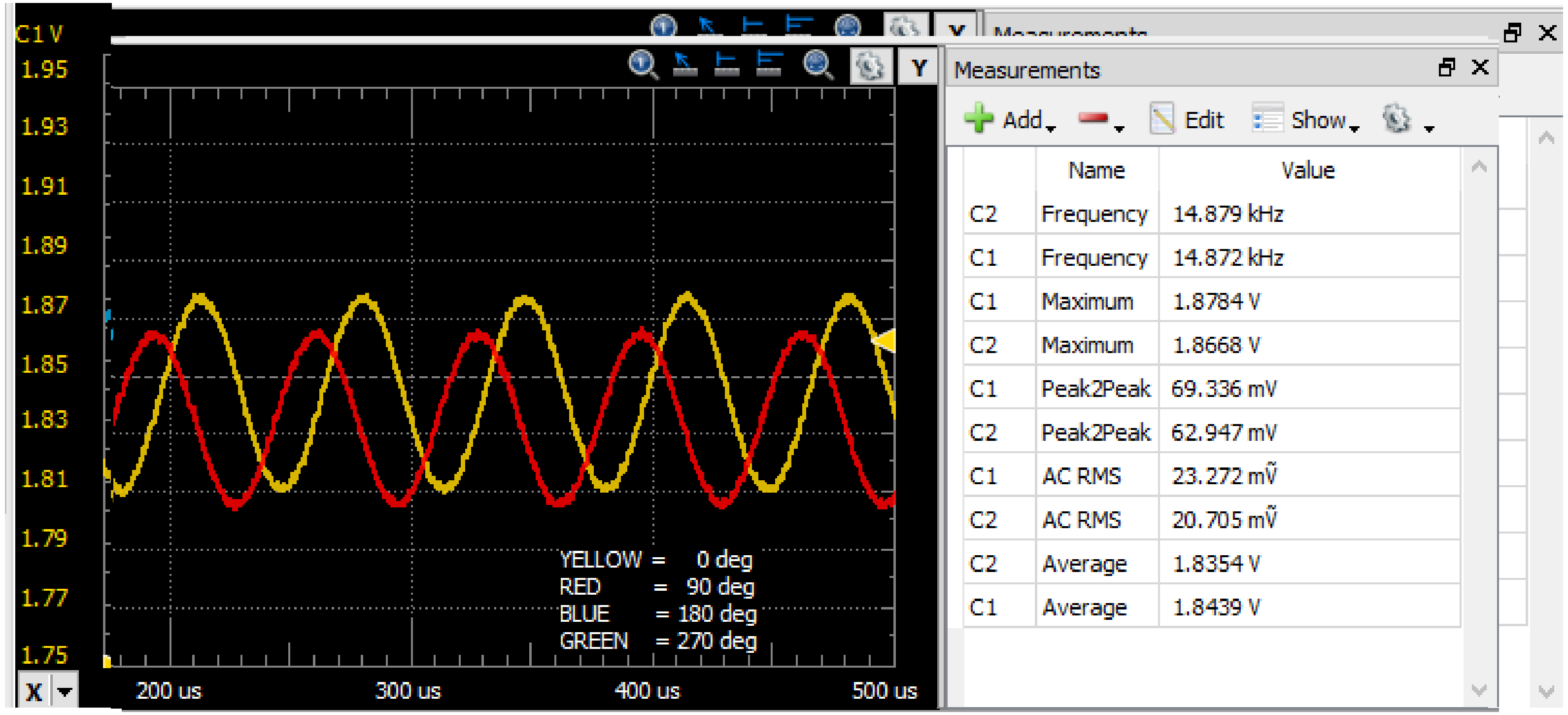

Johnson Counter output




Clock generator output

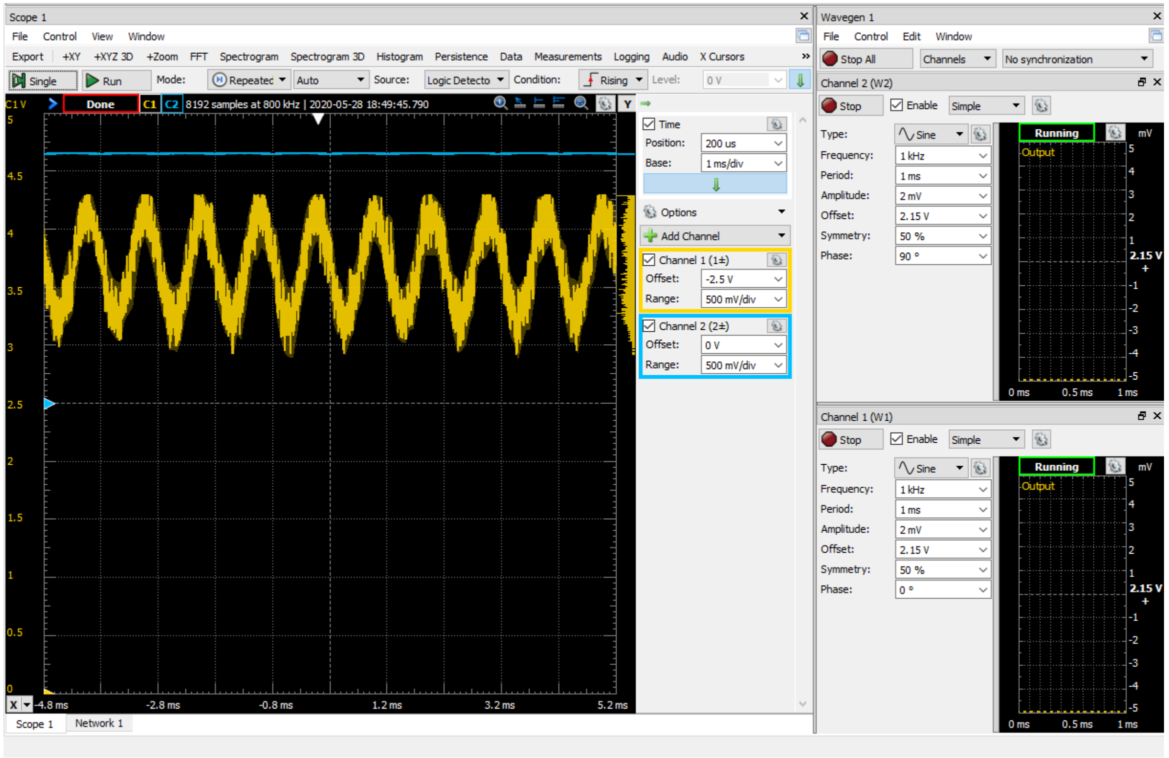
# Testing Results
(mixer)

Data obtained from Konrad's circuit.



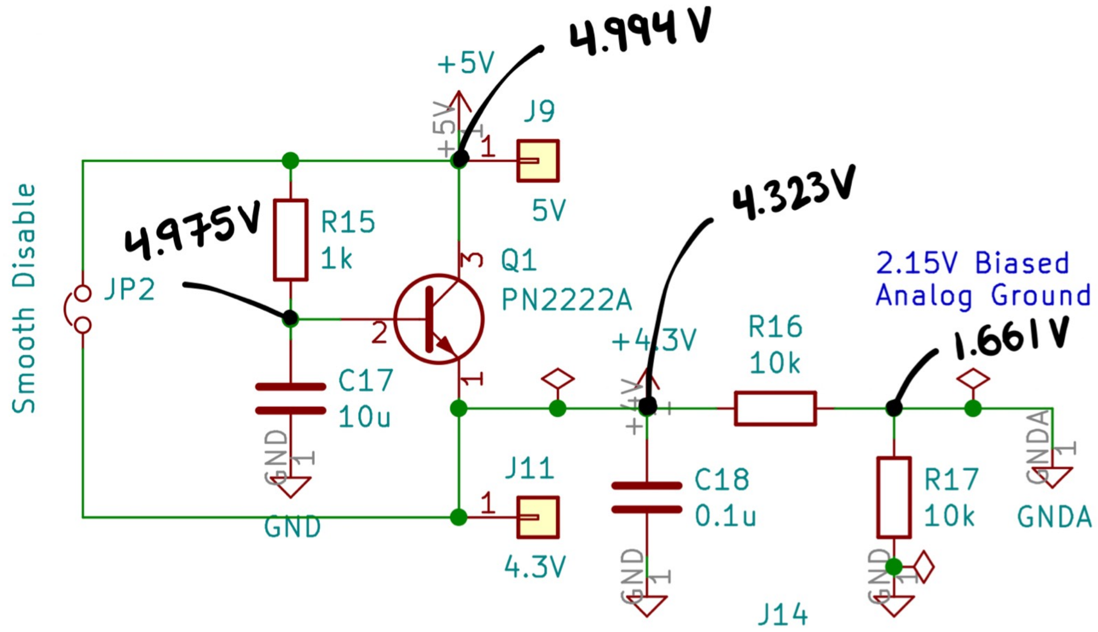
# Testing Results
## (instrumentation amps)

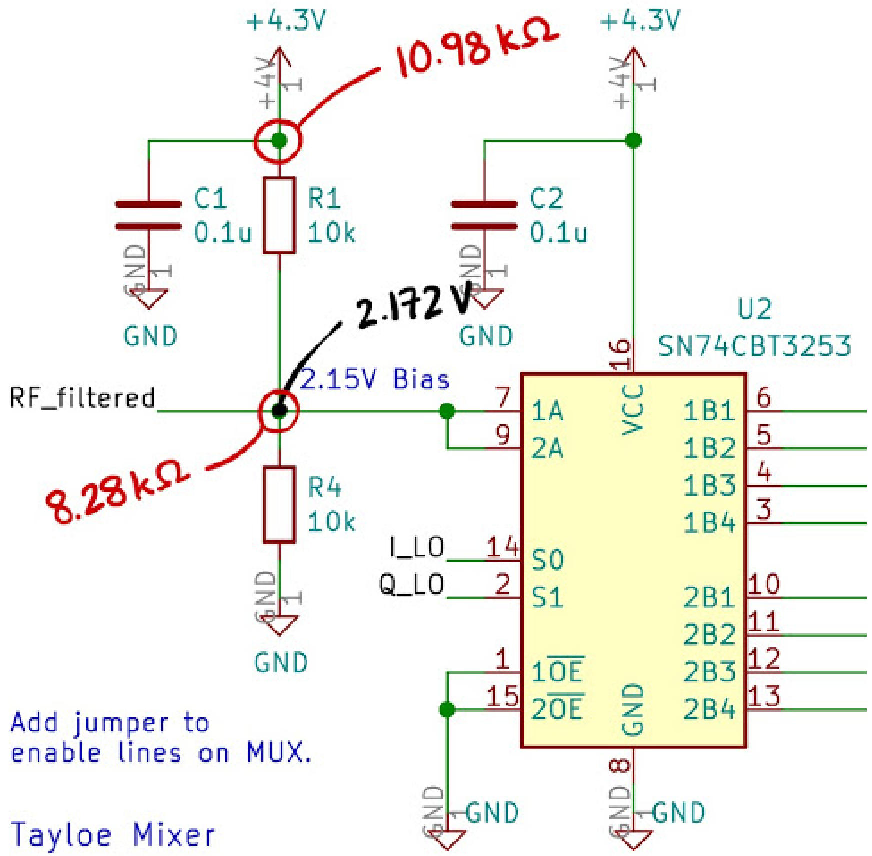
Data obtained from Caleb's circuit.



# Issues Encountered

- Analog Ground not at 2.15V.
  - Only seeing about 1.6V.



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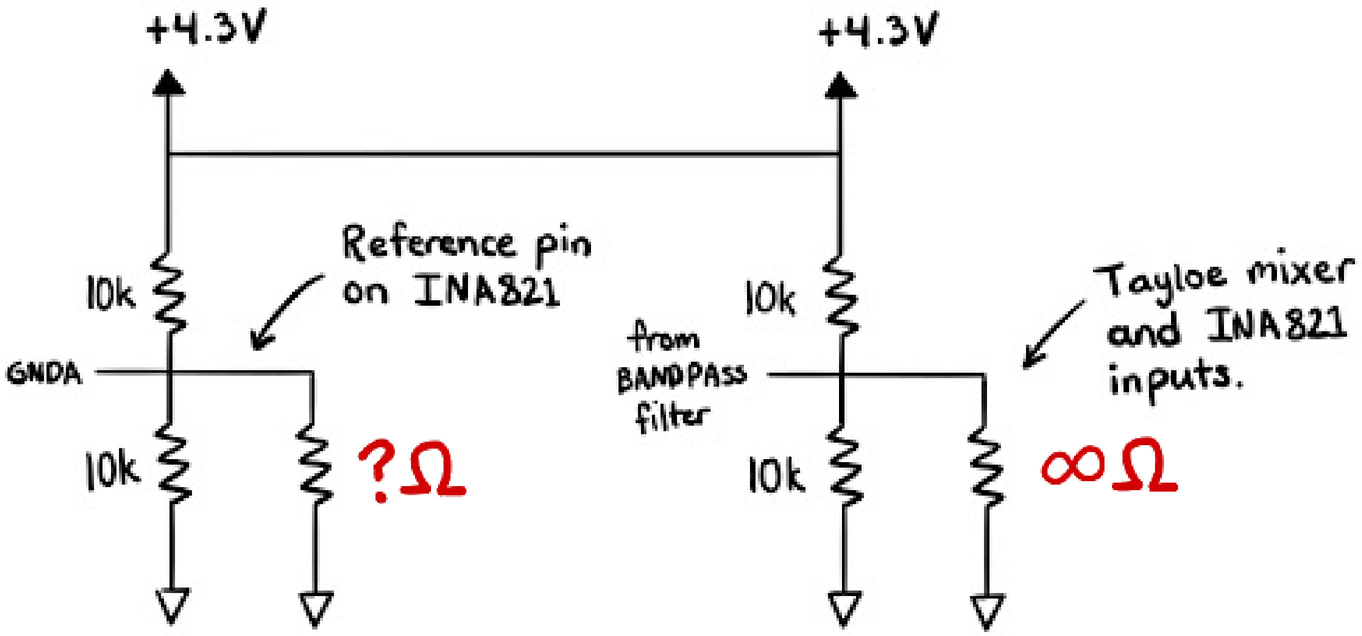

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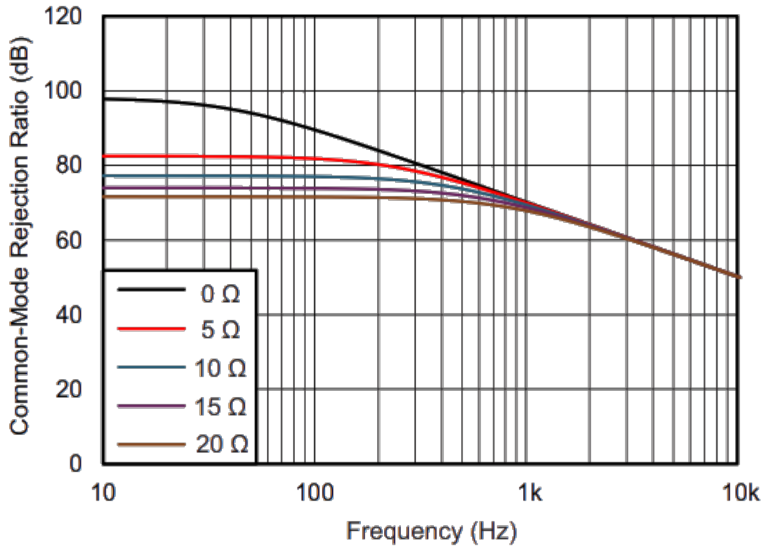



Figure 66. The Effect of Increasing Resistance at the Reference Pin

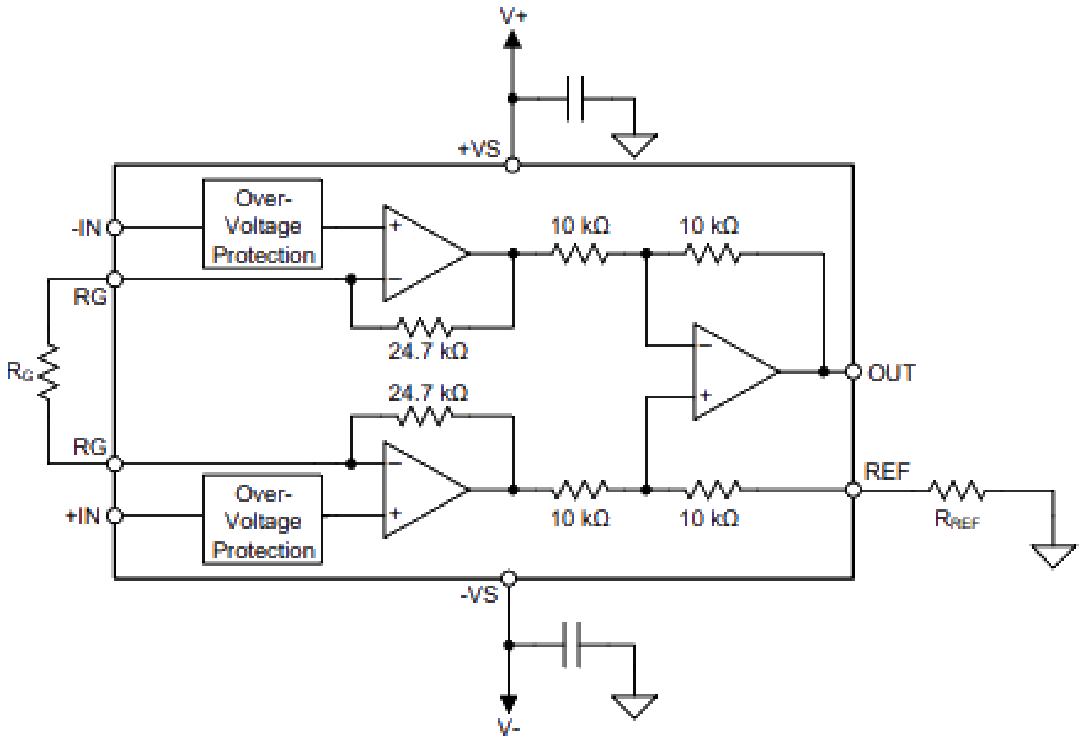


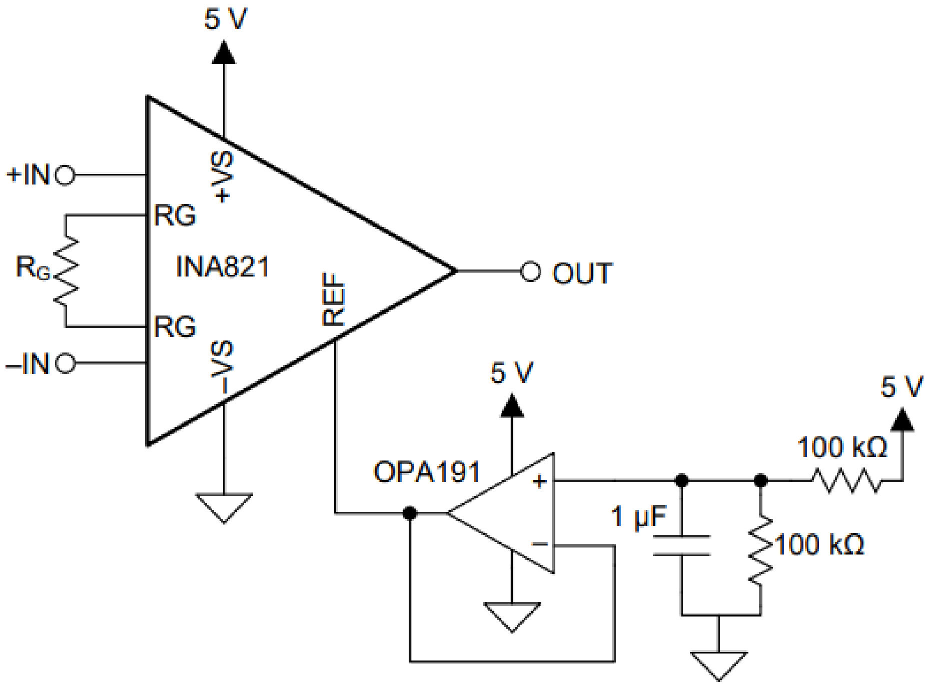

Figure 65. Parasitic Resistance Shown at the Reference Pin

Images from: http://www.ti.com/lit/ds/symlink/ina821.pdf

# Issues Encountered

- Analog Ground not at 2.15V.
  - Only seeing about 1.6V.
  - Reference pin of In Amps drew too much current.

Solution: Use LM741CN op-amps to buffer the input to the reference pin. This helped preserve our CMRR.



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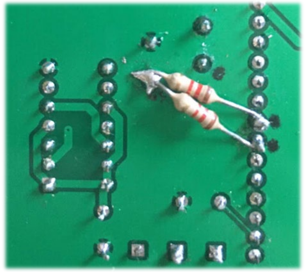
- Incorrect pins on PCB for SCL and SDA signals.
  - I (Caleb) had used A3 and A4 for the SDA and SCL signals when in fact they should've been A4 and A5.

Solution: Breadboard Arduino and connect via wires to PCB.

- Need pull up resistors for SCL and SDA signals.

Solution: Added pull-up resistors to back of PCB.



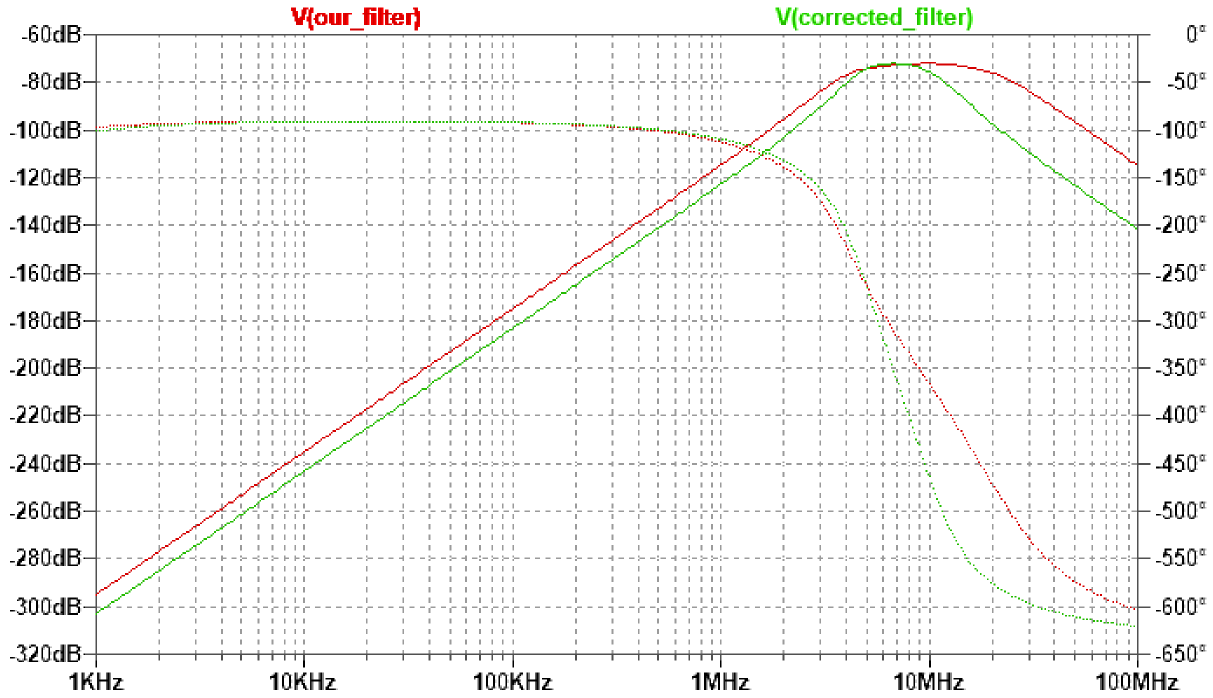
- IF frequency is not 10.7kHz. Instead it's currently 14kHz.

Possible Causes: Johnson Counter
Clock Generator
MUX Switching

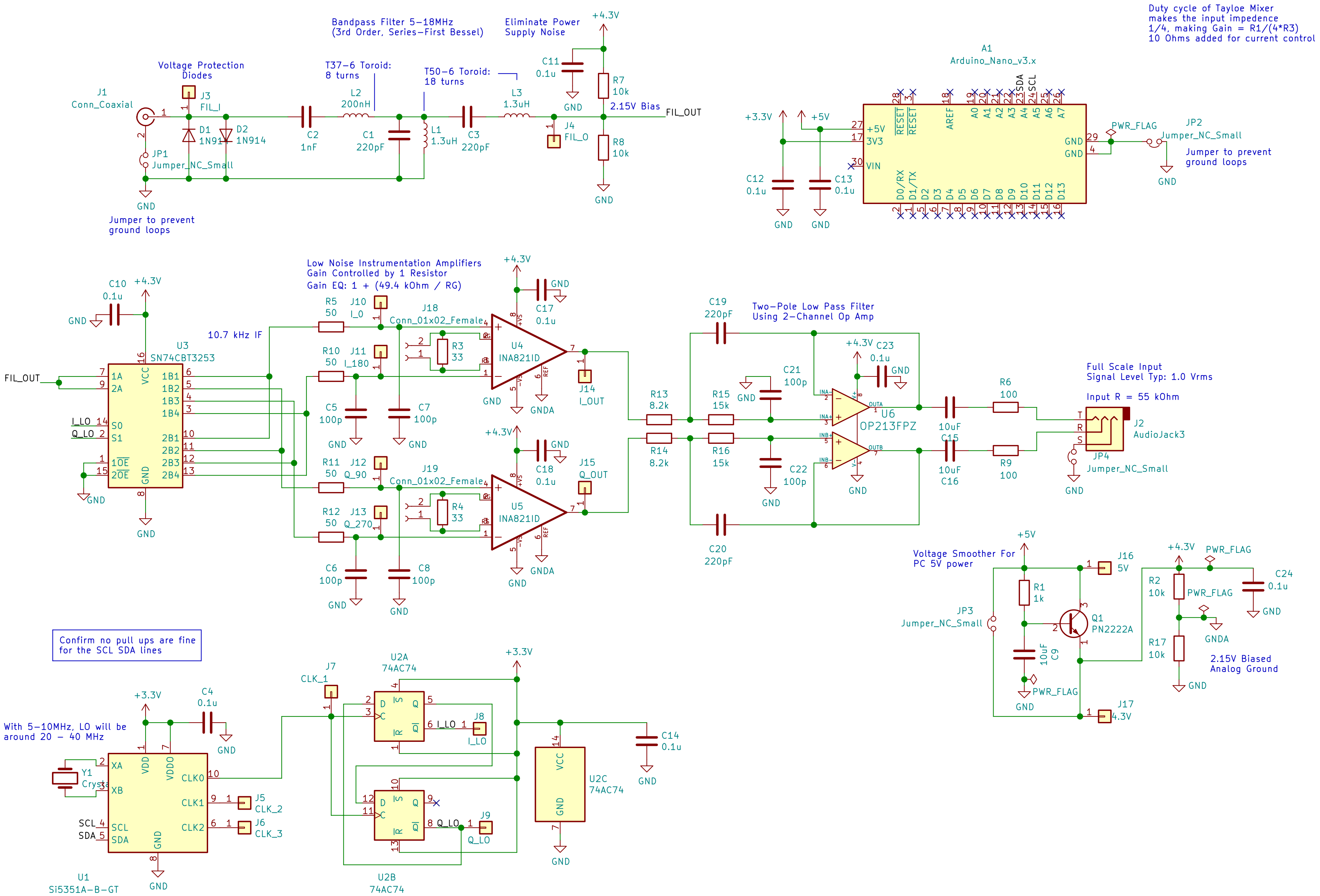
# Issues Encountered

- Bandpass filter response not as expected
  - Filter generation mistake. Values corrected for future revisions.

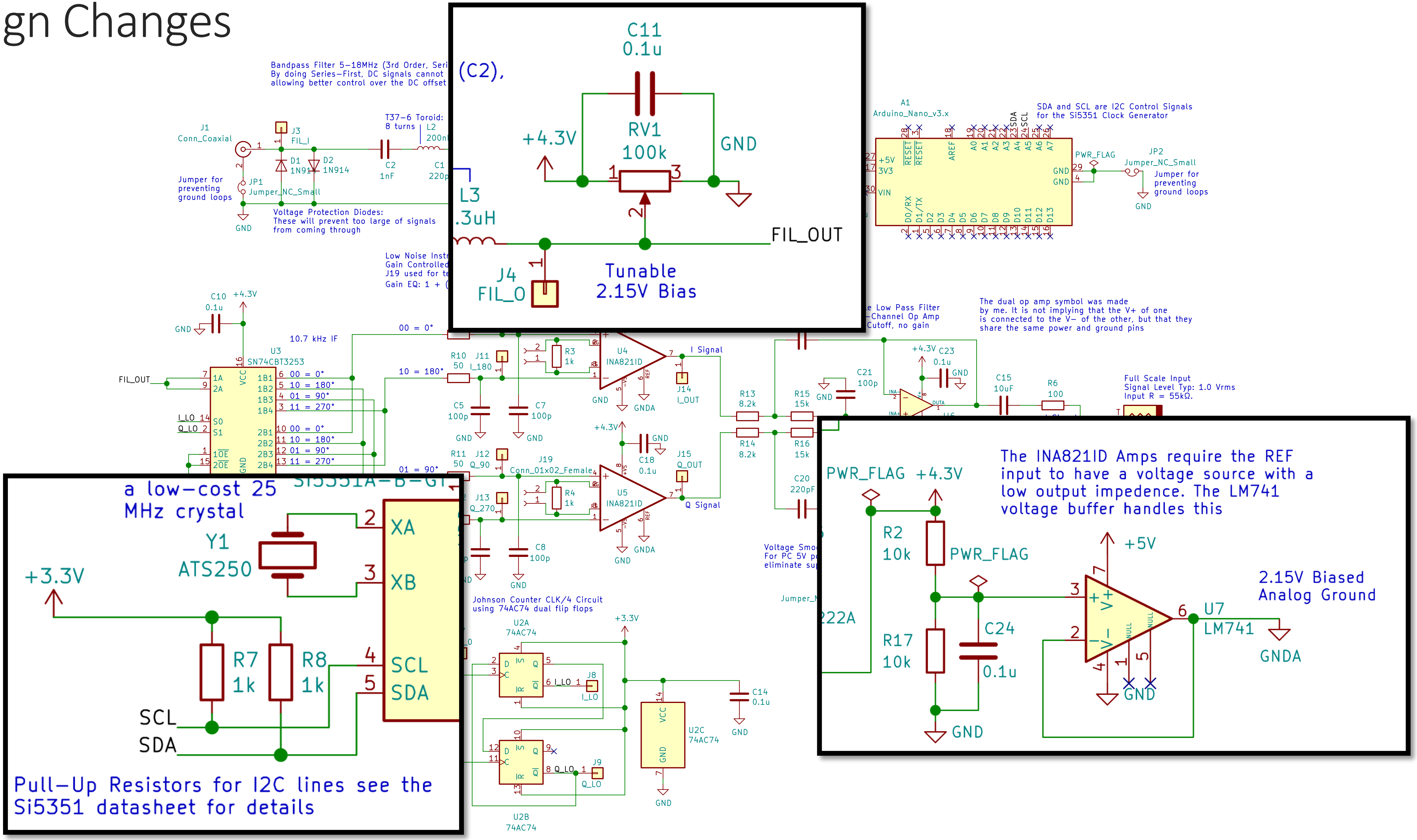
**Solution:** Regenerate the filter with corrected values. After testing in LTspice, the response is better than what we measured on ours.



# Design Changes



# Design Changes



# Results (Quisk)


Using Quisk we found our minimum discernable signal to be about 0.5uV

# Lessons Learned

- Document everything!
- Start a GitHub early!
- Compile a list of testing procedures.
- Test points and jumpers galore!

# Questions