

Attenuator Design Notes

Project Overview:

This stepped attenuator design is the first stepping stone in the design of an high frequency, Software-defined radio (SDR). Attenuators are very useful devices, and serve many purposes when working with RF devices. An attenuator can reduce a signal substantially and protect a circuit from receiving a signal that is too high to process. Additionally, attenuators are useful for improving input or output return loss of devices. This report describes the design of a simple step attenuator to be used with our HF SDR. My partner, Konrad McClure, and I worked together in the design and analysis of our stepped attenuator.

Design Goals:

The ultimate goal of this attenuator design was to produce Gerber files that would be used in the construction of our PCB board. A schematic and parts list were also required, and these were completed using KiCAD. The design criteria for our step attenuator were determined to be as follows:

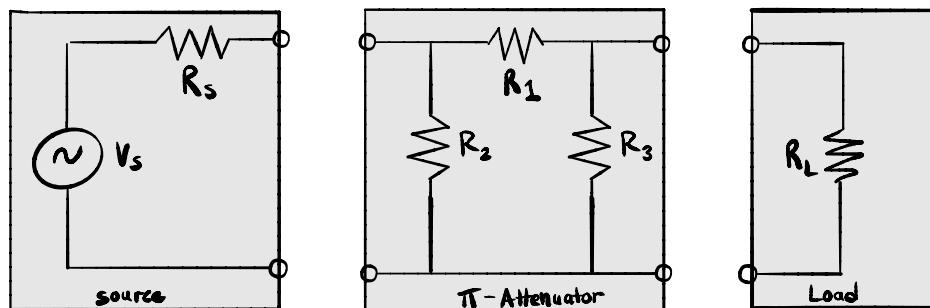
1. $V_{in\ rms} = \frac{5mV}{\sqrt{2}} = 3.5355\text{ mV}$
2. $V_{out\ rms} = 0.5\mu\text{V}$
3. gain; $A_V = \frac{0.5\mu\text{V}}{3.5355\text{ mV}} = 1.414227 \times 10^{-4}$
4. gain; dB = $20 \log_{10}(A_V) = -76.989\text{ dB}$
5. bandwidth: $0 \leq f \leq 30\text{ MHz}$
6. input/output impedance = 50Ω

Suggestions from our professor, Dr. Rob Froehne were as follows:

- * use at least 5 stages
- * use 0.1" headers and jumpers for switches
- * Model in LTSPICE

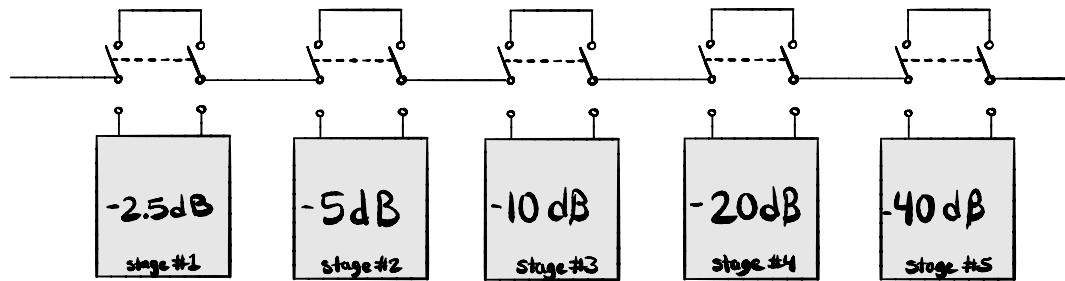
Design Ideas:

We decided to use a passive attenuator with purely resistive elements. As suggested in class we chose to use Π -attenuator pads. A sketch of a Π -attenuator is below:



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Design: We chose to use five (5) π -pad attenuators with the following dB attenuations:



this would give us a total dB gain of:

$$\text{total dB gain} = -77.5 \text{ dB}$$

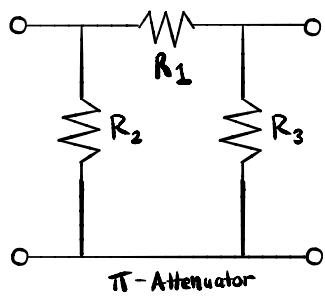
the gain in $\frac{V}{V}$ for each stage would be as follows:

$$A_v \text{ stage } \#1 = 10^{-2.5/20} = 0.74989 \frac{V}{V} \quad A_v \text{ stage } \#2 = 10^{-5/20} = 0.5623 \frac{V}{V}$$

$$A_v \text{ stage } \#3 = 10^{-10/20} = 0.316276 \frac{V}{V} \quad A_v \text{ stage } \#4 = 10^{-20/20} = 0.1 \frac{V}{V}$$

$$A_v \text{ stage } \#5 = 10^{-40/20} = 0.01 \frac{V}{V}$$

to choose the resistor values we used the equations below with the input and output impedance, $Z_{out} = Z_{in} = 50\Omega$.



$$R_1 = \frac{1}{2} \sqrt{Z_{in} \times Z_{out}} \left(\frac{K^2 - 1}{K} \right)$$

$$R_2 = Z_{in} \left(\frac{K^2 - 1}{K^2 - 2K \sqrt{Z_{in} \div Z_{out}} + 1} \right)$$

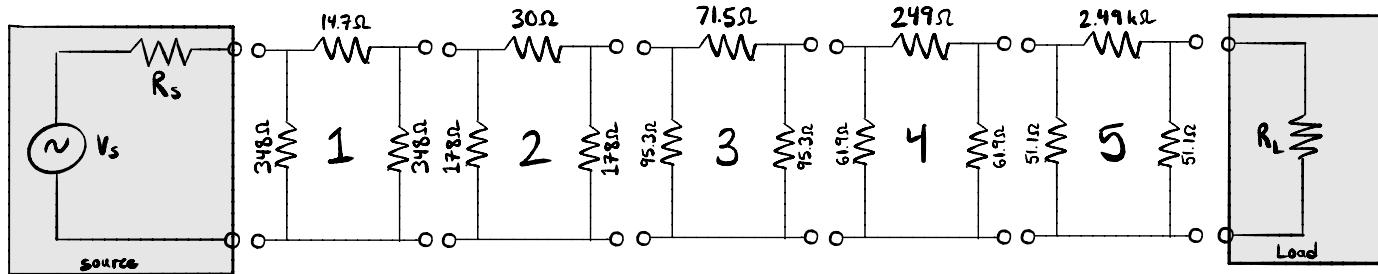
$$R_3 = Z_{out} \left(\frac{K^2 - 1}{K^2 - \frac{2K}{\sqrt{Z_{in} \div Z_{out}}} + 1} \right)$$

$$K = 10^{\frac{dB}{10}}, \text{ where } dB \text{ is desired attenuation.}$$

Using these equations, we completed designs for both 1% and 5% resistors. Simulation using LTSPICE confirmed that the input/output impedance was roughly 50Ω , as desired.

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Design: (1% Resistors)



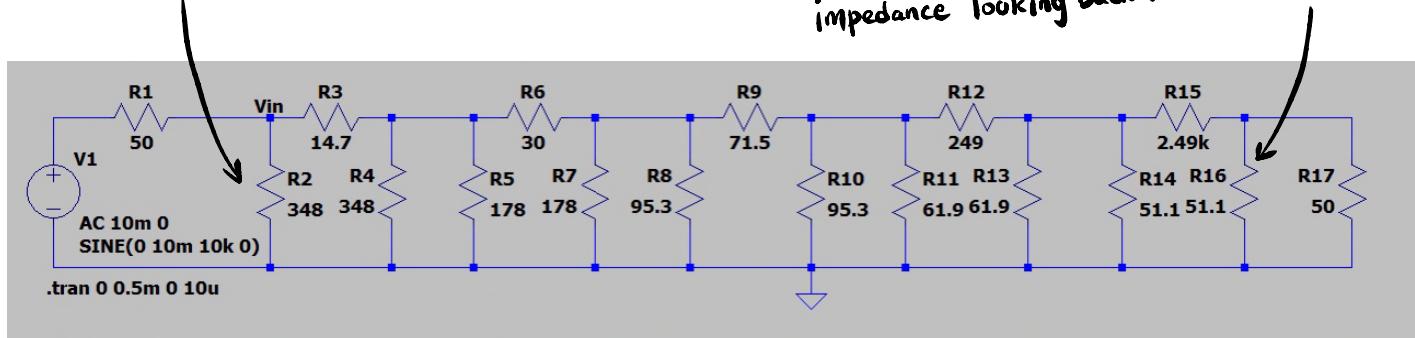
stage 1:	attenuation = 2.52 dB	input/output impedance = 50.022 Ω
stage 2:	attenuation = 4.97 dB	input/output impedance = 49.743 Ω
stage 3:	attenuation = 10.07 dB	input/output impedance = 49.797 Ω
stage 4:	attenuation = 19.95 dB	input/output impedance = 50.583 Ω
stage 5:	attenuation = 39.95 dB	input/output impedance = 50.083 Ω

$$\text{tot. attenuation} = 77.46 \text{ dB}$$

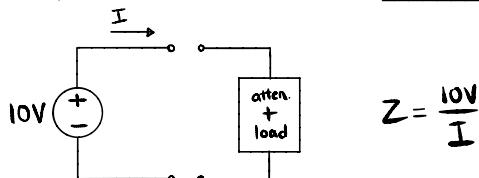
$$\text{avg. impedance} = 50.045 \Omega$$

input impedance via LTSPICE = -49.85Ω

impedance looking back into circuit = -50.041Ω



the impedance was calculated using Thevenin's theorem:

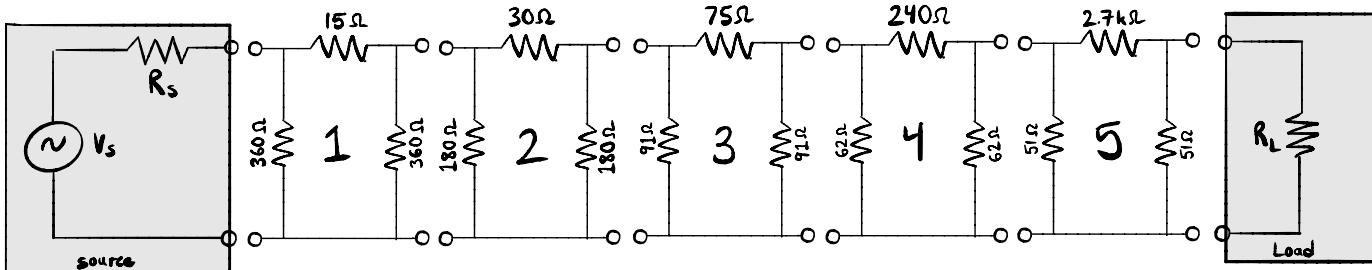


We put a 10V source in front of the attenuator network and measured the impedances listed above. A pictorial explanation of our method is seen to the left.

After consultation with our instructor, we redesigned the attenuator using 5% resistors. The 5% design is detailed on the next page:

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Design: (5% Resistors)

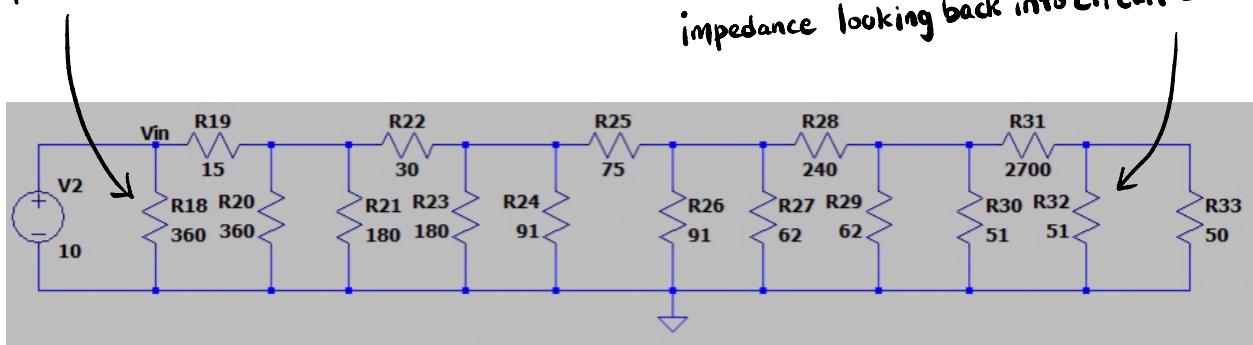


Stage 1:	attenuation = 2.5 dB	input/output impedance = 50.62 Ω
Stage 2:	attenuation = 4.95 dB	input/output impedance = 49.948 Ω
Stage 3:	attenuation = 10.5 dB	input/output impedance = 49.234 Ω
Stage 4:	attenuation = 19.68 dB	input/output impedance = 50.34 Ω
Stage 5:	attenuation = 40.66 dB	input/output impedance = 50.06 Ω

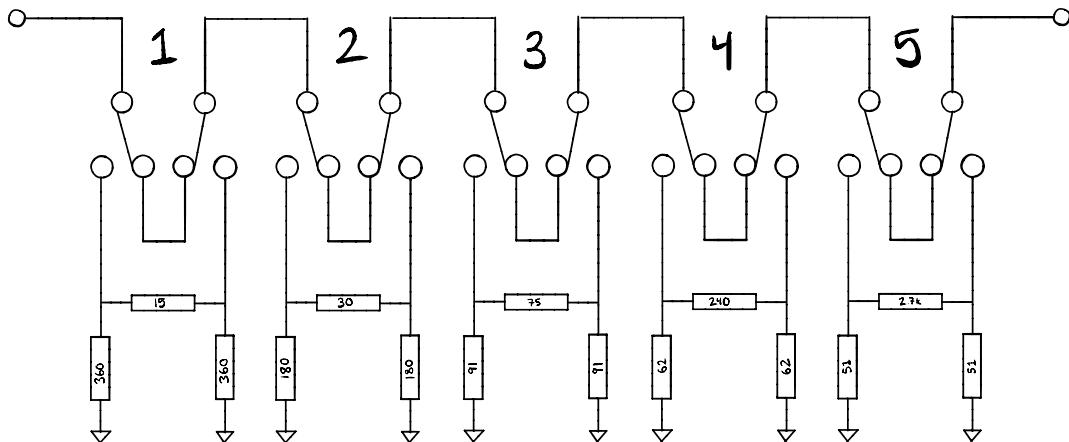
$$\text{tot. attenuation} = 78.29 \text{ dB}$$

input impedance via LTSPICE = -50.4 Ω

impedance looking back into circuit = -50.063 Ω

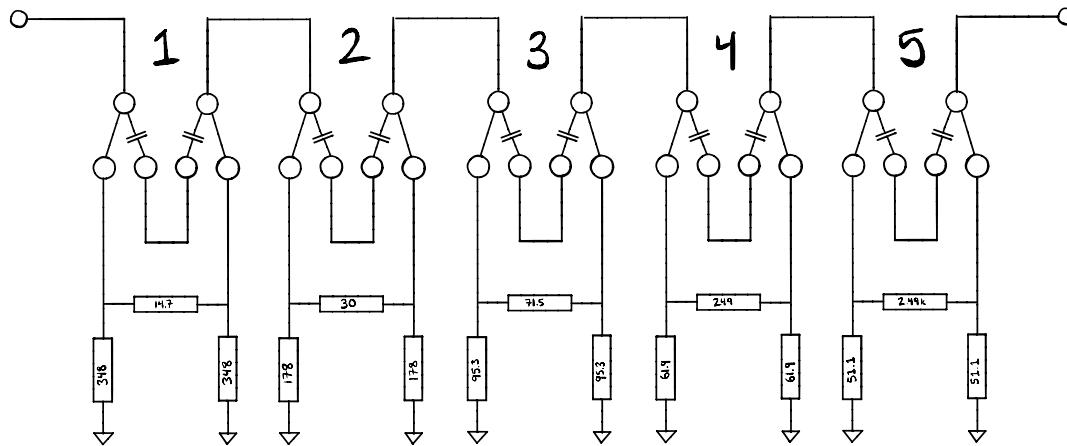


We wanted to use jumpers between the π -pad attenuators, thus, the design would look like below:

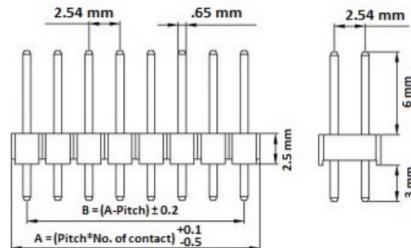


With a three pin switch, there is stray capacitance that can bypass the attenuator. With all of the jumpers connected to the attenuators, the capacitance between pins allows, at high frequencies, for the signal to bypass the attenuator network. This is pictured on the next page.

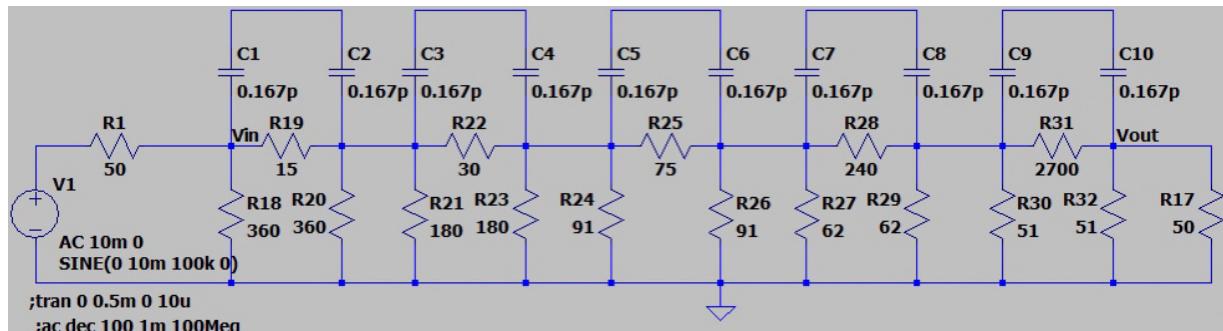
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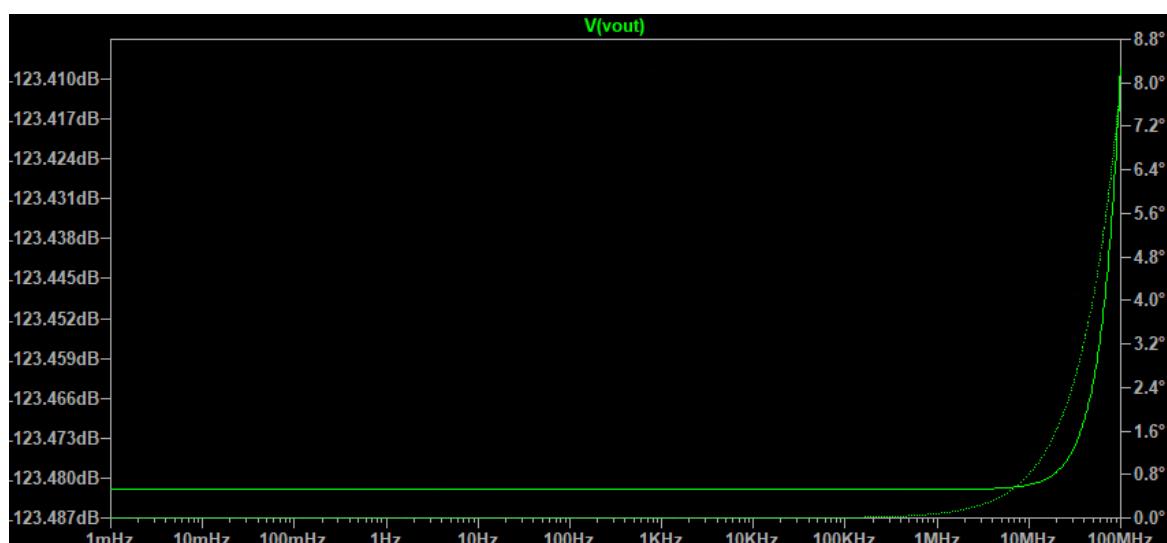
Our professor provided calculations to supply the capacitance between two pins. For the pin header dimensions as shown, the capacitance between two pins is: $C = 0.16667 \text{ pF}$.



To determine the effect of the capacitance between pins we modeled the worst case scenario using LTSPICE.



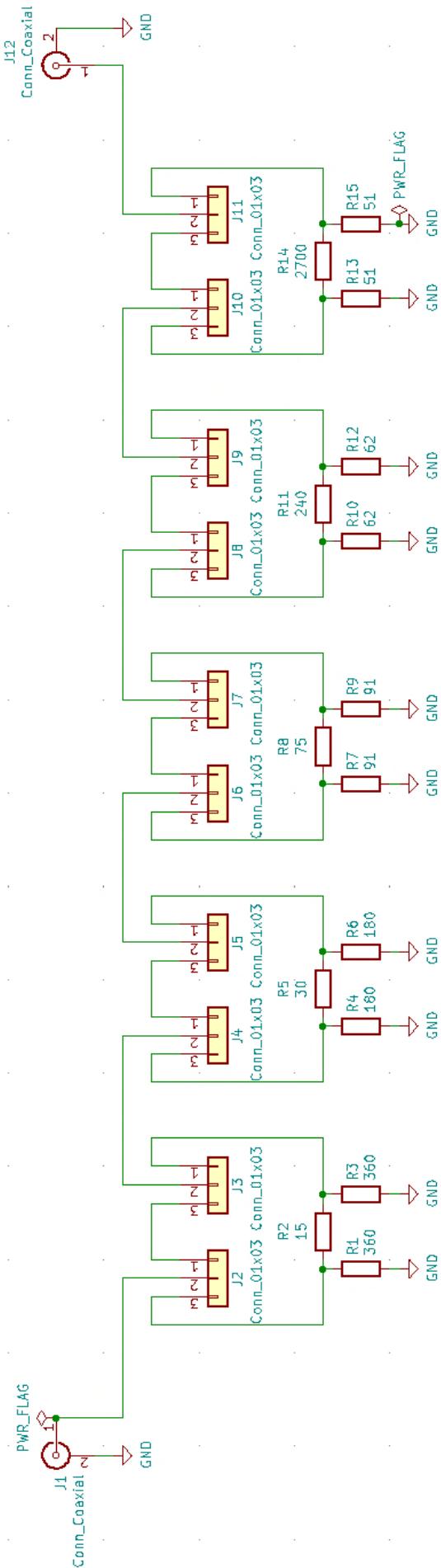
We simulated with an AC analysis over the frequency range from 1m to 100Meg. The resulting Bode plot is below:



Design: (5% Resistors) cont.

Through our analysis using LTSPICE we determined that the small capacitance between pins would not significantly affect the performance of our attenuator at high frequencies. Thus, we each proceeded with creating our KiCAD schematics and PCB board design. A couple pictures of my design are shown on the next page.

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