(1) Your name and student ID

Name:陳俊元 Student ID:110065536

(2) A comparison table like the following one, and an explanation of the result (The table should be built under a fixed core utilization and clock period and you should specify them in the report.)

Core utilization:0.93 clock period:20

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
Slack	18.106	18.096	18.039	18.113	18.039	18.113
Total wirelength(um)	286595	286833	282895	285171	282895.645	285171

(3) The difference(s) between the congestion-driven placement and timing-driven placement

timing-driven placement:

特別針對 timing critical 的 path 去做 placement，例如針對某 critical paths 去做 placement，來讓 critical 變短，但也許在我們針對某 critical path 變短的時候反而使別的 path 變長(變成 critical path)因此使用 timing-driven placement 時要特別注意 balance 的問題

Ref: https://www.cerc.utexas.edu/utda/publications/book_tdp.pdf

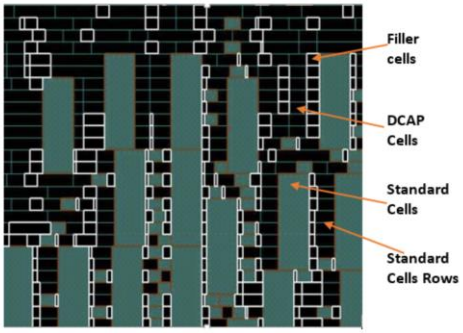
Congestion-driven placement:

簡單說就是讓 cell 排列的密度高或低，

Ref: https://chipedge.com/congestion-in-vlsi-physical-design-flow/

(4) An explanation of why we insert filler cells

當 P&R 完之後，cells 的中間還是會有一些間隔，而我們會用 filler cells(filler cells 是沒有作用的 cell) 幫助這些空格在適當的情況下填滿，而它的作用是穩定電壓和 clock



ref: https://www.physicaldesign4u.com/2019/12/physical-only-cells.html

(5) Show your best result (including clock period, total area, total wirelength, slack, congestion-driven effort and timing-driven on/off settings, and their snapshots) to maintain a non-negative slack and no DRC violation.

Nums Of attempts	Clock period(2x)	Core utilization	Timing driven	Congestion	Total area Of Chip(um^2)	Total wirelength (um)
1	10	0.93	1	High	41636.661	285170.820
2	10	0.95	0	Medium	40813.604	276601.335
3	8	0.99	0	Medium	39213.082	281950.192
4	8	0.97	0	Medium	39981.928	280004.400
5	1.8	0.96	0	Medium	40377.842	274580.875

Clock period:8

Total area:39981.928 um^2

Total wirelength:280004.400 um

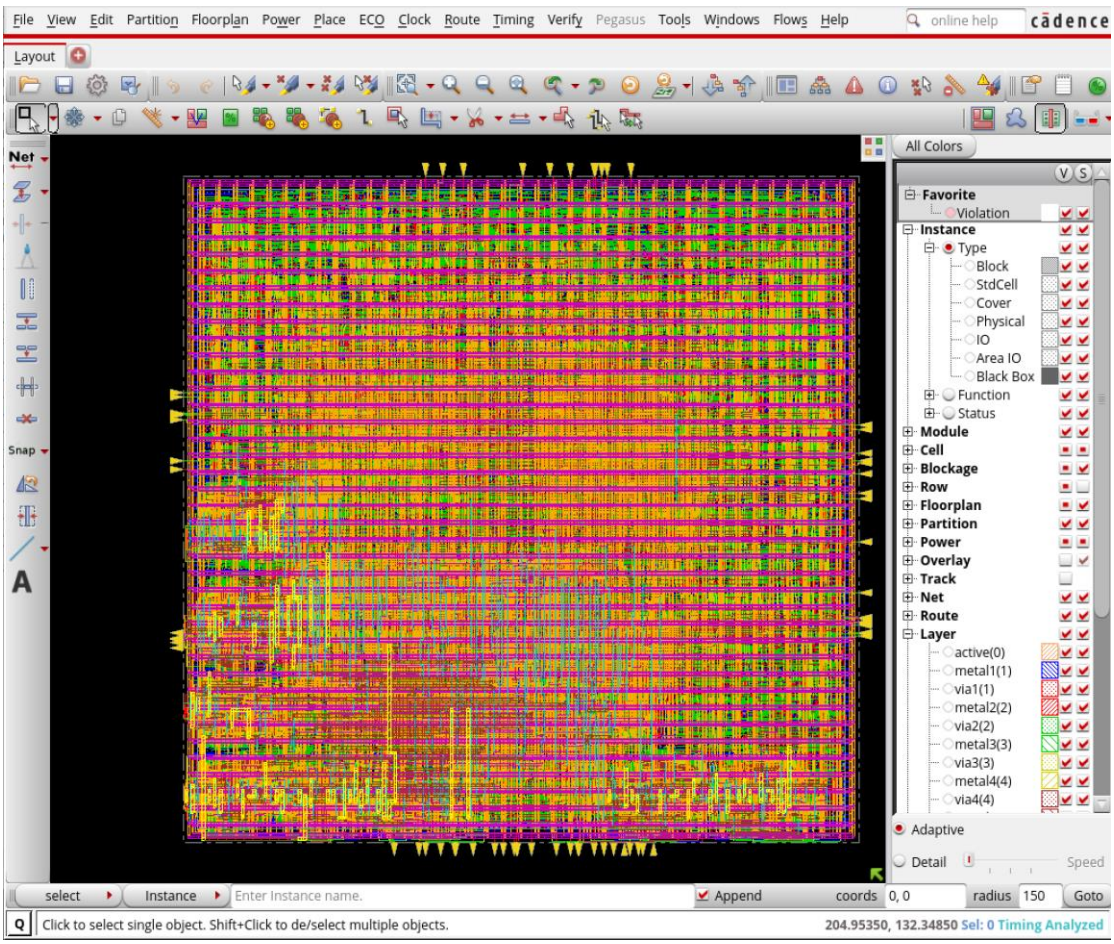
Slack:

```
Analysis View: generic_view
Other End Arrival Time          0.000
- Setup                         0.052
+ Phase Shift                   8.000
= Required Time                 7.948
- Arrival Time                  2.054
= Slack Time                    5.894
     Clock Rise Edge                     0.000
     + Clock Network Latency (Ideal)     0.000
     = Beginpoint Arrival Time           0.000
```

Congestion-driven : Medium

Timing-driven: off

Snapshots:



No DRC violation:

```
 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:03.0  ELAPSED TIME: 2.00  MEM: 0.0M) ***
```