Planning Pin and FPGA Resources

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This information is for board designers who need to determine the FPGA pin usage, to create the board layout for the system, as the board design process sometimes occurs concurrently with the RTL design process.

Use this document with the External Memory Interfaces chapter of the relevant device family handbook.

Typically, all external memory interfaces require the following FPGA resources:

- Interface pins
- PLL and clock network
- DLL
- Other FPGA resources—for example, core fabric logic, and on-chip termination (OCT) calibration blocks

After you know the requirements for your memory interface, you can start planning your system. The I/O pins and internal memory cannot be shared for other applications or memory interfaces. However, if you do not have enough PLLs, DLLs, or clock networks for your application, you may share these resources among multiple memory interfaces or modules in your system.

Ideally, any interface should reside entirely in a single bank; however, interfaces that span multiple adjacent banks or the entire side of a device are also fully supported. In addition, you may also have wraparound memory interfaces, where the design uses two adjacent sides of the device and the memory interface logic resides in a device quadrant. In some cases, top or bottom bank interfaces have higher supported clock rate than left or right or wraparound interfaces.

Interface Pins

Any I/O banks that do not support transceiver operations in Arria® II, Arria V, Stratix® III, Stratix IV, and Stratix V devices support memory interfaces. However, DQS (data strobe or data clock) and DQ (data) pins are listed in the device pin tables and fixed at specific locations in the device. You must adhere to these pin locations as these locations are optimized in routing to minimize skew and maximize margin. Always check the external memory interfaces chapters from the device handbooks for the number of DQS and DQ groups supported in a particular device and the pin table for the actual locations of the DQS and DQ pins.

For maximum performance and best skew across the interface, each required memory interface should completely reside within a single I/O bank, or at least one side of the device. Address and command pins can be constrained in a different side of the device if there are not enough pins available. For example, you may have the read and write data pins on the top side of the device, and have the address and command pins on the left side of the device. In memory interfaces with unidirectional data, you may also have all the

read data pins on the top side of the device and the write data pin on the left side of the device. However, you should not break a unidirectional pin group across multiple sides of the device. Memory interfaces typically have the following pin groups:

- Write data pin group and read data pin group
- Address and command pin group

The following table lists a summary of the number of pins required for various example memory interfaces. This table uses series OCT with calibration, parallel OCT with calibration, or dynamic calibrated OCT, when applicable, shown by the usage of R_{UP} and R_{DN} pins or RZQ pin.

Table 3-1: Pin Counts for Various Example Memory Interfaces *(1) (2)*

Memory Interface	FPGA DQS Bus Width	Number of DQ Pins	Number of DQS Pins	Number of DM/ BWSn Pins	Number of Address Pins *(3)*	Number of Command Pins	Number of Clock Pins	R_{UP}/R_{DN} Pins *(4)*	R_{ZQ} Pins *(11)*	Total Pins with R_{UP}/R_{DN}	Total Pins with R_{ZQ}
LPDDR2	×8	8	2	1	10	2	2	N/A	1	N/A	26
		16	4	2	10	2	2	N/A	1	N/A	37
		72	18	9	10	2	2	N/A	1	N/A	114
DDR3 SDRAM *(5) (6)*	×4	4	2	0 *(7)*	14	10	2	2	1	34	33
	×8	8	2	1	14	10	2	2	1	39	38
		16	4	2	14	10	2	2	1	50	49
		72	18	9	14	14	4	2	1	134	133
DDR2 SDRAM *(8)*	×4	4	1	1 *(7)*	15	9	2	2	1	34	33
	×8	8	1 *(9)*	1	15	9	2	2	1	38	37
		16	2 *(9)*	2	15	9	2	2	1	48	47
		72	9 *(9)*	9	15	12	6	2	1	125	124
DDR SDRAM *(6)*	×4	4	1	1 *(7)*	14	7	2	2	1	29	28
	×8	8	1	1	14	7	2	2	1	33	35
		16	2	2	14	7	2	2	1	43	42
		72	9	9	13	9	6	2	1	118	117
QDR II+ SRAM	×9	18	2	1	19	3 *(10)*	4	2	1	49	48
	×18	36	2	2	18	3 *(10)*	4	2	1	67	66
	×36	72	2	4	17	3 *(10)*	4	2	1	104	103

Memory Interface	FPGA DQS Bus Width	Number of DQ Pins	Number of DQS Pins	Number of DM/ BWSn Pins	Number of Address Pins (3)	Number of Command Pins	Number of Clock Pins	R_{UP}/R_{DN} Pins (4)	R_{ZQ} Pins (11)	Total Pins with R_{UP}/R_{DN}	Total Pins with R_{ZQ}
QDR II SRAM	×9	18	2	1	19	2	4	2	1	48	47
	×18	36	2	2	18	2	4	2	1	66	65
	×36	72	2	4	17	2	4	2	1	103	102
RLDRAM II CIO	×9	9	2	1	22	7 (10)	4	2	1	47	46
		18	2	1	21	7 (10)	6	2	1	57	56
	×18	36	2	1	20	7 (10)	8	2	1	76	75

Notes to table:

1. These example pin counts are derived from memory vendor data sheets. Check the exact number of addresses and command pins of the memory devices in the configuration that you are using.
2. PLL and DLL input reference clock pins are not counted in this calculation.
3. The number of address pins depend on the memory device density.
4. Some DQS or DQ pins are dual purpose and can also be required as R_{UP}, R_{DN}, or configuration pins. A DQS group is lost if you use these pins for configuration or as R_{UP} or R_{DN} pins for calibrated OCT. Pick R_{UP} and R_{DN} pins in a DQS group that is not used for memory interface purposes. You may need to place the DQS and DQ pins manually if you place the R_{UP} and R_{DN} pins in the same DQS group pins.
5. The TDQS and TDQS# pins are not counted in this calculation, as these pins are not used in the memory controller.
6. Numbers are based on 1-GB memory devices.
7. Altera® FPGAs do not support DM pins in ×4 mode with differential DQS signaling.
8. Numbers are based on 2-GB memory devices without using differential DQS, RDQS, and RDQS# pin support.
9. Assumes single ended DQS mode. DDR2 SDRAM also supports differential DQS, which makes these DQS and DM numbers identical to DDR3 SDRAM.
10. The QVLD pin that indicates read data valid from the QDR II+ SRAM or RLDRAM II device, is included in this number.
11. R_{ZQ} pins are supported by Arria V, Cyclone V, and Stratix V devices.

Note: Maximum interface width varies from device to device depending on the number of I/O pins and DQS or DQ groups available. Achievable interface width also depends on the number of address and command pins that the design requires. To ensure adequate PLL, clock, and device routing resources are available, you should always test fit any IP in the Quartus® II software before PCB sign-off.

Altera devices do not limit the width of external memory interfaces beyond the following requirements:

- Maximum possible interface width in any particular device is limited by the number of DQS groups available.
- Sufficient clock networks are available to the interface PLL as required by the IP.
- Sufficient spare pins exist within the chosen bank or side of the device to include all other address and command, and clock pin placement requirements.
- The greater the number of banks, the greater the skew, hence Altera recommends that you always generate a test project of your desired configuration and confirm that it meets timing.

Estimating Pin requirements

You should use the Quartus II software for final pin fitting; however, you can estimate whether you have enough pins for your memory interface using the following steps:

1. Find out how many read data pins are associated per read data strobe or clock pair, to determine which column of the DQS and DQ group availability (×4, ×8/×9, ×16/×18, or ×32/×36) look at the pin table.
2. Check the device density and package offering information to see if you can implement the interface in one I/O bank or on one side or on two adjacent sides.

   Note: If you target Arria II GX devices and you do not have enough I/O pins to have the memory interface on one side of the device, you may place them on the other side of the device. Arria II GX devices allow a memory interface to span across the top and bottom, or left and right sides of the device. For any interface that spans across two different sides, use the wraparound interface performance.

3. Calculate the number of other memory interface pins needed, including any other clocks (write clock or memory system clock), address, command, RUP, RDN, RZQ, and any other pins to be connected to the memory components. Ensure you have enough pins to implement the interface in one I/O bank or one side or on two adjacent sides.

   Note: The DQS groups in Arria II GX devices reside on I/O modules, each consisting of 16 I/O pins. You can only use a maximum of 12 pins per I/O modules when the pins are used as DQS or DQ pins or HSTL/SSTL output or HSTL/SSTL bidirectional pins. When counting the number of available pins for the rest of your memory interface, ensure you do not count the leftover four pins per I/O modules used for DQS, DQ, address and command pins. The leftover four pins can be used as input pins only.

   Note: Refer to the device pin-out tables and look for the blank space in the relevant DQS group column to identify the four pins that cannot be used in an I/O module for Arria II GX devices.

You should always try the proposed pin-outs with the rest of your design in the Quartus II software (with the correct I/O standard and OCT connections) before finalizing the pin-outs, as there may be some interactions between modules that are illegal in the Quartus II software that you may not find out unless you try compiling a design and use the Quartus II Pin Planner.

The following sections describe the pins for each memory interfaces.

DDR, DDR2, and DDR3 SDRAM Clock Signals

DDR, DDR2, and DDR3 SDRAM devices use CK and CK# signals to clock the address and command signals into the memory. Furthermore, the memory uses these clock signals to generate the DQS signal during a read through the DLL inside the memory. The SDRAM data sheet specifies the following timings:

- t_{DQSCK} is the skew between the CK or CK# signals and the SDRAM-generated DQS signal
- t_{DSH} is the DQS falling edge from CK rising edge hold time
- t_{DSS} is the DQS falling edge from CK rising edge setup time
- t_{DQSS} is the positive DQS latching edge to CK rising edge

These SDRAM have a write requirement (t_{DQSS}) that states the positive edge of the DQS signal on writes must be within ± 25% (± 90°) of the positive edge of the SDRAM clock input. Therefore, you should generate the CK and CK# signals using the DDR registers in the IOE to match with the DQS signal and reduce any variations across process, voltage, and temperature. The positive edge of the SDRAM clock, CK, is aligned with the DQS write to satisfy t_{DQSS}.

DDR3 SDRAM can use a daisy-chained control address command (CAC) topology, in which the memory clock must arrive at each chip at a different time. To compensate for this flight-time skew between devices across a typical DIMM, write leveling must be employed.

DDR, DDR2, and DDR3 SDRAM Command and Address Signals

Command and address signals in SDRAM devices are clocked into the memory device using the CK or CK# signal. These pins operate at single data rate (SDR) using only one clock edge. The number of address pins depends on the SDRAM device capacity. The address pins are multiplexed, so two clock cycles are required to send the row, column, and bank address.

The CS#, RAS, CAS, WE, CKE, and ODT pins are SDRAM command and control pins. DDR3 SDRAM has an additional pin, RESET#, while some DDR3 DIMMs have these additional pins: RESET#, PAR_IN, and ERR_OUT#. The RESET# pin uses the 1.5-V LVCMOS I/O standard, and the PAR_IN and ERR_OUT# pins use the SSTL-15 I/O standard.

The DDR2 SDRAM command and address inputs do not have a symmetrical setup and hold time requirement with respect to the SDRAM clocks, CK, and CK#.

For Altera SDRAM high-performance controllers in Stratix III and Stratix IV devices, the command and address clock is a dedicated PLL clock output whose phase can be adjusted to meet the setup and hold requirements of the memory clock. The command and address clock is also typically half-rate, although a full-rate implementation can also be created. The command and address pins use the DDIO output circuitry to launch commands from either the rising or falling edges of the clock. The chip select (mem_cs_n), clock enable (mem_cke), and ODT (mem_odt) pins are only enabled for one memory clock cycle and can be launched from either the rising or falling edge of the command and address clock signal. The address and other command pins are enabled for two memory clock cycles and can also be launched from either the rising or falling edge of the command and address clock signal.

In Arria II GX devices, the command and address clock is either shared with the write_clk_2x or the mem_clk_2x clock.

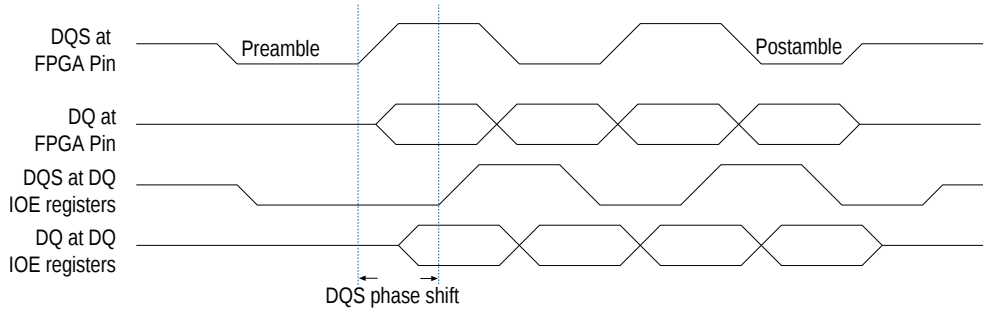
DDR, DDR2, and DDR3 SDRAM Data, Data Strobes, DM, and Optional ECC Signals

DDR SDRAM uses bidirectional single-ended data strobe (DQS); DDR3 SDRAM uses bidirectional differential data strobes. The DQSn pins in DDR2 SDRAM devices are optional but recommended for DDR2 SDRAM designs operating at more than 333 MHz. Differential DQS operation enables improved system timing due to reduced crosstalk and less simultaneous switching noise on the strobe output drivers. The DQ pins are also bidirectional.

Regardless of interface width, DDR SDRAM always operates in ×8 mode DQS groups. DQ pins in DDR2 and DDR3 SDRAM interfaces can operate in either ×4 or ×8 mode DQS groups, depending on your chosen memory device or DIMM, regardless of interface width. The ×4 and ×8 configurations use one pair of bidirectional data strobe signals, DQS and DQSn, to capture input data. However, two pairs of data strobes, UDQS and UDQS# (upper byte) and LDQS and LDQS# (lower byte), are required by the ×16 configuration devices. A group of DQ pins must remain associated with its respective DQS and DQSn pins.

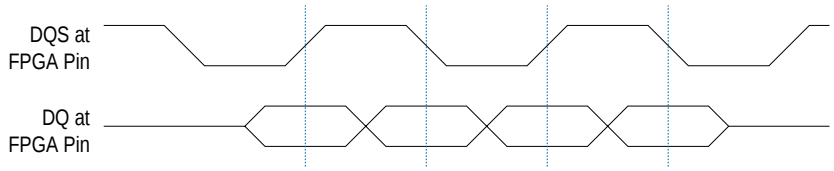
The DQ signals are edge-aligned with the DQS signal during a read from the memory and are center-aligned with the DQS signal during a write to the memory. The memory controller shifts the DQ signals by –90 degrees during a write operation to center align the DQ and DQS signals. The PHY IP delays the DQS signal during a read, so that the DQ and DQS signals are center aligned at the capture register. Altera devices use a phase-locked loop (PLL) to center-align the DQS signal with respect to the DQ signals during writes and Altera devices use dedicated DQS phase-shift circuitry to shift the incoming DQS signal during reads. The following figure shows an example where the DQS signal is shifted by 90 degrees for a read from the DDR2 SDRAM.

Figure 3-1: Edge-aligned DQ and DQS Relationship During a DDR2 SDRAM Read in Burst-of-Four Mode



The following figure shows an example of the relationship between the data and data strobe during a burst-of-four write.

Figure 3-2: DQ and DQS Relationship During a DDR2 SDRAM Write in Burst-of-Four Mode



The memory device's setup (t_{DS}) and hold times (t_{DH}) for the write DQ and DM pins are relative to the edges of DQS write signals and not the CK or CK# clock. Setup and hold requirements are not necessarily balanced inDDR2 and DDR3 SDRAM, unlike in DDR SDRAM devices.

The DQS signal is generated on the positive edge of the system clock to meet the t_{DQSS} requirement. DQ and DM signals use a clock shifted –90 from the system clock, so that the DQS edges are centered on the DQ or DM signals when they arrive at the DDR2 SDRAM. The DQS, DQ, and DM board trace lengths need to be tightly matched (within 20 ps).

The SDRAM uses the DM pins during a write operation. Driving the DM pins low shows that the write is valid. The memory masks the DQ signals if the DM pins are driven high. To generate the DM signal, Altera recommends that you use the spare DQ pin within the same DQS group as the respective data, to minimize skew.

The DM signal's timing requirements at the SDRAM input are identical to those for DQ data. The DDR registers, clocked by the –90 degree shifted clock, create the DM signals.

Some SDRAM modules support error correction coding (ECC) to allow the controller to detect and automatically correct error in data transmission. The 72-bit SDRAM modules contain eight extra data pins in addition to 64 data pins. The eight extra ECC pins should be connected to a single DQS or DQ group on the FPGA.

DDR, DDR2, and DDR3 SDRAM DIMM Options

Unbuffered DIMMs (UDIMMs) require one set of chip-select (CS#), on-die termination (ODT), clock-enable (CKE#), and clock pair (CK/CKn) for every physical rank on the DIMM. Registered DIMMs use only one pair of clocks and require a minimum of two chip-select signals, even in the case of a single rank RDIMM.

Compared to the unbuffered DIMMs (UDIMM), registered and load-reduced DIMMs (RDIMMs and LRDIMMs, respectively) use only one pair of clocks and at least two chip-select signals CS#[1:0] in DDR3. Both RDIMMs and LRDIMMs require an additional parity signal for address, RAS, CAS, and WE signals.

Unbuffered DIMMs require unique chip-select, ODT, CKE, and clock pair signals for every rank on the DIMM. RDIMMs differ slightly in that only one clock pair is required for the entire module and a minimum of two chip select signals must be present (even for single-rank DIMMs) for programming of the RDIMM buffer.

LRDIMMs expand on the operation of RDIMMs by buffering the DQ/DQS bus. Only one electrical load is presented to the controller regardless of the number of ranks, therefore only one clock enable and ODT signal are required for LRDIMMs, regardless of the number of physical ranks. Because the number of physical ranks may exceed the number of physical chip-select signals, LRDIMMs provide a feature known as rank multiplication, which aggregates two or four physical ranks into one larger logical rank. Refer to LRDIMM buffer documentation for details on rank multiplication.

Both RDIMMs and LRDIMMs require an additoinal parity input for address, RAS#, CAS#, and WE# signals. A parity error signal is asserted by the module whenever a parity error is detected.

The following table shows UDIMM and RDIMM pin options.

Table 3-2: UDIMM and RDIMM Pin Options

Pins	UDIMM Pins (Single Rank)	UDIMM Pins (Dual Rank)	RDIMM Pins (Single Rank)	RDIMM Pins (Dual Rank)
Data	72 bit DQ[71:0] = {CB[7:0], DQ[63:0]}	72 bit DQ[71:0] = {CB[7:0], DQ[63:0]}	72 bit DQ[71:0] = {CB[7:0], DQ[63:0]}	72 bit DQ[71:0]= {CB[7:0], DQ[63:0]}
Data Mask	DM[8:0]	DM[8.0]	DM[8.0]	DM[8.0]
Data Strobe (1)	DQS[8:0] and DQS#[8:0]	DQS[8:0] and DQS#[8:0]	DQS[8:0] and DQS#[8:0]	DQS[8:0] and DQS#[8:0]
Address	BA[2:0], A[15:0]– 2 GB: A[13:0] 4 GB: A[14:0] 8 GB: A[15:0]	BA[2:0], A[15:0]– 2 GB: A[13:0] 4 GB: A[14:0] 8 GB: A[15:0]	BA[2:0], A[15:0]– 2 GB: A[13:0] 4 GB: A[14:0] 8 GB: A[15:0]	BA[2:0], A[15:0]– 2 GB: A[13:0] 4 GB: A[14:0] 8 GB: A[15:0]
Clock	CK0/CK0#	CK0/CK0#, CK1/CK1#	CK0/CK0#	CK0/CK0#
Command	ODT, CS#, CKE, RAS#, CAS#, WE#	ODT[1:0], CS#[1:0], CKE[1:0], RAS#, CAS#, WE#	ODT, CS#[1:0], CKE, RAS#, CAS#, WE#	ODT[1:0], CS#[1:0], CKE[1:0], RAS#, CAS#, WE#
Parity	—	—	PAR_IN, ERR_OUT	PAR_IN, ERR_OUT

Pins	UDIMM Pins (Single Rank)	UDIMM Pins (Dual Rank)	RDIMM Pins (Single Rank)	RDIMM Pins (Dual Rank)
Other Pins	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#

Note to Table:

1. DQS#[8:0] is optional in DDR2 SDRAM and is not supported in DDR SDRAM interfaces.

The following table shows LRDIMM pin options.

Table 3-3: LRDIMM Pin Options

Pins	LRDIMM Pins (2R)	LRDIMM (4R, RM=1)	LRDIMM Pins (4R, RM=2)	LRDIMM Pins (8R, RM=2)	LDIMM Pins (8R, RM=4)
Data	72 bit DQ [71:0]={CB [7:0], DQ [63:0]}	72 bit DQ [71:0]={CB [7:0], DQ [63:0]}	72 bit DQ [71:0]={CB [7:0], DQ [63:0]}	72 bit DQ [71:0]={CB [7:0], DQ [63:0]}	72 bit DQ [71:0]={CB [7:0], DQ [63:0]}
Data Mask	—	—	—	—	—
Data Strobe	DQS[17:0] and DQS#[17:0]	DQS[17:0] and DQS#[17:0]	DQS[17:0] and DQS#[17:0]	DQS[17:0] and DQS#[17:0]	DQS[17:0] and DQS#[17:0]
Address	BA[2:0], A[15:0] -2GB:A[13:0] 4GB:A[14:0] 8GB:A[15:0]	BA[2:0], A[15:0] -2GB:A[13:0] 4GB:A[14:0] 8GB:A[15:0]	BA[2:0], A[16:0] -4GB:A[14:0] 8GB:A[15:0] 16GB:A[16:0]	BA[2:0], A[16:0] -4GB:A[14:0] 8GB:A[15:0] 16GB:A[16:0]	BA[2:0], A[17:0] -16GB:A[15:0] 32GB:A[16:0] 64GB:A[17:0]
Clock	CK0/CK0#	CK0/CK0#	CK0/CK0#	CK0/CK0#	CK0/CK0#
Command	ODT, CS[1:0]#, CKE, RAS#, CAS#, WE#	ODT, CS[3:0]#, CKE, RAS#, CAS#, WE#	ODT, CS[1:0]#, CKE, RAS#, CAS#, WE#	ODT, CS[3:0]#, CKE, RAS#, CAS#, WE#	ODT, CS[1:0]#, CKE, RAS#, CAS#, WE#
Parity	PAR_IN, ERR_OUT	PAR_IN, ERR_OUT	PAR_IN, ERR_OUT	PAR_IN, ERR_OUT	PAR_IN, ERR_OUT
Other Pins	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#	SA[2:0], SDA, SCL, EVENT#, RESET#

Notes to Table:

1. DM pins are not used for LRDIMMs because they are constructed using ×4 components for greater memory density.
2. CS2# is treated as A[16] and CS3# is treated as A[17] for certain rank multiplication configurations. Consult LRDIMM documentation for details.

QDR II+ and QDR II SRAM Clock Signals

QDR II+ and QDR II SRAM devices have three pairs of clocks, listed below.

- Input clocks K and K#
- Input clocks C and C#
- Echo clocks CQ and CQ#

The positive input clock, K, is the logical complement of the negative input clock, K#. Similarly, C and CQ are complements of C# and CQ#, respectively. With these complementary clocks, the rising edges of each clock leg latch the DDR data.

The QDR II+ and QDR II SRAM devices use the K and K# clocks for write access and the C and C# clocks for read accesses only when interfacing more than one QDR II+ or QDR II SRAM device. Because the number of loads that the K and K# clocks drive affects the switching times of these outputs when a controller drives a single QDR II+ or QDR II SRAM device, C and C# are unnecessary. This is because the propagation delays from the controller to the QDR II+ or QDR II SRAM device and back are the same. Therefore, to reduce the number of loads on the clock traces, QDR II+ and QDR II SRAM devices have a single clock mode, and the K and K# clocks are used for both reads and writes. In this mode, the C and C# clocks are tied to the supply voltage (VDD).

CQ and CQ# are the source-synchronous output clocks from the QDR II or QDR II+ SRAM device that accompanies the read data.

The Altera device outputs the K and K# clocks, data, address, and command lines to the QDR II+ or QDR II SRAM device. For the controller to operate properly, the write data (D), address (A), and control signal trace lengths (and therefore the propagation times) should be equal to the K and K# clock trace lengths.

You can generate C, C#, K, and K# clocks using any of the PLL registers via the DDR registers. Because of strict skew requirements between K and K# signals, use adjacent pins to generate the clock pair. The propagation delays for K and K# from the FPGA to the QDR II+ or QDR II SRAM device are equal to the delays on the data and address (D, A) signals. Therefore, the signal skew effect on the write and read request operations is minimized by using identical DDR output circuits to generate clock and data inputs to the memory.

QDR II+ and QDR II SRAM Command Signals

QDR II+ and QDR II SRAM devices use the write port select (WPSn) signal to control write operations and the read port select (RPSn) signal to control read operations.

The byte write select signal (BWSn) is a third control signal that indicates to the QDR II+ or QDR II SRAM device which byte to write into the QDR II+ or QDR II SRAM device. You can use any of the FPGA's user I/O pins to generate control signals, preferably on the same side and the same bank. Assign the BWSn pin within the same DQS group as the corresponding the write data.

QDR II+ and QDR II SRAM Address Signals

QDR II+ and QDR II SRAM devices use one address bus (A) for both read and write addresses. You can use any of the FPGA's user I/O pins to generate address signals, preferably on the same side and the same banks.

QDR II+ and QDR II SRAM Data and QVLD Signals

QDR II+ and QDR II SRAM devices use two unidirectional data buses: one for writes (D) and one for reads (Q).

The read data is edge-aligned with the CQ and CQ# clocks while the write data is center-aligned with the K and K# clocks (see the following figures).

Figure 3-3: Edge-aligned CQ and Q Relationship During QDR II+ SRAM Read

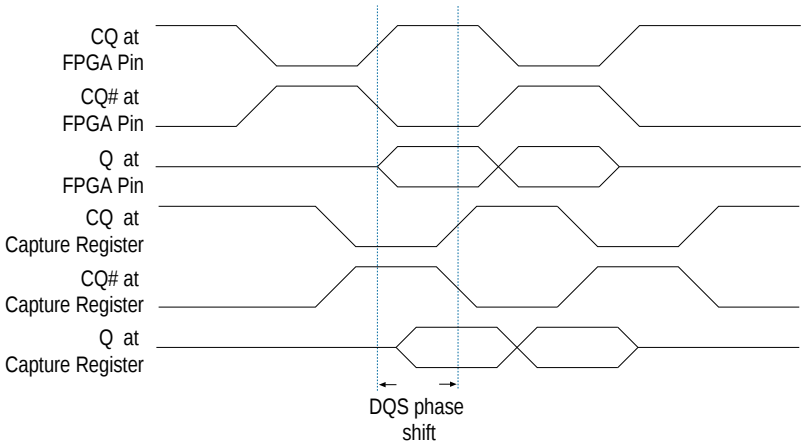
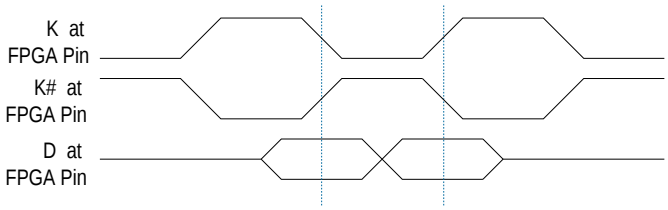


Figure 3-4: Center-aligned K and D Relationship During QDR II+ SRAM Write



QDR II+ SRAM devices also have a QVLD pin that indicates valid read data. The QVLD signal is edge-aligned with the echo clock and is asserted high for approximately half a clock cycle before data is output from memory.

Note: The Altera QDR II+ SRAM Controller with UniPHY IP does not use the QVLD signal.

RLDRAM II and RLDRAM 3 Clock Signals

RLDRAM II and RLDRAM 3 devices use CK and CK# signals to clock the command and address bus in single data rate (SDR). There is one pair of CK and CK# pins per RLDRAM II or RLDRAM 3 device.

Instead of a strobe, RLDRAM II and RLDRAM 3 devices use two sets of free-running differential clocks to accompany the data. The DK and DK# clocks are the differential input data clocks used during writes while the QK or QK# clocks are the output data clocks used during reads. Even though QK and QK# signals are not differential signals according to the RLDRAM II and RLDRAM 3 data sheets, Micron treats these signals as such for their testing and characterization. Each pair of DK and DK#, or QK and QK# clocks are associated with either 9 or 18 data bits.

The exact clock-data relationships are as follows:

- RLDRAM II: For ×36 data bus width configuration, there are 18 data bits associated with each pair of write and read clocks. So, there are two pairs of DK and DK# pins and two pairs of QK or QK# pins.
- RLDRAM 3: For ×36 data bus width configuration, there are 18 data bits associated with each pair of write clocks. There are 9 data bits associated with each pair of read clocks. So, there are two pairs of DK and DK# pins and four pairs of QK and QK# pins.
- RLDRAM II: For ×18 data bus width configuration, there are 18 data bits per one pair of write clocks and nine data bits per one pair of read clocks. So, there is one pair of DK and DK# pins, but there are two pairs of QK and QK# pins.
- RLDRAM 3: For ×18 data bus width configuration, there are 9 data bits per one pair of write clocks and nine data bits per one pair of read clocks. So, there are two pairs of DK and DK# pins, and two pairs of QK and QK# pins
- RLDRAM II: For ×9 data bus width configuration, there are nine data bits associated with each pair of write and read clocks. So, there is one pair of DK and DK# pins and one pair of QK and QK# pins each.
- RLDRAM 3: RLDRAM 3 does not have the ×9 data bus width configuration.

There are t_{CKDK} timing requirements for skew between CK and DK or CK# and DK#.

For both RLDRAM II and RLDRAM 3, because of the loads on these I/O pins, the maximum frequency you can achieve depends on the number of memory devices you are connecting to the Altera device. Perform SPICE or IBIS simulations to analyze the loading effects of the pin-pair on multiple RLDRAM II devices.

RLDRAM II and RLDRAM 3 Commands and Addresses

The CK and CK# signals clock the commands and addresses into the memory devices.

These pins operate at single data rate using only one clock edge. RLDRAM II and RLDRAM 3 support both non-multiplexed and multiplexed addressing. Multiplexed addressing allows you to save a few user I/O pins while non-multiplexed addressing allows you to send the address signal within one clock cycle instead of two clock cycles. CS#, REF#, and WE# pins are input commands to the RLDRAM II or RLDRAM 3 device.

The commands and addresses must meet the memory address and command setup (t_{AS}, t_{CS}) and hold (t_{AH}, t_{CH}) time requirements.

Note: UniPHY IP does not support multiplexed addressing.

RLDRAM II and RLDRAM 3 Data, DM and QVLD Signals

The read data is edge-aligned with the QK or QK# clocks while the write data is center-aligned with the DK and DK# clocks (see the following figures). The memory controller shifts the DK or DK# signal to center align the DQ and DK or DK# signal during a write and to shift the QK signal during a read, so that read data (DQ or Q signals) and QK clock is center-aligned at the capture register.

Altera devices use dedicated DQS phase-shift circuitry to shift the incoming QK signal during reads and use a PLL to center-align the DK and DK# signals with respect to the DQ signals during writes.

Figure 3-5: Edge-aligned DQ and QK Relationship During RLDRAM II or RLDRAM 3 Read

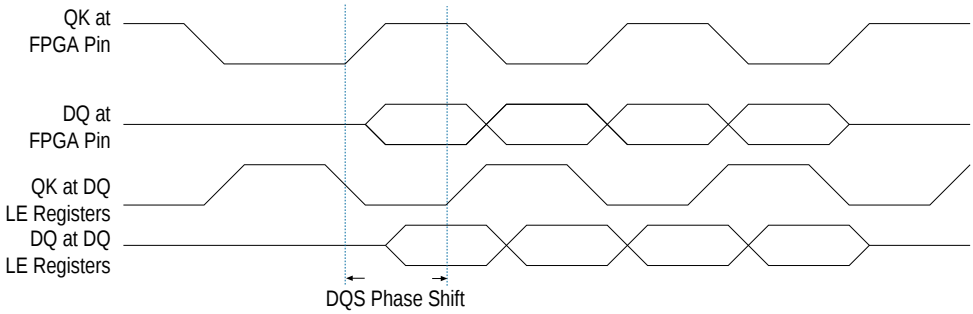
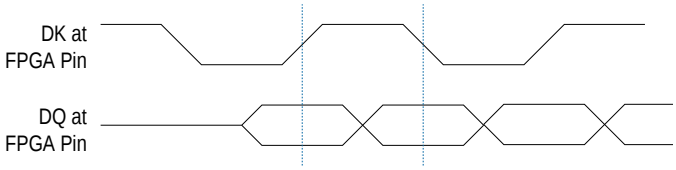


Figure 3-6: Center-aligned DQ and DK Relationship During RLDRAM II or RLDRAM 3 Write



For RLDRAM II and RLDRAM 3, data mask (DM) pins are only used during a write. The memory controller drives the DM signal low when the write is valid and drives it high to mask the DQ signals. There is one DM pin per memory device.

The DM timing requirements at the input to the memory device are identical to those for DQ data. The DDR registers, clocked by the write clock, create the DM signals. This reduces any skew between the DQ and DM signals.

The RLDRAM II or RLDRAM 3 device's setup time (t_{DS}) and hold (t_{DH}) time for the write DQ and DM pins are relative to the edges of the DK or DK# clocks. The DK and DK# signals are generated on the positive edge of system clock, so that the positive edge of CK or CK# is aligned with the positive edge of DK or DK# respectively to meet the tCKDK requirement. The DQ and DM signals are clocked using a shifted clock so that the edges of DK or DK# are center-aligned with respect to the DQ and DM signals when they arrive at the RLDRAM II or RLDRAM 3 device.

The clocks, data, and DM board trace lengths should be tightly matched to minimize the skew in the arrival time of these signals.

RLDRAM II and RLDRAM 3 devices also have a QVLD pin indicating valid read data. The QVLD signal is edge-aligned with QK or QK# and is high approximately half a clock cycle before data is output from the memory.

Note: The RLDRAM II Controller with UniPHY IP and the RLDRAM 3 PHY-only IP do not use the QVLD signal.

LPDDR2 Clock Signal

CK and CKn are differential clock inputs to the LPDDR2 interface. All the double data rate (DDR) inputs are sampled on both the positive and negative edges of the clock. Single data rate (SDR) inputs, CSn and CKE, are sampled at the positive clock edge.

The clock is defined as the differential pair which consists of CK and CKn. The positive clock edge is defined by the cross point of a rising CK and a falling CKn. The negative clock edge is defined by the cross point of a falling CK and a rising CKn.

The SDRAM data sheet specifies timing data for the following:

- t_{DSH} is the DQS falling edge hold time from CK.
- t_{DSS} is the DQS falling edge to the CK setup time.
- t_{DQSS} is the Write command to the first DQS latching transition.
- t_{DQSCK} is the DQS output access time from CK_t/CK_c.

LPDDR2 Command and Address Signal

All LPDDR2 devices use double data rate architecture on the command/address bus to reduce the number of input pins in the system. The 10-bit command/address bus contains command, address, and bank/row buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edges of the clock.

LPDDR2 Data, Data Strobe, and DM Signals

LPDDR2 devices use bidirectional and differential data strobes.

Differential DQS operation enables improved system timing due to reduced crosstalk and less simultaneous switching noise on the strobe output drivers. The DQ pins are also bidirectional. DQS is edge-aligned during the read data and centered during the write data.

DM is the input mask for the write data signal. Input data is masked when DM is sampled high coincident with that input data during a write access.

Maximum Number of Interfaces

The maximum number of interfaces supported for a given memory protocol varies, depending on the FPGA in use.

Unless otherwise noted, the calculation for the maximum number of interfaces is based on independent interfaces where the address or command pins are not shared. The maximum number of independent interfaces is limited to the number of PLLs each FPGA device has.

Note: You must share DLLs if the total number of interfaces exceeds the number of DLLs available in a specific FPGA device. You may also need to share PLL clock outputs depending on your clock network usage, refer to "PLLs and Clock Networks".

Note: For information about the number of DQ and DQS in other packages, refer to the DQ and DQS tables in the relevant device handbook.

Timing closure depends on device resource and routing utilization. For more information about timing closure, refer to the *Area and Timing Optimization Techniques* chapter in the *Quartus II Handbook*.

Related Information

- **Quartus II Handbook**
- **PLLs and Clock Networks** on page 3-45

Maximum Number of DDR SDRAM Interfaces Supported per FPGA

The following table describes the maximum number of ×8 DDR SDRAM components fit in the smallest and biggest devices and pin packages assuming the device is blank.

Each interface of size *n*, where *n* is a multiple of 8, consists of:

- *n* DQ pins (including error correction coding (ECC))
- *n*/8 DM pins
- *n*/8 DQS pins
- 18 address pins
- 6 command pins (CAS, RAS, WE, CKE, reset, and CS)
- 1 CK, CK# pin pair for up to every three ×8 DDR SDRAM components

Table 3-4: Maximum Number of DDR SDRAM Interfaces Supported per FPGA

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Arria II GX	EP2AGX190 EP2AGX260	1,152	Four ×8 interfaces or one ×72 interface on each side (no DQ pins on left side)
	EP2AGX45 EP2AGX65	358	• On top side, one ×16 interface • On bottom side, one ×16 interface • On right side (no DQ pins on left side), one ×8 interface
Arria II GZ	EP2AGZ300 EP2AGZ350 EP2AGZ225	F1,517	Four ×8 interfaces or one ×72 interface on each side
	EP2AGZ300 EP2AGZ350	F780	• On top side, three ×8 interfaces or one ×64 interface • On bottom side, three ×8 interfaces or one ×64 interface • No DQ pins on the left and right sides
Stratix III	EP3SL340	1,760	• Two ×72 interfaces on both top and bottom sides • One ×72 interface on both right and left sides
	EP3SE50	484	• Two ×8 interfaces on both top and bottom sides • Three ×8 interface on both right and left sides

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Stratix IV	EP4SGX290 EP4SGX360 EP4SGX530	1,932	• One ×72 interface on each side or • One ×72 interface on each side and two additional ×72 wraparound interfaces, only if sharing DLL and PLL resources
	EP4SE530 EP4SE820	1,760	
	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	780	• Three ×8 interfaces or one ×64 interface on both top and bottom sides • On left side, one ×48 interface or two ×8 interfaces • No DQ pins on the right side

Maximum Number of DDR2 SDRAM Interfaces Supported per FPGA

The following table lists the maximum number of ×8 DDR2 SDRAM components that can be fitted in the smallest and biggest devices and pin packages assuming the device is blank.

Each interface of size *n*, where *n* is a multiple of 8, consists of:

- *n* DQ pins (including ECC)
- *n*/8 DM pins
- *n*/8 DQS, DQSn pin pairs
- 18 address pins
- 7 command pins (CAS, RAS, WE, CKE, ODT, reset, and CS)
- 1 CK, CK# pin pair up to every three ×8 DDR2 components

Table 3-5: Maximum Number of DDR2 SDRAM Interfaces Supported per FPGA

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Arria II GX	EP2AGX190 EP2AGX260	1,152	Four ×8 interfaces or one ×72 interface on each side (no DQ pins on left side)
	EP2AGX45 EP2AGX65	358	• One ×16 interface on both top and bottom sides • On right side (no DQ pins on left side), one ×8 interface
Arria II GZ	EP2AGZ300 EP2AGZ350 EP2AGZ225	F1,517	Four ×8 interfaces or one ×72 interface on each side
	EP2AGZ300 EP2AGZ350	F780	• Three ×8 interfaces or one ×64 interface on both top and bottom sides • No DQ pins on the left and right sides

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Arria V	5AGXB1 5AGXB3 5AGXB5 5AGXB7 5AGTD3 5AGTD7	1,517	• Two ×72 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGXA1 5AGXA3	672	• One ×56 interface or two x24 interfaces on both top and bottom sides • One ×32 interface on the right side • No DQ pins on the left side
	5AGXA5 5AGXA7	672	• One ×56 interface or two x24 interfaces on both top and bottom sides • No DQ pins on the left side
Arria V GZ	5AGZE5 5AGZE7	1,517	• Three ×72 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGZE1 5AGZE3	780	• On top side, two ×8 interfaces • On bottom side, four ×8 interfaces or one ×72 interface • No DQ pins on left and right sides
Cyclone V	5CGTD9 5CEA9 5CGXC9	1,152	• One ×72 interface or two ×32 interfaces on each of the top, bottom, and right sides • No DQ pins on the left side
	5CEA7 5CGTD7 5CGXC7	484	• One ×48 interface or two ×16 interfaces on both top and bottom sides • One x8 interface on the right side • No DQ pins on the left side
Stratix III	EP3SL340	1,760	• Two ×72 interfaces on both top and bottom sides • One ×72 interface on both right and left sides
	EP3SE50	484	• Two ×8 interfaces on both top and bottom sides • Three ×8 interfaces on both right and left sides

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Stratix IV	EP4SGX290 EP4SGX360 EP4SGX530	1,932	• One ×72 interface on each side or • One ×72 interface on each side and two additional ×72 wraparound interfaces only if sharing DLL and PLL resources
	EP4SE530 EP4SE820	1,760	
	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	780	• Three ×8 interfaces or one ×64 interface on top and bottom sides • On left side, one ×48 interface or two ×8 interfaces • No DQ pins on the right side
Stratix V	5SGXA5 5SGXA7	1,932	• Three ×72 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5SGXA3 5SGXA4	780	• On top side, two ×8 interfaces • On bottom side, four ×8 interfaces or one ×72 interface • No DQ pins on left and right sides

Maximum Number of DDR3 SDRAM Interfaces Supported per FPGA

The following table lists the maximum number of ×8 DDR3 SDRAM components that can be fitted in the smallest and biggest devices and pin packages assuming the device is blank.

Each interface of size *n*, where *n* is a multiple of 8, consists of:

- *n* DQ pins (including ECC)
- *n*/8 DM pins
- *n*/8 DQS, DQSn pin pairs
- 17 address pins
- 7 command pins (CAS, RAS, WE, CKE, ODT, reset, and CS)
- 1 CK, CK# pin pair

Table 3-6: Maximum Number of DDR3 SDRAM Interfaces Supported per FPGA

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Arria II GX	EP2AGX190 EP2AGX260	1,152	Four ×8 interfaces or one ×72 interface on each side (no DQ pins on left side)
	EP2AGX45 EP2AGX65	358	• One ×16 interface on both top and bottom sides • On right side, one ×8 interface (no DQ pins on left side)

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Arria II GZ	EP2AGZ300 EP2AGZ350 EP2AGZ225	F1,517	Four ×8 interfaces on each side
	EP2AGZ300 EP2AGZ350	F780	• Three ×8 interfaces on both top and bottom sides • No DQ pins on left and right sides
Arria V	5AGXB1 5AGXB3 5AGXB5 5AGXB7 5AGTD3 5AGTD7	1,517	• Two ×72 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGXA1 5AGXA3	672	• One ×56 interface or two ×24 interfaces on top and bottom sides • One ×32 interface on the right side • No DQ pins on the left side
	5AGXA5 5AGXA7	672	• One ×56 interface or two ×24 interfaces on both top and bottom sides • No DQ pins on the left side
Arria V GZ	5AGZE5 5AGZE7	1,517	• Two ×72 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGZE1 5AGZE3	780	• On top side, two ×8 interfaces • On bottom side, four ×8 interfaces • No DQ pins on left and right sides
Cyclone V	5CGTD9 5CEA9 5CGXC9	1,152	• One ×72 interface or two ×32 interfaces on each of the top, bottom, and right sides • No DQ pins on the left side
	5CEA7 5CGTD7 5CGXC7	484	• One ×48 interface or two ×16 interfaces on both top and bottom sides • One x8 interface on the right side • No DQ pins on the left side
Stratix III	EP3SL340	1,760	• Two ×72 interfaces on both top and bottom sides • One ×72 interface on both right and left sides
	EP3SE50	484	• Two ×8 interfaces on both top and bottom sides • Three ×8 interfaces on both right and left sides

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Stratix IV	EP4SGX290 EP4SGX360 EP4SGX530	1,932	• One ×72 interface on each side or • One ×72 interface on each side and 2 additional ×72 wraparound interfaces only if sharing DLL and PLL resources
	EP4SE530 EP4SE820	1,760	
	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	780	• Three ×8 interfaces or one ×64 interface on both top and bottom sides • On left side, one ×48 interface or two ×8 interfaces (no DQ pins on right side)
Stratix V	5SGXA5 5SGXA7	1,932	• Two ×72 interfaces (800 MHz) on both top and bottom sides • No DQ pins on left and right sides
	5SGXA3 5SGXA4	780	• On top side, two ×8 interfaces • On bottom side, four ×8 interfaces • No DQ pins on left and right sides

Maximum Number of QDR II and QDR II+ SRAM Interfaces Supported per FPGA

The following table lists the maximum number of independent QDR II+ or QDR II SRAM interfaces that can be fitted in the smallest and biggest devices and pin packages assuming the device is blank.

One interface of ×36 consists of:

- 36 Q pins
- 36 D pins
- 1 K, K# pin pairs
- 1 CQ, CQ# pin pairs
- 19 address pins
- 4 BSWn pins
- WPS, RPS

One interface of ×9 consists of:

- 9 Q pins
- 9 D pins
- 1 K, K# pin pairs
- 1 CQ, CQ# pin pairs
- 21 address pins
- 1 BWSn pin
- WPS, RPS

Table 3-7: Maximum Number of QDR II and QDR II+ SRAM Interfaces Supported per FPGA

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Arria II GX	EP2AGX190 EP2AGX260	1,152	One ×36 interface and one ×9 interface one each side
	EP2AGX45 EP2AGX65	358	One ×9 interface on each side (no DQ pins on left side)
Arria II GZ	EP2AGZ300 EP2AGZ350 EP2AGZ225	F1,517	• Two ×36 interfaces and one ×9 interface on both top and bottom sides • Four ×9 interfaces on right and left sides
	EP2AGZ300 EP2AGZ350	F780	• Three ×9 interfaces on both top and bottom sides • No DQ pins on right and left sides
Arria V	5AGXB1 5AGXB3 5AGXB5 5AGXB7 5AGTD3 5AGTD7	1,517	• Two ×36 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGXA1 5AGXA3	672	• Two ×9 interfaces on both top and bottom sides • One ×9 interface on the right side • No DQ pins on the left side
	5AGXA5 5AGXA7	672	• Two ×9 interfaces on both top and bottom sides • No DQ pins on the left side
Arria V GZ	5AGZE5 5AGZE7	1,517	• Two ×36 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGZE1 5AGZE3	780	• On top side, one ×36 interface or three ×9 interfaces • On bottom side, two ×9 interfaces • No DQ pins on left and right sides
Stratix III	EP3SL340	1,760	• Two ×36 interfaces and one ×9 interface on both top and bottom sides • Five ×9 interfaces on both right and left sides
	EP3SE50 EP3SL50 EP3SL70	484	• One ×9 interface on both top and bottom sides • Two ×9 interfaces on both right and left sides

Device	Device Type	Package Pin Count	Maximum Number of Interfaces
Stratix IV	EP4SGX290 EP4SGX360 EP4SGX530	1,932	• Two ×36 interfaces on both top and bottom sides • One ×36 interface on both right and left sides
	EP4SE530 EP4SE820	1,760	
	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	780	Two ×9 interfaces on each side (no DQ pins on right side)
Stratix V	5SGXA5 5SGXA7	1,932	• Two ×36 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5SGXA3 5SGXA4	780	• On top side, one ×36 interface or three ×9 interfaces • On bottom side, two ×9 interfaces • No DQ pins on left and right sides

Maximum Number of RLDRAM II Interfaces Supported per FPGA

The following table lists the maximum number of independent RLDRAM II interfaces that can be fitted in the smallest and biggest devices and pin packages assuming the device is blank.

One common I/O ×36 interface consists of:

- 36 DQ
- 1 DM pin
- 2 DK, DK# pin pairs
- 2 QK, QK# pin pairs
- 1 CK, CK# pin pair
- 24 address pins
- 1 CS# pin
- 1 REF# pin
- 1 WE# pin
- 1 QVLD pin

One common I/O ×9 interface consists of:

- 9 DQ
- 1 DM pins
- 1 DK, DK# pin pair
- 1 QK, QK# pin pair
- 1 CK, CK# pin pair
- 25 address pins
- 1 CS# pin

- 1 REF# pin
- 1 WE# pin
- 1 QVLD pin

Table 3-8: Maximum Number of RLDRAM II Interfaces Supported per FPGA

Device	Device Type	Package Pin Count	Maximum Number of RLDRAM II CIO Interfaces
Arria II GZ	EP2AGZ300 EP2AGZ350 EP2AGZ225	F1,517	Two ×36 interfaces on each side
	EP2AGZ300 EP2AGZ350	F780	• Three ×9 interfaces or one ×36 interface on both top and bottom sides • No DQ pins on the left and right sides
Arria V	5AGXB1 5AGXB3 5AGXB5 5AGXB7 5AGTD3 5AGTD7	1,517	• Two ×36 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGXA1 5AGXA3	672	• One ×36 interface on both top and bottom sides • One ×18 interface on the right side • No DQ pins on the left side
	5AGXA5 5AGXA7	672	• One ×36 interface on both top and bottom sides • No DQ pins on the left side
Arria V GZ	5ZGZE5 5ZGZE7	1,517	• Four ×36 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5AGZE1 5AGZE3	780	• On top side, three ×9 interfaces or two ×36 interfaces • On bottom side, two ×9 interfaces or one ×36 interfaces • No DQ pins on left and right sides
Stratix III	EP3SL340	1,760	• Four ×36 components on both top and bottom sides • Three ×36 interfaces on both right and left sides
	EP3SE50 EP3SL50 EP3SL70	484	One ×9 interface on both right and left sides

Device	Device Type	Package Pin Count	Maximum Number of RLDRAM II CIO Interfaces
Stratix IV	EP4SGX290 EP4SGX360 EP4SGX530	1,932	• Three ×36 interfaces on both top and bottom sides • Two ×36 interfaces on both right and left sides
	EP4SE530 EP4SE820	1,760	• Three ×36 interfaces on each side
	EP4SGX70 EP4SGX110 EP4SGX180 EP4SGX230	780	One ×36 interface on each side (no DQ pins on right side)
Stratix V	5SGXA5 5SGXA7	1,932	• Four ×36 interfaces on both top and bottom sides • No DQ pins on left and right sides
	5SGXA3 5SGXA4	780	• On top side, two ×9 interfaces or one ×18 interfaces • On bottom side, three ×9 interfaces or two ×36 interfaces • No DQ pins on left and right sides

Maximum Number of LPDDR2 SDRAM Interfaces Supported per FPGA

The following table lists the maximum number of x8 LPDDR2 SDRAM components that can fit in the smallest and largest devices and pin packages, assuming the device is blank.

Each interface of size *n*, where *n* is a multiple of 8, consists of:

- *n* DQ pins (including ECC)
- *n*/8 DM pins
- *n*/8 DQS, DQSn pin pairs
- 10 address pins
- 2 command pins (CKE and CSn)
- 1 CK, CK# pin pair up to every three x8 LPDDR2 components

Table 3-9: Maximum Number of LPDDR2 SDRAM Interfaces Supported per FPGA

Device	Device Type	Package Pin Count	Maximum Number of RLDRAM II CIO Interfaces
Arria V	5AGXB1 5AGXB3 5AGXB5 5AGXB7 5AGTD3 5AGTD7	1,517	• One ×72 interface on both top and bottom sides • No DQ pins on the left and right sides
	5AGXA1 5AGXA3	672	• One ×64 interface or two ×24 interfaces on both top and bottom sides • One ×32 interface on the right side
	5AGXA5 5AGXA7	672	• One ×64 interface or two ×24 interfaces on both the top and bottom sides • No DQ pins on the left side
Cyclone V	5CGTD9 5CEA9 5CGXC9	1,152	• One ×72 interface or two ×32 interfaces on each of the top, bottom, and right sides • No DQ pins on the left side
	5CEA7 5CGTD7 5CGXC7	484	• One ×48 interface or two ×16 interfaces on both the top and bottom sides • One ×8 interface on the right side • No DQ pins on the left side

OCT Support for Arria II GX, Arria II GZ, Arria V, Arria V GZ, Cyclone V, Stratix III, Stratix IV, and Stratix V Devices

If the memory interface uses any FPGA OCT calibrated series, parallel, or dynamic termination for any I/O in your design, you need a calibration block for the OCT circuitry. This calibration block is not required to be within the same bank or side of the device as the memory interface pins. However, the block requires a pair of R_{UP} and R_{DN} or R_{ZQ} pins that must be placed within an I/O bank that has the same VCCIO voltage as the VCCIO voltage of the I/O pins that use the OCT calibration block.

The R_{ZQ} pin in Stratix V, Arria V, and Cyclone V devices is a dual functional pin that can also be used as DQ and DQS pins when it is not used to support OCT. You can use the DQS group in ×4 mode with non-differential DQS pins if the RZQ pin is part of a ×4 DQS group.

The R_{UP} and R_{DN} pins in Arria II GX, Arria II GZ, Stratix III, and Stratix IV devices are dual functional pins that can also be used as DQ and DQS pins in when they are not used to support OCT, giving the following impacts on your DQS groups:

- If the R_{UP} and R_{DN} pins are part of a ×4 DQS group, you cannot use that DQS group in ×4 mode.
- If the R_{UP} and R_{DN} pins are part of a ×8 DQS group, you can only use this group in ×8 mode if any of the following conditions apply:
  - You are not using DM or BWSn pins.
  - You are not using a ×8 or ×9 QDR II and QDR II+ SRAM devices, as the R_{UP} and R_{DN} pins may have dual purpose function as the CQn pins. In this case, pick different pin locations for R_{UP} and R_{DN} pins, to avoid conflict with memory interface pin placement. You have the choice of placing the R_{UP} and R_{DN} pins in the same bank as the write data pin group or address and command pin group.
  - You are not using complementary or differential DQS pins.

Note: The QDR II and QDR II+ SRAM controller with UniPHY do not support ×8 QDR II and QDR II+ SRAM devices in the Quartus II software.

A DQS/DQ ×8/×9 group in Arria II GZ, Stratix III, and Stratix IV devices comprises 12 pins. A typical ×8 memory interface consists of one DQS, one DM, and eight DQ pins which add up to 10 pins. If you choose your pin assignment carefully, you can use the two extra pins for R_{UP} and R_{DN}. However, if you are using differential DQS, you do not have enough pins for R_{UP} and R_{DN} as you only have one pin leftover. In this case, as you do not have to put the OCT calibration block with the DQS or DQ pins, you can pick different locations for the R_{UP} and R_{DN} pins. As an example, you can place it in the I/O bank that contains the address and command pins, as this I/O bank has the same VCCIO voltage as the I/O bank containing the DQS and DQ pins.

There is no restriction when using ×16/×18 or ×32/×36 DQS groups that include the ×4 groups when pin members are used as R_{UP} and R_{DN} pins, as there are enough extra pins that can be used as DQS or DQ pins.

You must pick your DQS and DQ pins manually for the ×8, ×9, ×16 and ×18, or ×32 and ×36 groups, if they are using R_{UP} and R_{DN} pins within the group. The Quartus II software might not place these pins optimally and might be unable to fit the design.

General Pin-out Guidelines

Altera recommends that you place all the pins for one memory interface (attached to one controller) on the same side of the device. For projects where I/O availability is a challenge and therefore it is necessary spread the interface on two sides, for optimal performance, place all the input pins on one side, and the output pins on an adjacent side of the device along with their corresponding source-synchronous clock.

Note: For a unidirectional data bus as in QDR II and QDR II+ SRAM interfaces, do not split a read data pin group or a write data pin group onto two sides. You should also not split the address and command group onto two sides either, especially when you are interfacing with QDR II and QDR II+ SRAM burst-length-of-two devices, where the address signals are double data rate. Failure to adhere to these rules might result in timing failure.

In addition, there are some exceptions for the following interfaces:

- ×36 emulated QDR II and QDR II+ SRAM in Arria II, Stratix III, and Stratix IV devices.
- RLDRAM II and RLDRAM 3 CIO devices.
- QDR II/+ SDRAM burst-length-of-two devices.
- You must compile the design in the Quartus II software to ensure that you are not violating signal integrity and Quartus II placement rules, which is critical when you have transceivers in the same design.

The following are general guidelines for placing pins optimally for your memory interfaces:

1. For Arria II GZ, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V designs, if you are using OCT, the RUP and RDN, or RZQ pins must be in any bank with the same I/O voltage as your memory interface signals and often use two DQS and DQ pins from a group. If you decide to place the RUP and RDN, or RZQ pins in a bank where the DQS and DQ groups are used, place these pins first and then determine how many DQ pins you have left, to find out if your data pins can fit in the remaining pins. Refer to *OCT Support for Arria II GX, Arria II GZ, Arria V, Arria V GZ, Cyclone V, Stratix III, Stratix IV, and Stratix V Devices*.
2. Use the PLL that is on the same side of the memory interface. If the interface is spread out on two adjacent sides, you may use the PLL that is located on either adjacent side. You must use the dedicated input clock pin to that particular PLL as the reference clock for the PLL as the input of the memory interface PLL cannot come from the FPGA clock network.
3. The Altera IP uses the output of the memory interface PLL for the DLL input reference clock. Therefore, ensure you select a PLL that can directly feed a suitable DLL.

   Note: Alternatively, you can use an external pin to feed into the DLL input reference clock. The available pins are also listed in the External Memory Interfaces chapter of the relevant device family handbook. You can also activate an unused PLL clock outputs, set it at the desired DLL frequency, and route it to a PLL dedicated output pin. Connect a trace on the PCB from this output pin to the DLL reference clock pin, but be sure to include any signal integrity requirements such as terminations.

4. Read data pins require the usage of DQS and DQ group pins to have access to the DLL control signals.

   Note: In addition, QVLD pins in RLDRAM II and RLDRAM 3, and QDR II+ SRAM must use DQS group pins, when the design uses the QVLD signal. None of the Altera IP uses QVLD pins as part of read capture, so theoretically you do not need to connect the QVLD pins if you are using the Altera solution. It is good to connect it anyway in case the Altera solution gets updated to use QVLD pins.

5. In differential clocking (DDR3/DDR2 SDRAM, RLDRAM II, and RLDRAM 3 interfaces), connect the positive leg of the read strobe or clock to a DQS pin, and the negative leg of the read strobe or clock to a DQSn pin. For QDR II or QDR II+ SRAM devices with 2.5 or 1.5 cycles of read latency, connect the CQ pin to a DQS pin, and the CQn pin to a CQn pin (and not the DQSn pin). For QDR II or QDR II+ SRAM devices with 2.0 cycles of read latency, connect the CQ pin to a CQn pin, and the CQn pin to a DQS pin.
6. Write data (if unidirectional) and data mask pins (DM or BWSn) pins must use DQS groups. While the DLL phase shift is not used, using DQS groups for write data minimizes skew, and must use the SW and TCCS timing analysis methodology.
7. Assign the write data strobe or write data clock (if unidirectional) in the corresponding DQS/DQSn pin with the write data groups that place in DQ pins (except in RLDRAM II and RLDRAM 3 CIO devices, refer to the *Pin-out Rule Exceptions* for your memory interface protocol.

Note: When interfacing with a DDR, or DDR2, or DDR3 SDRAM without leveling, put the three CK and CK# pairs in a single ×4 DQS group to minimize skew between clocks and maximize margin for the t_{DQSS}, t_{DSS}, and t_{DSH} specifications from the memory devices.

8. Assign any address pins to any user I/O pin. To minimize skew within the address pin group, you should assign the address and command pins in the same bank or side of the device.
9. Assign the command pins to any I/O pins and assign the pins in the same bank or device side as the other memory interface pins, especially address and memory clock pins. The memory device usually uses the same clock to register address and command signals.
   - In QDR II and QDR II+ SRAM interfaces where the memory clock also registers the write data, assign the address and command pins in the same I/O bank or same side as the write data pins, to minimize skew.
   - For more information about assigning memory clock pins for different device families and memory standards, refer to *Pin Connection Guidelines Tables*.

Related Information

- **Pin Connection Guidelines Tables** on page 3-36
- **Additional Guidelines for Arria V GZ and Stratix V Devices** on page 3-42
- **OCT Support for Arria II GX, Arria II GZ, Arria V, Arria V GZ, Cyclone V, Stratix III, Stratix IV, and Stratix V Devices** on page 3-24
- **Pin-out Rule Exceptions for ×36 Emulated QDR II and QDR II+ SRAM Interfaces in Arria II, Stratix III and Stratix IV Devices** on page 3-28
- **Pin-out Rule Exceptions for QDR II and QDR II+ SRAM Burst-length-of-two Interfaces** on page 3-35
- **Pin-out Rule Exceptions for RLDRAM II and RLDRAM 3 Interfaces** on page 3-33

Arria 10 Pin Placement Rules and Guidelines

You must follow specific rules and guidelines when performing pin placement.

The Arria 10 I/O subsystem is located in the I/O columns. The device has up to two I/O columns that can be used by memory interfaces. Each column consists of multiple I/O banks. Each bank consists of four I/O lanes. A lane is a group of 12 I/Os.

The following topics describe pin placement rules and guidelines.

Arria 10 Pin Placement Rules and Guidelines: Interface-Level

Observe the following rules and guidelines for interface-level pin placement.

1. The pins of a single memory interface must reside within a single I/O column.
2. A memory interface can occupy one or more banks. When an interface must occupy multiple banks, those banks must be adjacent to one another.
3. Any pin that is not used by an external memory interface is available for use as a general purpose I/O of compatible voltage and termination settings.

Arria 10 Pin Placement Rules and Guidelines: Address/Command Pins

Observe the following rules and guidelines for address and command pin placement.

1. All address/command pins for a memory interface must reside within a single bank. This bank is denoted as the address/command bank.
2. You should select the center bank of the interface as the address/command bank, to minimize latency.
3. Address and command pins within the address/command bank must follow a fixed pinout scheme, as defined in the <*variation_name*>_**readme.txt** file which is generated with your IP. The pinout scheme varies according to the topology of the memory interface. The pinout scheme is a hardware requirement that you must follow. Some schemes require three lanes to implement address and command pins, while others require four lanes.
4. You do not need to specify the location of every address and command pin manually. If you assign the location for one address and command pin, the Fitter will automatically place the remaining address and command pins.
5. An unused I/O lane in the address and command bank can serve to implement a data group, such as a x8 DQS group.
6. A lane must not be used by both address and command pins and data pins.

Arria 10 Pin Placement Rules and Guidelines: Data Pins

Observe the following rules and guidelines for data pin placement.

1. You must place read data groups according to the DQS/CQ/QK grouping in the pin table. Read data strobes and clocks must reside at physical pins capable of functioning as DQS/CK/QK for a specific read data group size. The associated data pins must be placed within the same group.
2. For protocols and topologies where a write data group consists of multiple read data groups, you should place the read data groups in the same bank to improve I/O timing.
3. You do not need to specify the location of every data pin manually. If you assign the location for the read capture strobe/clock pin pairs, the Fitter will automatically place the remaining data pins.

Arria 10 Pin Placement Rules and Guidelines: Other Pins

Observe the following rules and guidelines for other pin placement.

1. PLL reference clock pins, if applicable, must be placed inside the address and command bank. Consult the <*variation_name*>_**readme.txt** file generated with your IP for the relative location of the PLL reference clock pin (or pin pair) within the bank.
2. RZQ pin, if applicable, must be placed inside the address and command bank. Consult the <*variation_name*>_**readme.txt** file generated with your IP for the relative location of the RZQ pin within the bank.

Pin-out Rule Exceptions for ×36 Emulated QDR II and QDR II+ SRAM Interfaces in Arria II, Stratix III and Stratix IV Devices

A few packages in the Arria II, Arria v GZ, Stratix III, Stratix IV, and Stratix V device families do not offer any ×32/×36 DQS groups where one read clock or strobe is associated with 32 or 36 read data pins. This limitation exists in the following I/O banks:

- All I/O banks in U358- and F572-pin packages for all Arria II GX devices
- All I/O banks in F484-pin packages for all Stratix III devices
- All I/O banks in F780-pin packages for all Arria II GZ, Stratix III, and Stratix IV devices; top and side I/O banks in F780-pin packages for all Stratix V and Arria V GZ devices
- All I/O banks in F1152-pin packages for all Arria II GZ, Stratix III, and Stratix IV devices, except EP4SGX290, EP4SGX360, EP4SGX530, EPAGZ300, and EPAGZ350 devices
- Side I/O banks in F1517- and F1760-pin packages for all Stratix III devices
- All I/O banks in F1517-pin for EP4SGX180, EP4SGX230, EP4S40G2, EP4S40G5, EP4S100G2, EP4S100G5, and EPAGZ225 devices
- Side I/O banks in F1517-, F1760-, and F1932-pin packages for all Arria II GZ and Stratix IV devices

This limitation limits support for ×36 QDR II and QDR II+ SRAM devices. To support these memory devices, this following section describes how you can emulate the ×32/×36 DQS groups for these devices.

- The maximum frequency supported in ×36 QDR II and QDR II+ SRAM interfaces using ×36 emulation is lower than the maximum frequency when using a native ×36 DQS group.

Note: The F484-pin package in Stratix III devices cannot support ×32/×36 DQS group emulation, as it does not support ×16/×18 DQS groups.

To emulate a ×32/×36 DQS group, combine two ×16/×18 DQS groups together. For ×36 QDR II and QDR II+ SRAM interfaces, the 36-bit wide read data bus uses two ×16/×18 groups; the 36-bit wide write data uses another two ×16/×18 groups or four ×8/×9 groups. The CQ and CQn signals from the QDR II and QDR II+ SRAM device traces are then split on the board to connect to two pairs of CQ/CQn pins in the FPGA. You might then need to split the QVLD pins also (if you are connecting them). These connections are the only connections on the board that you need to change for this implementation. There is still only one pair of K and Kn# connections on the board from the FPGA to the memory (see the following figure). Use an external termination for the CQ/CQn signals at the FPGA end. You can use the FPGA OCT features on the other QDR II interface signals with ×36 emulation. In addition, there may be extra assignments to be added with ×36 emulation.

Note: Other QDR II and QDR II+ SRAM interface rules also apply for this implementation.

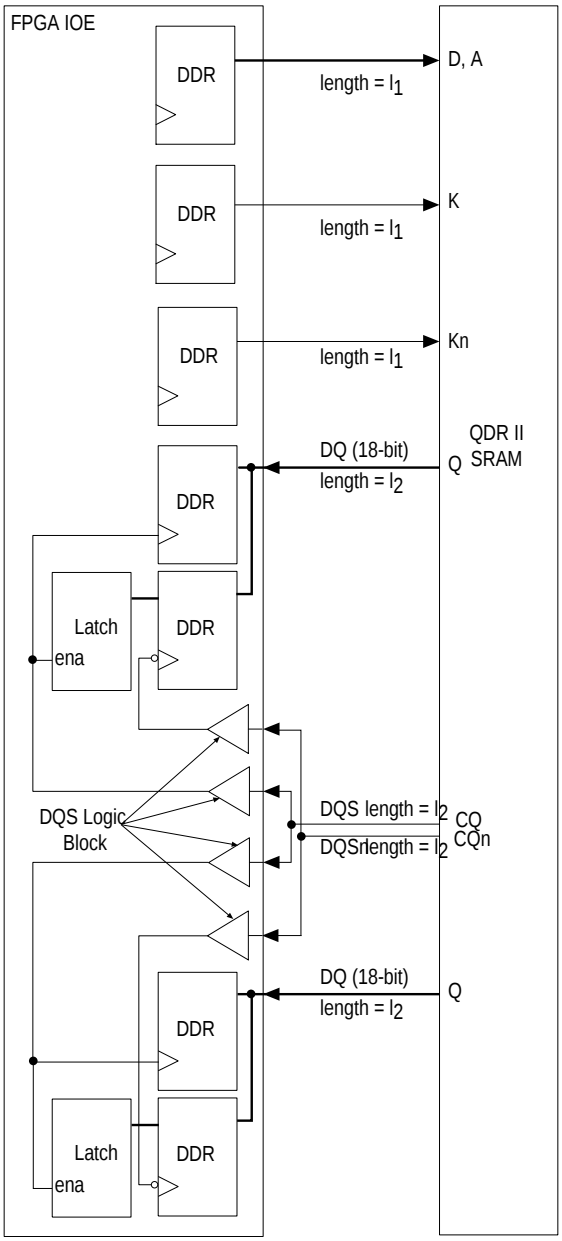
You may also combine four ×9 DQS groups (or two ×9 DQS groups and one ×18 group) on the same side of the device, if not the same I/O bank, to emulate a x36 write data group, if you need to fit the QDR II interface in a particular side of the device that does not have enough ×18 DQS groups available for write data pins. Altera does not recommend using ×4 groups as the skew may be too large, as you need eight ×4 groups to emulate the ×36 write data bits.

You cannot combine four ×9 groups to create a ×36 read data group as the loading on the CQ pin is too large and hence the signal is degraded too much.

When splitting the CQ and CQn signals, the two trace lengths that go to the FPGA pins must be as short as possible to reduce reflection. These traces must also have the same trace delay from the FPGA pin to the Y or T junction on the board. The total trace delay from the memory device to each pin on the FPGA should match the Q trace delay (I2).

Note: You must match the trace delays. However, matching trace length is only an approximation to matching actual delay.

Figure 3-7: Board Trace Connection for Emulated x36 QDR II and QDR II+ SRAM Interface



Timing Impact on x36 Emulation

With ×36 emulation, the CQ/CQn signals are split on the board, so these signals see two loads (to the two FPGA pins)—the DQ signals still only have one load. The difference in loading gives some slew rate degradation, and a later CQ/CQn arrival time at the FPGA pin.

The slew rate degradation factor is taken into account during timing analysis when you indicate in the UniPHY Preset Editor that you are using ×36 emulation mode. However, you must determine the difference in CQ/CQn arrival time as it is highly dependent on your board topology.

The slew rate degradation factor for ×36 emulation assumes that CQ/CQn has a slower slew rate than a regular ×36 interface. The slew rate degradation is assumed not to be more than 500 ps (from 10% to 90%

V_{CCIO} swing). You may also modify your board termination resistor to improve the slew rate of the ×36-emulated CQ/CQn signals. If your modified board does not have any slew rate degradation, you do not need to enable the ×36 emulation timing in the UniPHY-based controller MegaWizard™ interface.

For more information about how to determine the CQ/CQn arrival time skew, refer to *Determining the CQ/CQn Arrival Time Skew*.

Because of this effect, the maximum frequency supported using x36 emulation is lower than the maximum frequency supported using a native x36 DQS group.

Related Information

Determining the CQ/CQn Arrival Time Skew on page 3-31

Rules to Combine Groups

For devices that do not have four ×16/×18 groups in a single side of the device to form two ×36 groups for read and write data, you can form one ×36 group on one side of the device, and another ×36 group on the other side of the device. All the read groups have to be on the same edge (column I/O or row I/O) and all write groups have to be on the same type of edge (column I/O or row I/O), so you can have an interface with the read group in column I/O and the write group in row I/O. The only restriction is that you cannot combine an ×18 group from column I/O with an ×18 group from row IO to form a x36-emulated group.

For vertical migration with the ×36 emulation implementation, check if migration is possible and enable device migration in the Quartus II software.

Note: I/O bank 1C in both Stratix III and Stratix IV devices has dual-function configuration pins. Some of the DQS pins may not be available for memory interfaces if these are used for device configuration purposes.

Each side of the device in these packages has four remaining ×8/×9 groups. You can combine four of the remaining for the write side (only) if you want to keep the ×36 QDR II and QDR II+ SRAM interface on one side of the device, by changing the **Memory Interface Data Group** default assignment, from the default **18** to **9**.

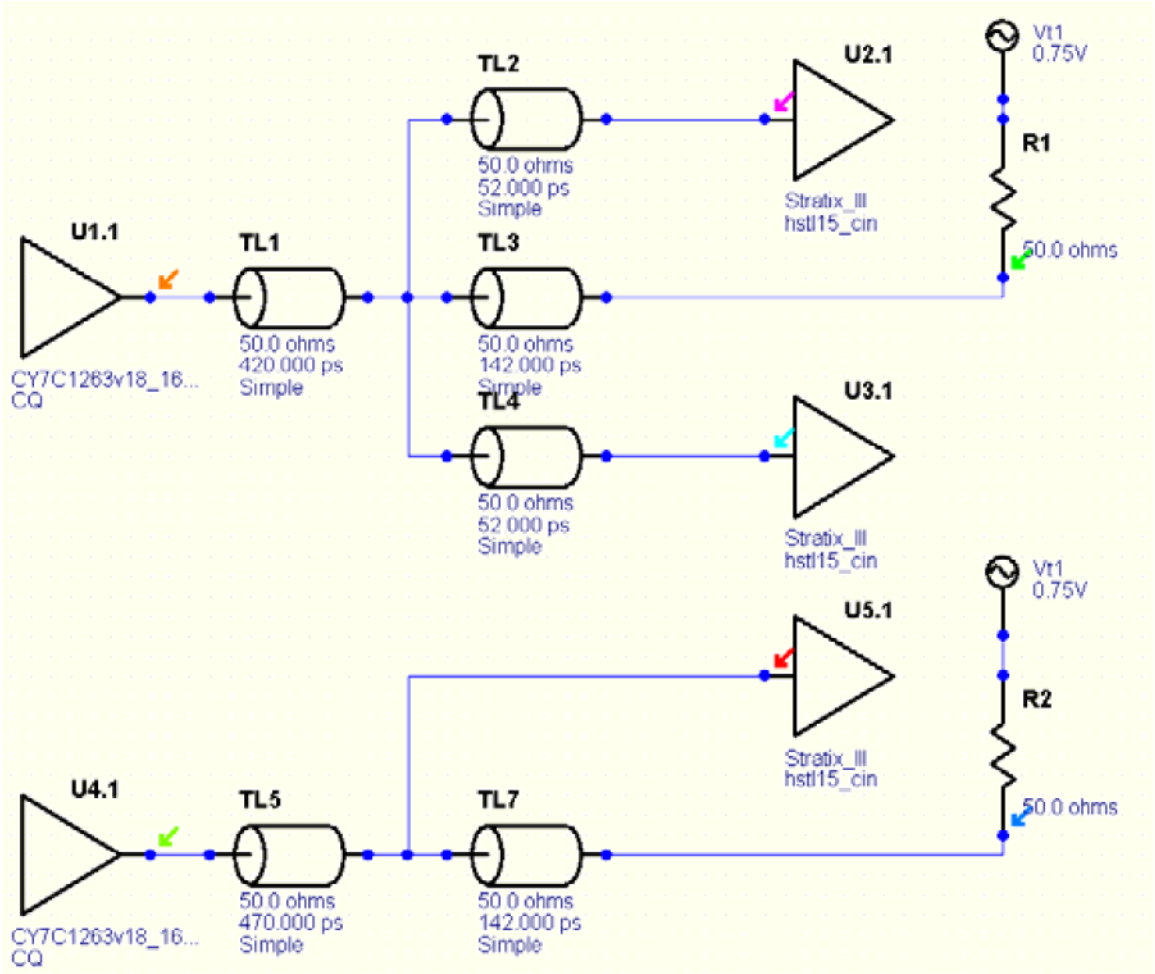
For more information about rules to combine groups for your target device, refer to the External Memory Interfaces chapter in the respective device handbooks.

Determining the CQ/CQn Arrival Time Skew

Before compiling a design in the Quartus II software, you need to determine the CQ/CQn arrival time skew based on your board simulation. You then need to apply this skew in the **report_timing.tcl** file of your QDR II and QDR II+ SRAM interface in the Quartus II software.

The following figure shows an example of a board topology comparing an emulated case where CQ is double-loaded and a non-emulated case where CQ only has a single load.

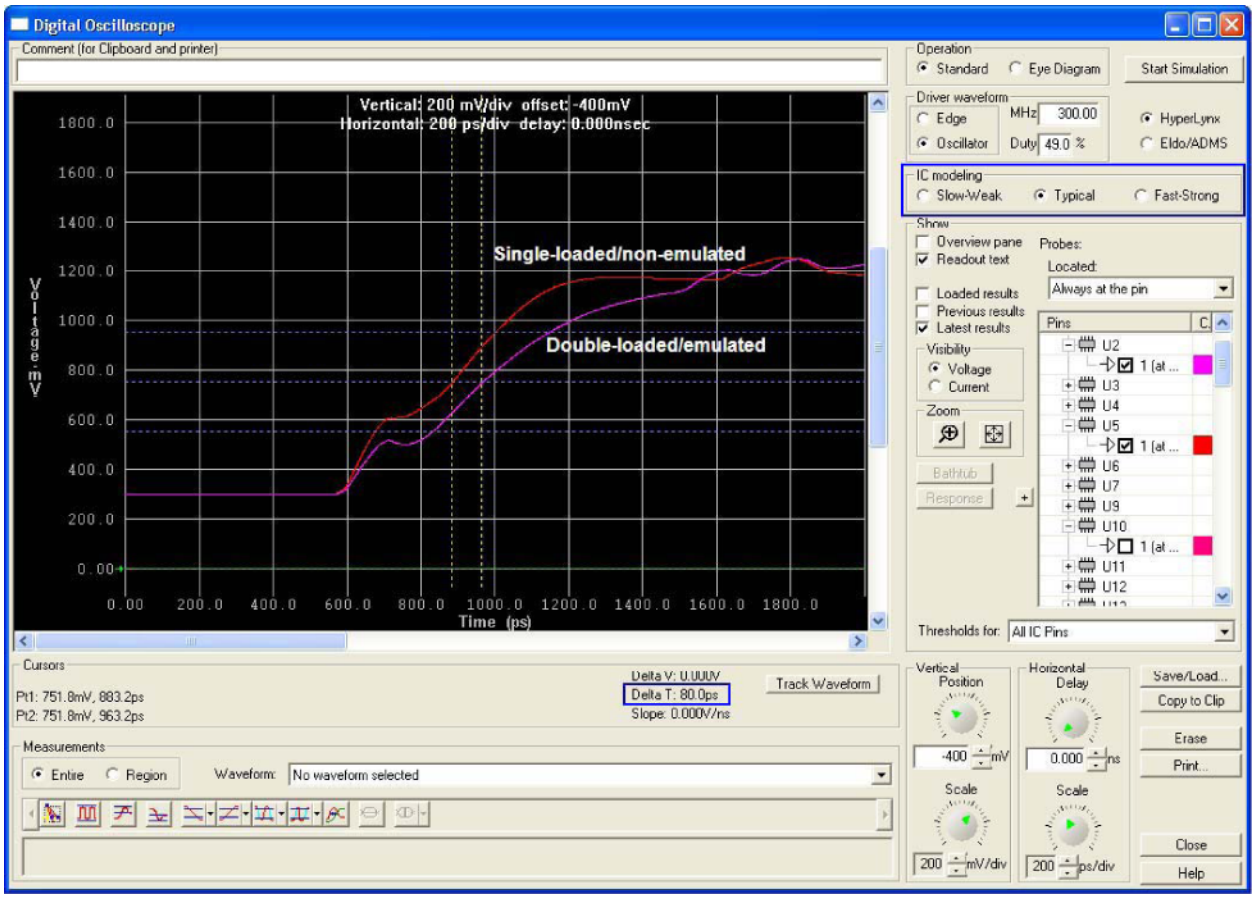
Figure 3-8: Board Simulation Topology Example



Run the simulation and look at the signal at the FPGA pin. The following figure shows an example of the simulation results from the preceding figure. As expected, the double-loaded emulated signal, in pink, arrives at the FPGA pin later than the single-loaded signal, in red. You then need to calculate the difference of this arrival time at VREF level (0.75 V in this case). Record the skew and rerun the simulation in the other two cases (slow-weak and fast-strong). To pick the largest and smallest skew to be included in Quartus II timing analysis, follow these steps:

1. Open the <*variation_name*>**_report_timing.tcl** and search for `tmin_additional_dqs_variation`.
2. Set the minimum skew value from your board simulation to `tmin_additional_dqs_variation`.
3. Set the maximum skew value from your board simulation to `tmax_additional_dqs_variation`.
4. Save the **.tcl** file.

Figure 3-9: Board Simulation Results



Pin-out Rule Exceptions for RLDRAM II and RLDRAM 3 Interfaces

RLDRAM II and RLDRAM 3 CIO devices have one bidirectional bus for the data, but there are two different sets of clocks: one for read and one for write. As the QK and QK# already occupies the DQS and DQSn pins needed for read, placement of DK and DK# pins are restricted due to the limited number of pins in the FPGA. This limitations causes the exceptions to the previous rules, which are discussed below.

The address or command pins of RLDRAM II must be placed in a DQ-group because these pins are driven by the PHY clock. Half-rate RLDRAM II interfaces and full-rate RLDRAM 3 interfaces use the PHY clock for both the DQ pins and the address or command pins.

Interfacing with ×9 RLDRAM II CIO Devices

RLDRAM 3 devices do not have the x9 configuration.

RLDRAM II devices have the following pins:

- 2 pins for QK and QK# signals
- 9 DQ pins (in a ×8/×9 DQS group)
- 2 pins for DK and DK# signals
- 1 DM pin
- 14 pins total (15 if you have a QVLD)

In the FPGA, the ×8/×9 DQS group consists of 12 pins: 2 for the read clocks and 10 for the data. In this case, move the QVLD (if you want to keep this connected even though this is not used in the Altera memory interface solution) and the DK and DK# pins to the adjacent DQS group. If that group is in use, move to any available user I/O pins in the same I/O bank.

Interfacing with ×18 RLDRAM II and RLDRAM 3 CIO Devices

This topic describes interfacing with x18 RLDRAM II and RLDRAM 3 devices.

RLDRAM II devices have the following pins:

- 4 pins for QK/QK# signals
- 18 DQ pins (in ×8/×9 DQS group)
- 2 pins for DK/DK# signals
- 1 DM pin
- 25 pins total (26 if you have a QVLD)

In the FPGA, you use two ×8/×9 DQS group totaling 24 pins: 4 for the read clocks and 18 for the read data.

Each ×8/×9 group has one DQ pin left over that can either use QVLD or DM, so one ×8/×9 group has the DM pin associated with that group and one ×8/×9 group has the QVLD pin associated with that group.

RLDRAM 3 devices have the following pins:

- 4 pins for QK/QK# signals
- 18 DQ pins (in ×8/×9 DQS group)
- 4 pins for DK/DK# signals
- 2 DM pins
- 28 pins total (29 if you have a QVLD)

In the FPGA, you use two ×8/×9 DQS group totaling 24 pins: 4 for the read clocks and 18 for the read data.

Each ×8/×9 group has one DQ pin left over that can either use QVLD or DM, so one ×8/×9 group has the DM pin associated with that group and one ×8/×9 group has the QVLD pin associated with that group.

Interfacing with RLDRAM II and RLDRAM 3 ×36 CIO Devices

This topic describes interfacing with RLDRAM II and RLDRAM 3 x36 CIO devices.

RLDRAM II devices have the following pins:

- 4 pins for QK/QK# signals
- 36 DQ pins (in x16/x18 DQS group)
- 4 pins for DK/DK# signals
- 1 DM pins
- 46 pins total (47 if you have a QVLD)

In the FPGA, you use two ×16/×18 DQS groups totaling 48 pins: 4 for the read clocks and 36 for the read data. Configure each ×16/×18 DQS group to have:

- Two QK/QK# pins occupying the DQS/DQSn pins
- Pick two DQ pins in the ×16/×18 DQS groups that are DQS and DQSn pins in the ×4 or ×8/×9 DQS groups for the DK and DK# pins
- 18 DQ pins occupying the DQ pins
- There are two DQ pins leftover that you can use for QVLD or DM pins. Put the DM pin in the group associated with `DK[1]` and the QVLD pin in the group associated with `DK[0]`.
- Check that DM is associated with `DK[1]` for your chosen memory component.

RLDRAM 3 devices have the following pins:

- 8 pins for QK/QK# signals
- 36 DQ pins (in x8/x9 DQS group)
- 4 pins for DK/DK# signals
- 2 DM pins
- 48 pins total (49 if you have a QVLD)

In the FPGA, you use four ×8/×9 DQS groups.

In addition, observe the following placement rules for RLDRAM 3 interfaces:

For ×18 devices:

- Use two ×8/×9 DQS groups. Assign the QK/QK# pins and the DQ pins of the same read group to the same DQS group.
- DQ, DM, and DK/DK# pins belonging to the same write group should be assigned to the same I/O sub-bank, for timing closure.
- Whenever possible, assign CK/CK# pins to the same I/O sub-bank as the DK/DK# pins, to improve tCKDK timing.

For ×36 devices:

- Use four ×8/×9 DQS groups. Assign the QK/QK# pins and the DQ pins of the same read group to the same DQS group.
- DQ, DM, and DK/DK# pins belonging to the same write group should be assigned to the same I/O sub-bank, for timing closure.
- Whenever possible, assign CK/CK# pins to the same I/O sub-bank as the DK/DK# pins, to improve tCKDK timing.

Pin-out Rule Exceptions for QDR II and QDR II+ SRAM Burst-length-of-two Interfaces

If you are using the QDR II and QDR II+ SRAM burst-length-of-two devices, you may want to place the address pins in a DQS group to minimize skew, because these pins are now double data rate too.

The address pins typically do not exceed 22 bits, so you may use one ×18 DQS groups or two ×9 DQS groups on the same side of the device, if not the same I/O bank. In Arria V GZ, Stratix III, Stratix IV, and Stratix V devices, one ×18 group typically has 22 DQ bits and 2 pins for DQS/DQSn pins, while one ×9 group typically has 10 DQ bits with 2 pins for DQS/DQSn pins. Using ×4 DQS groups should be a last resort.

Pin Connection Guidelines Tables

The following table lists the FPGA pin utilization for DDR, DDR2, and DDR3 SDRAM without leveling interfaces.

Table 3-10: FPGA Pin Utilization for DDR, DDR2, and DDR3 SDRAM without Leveling Interfaces

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization		
		Arria II GX	Arria II GZ, Stratix III, and Stratix IV	Arria V, Cyclone V, and Stratix V
Memory System Clock	CK and CK# (1) (2)	If you are using single-ended DQS signaling, place any unused DQ or DQS pins with `DIFFOUT` capability located in the same bank or on the same side as the data pins. If you are using differential DQS signaling in UniPHY IP, place on `DIFFOUT` in the same single DQ group of adequate width to minimize skew.	If you are using single-ended DQS signaling, place any `DIFFOUT` pins in the same bank or on the same side as the data pins If you are using differential DQS signaling in UniPHY IP, place any `DIFFOUT` pins in the same bank or on the same side as the data pins. If there are multiple CK/CK# pairs, place them on `DIFFOUT` in the same single DQ group of adequate width. For example, DIMMs requiring three memory clock pin-pairs must use a ×4 DQS group.	If you are using single-ended DQS signaling, place any unused DQ or DQS pins with `DIFFOUT` capability in the same bank or on the same side as the data pins. If you are using differential DQS signaling, place any unused DQ or DQS pins with `DIFFOUT` capability for the `mem_clk[n:0]` and `mem_clk_n[n:0]` signals (where `n>=0`). CK pins must use the differential pairs where both pins of the pair are DQ or DQS pins. Do not place CK and CK# pins in the same group as any other DQ or DQS pins. If there are multiple CK and CK# pin pairs, place them on `DIFFOUT` in the same single DQ group of adequate width.
Clock Source	—	Dedicated PLL clock input pin with direct connection to the PLL (not using the global clock network). For Arria II GX, Arria II GZ, Arria V GZ, Stratix III, Stratix IV and Stratix V Devices, also ensure that the PLL can supply the input reference clock to the DLL. Otherwise, refer to alternative DLL input reference clocks (see *General Pin-out Guidelines*).		
Reset	—	Dedicated clock input pin to accommodate the high fan-out signal.		
Data	DQ	DQ in the pin table, marked as Q in the Quartus II Pin Planner. Each DQ group has a common background color for all of the DQ and DM pins, associated with DQS (and DQSn) pins.		
Data mask	DM			

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization		
		Arria II GX	Arria II GZ, Stratix III, and Stratix IV	Arria V, Cyclone V, and Stratix V
Data strobe	DQS or DQS and DQSn (DDR2 and DDR2 SDRAM only)	DQS (S in the Quartus II Pin Planner) for single-ended DQS signaling or DQS and DQSn (S and Sbar in the Quartus II Pin Planner) for differential DQS signaling. DDR2 supports either single-ended or differential DQS signaling. DDR3 SDRAM mandates differential DQS signaling.		
Address and command	A[], BA[], CAS#, CKE, CS#, ODT, RAS#, WE#, RESET#	Any user I/O pin. To minimize skew, you must place the address and command pins in the same bank or side of the device as the CK/CK# pins, DQ, DQS, or DM pins. The reset# signal is only available in DDR3 SDRAM interfaces. Altera devices use the SSTL-15 I/O standard on the RESET# signal to meet the voltage requirements of 1.5 V CMOS at the memory device. Altera recommends that you do not terminate the RESET# signal to VTT.		

Notes to Table:

1. The first CK/CK# pair refers to `mem_clk[0]` or `mem_clk_n[0]` in the IP core.
2. The restriction on the placement for the first CK/CK# pair is required because this placement allows the mimic path that the IP VT tracking uses to go through differential I/O buffers to mimic the differential DQS signals.

Related Information

General Pin-out Guidelines on page 3-25

DDR3 SDRAM With Leveling Interface Pin Utilization Applicable for Arria V GZ, Stratix III, Stratix IV, and Stratix V Devices

The following table lists the FPGA pin utilization for DDR3 SDRAM with leveling interfaces.

Table 3-11: DDR3 SDRAM With Leveling Interface Pin Utilization Applicable for Arria V GZ, Stratix III, Stratix IV, and Stratix V Devices

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Data	DQ	DQ in the pin table, marked as Q in the Quartus II Pin Planner. Each DQ group has a common background color for all of the DQ and DM pins, associated with DQS (and DQSn) pins. The ×4 DIMM has the following mapping between DQS and DQ pins: • DQS[0] maps to DQ[3:0] • DQS[9] maps to DQ[7:4] • DQS[1] maps to DQ[11:8] • DQS[10] maps to DQ[15:12] The DQS pin index in other DIMM configurations typically increases sequentially with the DQ pin index (DQS[0]: DQ[3:0]; DQS[1]: DQ[7:4]; DQS[2]: DQ[11:8]). In this DIMM configuration, the DQS pins are indicted this way to ensure pin out is compatible with both ×4 and ×8 DIMMs.
Data Mask	DM	
Data Strobe	DQS and DQSn	DQS and DQSn (S and Sbar in the Quartus II Pin Planner)
Address and Command	A[], BA[], CAS#, CKE, CS#, ODT, RAS#, WE#,	Any user I/O pin. To minimize skew, you should place address and command pins in the same bank or side of the device as the following pins: CK/CK# pins, DQ, DQS, or DM pins.
	RESET#	Altera recommends that you use the 1.5V CMOS I/O standard on the RESET# signal. If your board is already using the SSTL-15 I/O standard, you do not terminate the RESET# signal to VTT.
Memory system clock	CK and CK#	For controllers with UniPHY IP, you can assign the memory clock to any unused DIFF_OUT pins in the same bank or on the same side as the data pins. However, for Arria V GZ and Stratix V devices, place the memory clock pins to any unused DQ or DQS pins. Do not place the memory clock pins in the same DQ group as any other DQ or DQS pins. If there are multiple CK/CK# pin pairs using Arria V GZ or Stratix V devices, you must place them on DIFFOUT in the same single DQ groups of adequate width. For example, DIMMs requiring three memory clock pin-pairs must use a ×4 DQS group. Placing the multiple CK/CK# pin pairs on DIFFOUT in the same single DQ groups for Stratix III and Stratix IV devices improves timing.
Clock Source	—	Dedicated PLL clock input pin with direct (not using a global clock net) connection to the PLL and optional DLL required by the interface.

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Reset	—	Dedicated clock input pin to accommodate the high fan-out signal.

QDR II and QDR II+ SRAM Pin Utilization for Arria II, Arria V, Stratix III, Stratix IV, and Stratix V Devices

The following table lists the FPGA pin utilization for QDR II and QDR II+ SRAM interfaces.

Table 3-12: QDR II and QDR II+ SRAM Pin Utilization for Arria II, Arria V, Stratix III, Stratix IV, and Stratix V Devices

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Read Clock	CQ and CQ# (1)	For QDR II SRAM devices with 1.5 or 2.5 cycles of read latency or QDR II+ SRAM devices with 2.5 cycles of read latency, connect CQ to DQS pin (S in the Quartus II Pin Planner), and CQn to CQn pin (Qbar in the Quartus II Pin Planner). For QDR II or QDR II+ SRAM devices with 2.0 cycles of read latency, connect CQ to CQn pin (Qbar in the Quartus II Pin Planner), and CQn to DQS pin (S in the Quartus II Pin Planner). Arria V devices do not use CQn. The CQ rising and falling edges are used to clock the read data, instead of separate CQ and CQn signals.
Read Data	Q	DQ pins (Q in the Quartus II Pin Planner). Ensure that you are using the DQ pins associated with the chosen read clock pins (DQS and CQn pins). QVLD pins are only available for QDR II+ SRAM devices and note that Altera IP does not use the QVLD pin.
Data Valid	QVLD	
Memory and Write Data Clock	K and K#	Differential or pseudo-differential DQ, DQS, or DQSn pins in or near the write data group.
Write Data	D	DQ pins. Ensure that you are using the DQ pins associated with the chosen memory and write data clock pins (DQS and DQS pins).
Byte Write Select	BWS#, NWS#	
Address and Control Signals	A, WPS#, RPS#	Any user I/O pin. To minimize skew, you should place address and command pins in the same bank or side of the device as the following pins: K and K# pins, DQ, DQS, BWS#, and NWS# pins. If you are using burst-length-of-two devices, place the address signals in a DQS group pin as these signals are now double data rate.
Clock source	—	Dedicated PLL clock input pin with direct (not using a global clock net) connection to the PLL and optional DLL required by the interface.

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Reset	—	Dedicated clock input pin to accommodate the high fan-out signal

Note to table:

1. For Arria V designs with integer latency, connect the CQ# signal to the CQ/CQ# pins from the pin table and ignore the polarity in the Pin Planner. For Arria V designs with fractional latency, connect the CQ signal to the CQ/CQ# pins from the pin table.

RLDRAM II CIO Pin Utilization for Arria II GZ, Arria V, Stratix III, Stratix IV, and Stratix V Devices

The following table lists the FPGA pin utilization for RLDRAM II CIO and RLDRAM 3 interfaces.

Table 3-13: RLDRAM II CIO Pin Utilization for Arria II GZ, Arria V, Stratix III, Stratix IV, and Stratix V Devices and RLDRAM 3 Pin Utilization for Arria V GZ and Stratix V Devices

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Read Clock	QK and QK# (1)	DQS and DQSn pins (S and Sbar in the Quartus II Pin Planner)
Data	Q	DQ pins (Q in the Quartus II Pin Planner). Ensure that you are using the DQ pins associated with the chosen read clock pins (DQS and DQSn pins). Altera IP does not use the QVLD pin. You may leave this pin unconnected on your board. You may not be able to fit these pins in a DQS group. For more information about how to place these pins, refer to "Exceptions for RLDRAM II and RLDRAM 3 Interfaces" on page 3–34.
Data Valid	QVLD	
Data Mask	DM	
Write Data Clock	DK and DK#	DQ pins in the same DQS group as the read data (Q) pins or in adjacent DQS group or in the same bank as the address and command pins. For more information, refer to "Exceptions for RLDRAM II and RLDRAM 3 Interfaces" on page 3–34. DK/DK# must use differential output-capable pins. For Nios-based configuration, the DK pins must be in a DQ group but the DK pins do not have to be in the same group as the data or QK pins.
Memory Clock	CK and CK#	Any differential output-capable pins. For Arria V GZ and Stratix V devices, place any unused DQ or DQS pins with DIFFOUT capability. Place the memory clock pins either in the same bank as the DK or DK# pins to improve DK versus CK timing, or in the same bank as the address and command pins to improve address command timing. Do not place CK and CK# pins in the same DQ group as any other DQ or DQS pins.

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Address and Control Signals	A, BA, CS#, REF#, WE#	Any user I/O pins. To minimize skew, you should place address and command pins in the same bank or side of the device as the following pins: CK/CK# pins, DQ, DQS, and DM pins.
Clock source	—	Dedicated PLL clock input pin with direct (not using a global clock net) connection to the PLL and optional DLL required by the interface.
Reset	—	Dedicated clock input pin to accommodate the high fan-out signal

Note to Table:

1. For Arria V devices, refer to the pin table for the QK and QK# pins. Connect QK and QK# signals to the QK and QK# pins from the pin table and ignore the polarity in the Pin Planner.

Related Information

Pin-out Rule Exceptions for RLDRAM II and RLDRAM 3 Interfaces on page 3-33

LPDDR2 Pin Utilization for Arria V, Cyclone V, and Stratix V Devices

The following table lists the FPGA pin utilization for LPDDR2 SDRAM.

Table 3-14: LPDDR2 Pin Utilization for Arria V, Cyclone V, and Stratix V Devices

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Memory Clock	CK, CKn	Differential clock inputs. All double data rate (DDR) inputs are sampled on both positive and negative edges of the CK signal. Single data rate (SDR) inputs are sampled at the positive clock edge. Place any unused DQ or DQS pins with DIFFOUT capability for the mem_clk[n:0] and mem_clk_n[n:0] signals (where n>=0). Do not place CK and CK# pins in the same group as any other DQ or DQS pins. If there are multiple CK and CK# pin pairs, place them on DIFFOUT in the same single DQ group of adequate width.
Address and Command	CA0-CA9 CSn CKE	Unidirectional DDR command and address bus inputs. Chip Select: CSn is considered to be part of the command code.Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Place address and command pins in any DDR-capable I/O pin. To minimize skew, Altera recommends using address and command pins in the same bank or side of the device as the CK/CK#, DQ. DQS, or DM pins..

Interface Pin Description	Memory Device Pin Name	FPGA Pin Utilization
Data	DQ0-DQ7 (×8) DQ0-DQ15 (×16) DQ0-DQ31 (×32)	Bidirectional data bus. Pins are used as data inputs and outputs. DQ in the pin table is marked as Q in the Pin Planner. Each DQ group has a common background color for all of the DQ and DM pins associated with DQS (and DQSn) pins. Place on DQ group pin marked Q in the Pin Planner.
Data Strobe	DQS, DQSn	Data Strobe. The data strobe is bidirectional (used for read and write data) and differential (DQS and DQSn). It is output with read data and input with write data. Place on DQS and DQSn (S and Sbar in the Pin Planner) for differential DQS signaling.
Data Mask	DM0 (×8) DM0-DM1 (×16) DM0-DM3 (×32)	Input Data Mask. DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a write access. DM is sampled on both edges of DQS. DQ in the pin table is marked as Q in the Pin Planner. Each DQ group has a common background color for all of the DQ and DM pins, associated with DQS (and DQSn) pins. Place on DQ group pin marked Q in the Pin Planner.
Clock Source	—	Dedicated PLL clock input pin with direct (not using a global clock net) connection to the PLL and optional DLL required by the interface.
Reset	—	Dedicated clock input pin to accommodate the high fan-out signal.

Additional Guidelines for Arria V GZ and Stratix V Devices

This section provides guidelines for improving timing for Arria V GZ and Stratix V devices and the rules that you must follow to overcome timing failures.

Performing Manual Pin Placement

The following table lists rules that you can follow to perform proper manual pin placement and avoid timing failures.

The rules are categorized as follows:

- **Mandatory**—This rule is mandatory and cannot be violated as it would result in a no-fit error.
- **Recommended**—This rule is recommended and if violated the implementation is legal but the timing is degraded.
- **Highly Recommended**—This rule is not mandatory but is highly recommended because disregarding this rule might result in timing violations.

Table 3-15: Manual Pin Placement Rules

Rules	Frequency	Device	Reason
Mandatory			

Rules	Frequency	Device	Reason
Must place all CK, CK#, address, control, and command pins of an interface in the same I/O sub-bank.	> 800 MHz	All	For optimum timing, clock and data output paths must share as much hardware as possible. For write data pins (for example, DQ/DQS), the best timing is achieved through the DQS Groups.
Must not split interface between top and bottom sides	Any	All	Because PLLs and DLLs on the top edge cannot access the bottom edge of a device and vice-versa.
Must not place pins from separate interfaces in the same I/O sub-banks unless the interfaces share PLL or DLL resources.	Any	All	All pins require access to the same leveling block.
Must not share the same PLL input reference clock unless the interfaces share PLL or DLL resources.	Any	All	Because sharing the same PLL input reference clock forces the same ff-PLL to be used. Each ff-PLL can drive only one PHY clock tree and interfaces not sharing a PLL cannot share a PHY clock tree.
Recommended			
Place all CK, CK#, address, control, and command pins of an interface in the same I/O sub-bank.	<800 MHz	All	Place all CK/CK#, address, control, and command pins in the same I/O sub-bank when address and command timing is critical. For optimum timing, clock and data output paths should share as much hardware as possible. For write data pins (for example, DQ/DQS), the best timing is achieved through the DQS Groups.
Avoid using I/Os at the device corners (for example, sub-bank "A") .	Any	A7 *(1)*	The delay from the FPGA core fabric to the I/O periphery is higher toward the sub-banks in the corners. By not using I/Os at the device corners, you can improve core timing closure.
	>=800 MHz	All	Corner I/O pins use longer delays, therefore avoiding corner I/O pins is recommended for better memory clock performance.
Avoid straddling an interface across the center PLL.	Any	All	Straddling the center PLL causes timing degradation, because it increases the length of the PHY clock tree and increases jitter. By not straddling the center PLL, you can improve core timing closure.

Rules	Frequency	Device	Reason
Use the center PLL(f-PLL1) for a wide interface that must straddle across center PLL.	>= 800 MHz	All	Using a non-center PLL results in driving a sub-bank in the opposite quadrant due to long PHY clock tree delay.
Place the DQS/DQS# pins such that all DQ groups of the same interface are next to each other and do not span across the center PLL.	Any	All	To ease core timing closure. If the pins are too far apart then the core logic is also placed apart which results in difficult timing closure.
Place CK, CK#, address, control, and command pins in the same quadrant as DQ groups for improved timing in general.	Any	All	
Highly Recommended			
Place all CK, CK#, address, control, and command pins of an interface in the same I/O sub-bank.	800 MHz	All	For optimum timing, clock and data output paths should share as much hardware as possible. For write data pins (for example, DQ/DQS), the best timing is achieved through the DQS Groups.
Use center PLL and ensure that the PLL input reference clock pin is placed at a location that can drive the center PLL.	>= 800 MHz	All	Using a non-center PLL results in driving a sub-bank in the opposite quadrant due to long PHY clock tree delay.
If center PLL is not accessible, place pins in the same quadrant as the PLL.	>= 800 MHz	All	

Note to Table:

1. This rule is currently applicable to A7 devices only. This rule might be applied to other devices in the future if they show the same failure.

Additional Guidelines for Arria V (Except Arria V GZ) Devices

This section provides guidelines on how to improve timing for Arria V devices and the rules that you must follow to overcome timing failures.

Performing Manual Pin Placement

The following table lists rules you can follow to perform proper manual pin placement and avoid timing failures.

The rules are categorized as follows:

- **Mandatory**—This rule is mandatory and cannot be violated as it would result in a no-fit error.
- **Recommended**—This rule is recommended and if violated the implementation is legal but the timing is degraded.

Table 3-16: Manual Pin Placement Rules for Arria V (Except Arria V GZ) Devices

Rules	Frequency	Device	Reason
Mandatory			
Must place all CK, CK#, address, control, and command pins of an interface on the same device edge as the DQ groups.	All	All	For optimum timing, clock and data output ports must share as much hardware as possible.
Must not place pins from separate interfaces in the same I/O sub-banks unless the interfaces share PLL or DLL resources. To share resources, the interfaces must use the same memory protocol, frequency, controller rate, and phase requirements.	All	All	All pins require access to the same PLL/DLL block.
Must not split interface between top, bottom, and right sides.	All	All	PHYCLK network support interfaces at the same side of the I/O banks only. PHYCLK networks do not support split interface.
Recommended			
Place the DQS/DQS# pins such that all DQ groups of the same interface are next to each other and do not span across the center PLL.	All	All	To ease core timing closure. If the pins are too far apart then the core logic is also placed apart which results in difficult timing closure.
Place all pins for a memory interface in an I/O bank and use the nearest PLL to that I/O bank for the memory interface.	All	All	Improve timing performance by reducing the PHY clock tree delay.

Additional Guidelines for Cyclone V Devices

This topic provides guidelines for improving performance for Cyclone V devices.

I/O Pins Connect to Ground for Hard Memory Interface Operation

According to the Cyclone V pin-out file, there are some general I/O pins that are connected to ground for hard memory interface operation. These I/O pins should be grounded to reduce crosstalk from neighboring I/O pins and to ensure the performance of the hard memory interface.

The grounded user I/O pins can also be used as regular I/O pins if you run short of available I/O pins; however, the hard memory interface performance will be reduced if these pins are not connected to ground.

PLLs and Clock Networks

The exact number of clocks and PLLs required in your design depends greatly on the memory interface frequency, and on the IP that your design uses.

For example, you can build simple DDR slow-speed interfaces that typically require only two clocks: system and write. You can then use the rising and falling edges of these two clocks to derive four phases (0°, 90°, 180°, and 270°). However, as clock speeds increase, the timing margin decreases and additional clocks are required, to optimize setup and hold and meet timing. Typically, at higher clock speeds, you need to have dedicated clocks for resynchronization, and address and command paths.

Altera memory interface IP uses one PLL, which generates the various clocks needed in the memory interface data path and controller, and provides the required phase shifts for the write clock and address and command clock. The PLL is instantiated when you generate the Altera memory IPs.

By default, the memory interface IP uses the PLL to generate the input reference clock for the DLL, available in all supported device families. This method eliminates the need of an extra pin for the DLL input reference clock.

The input reference clock to the DLL can come from certain input clock pins or clock output from certain PLLs.

Note: Altera recommends using integer PLLs for memory interfaces; handbook specifications are based on integer PLL implementations.

For the actual pins and PLLs connected to the DLLs, refer to the *External Memory Interfaces* chapter of the relevant device family handbook.

You must use the PLL located in the same device quadrant or side as the memory interface and the corresponding dedicated clock input pin for that PLL, to ensure optimal performance and accurate timing results from the Quartus II software.

The input clock to the PLL can fan out to logic other than the PHY, so long as the clock input pin to the PLL is a dedicated input clock path, and you ensure that the clock domain transfer between UniPHY and the core logic is clocked by the reference clock going into a global clock.

Number of PLLs Available in Altera Device Families

The following table lists the number of PLLs available in Altera device families.

Table 3-17: Number of PLLs Available in Altera Device Families

Device Family	Enhanced PLLs Available
Arria II GX	4-6
Arria II GZ	3-8
Arria V	16-24
Arria V GZ (fPLL)	22-28
Cyclone V	4-8
Stratix III	4-12
Stratix IV	3-12
Stratix V (fPLL)	22-28

Note to Table:

1. For more details, refer to the *Clock Networks and PLL* chapter of the respective device family handbook.

Number of Enhanced PLL Clock Outputs and Dedicated Clock Outputs Available in Altera Device Families

The following table lists the number of enhanced PLL clock outputs and dedicated clock outputs available in Altera device families.

Table 3-18: Number of Enhanced PLL Clock Outputs and Dedicated Clock Outputs Available in Altera Device Families (1)

Device Family	Number of Enhanced PLL Clock Outputs	Number Dedicated Clock Outputs
Arria II GX (2)	7 clock outputs each	1 single-ended or 1 differential pair 3 single-ended or 3 differential pair total (3)
Arria V	18 clock outputs each	4 single-ended or 2 single-ended and 1 differential pair
Stratix III	Left/right: 7 clock outputs Top/bottom: 10 clock outputs	Left/right: 2 single-ended or 1 differential pair Top/bottom: 6 single-ended or 4 single-ended and 1 differential pair
Arria II GZ and Stratix IV	Left/right: 7 clock outputs Top/bottom: 10 clock outputs	Left/right: 2 single-ended or 1 differential pair Top/bottom: 6 single-ended or 4 single-ended and 1 differential pair
Arria V GZ and Stratix V	18 clock outputs each	4 single-ended or 2 single-ended and 1 differential pair

Notes to Table:

1. For more details, refer to the *Clock Networks and PLL* chapter of the respective device family handbook.
2. PLL_5 and PLL_6 of Arria II GX devices do not have dedicated clock outputs.
3. The same PLL clock outputs drives three single-ended or three differential I/O pairs, which are only supported in PLL_1 and PLL_3 of the EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260 devices.

Number of Clock Networks Available in Altera Device Families

The following table lists the number of clock networks available in Altera device families.

Table 3-19: Number of Clock Networks Available in Altera Device Families (1)

Device Family	Global Clock Network	Regional Clock Network
Arria II GX	16	48
Arria II GZ	16	64–88

Device Family	Global Clock Network	Regional Clock Network
Arria V	16	88
Arria V GZ	16	92
Cyclone V	16	N/A
Stratix III	16	64–88
Stratix IV	16	64–88
Stratix V	16	92

Note to Table:

1. For more information on the number of available clock network resources per device quadrant to better understand the number of clock networks available for your interface, refer to the *Clock Networks and PLL* chapter of the respective device family handbook.

Note: You must decide whether you need to share clock networks, PLL clock outputs, or PLLs if you are implementing multiple memory interfaces.

Clock Network Usage in UniPHY-based Memory Interfaces—DDR2 and DDR3 SDRAM *(1) (2)*

The following table lists clock network usage in UniPHY-based memory interfaces for DDR2 and DDR3 protocols.

Table 3-20: Clock Network Usage in UniPHY-based Memory Interfaces—DDR2 and DDR3 SDRAM

Device	DDR3 SDRAM		DDR2 SDRAM	
	Half-Rate		Half-Rate	
	Number of full-rate clock	Number of half-rate clock	Number of full-rate clock	Number of half-rate clock
Stratix III	3 global	1 global 1 regional	1 global 2 global	1 global 1 regional
Arria II GZ and Stratix IV	3 global	1 global 1 regional	1 regional 2 regional	1 global 1 regional
Arria V GZ and Stratix V	1 global 2 regional	2 global	1 regional 2 regional	2 global

Device	DDR3 SDRAM		DDR2 SDRAM	
	Half-Rate		Half-Rate	
	Number of full-rate clock	Number of half-rate clock	Number of full-rate clock	Number of half-rate clock

Notes to Table:

1. There are two additional regional clocks, `pll_avl_clk` and `pll_config_clk` for DDR2 and DDR3 SDRAM with UniPHY memory interfaces.
2. In multiple interface designs with other IP, the clock network might need to be modified to get a design to fit. For more information, refer to the *Clock Networks and PLLs* chapter in the respective device handbooks.

Clock Network Usage in UniPHY-based Memory Interfaces—RLDRAM II, and QDR II and QDR II+ SRAM

The following table lists clock network usage in UniPHY-based memory interfaces for RLDRAM II, QDR II, and QDR II+ protocols.

Table 3-21: Clock Network Usage in UniPHY-based Memory Interfaces—RLDRAM II, and QDR II and QDR II+ SRAM

Device	RLDRAM II			QDR II/QDR II+ SRAM		
	Half-Rate		Full-Rate	Half-Rate		Full-Rate
	Number of full-rate clock	Number of half-rate clock	Number of full-rate clock	Number of full-rate clock	Number of half-rate clock	Number of full-rate clock
Arria II GX	—	—	—	2 global	2 global	4 global
Stratix III	2 regional	1 global 1 regional	1 global 2 regional	1 global 1 regional	2 regional	1 global 2 regional
Arria II GZ and Stratix IV	2 regional	1 global 1 regional	1 global 2 regional	1 global 1 regional	2 regional	1 global 2 regional

Note: For more information about the clocks used in UniPHY-based memory standards, refer to the *Functional Description—UniPHY* chapter in volume 3 of the External Memory Interface Handbook.

Related Information

Functional Description—UniPHY

PLL Usage for DDR, DDR2, and DDR3 SDRAM Without Leveling Interfaces

The following table lists PLL usage for DDR, DDR2, and DDR3 protocols without leveling interfaces.

Table 3-22: PLL Usage for DDR, DDR2, and DDR3 SDRAM Without Leveling Interfaces

Clock	Arria II GX Devices	Stratix III and Stratix IV Devices
C0	• phy_clk_1x in half-rate designs • aux_half_rate_clk • PLL scan_clk	• phy_clk_1x in half-rate designs • aux_half_rate_clk • PLL scan_clk
C1	• phy_clk_1x in full-rate designs • aux_full_rate_clk • mem_clk_2x to generate DQS and CK/CK# signals • ac_clk_2x • cs_n_clk_2x	• mem_clk_2x
C2	• Unused	• phy_clk_1x in full-rate designs • aux_full_rate_clk
C3	• write_clk_2x (for DQ) • ac_clk_2x • cs_n_clk_2x	• write_clk_2x
C4	• resync_clk_2x	• resync_clk_2x
C5	• measure_clk_2x	• measure_clk_1x
C6	—	• ac_clk_1x

PLL Usage for DDR3 SDRAM With Leveling Interfaces

The following table lists PLL usage for DDR3 protocols with leveling interfaces.

Table 3-23: PLL Usage for DDR3 SDRAM With Leveling Interfaces

Clock	Stratix III and Stratix IV Devices
C0	• phy_clk_1x in half-rate designs • aux_half_rate_clk • PLL scan_clk
C1	• mem_clk_2x
C2	• aux_full_rate_clk
C3	• write_clk_2x
C4	• resync_clk_2x
C5	• measure_clk_1x
C6	• ac_clk_1x

Using PLL Guidelines

When using PLL for external memory interfaces, you must consider the following guidelines:

- For the clock source, use the clock input pin specifically dedicated to the PLL that you want to use with your external memory interface. The input and output pins are only fully compensated when you use the dedicated PLL clock input pin. If the clock source for the PLL is not a dedicated clock input pin for the dedicated PLL, you would need an additional clock network to connect the clock source to the PLL block. Using additional clock network may increase clock jitter and degrade the timing margin.
- Pick a PLL and PLL input clock pin that are located on the same side of the device as the memory interface pins.
- Share the DLL and PLL static clocks for multiple memory interfaces provided the controllers are on the same or adjacent side of the device and run at the same memory clock frequency.
- If your design uses a dedicated PLL to only generate a DLL input reference clock, you must set the PLL mode to **No Compensation** in the Quartus II software to minimize the jitter, or the software forces this setting automatically. The PLL does not generate other output, so it does not need to compensate for any clock path.
- If your design cascades PLL, the source (upstream) PLL must have a low-bandwidth setting, while the destination (downstream) PLL must have a high-bandwidth setting to minimize jitter. Altera does not recommend using cascaded PLLs for external memory interfaces because your design gets accumulated jitters. The memory output clock may violate the memory device jitter specification.
- Use cascading PLLs at your own risk. For more information, refer to "PLL Cascading".
- If you are using Arria II GX devices, for a single memory instance that spans two right-side quadrants, use a middle-side PLL as the source for that interface.
- If you are using Arria II GZ, Arria V GZ, Stratix III, Stratix IV, or Stratix V devices, for a single memory instance that spans two top or bottom quadrants, use a middle top or bottom PLL as the source for that interface. The ten dual regional clocks that the single interface requires must not block the design using the adjacent PLL (if available) for a second interface.

Related Information

PLL Cascading on page 3-51

PLL Cascading

Arria II GZ PLLs, Stratix III PLLs, Stratix IV PLLs, Stratix V and Arria V GZ fractional PLLs (fPLLs), and the two middle PLLs in Arria II GX EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260 devices can be cascaded using either the global or regional clock trees, or the cascade path between two adjacent PLLs.

Note: Use cascading PLLs at your own risk. You should use faster memory devices to maximize timing margins.

The UniPHY IP supports PLL cascading using the cascade path without any additional timing derating when the bandwidth and compensation rules are followed. The timing constraints and analysis assume that there is no additional jitter due to PLL cascading when the upstream PLL uses no compensation and low bandwidth, and the downstream PLL uses no compensation and high bandwidth.

The UniPHY IP does not support PLL cascading using the global and regional clock networks. You can implement PLL cascading at your own risk without any additional guidance and specifications from Altera. The Quartus II software does issue a critical warning suggesting use of the cascade path to minimize jitter, but does not explicitly state that Altera does not support cascading using global and regional clock networks.

Some Arria II GX devices (EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260) have direct cascade path for two middle right PLLs. Arria II GX PLLs have the same bandwidth options as Stratix IV GX left and right PLLs.

DLL

The Altera memory interface IP uses one DLL. The DLL is located at the corner of the device and can send the control signals to shift the DQS pins on its adjacent sides for Stratix-series devices, or DQS pins in any I/O banks in Arria II GX devices.

For example, the top-left DLL can shift DQS pins on the top side and left side of the device. The DLL generates the same phase shift resolution for both sides, but can generate different phase offset to the two different sides, if needed. Each DQS pin can be configured to use or ignore the phase offset generated by the DLL.

The DLL cannot generate two different phase offsets to the same side of the device. However, you can use two different DLLs to for this functionality.

DLL reference clocks must come from either dedicated clock input pins located on either side of the DLL or from specific PLL output clocks. Any clock running at the memory frequency is valid for the DLLs.

To minimize the number of clocks routed directly on the PCB, typically this reference clock is sourced from the memory controllers PLL. In general, DLLs can use the PLLs directly adjacent to them (corner PLLs when available) or the closest PLL located in the two sides adjacent to its location.

Note: By default, the DLL reference clock in Altera external memory IP is from a PLL output.

When designing for 780-pin packages with EP3SE80, EP3SE110, EP3SL150, EP4SE230, EP4SE360, EP4SGX180, and EP4SGX230 devices, the PLL to DLL reference clock connection is limited. DLL2 is isolated from a direct PLL connection and can only receive a reference clock externally from pins `CLK[11:4]p` in EP3SE80, EP3SE110, EP3SL150, EP4SE230, and EP4SE360 devices. In EP4SGX180 and EP4SGX230 devices, DLL2 and DLL3 are not directly connected to PLL. DLL2 and DLL3 receive a reference clock externally from pins `CLK[7:4]p` and `CLK[15:12]p` respectively.

For more DLL information, refer to the respective device handbooks.

The DLL reference clock should be the same frequency as the memory interface, but the phase is not important.

The required DQS capture phase is optimally chosen based on operating frequency and external memory interface type (DDR, DDR2, DDR3 SDRAM, and QDR II SRAM, or RLDRAM II). As each DLL supports two possible phase offsets, two different memory interface types operating at the same frequency can easily share a single DLL. More may be possible, depending on the phase shift required.

Altera memory IP always specifies a default optimal phase setting, to override this setting, refer to *Implementing and Parameterizing Memory IP* .

When sharing DLLs, your memory interfaces must be of the same frequency. If the required phase shift is different amongst the multiple memory interfaces, you can use a different delay chain in the DQS logic block or use the DLL phase offset feature.

To simplify the interface to IP connections, multiple memory interfaces operating at the same frequency usually share the same system and static clocks as each other where possible. This sharing minimizes the number of dedicated clock nets required and reduces the number of different clock domains found within the same design.

As each DLL can directly drive four banks, but each PLL only has complete C (output) counter coverage of two banks (using dual regional networks), situations can occur where a second PLL operating at the same

frequency is required. As cascaded PLLs increase jitter and reduce timing margin, you are advised to first ascertain if an alternative second DLL and PLL combination is not available and more optimal.

Select a DLL that is available for the side of the device where the memory interface resides. If you select a PLL or a PLL input clock reference pin that can also serve as the DLL input reference clock, you do not need an extra input pin for the DLL input reference clock.

Other FPGA Resources

The Altera memory interface IP uses FPGA fabric, including registers and the Memory Block to implement the memory interface.

For resource utilization examples to ensure that you can fit your other modules in the device, refer to the "Resource Utilization" section in the *Introduction to UniPHY IP* chapter of the External Memory Interface Handbook.

One OCT calibration block is used if you are using the FPGA OCT feature in the memory interface.The OCT calibration block uses two pins (RUP and RDN), or single pin (RZQ) ("OCT Support for Arria II GX, Arria II GZ, Arria V, Arria V GZ, Cyclone V, Stratix III, Stratix IV, and Stratix V Devices"). You can select any of the available OCT calibration block as you do not need to place this block in the same bank or device side of your memory interface. The only requirement is that the I/O bank where you place the OCT calibration block uses the same VCCIO voltage as the memory interface. You can share multiple memory interfaces with the same OCT calibration block if the VCCIO voltage is the same.

Related Information

- **OCT Support for Arria II GX, Arria II GZ, Arria V, Arria V GZ, Cyclone V, Stratix III, Stratix IV, and Stratix V Devices** on page 3-24
- **Introduction to UniPHY IP**

Document Revision History

Date	Version	Changes
December 2013	2013.12.16	• Removed references to ALTMEMPHY and HardCopy. • Removed references to Cyclone III and Cyclone IV devices.
November 2012	6.0	• Added Arria V GZ information. • Added RLDRAM 3 information. • Added LRDIMM information.
June 2012	5.0	• Added LPDDR2 information. • Added Cyclone V information. • Added Feedback icon.

Date	Version	Changes
November 2011	4.0	• Moved and reorganized *Planning Pin and Resource* section to Volume 2:Design Guidelines. • Added *Additional Guidelines for Arria V GZ and Stratix V Devices* section. • Added Arria V and Cyclone V information.
June 2011	3.0	• Moved *Select a Device* and *Memory IP Planning* chapters to Volume 1. • Added information about interface pins. • Added guidelines for using PLL.
December 2010	2.1	• Added a new section on controller efficiency. • Added Arria II GX and Stratix V information.
July 2010	2.0	Updated information about UniPHY-based interfaces and Stratix V devices.
April 2010	1.0	Initial release.