WISHBONE TO AHB BRIDGE

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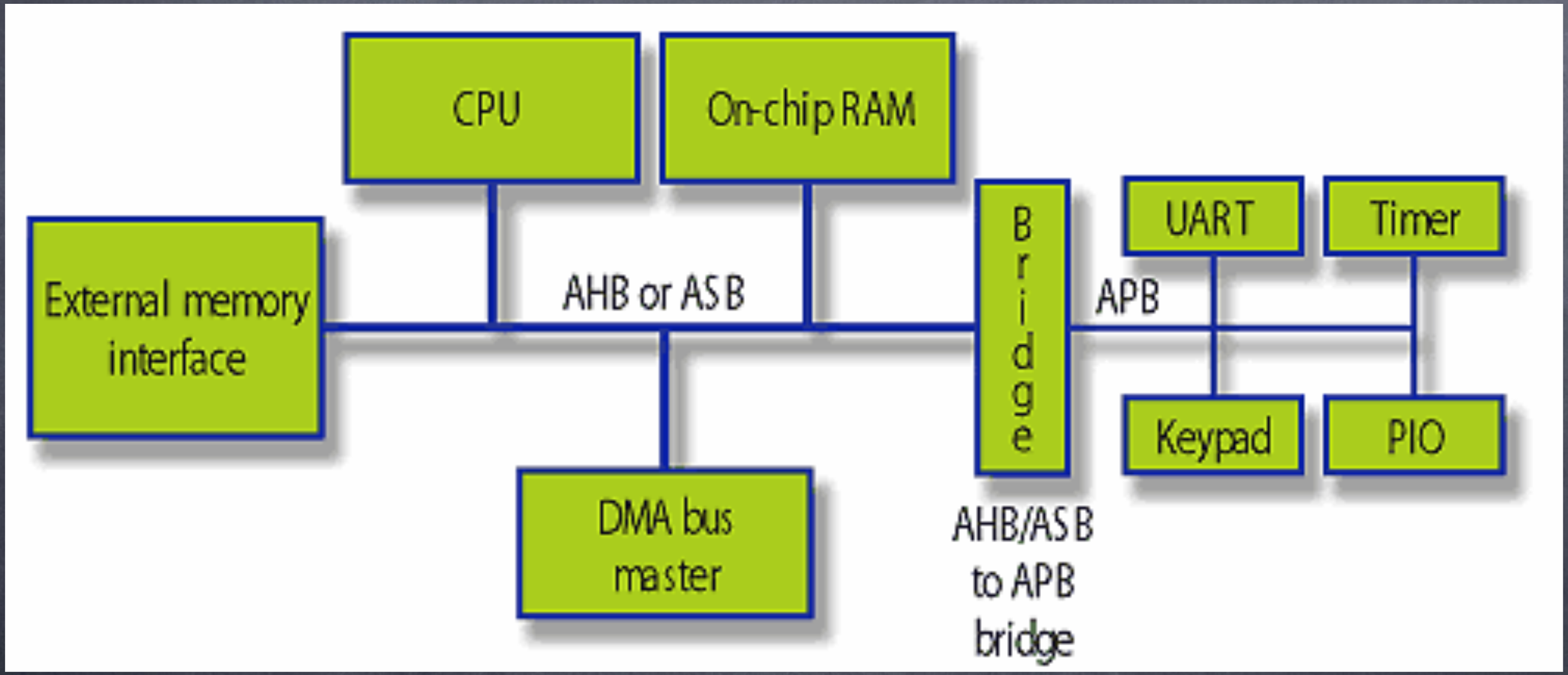
GROUP 3

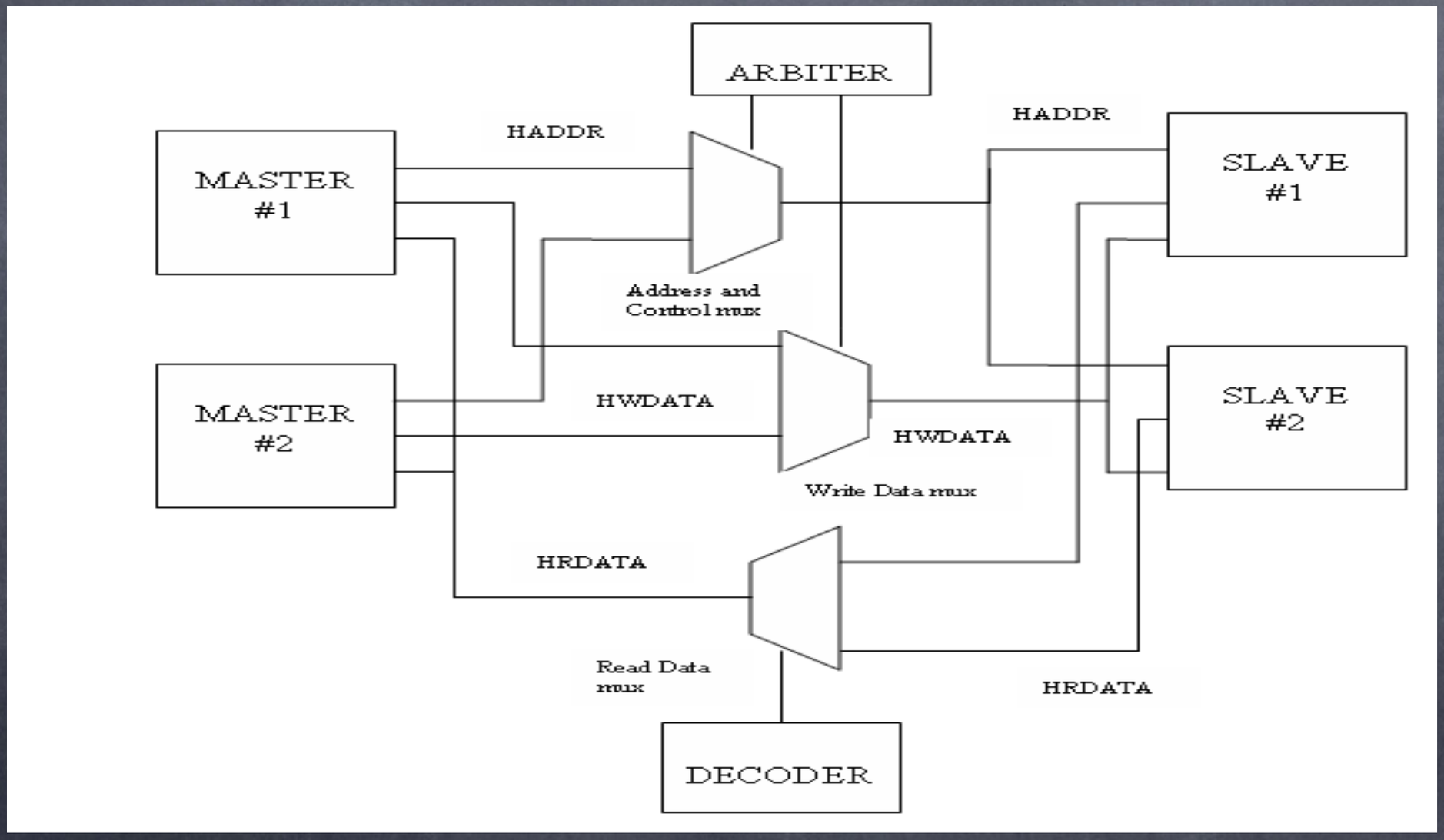
Typical AMBA Systems



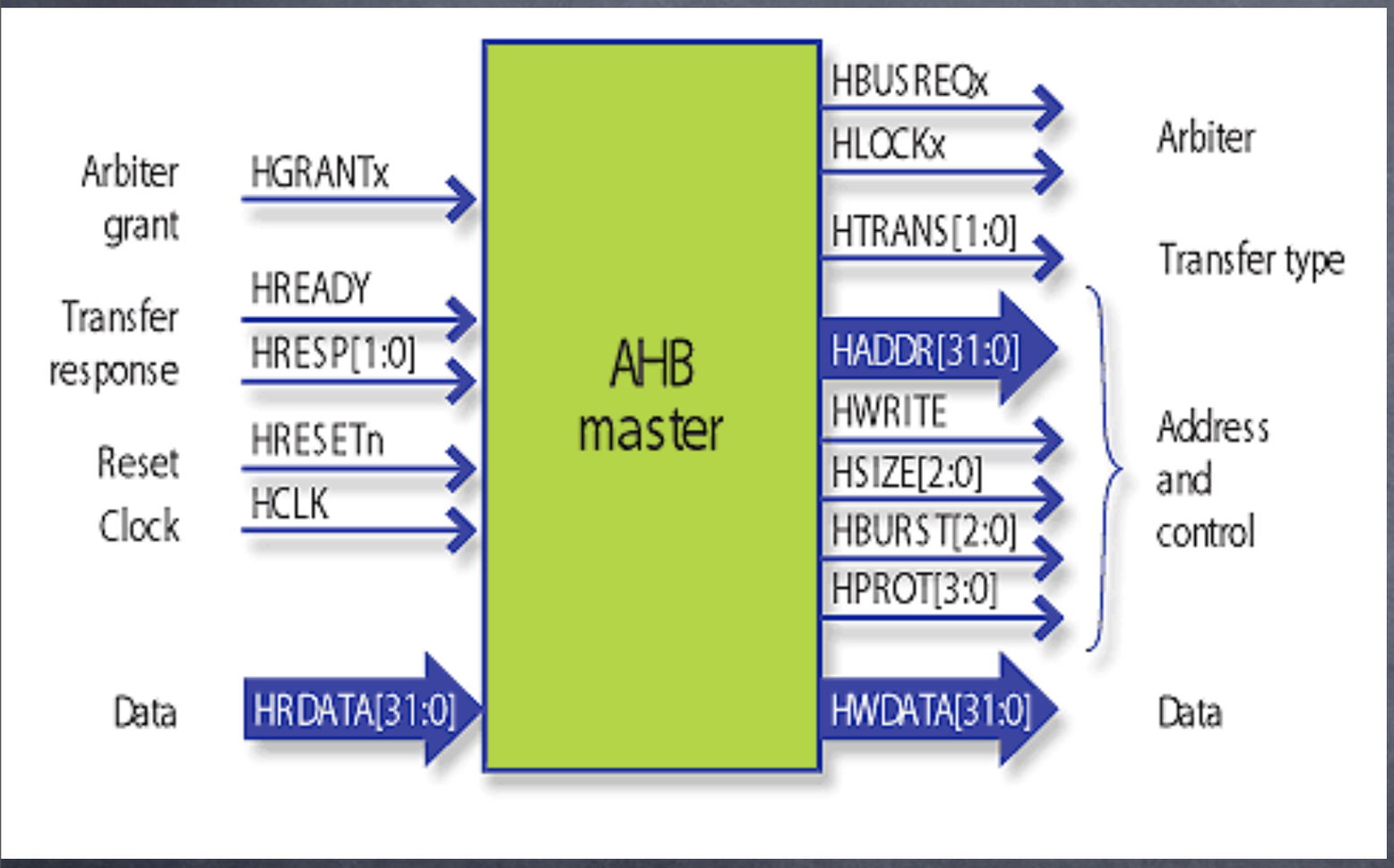
Wishbone Definition

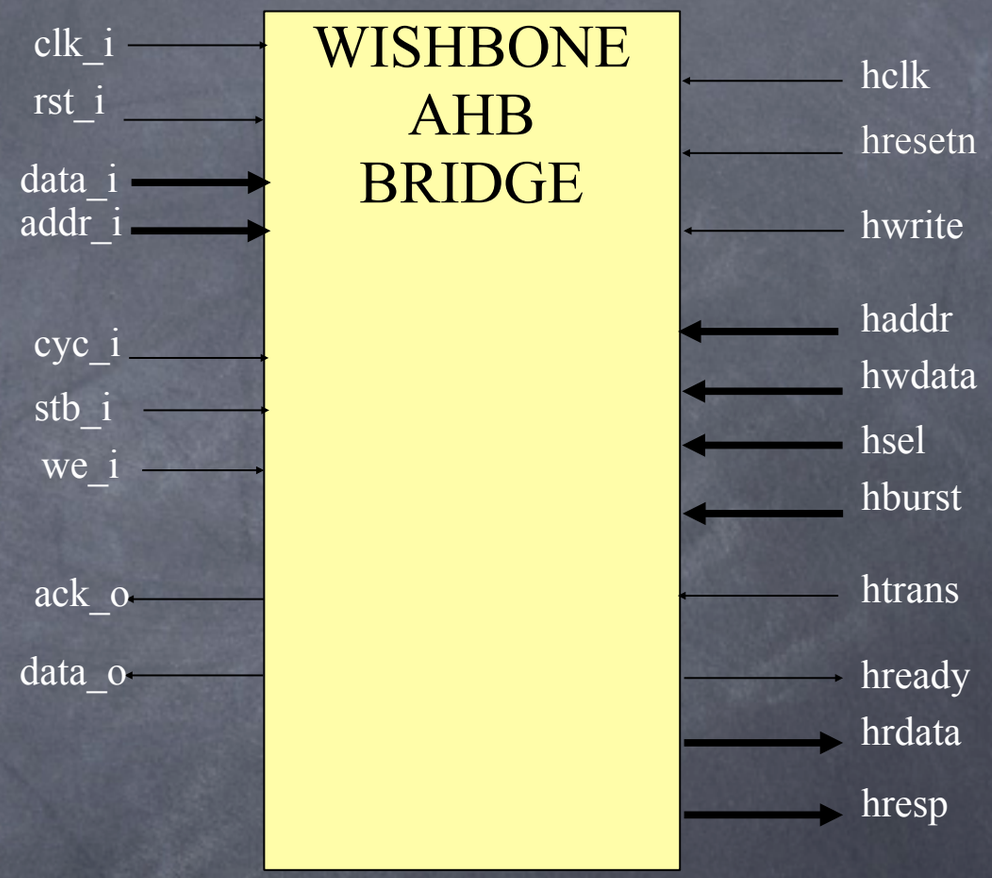
- It's a SOC Interconnect architecture for Portable IP cores
- it's purpose is to foster design reuse by alleviating SOC integration problems
- improves portability and reliability by creating a common logical interface between IP cores
- it's not an IP core but a specification for creating IP cores.

AMBA AHB design with two masters and two slaves.



This file is a BRIDGE that is used to interconnect AHB Master and WISHBONE Slave





AHB MASTER INTERFACE

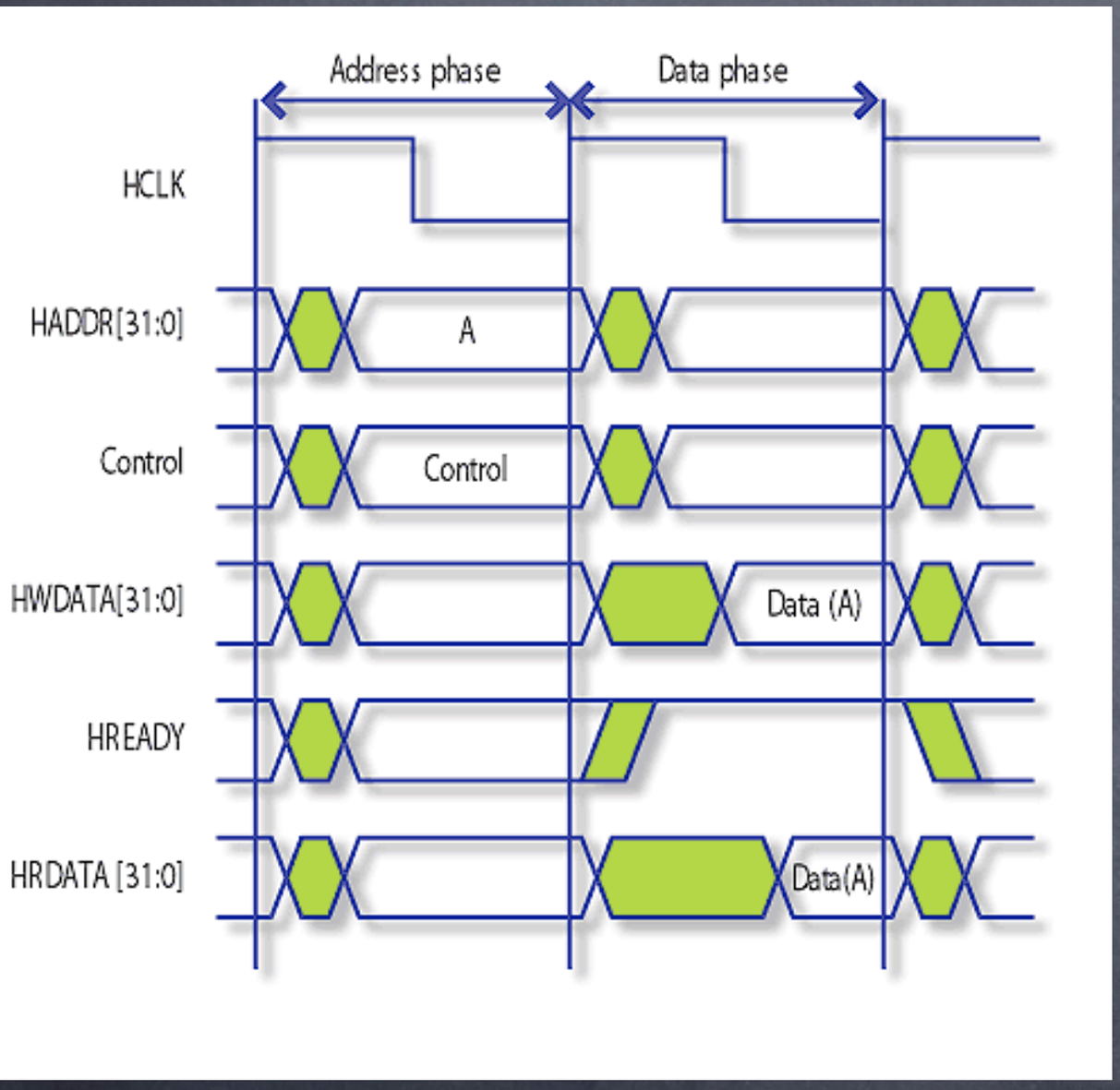
- HADDR[31:0]
- HWDATA [31:0] WRITE DATA BUS
- HRDATA[31:0]: READ DATA BUS
- HWRITE[0] WRITE/READ CONTROL
- HTRANS[1:0] TRANSFER TYPE
- HSIZE[2:0]: SIZE OF DATA CONTROL
- HREADY: SIGNAL TO BE SEND OUT To indicate bridge is ready
- HRESP[1:0]: RESPONSE FROM AHB SLAVE

WISHBONE SLAVE INTERFACE CONNECTED TO WB MASTER

- clk_i Wb clk input
- rst_i Wb active high reset
- data_i [31:0] Wb data input
- cyc_i Wb cycle input
- stb_i Wb strobe input
- we_i Wb write/read control
- ack_o Wb aknowledge
- data_o [31:0] Wb data output

AHB MASTER TO WB SLAVE, TOP LEVEL CIRCUIT

A single AHB cycle read or write transfer between master and slave



It can be seen that all AHB transfers may be divided into an address phase, where the master generates the address and control information and a data phase. In the data phase, data is transferred either from the master to the slave (a write) or from slave to the master (a read). All signals are generated from the rising edge of HCLK. The address and data phases are pipelined. The master must hold the address phase until the data phase of the previous transfer is complete. The data phase is signalled complete by the slave driving HREADY high. The master should sample the slave response only when HREADY is high. The slave does not have the opportunity to extend the address phase, it can only extend the data phase.

Wishbone Master Write Cycle

- When we_i is HIGH, this signal indicates a write transfer and the master will broadcast data on the write data bus(data_i) when cyc_i and stb_i signal is HIGH.

- At 1st clock edge the address(A1) and data (D1)is sampled by the WISHBONE slave on addr_i and data_i bus respectively.

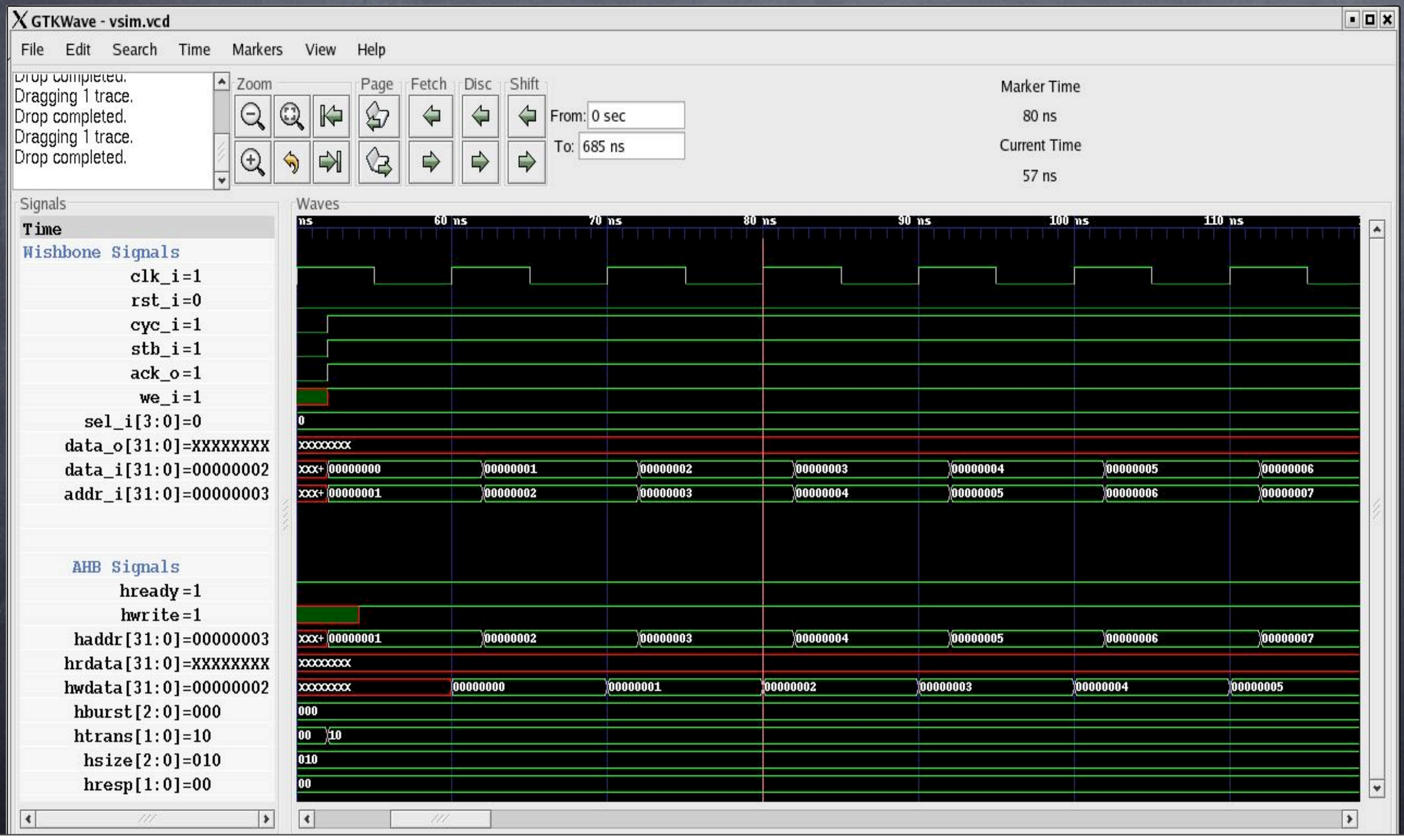
- At 1st clock edge the address(A1) and data (D1)is sampled by the WISHBONE slave on addr_i and data_i bus respectively.

- At 1st clock edge ack_o is also asserted. This address sampled is transfered asynchronously to the AHB master on haddr.

At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB master on to hwdata bus irrespective of hready status.
This data is written into the AHB slave synchronously on hwdata bus.

- Htrans is asserted to "Non – Seq (10)" transfer type at clock edge when cyc_i and stb_i are HIGH.

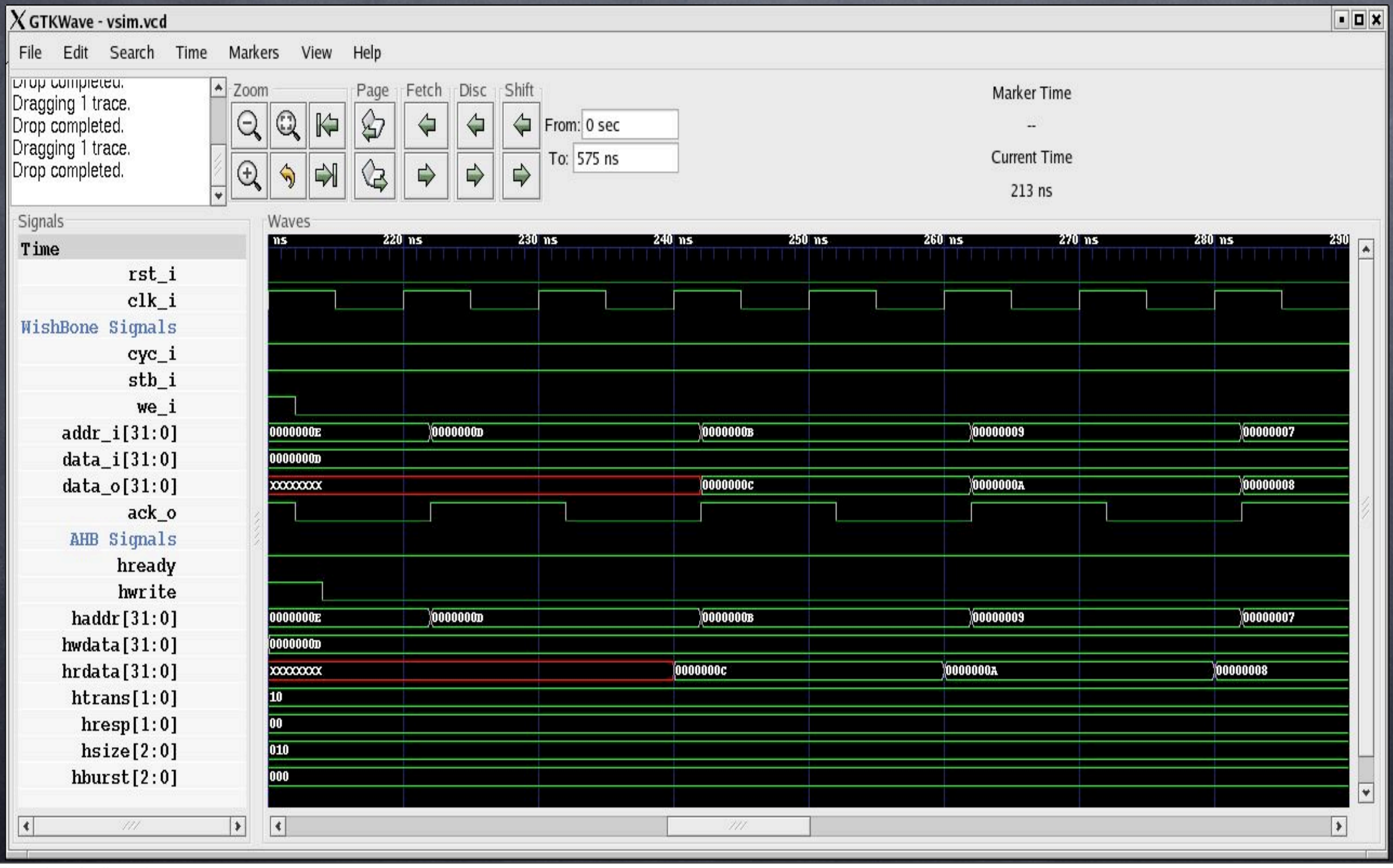
Write cycle


GTKWave - vsim.vcd
File Edit Search Time Markers View Help
Dragging 1 trace.
Drop completed.
Dragging 1 trace.
Drop completed.
Zoom
Page
Fetch
Disc
Shift
From: 0 sec
To: 685 ns
Marker Time
80 ns
Current Time
57 ns
Signals
Waves
Time
Wishbone Signals
clk_i=1
rst_i=0
cyc_i=1
stb_i=1
ack_o=1
we_i=1
sel_i[3:0]=0
data_o[31:0]=XXXXXXXX
data_i[31:0]=00000002
addr_i[31:0]=00000003
AHB Signals
hready=1
hwrite=1
haddr[31:0]=00000003
hrdata[31:0]=XXXXXXXX
hwdata[31:0]=00000002
hburst[2:0]=000
htrans[1:0]=10
hsize[2:0]=010
hresp[1:0]=00
ns
60 ns
70 ns
80 ns
90 ns
100 ns
110 ns

Read cycle

- When we_i is LOW, this signal indicates a read transfer and the master will receive data on the read data bus (data_o) provided the ack_o signal is HIGH.
- At 1st clock edge the address(A1) is sampled by the WISHBONE slave on addr_i.
- This address will be transfered asynchronously to AHB master on haddr provided hready is HIGH.
- At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB on hrdata.
- Data (D1) is latched on hrdata bus asynchronously when hready is asserted.
- Data (D1) is latched on data_o asynchronously at the same time.
- At 2nd clock edge ack_o is asserted.
- Htrans is asserted to "Non - Seq (10)" transfer type at clock edge when cyc_i and stb_i are HIGH.

Read cycle


GTKWave - vsim.vcd
File Edit Search Time Markers View Help
Dragging 1 trace.
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Drop completed.
Zoom
Page
Fetch
Disc
Shift
From: 0 sec
To: 575 ns
Marker Time
--
Current Time
213 ns
Signals
Waves
Time
rst_i
clk_i
WishBone Signals
cyc_i
stb_i
we_i
addr_i[31:0]
data_i[31:0]
data_o[31:0]
ack_o
AHB Signals
hready
hwrite
haddr[31:0]
hwdata[31:0]
hrdata[31:0]
htrans[1:0]
hresp[1:0]
hsize[2:0]
hburst[2:0]
ns
220 ns
230 ns
240 ns
250 ns
260 ns
270 ns
280 ns
290
0000000E
0000000D
0000000B
00000009
00000007
0000000D
xxxxxxxx
0000000C
0000000A
00000008
10
00
010
000

Synthesizability

- This code is completely synthesizable.
- The only care that has to be taken is that the AHB clock(hclk) and reset(hresetn) signals have been left unconnnected inside the design. The whole design is working on Wishbone clock and reset signals that should be provided by Wishbone master.