CS230 - Digital Logic Design and Computer Architecture

Problem Set 5

Autumn 2023

Q1. We want to compare the computers R1 and R2, which differ in that R1 has the machine instructions for the floating point operations, while R2 does not (FP operations are implemented in the software using several non-FP instructions). Both computers have a clock frequency of 400 MHz. In both we perform the same program, which has the following mixture of commands:

Type of command	Dynamic Share of instr	No of clock period R1	No of clock period R2
FP addition	16%	6	20
FP multiplication	10%	8	32
FP Division	8%	10	66
Non-FP instruction	66%	3	3

a) Calculate the MIPS for the computers R1 and R2.

b) Calculate the CPU program time on the computers R1, R2, if there are 12000 instructions in the program?

Q2. Suppose that when Program A is run, the user CPU time is 3 seconds, the elapsed wallclock time is 4 seconds, and the system performance is 10 MFLOP/sec. Assume that there are no other processes taking any significant amount of time, and the computer is either doing calculations in the CPU, or doing I/O, but it can't do both at the same time. We now replace the processor with one that runs six times faster, but doesn't affect the I/O speed. What will the user CPU time, the wallclock time, and the MFLOP/sec performance be now?

Q3. Suppose a program (or a program task) takes 1 billion instructions to execute on a processor running at 2 GHz. Suppose also that 50% of the instructions execute in 3 clock cycles, 30% execute in 4 clock cycles, and 20% execute in 5 clock cycles. What is the execution time for the program or task?

Q4. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark B, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	Frequency	Cycles
Load and stores	30%	6 cycles
Arithmetic Instructions	50%	4 cycles
All others	20%	3 cycles

Calculate the CPI for Benchmark B.

Q5. ACPU has a five-stage pipeline and runs at 1*GHz* frequency.Instruction fetch happens in the first stage of the pipeline. Conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is ?