CS230 - Digital Logic Design and Computer Architecture

Problem Set 6

Autumn 2023

Q1. Consider an array of 4 elements, and each element occupies 4-bytes. A 16-byte cache is used and divided into a block of 8 bytes. If the following code is executed, what is the hit ratio? (Use column-major order)

```
for (i = 0; i < 2; i ++)
    for (j = 0; j < 2; j ++)
        x = A [i , j] + A [j , i]
```

Q2. A memory system consisting of two levels L1 and L2. The required access times of those are 5 ns and 120 ns, respectively. Another memory system also has two levels L1' and L2', whose access times are 10 ns and 150 ns, respectively. The hit ratio of the second system is 0.8, and the average access time is twice that of the first system. What is the hit ratio of the first system?

Q3. A CPU has a 32 bit memory address and a 256KB cache memory. The cache is organized as a 4-way set associative cache with a cache block size 16 of bytes.

A. What is the number of sets in the cache?
B. What is the size (in bits) of the tag field per cache block?
C. What is the number and size of comparators required for tag matching?
D. How many address bits are required to find the byte offset within a cache block?
E. What is the total amount of extra memory (in bytes) required for the tag bits?

Q4. Consider a fully associative cache with 8 cache blocks and the following sequence of memory block requests - 41, 33, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 33, 16, 25, 73. If the LRU replacement policy is used, which cache block will have memory block 73? (Assume cache blocks are numbered from 0-7)

Q5. The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, what is the length (in number of bits) of the tag field?