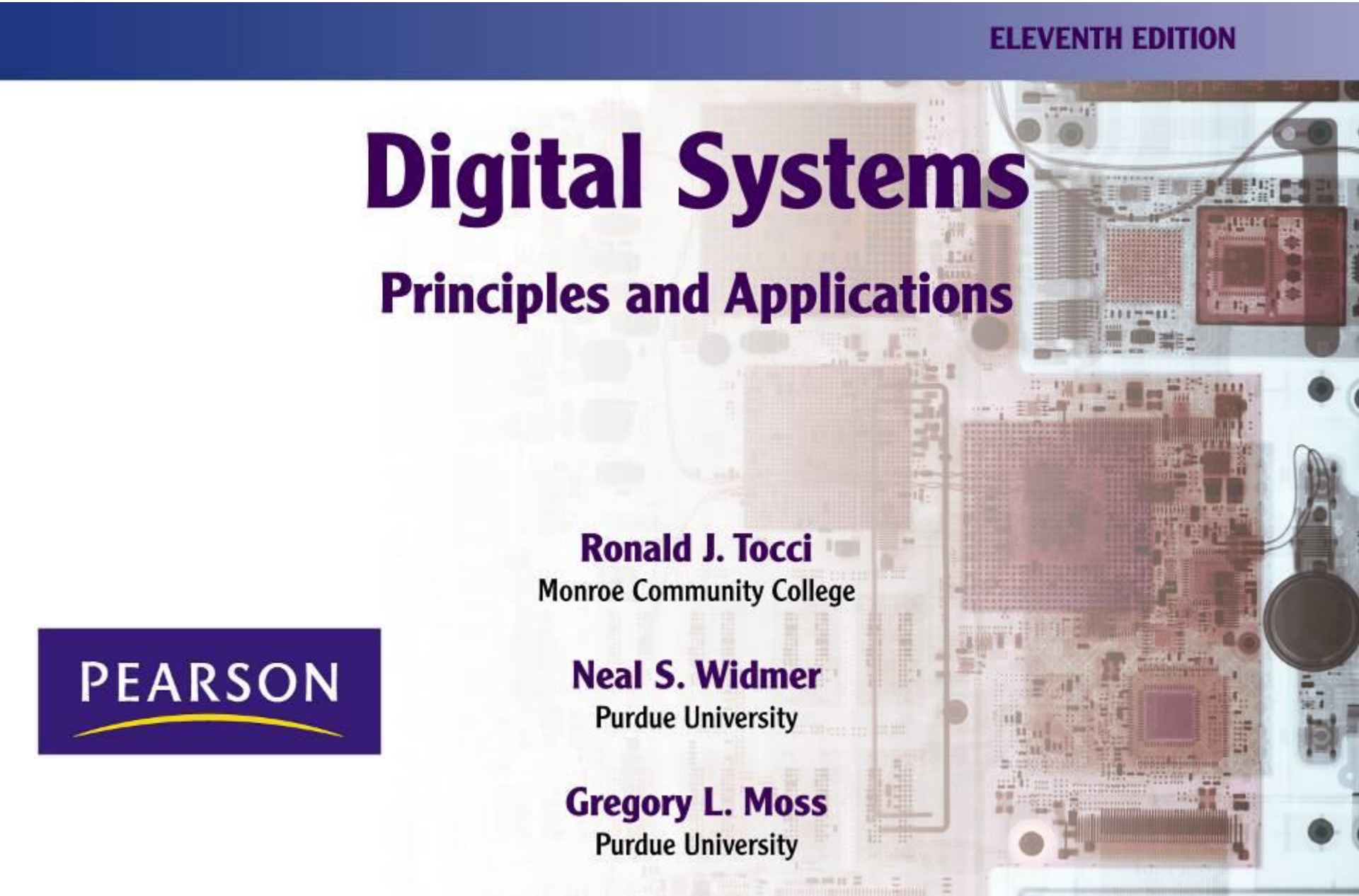

PEARSON

Chapter 8 – Integrated Circuit Logic Families



Chapter 8 Objectives

- *Selected areas covered in this chapter*:
  - Digital IC terminology as in manufacturer data sheets.
  - Characteristics of various TTL series.
  - Characteristics of the various CMOS series.
  - Major characteristics & differences among TTL, ECL, MOS, and CMOS logic families.
  - Considerations when interfacing digital circuits from different logic families.
  - Using voltage comparators to allow a digital system to be controlled by analog signals.
  - Using a logic pulser and a logic probe as digital circuit troubleshooting tools.

- Digital IC technology has advanced rapidly from integrations which can 1 million or more gates.
- ICs pack more circuitry in a small package, so overall size of almost any system is reduced.
  - Cost is reduced because of the economies of mass-producing large volumes of similar devices.
- ICs have made digital systems more reliable by reducing the number of external interconnections from one device to another.
  - Protected from poor soldering, breaks or shorts in connecting paths on a circuit board, and other physical problems.

- ICs cannot handle very large currents or voltage.
  - Heat generated in such small spaces would cause temperatures to rise beyond acceptable limits.
    - For higher power levels, an interfacing circuit will be needed—typically of components or special power ICs.
- ICs can't easily implement certain devices such as inductors, transformers, and large capacitors.
  - Principally used to perform low-power circuit operations—commonly called *information processing*.

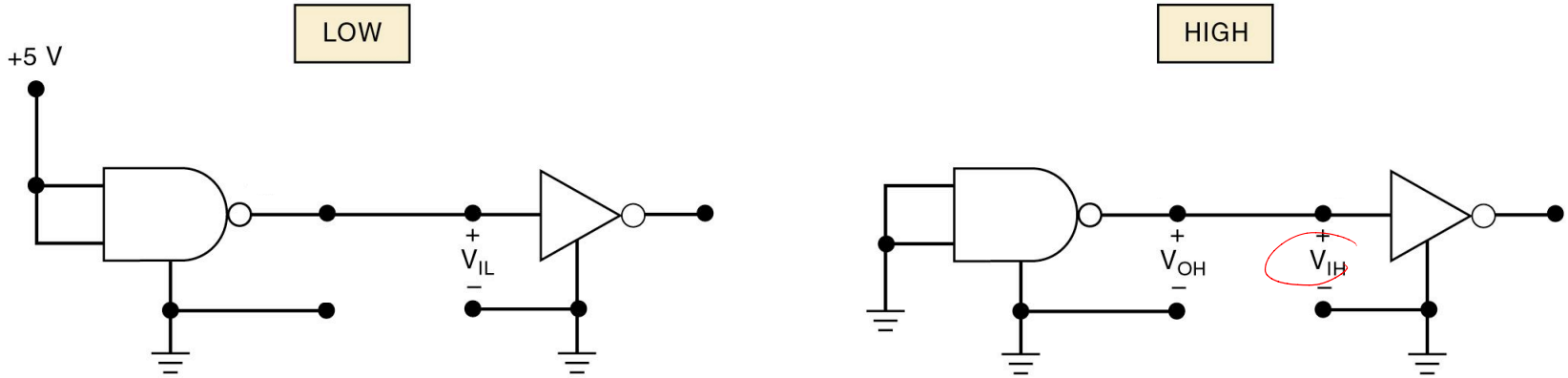
- Various logic families differ in major components in their circuitry.
  - TTL and ECL use *bipolar* transistors as their major circuit element.
  - PMOS, NMOS, and CMOS use unipolar *MO*SFET transistors.

IC nomenclature & terminology is fairly standardized.

V_{IH}(min)—High-Level Input Voltage. The minimum voltage level required for a logical 1 at an *input*. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

V_{IL}(max)—Low-Level Input Voltage. The maximum voltage level required for a logic 0 at an *input*. Any voltage above this level will not be accepted as a LOW by the logic circuit.

V_{OH}(min)—High-Level Output Voltage. The minimum voltage level at a logic circuit *output* in the logical 1 state under defined load conditions.



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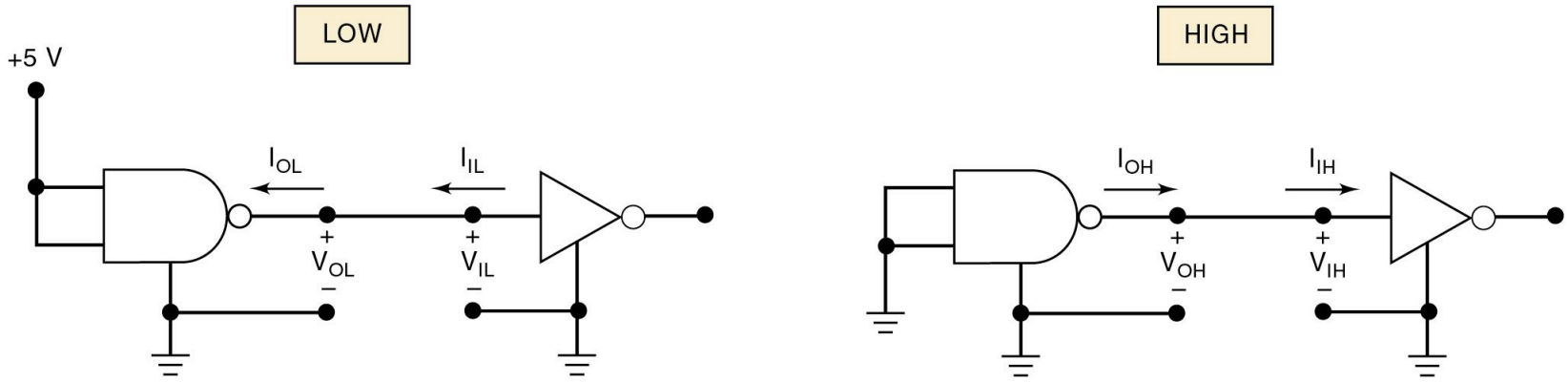


V_{OL}(max)—Low-Level Output Voltage. The maximum voltage level at a logic circuit *output* in the logical 0 state under defined load conditions.

I_{IH}—High-Level Input Current. The current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL}—Low-Level Input Current. The current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH}—High-Level Output Current. The current that flows from an output in the logical 1 state under specified load conditions.

I_{OL}—Low-Level Output Current. The current that flows from an output in the logical 0 state under specified load conditions.

8-1 Digital IC Terminology – Fan Out

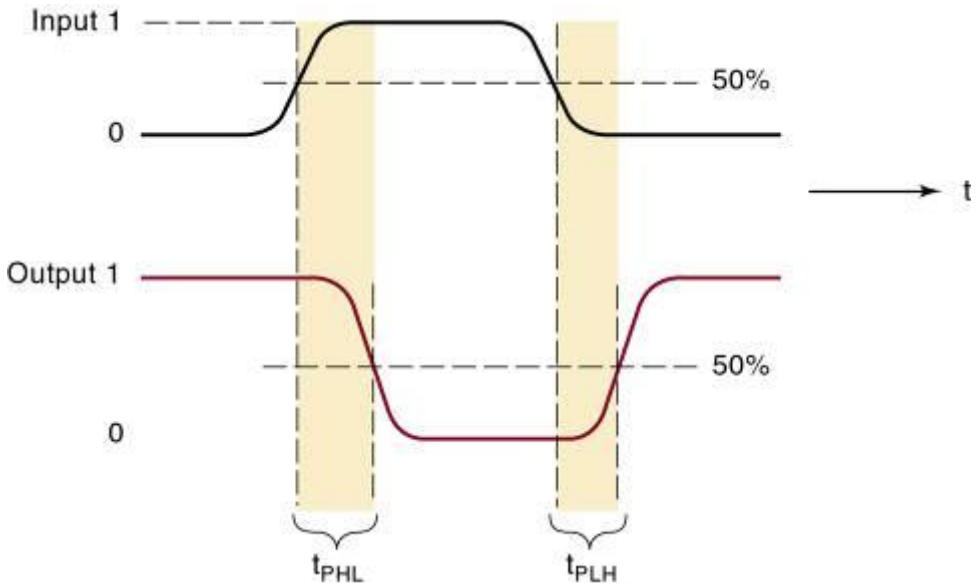
- A logic-circuit output is generally required to drive several logic inputs.
  - Sometimes all ICs are from the same logic family.
    - But many systems have a mix of various logic families.
  - The **fan-out**—*loading factor*—is the *maximum* number of logic inputs an output can drive reliably.

8-1 Digital IC Terminology – Propogation Delay

- A logic signal always experiences a delay going through a circuit.
  - The two propagation delay times are defined as:

t_{PLH}. Delay time in going from logical 0 to logical 1 state (LOW to HIGH)
t_{PHL}. Delay time in going from logical 1 to logical 0 state (HIGH to LOW)

Propagation delays.



8-1 Digital IC Terminology – Power Requirements

- Every IC requires a certain amount of electrical power to operate.
  - Supplied by one or more power-supply voltages connected at V_{CC} (TTL) or V_{DD} (MOS devices).
  - For many ICs, current drawn from the supply varies depending on logic states of the circuits on the chip.

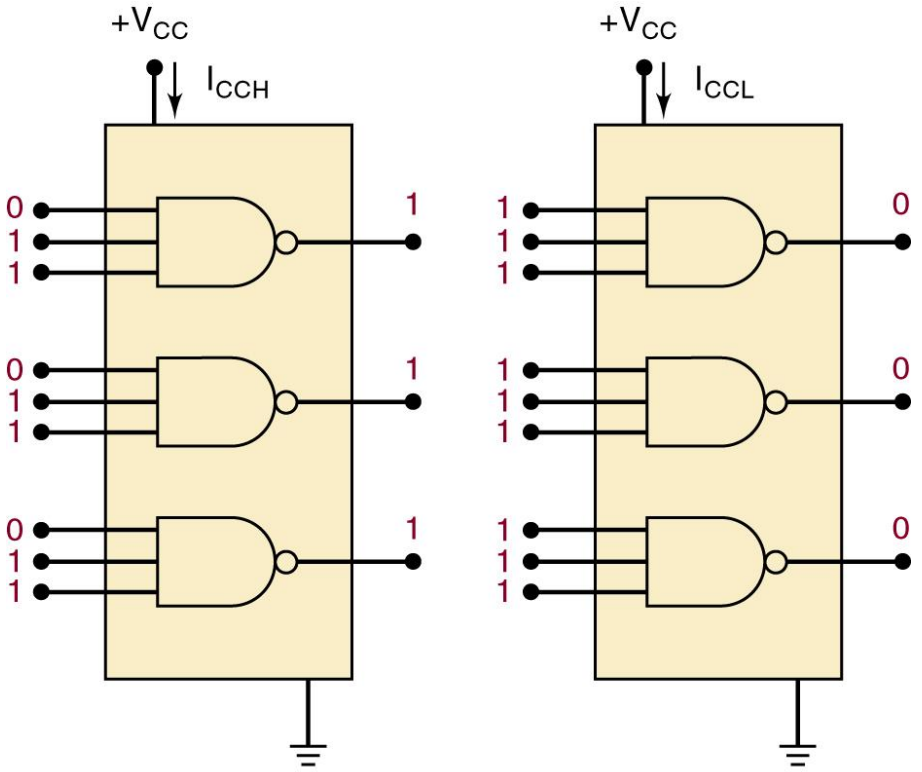
$P = VI$

8-1 Digital IC Terminology – Power Requirements

- The amount of power an IC requires is determined by the current, I_{CC} (or I_{DD}) it draws from the supply.
  - Actual power is the product I_{CC} x V_{CC} (I_{DD} x V_{DD}).

In some logic circuits, average current is computed based on the assumption that gate outputs are LOW half the time and HIGH half the time.

$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$



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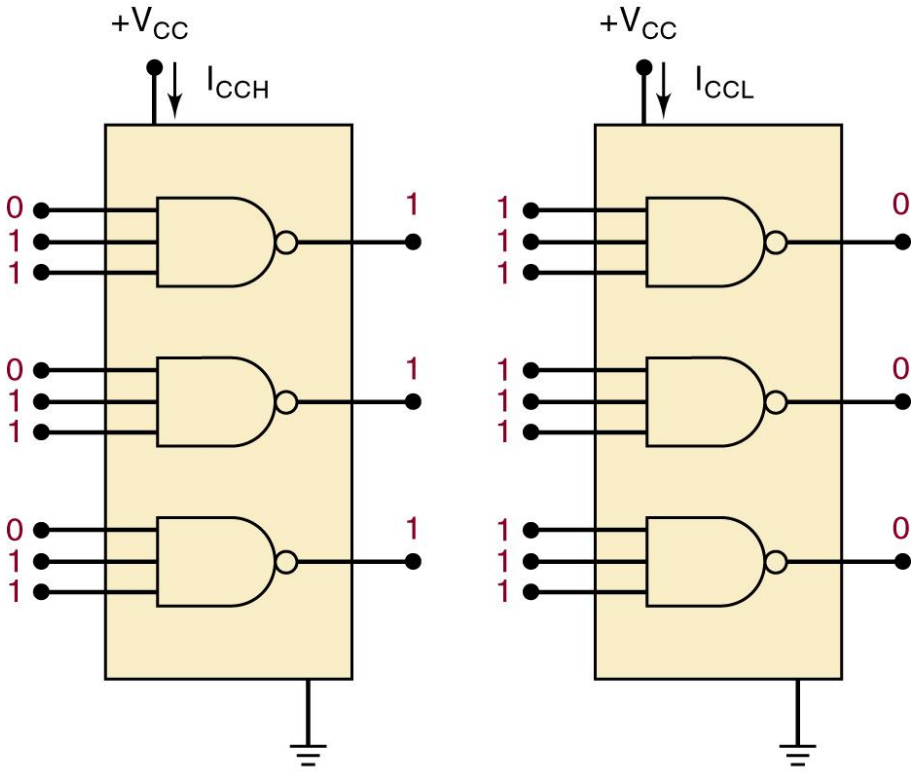
$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$

can be rewritten to calculate average power dissipated:

$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$



8-1 Digital IC Terminology – Noise

- Stray electric/magnetic fields can induce voltages on the connecting wires between logic circuits
  - Called *noise,* these unwanted, spurious signals can sometimes cause unpredictable operation.

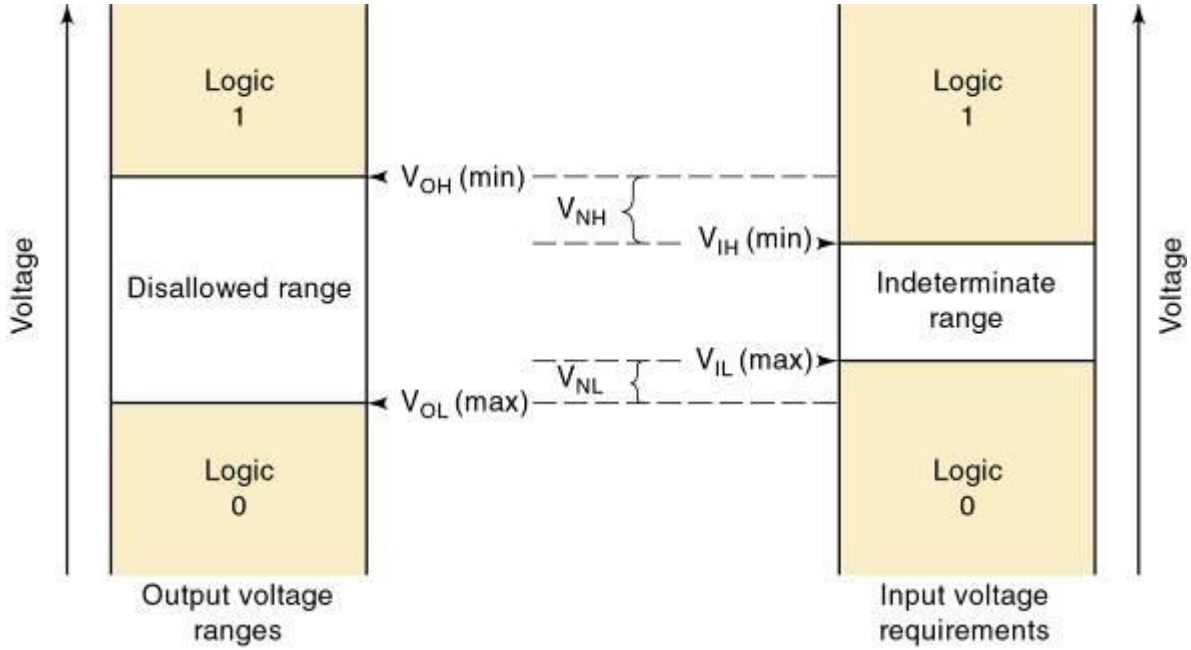
- **Noise immunity** refers to the circuit's ability to tolerate noise without changes in output voltage.
  - A quantitative measure is called **noise margin**.

High-state noise margin:

$$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$$
$$= 2.4\,\text{V} - 2.0\,\text{V} = 0.4\,\text{V}$$

Low-state noise margin:

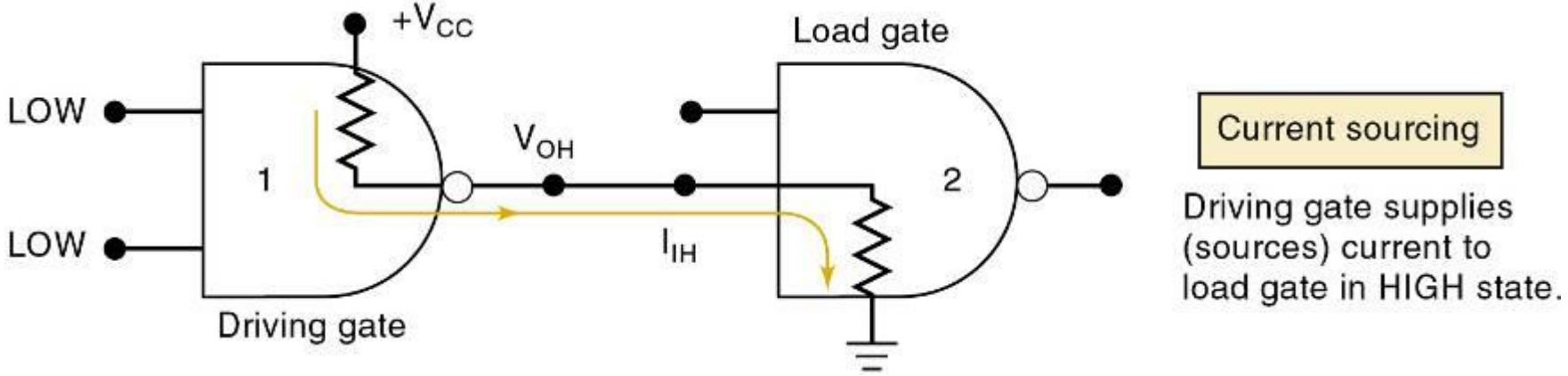
$$V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$$



8-1 Digital IC Terminology – Invalid Voltage

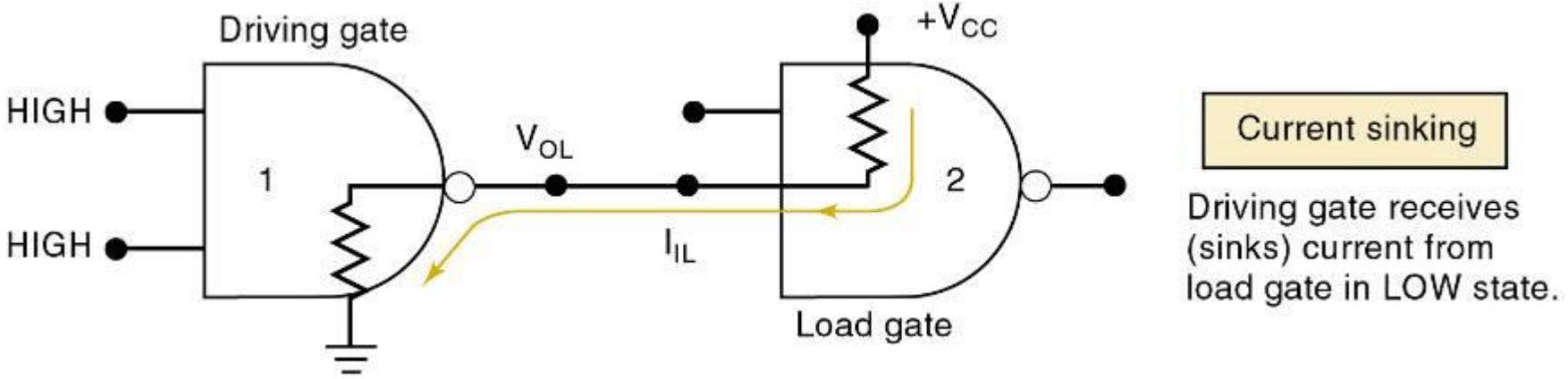
- For proper operation, logic circuit input voltage levels must be kept out of the indeterminate range.
  - Lower than V_{IL}(max) or higher than V_{IH} (min).
    - *Invalid* voltage will produce unpredictable output.
- It is important to know valid voltage ranges for the logic family being used so invalid conditions can be recognized when testing or troubleshooting.
- Logic families can be described by how current flows between the output of one logic circuit and the input of another.

8-1 Digital IC Terminology – Current Sourcing/Sinking



- **Current-sourcing** action.
  - When the output of gate 1 is HIGH, it supplies current I_{IH} to the input of gate 2.
    - Which acts essentially as a resistance to ground.
  - The output of gate 1 is acting as a *source* of current for the gate 2 input.

8-1 Digital IC Terminology – Current Sourcing/Sinking



- **Current-sinking** action.
  - Input circuitry of gate 2 is represented as a resistance tied to $+V_{CC}$ —the positive terminal of a power supply.
  - When gate 1 output goes LOW, current will flow from the input circuit of gate 2 back through the output resistance of gate 1, to ground.
    - Circuit output that drives the input of gate 2 must be able to *sink* a current, I_{IL} , coming from that input.

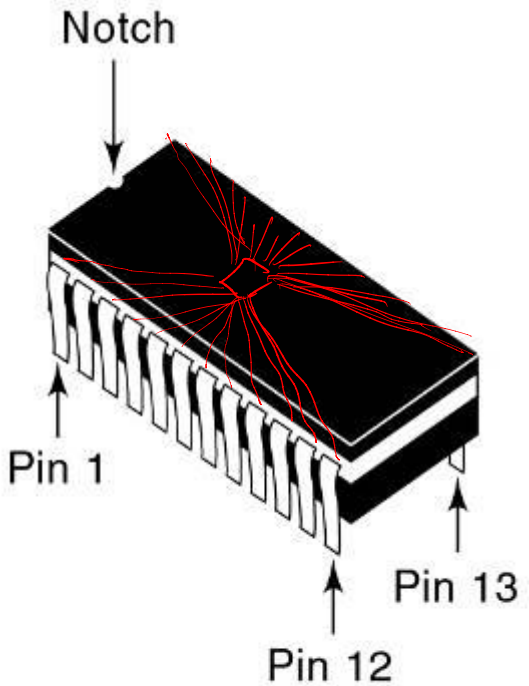
8-1 Digital IC Terminology – IC Packages

- There are many IC packages, differing in physical size, environmental & power consumption conditions, and circuit board mounting

The DIP (dual-in-line package) has pins (leads) down the two long sides of the rectangular package.

The notch on one end, is used to locate pin 1.

Some DIPs use a small dot to locate pin 1.



24-pin DIP

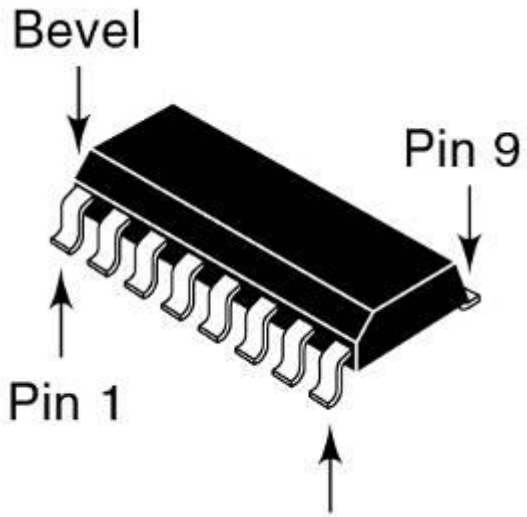
8-1 Digital IC Terminology – IC Packages

- Current manufacturing methods use surface-mount technology (SMT), which places an IC onto conductive pads on the surface of the board.

Held in place by a solder paste, and the entire board is heated to create a soldered connection.

Precision machine placement allows for very tight lead spacing.

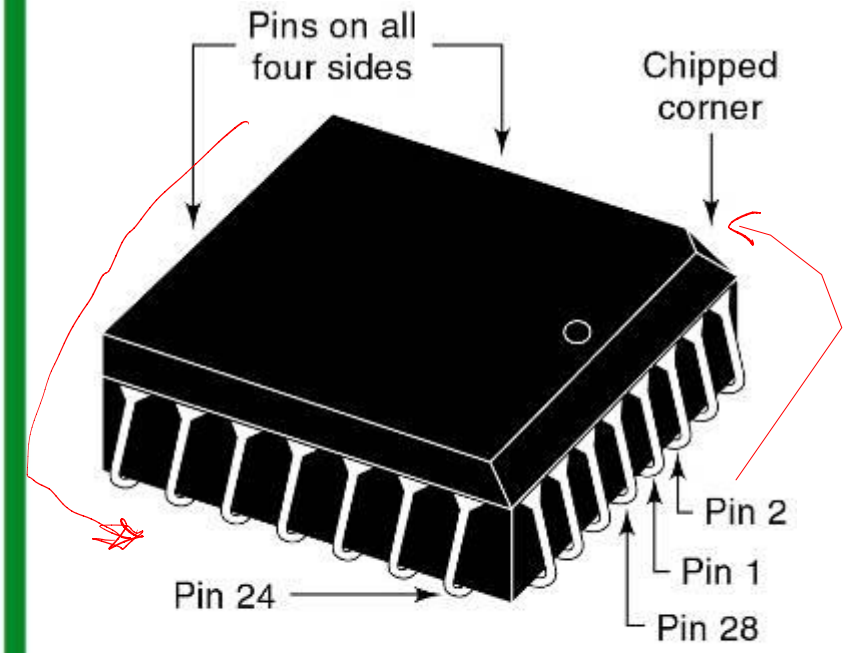
Leads are bent out from the plastic case, providing adequate surface area for the solder joint.



16-pin SOIC (gull-wing) surface-mount

8-1 Digital IC Terminology – IC Packages

- Need for more connections to a complex IC has resulted in another very popular package with pins on all four sides of the chip.



28-pin PLCC
(J-lead)
socket or surface-mount

The PLCC has J-shaped leads that curl under the IC.

These devices can be surface-mounted to a circuit board—but can also be placed in a special socket.

Commonly used for components likely to need to be replaced for repair or upgrade.

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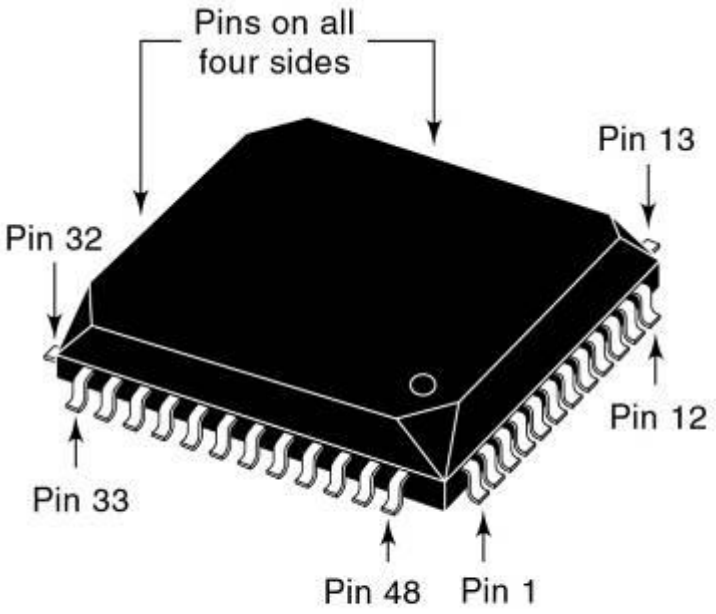


48-pin QFP (gull-wing) surface-mount

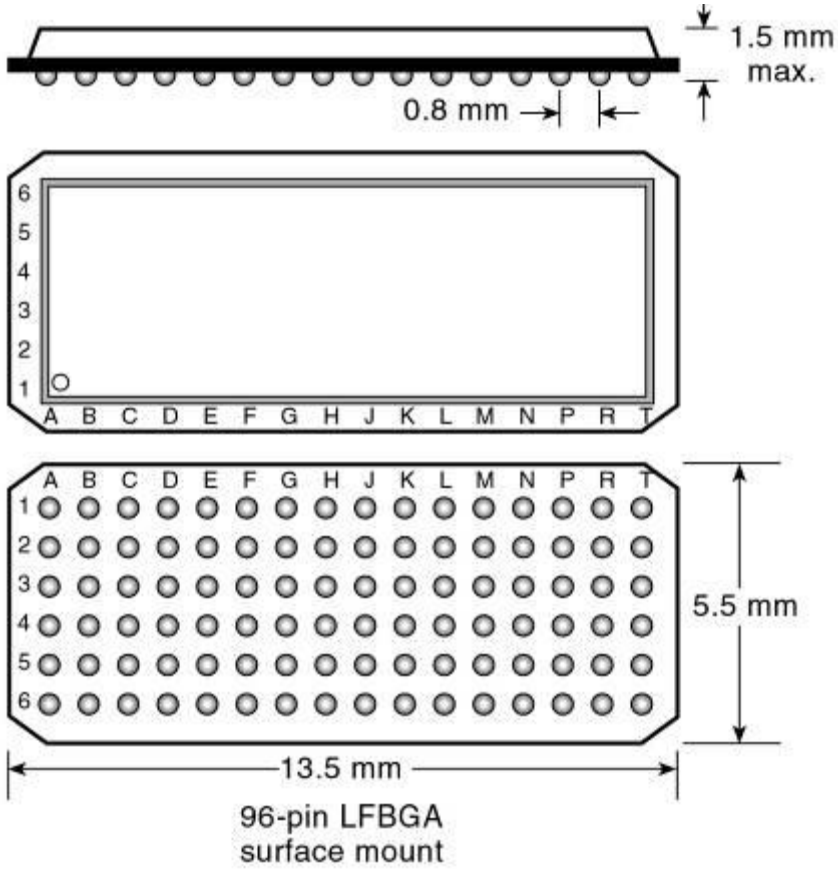
QFP and TQFP packages have pins on all four sides in a gull-wing surface-mount package.

8-1 Digital IC Terminology – IC Packages

- The ball grid array (BGA) shown in is a surface-mount package that offers even more density.

The pin grid array (PGA) is a similar package, use when components must be in a socket to allow easy removal.

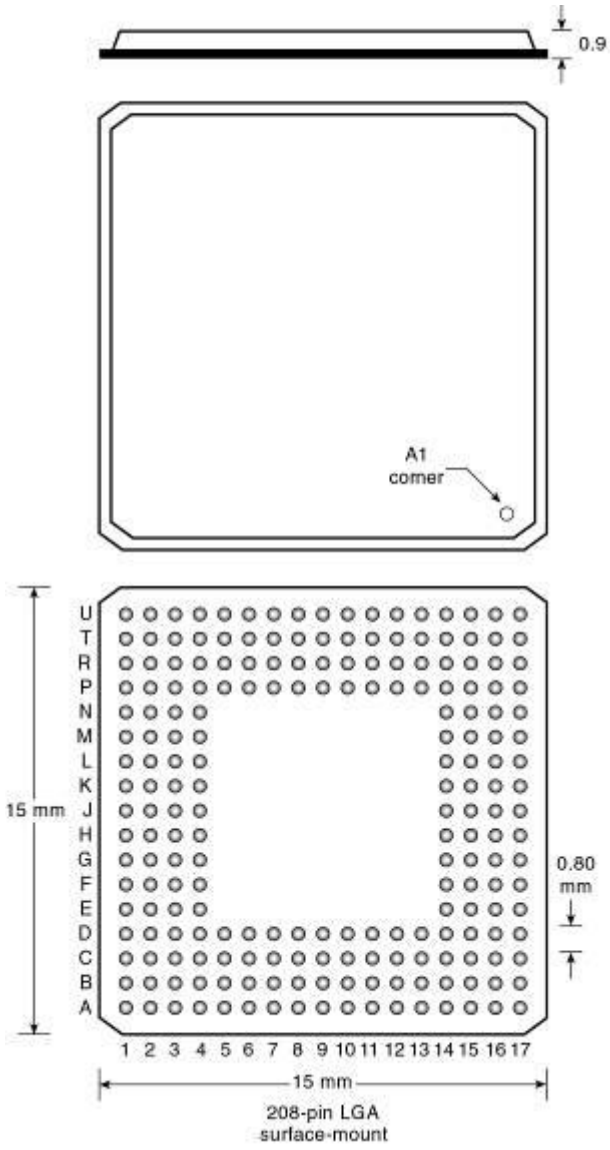
The PGA has a long pin instead of a contact ball (BGA) at each position in the grid.



96-pin LFBGA
surface mount

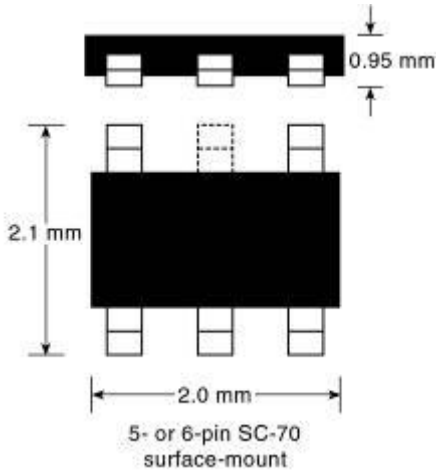
8-1 Digital IC Terminology – IC Packages

- The land grid array (LGA) package is essentially a BGA package without the solder balls attached.



8-1 Digital IC Terminology – IC Packages

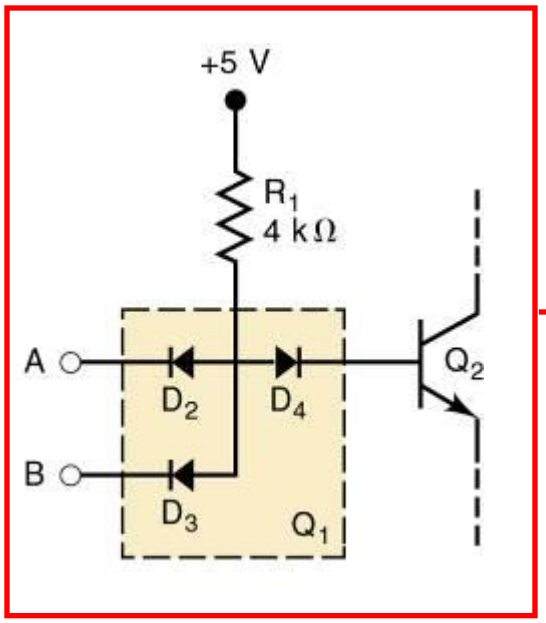
Logic gates are available in individual surface-mount packages containing one, two, or three gates, and as few as five or six pins (power, ground, two to three inputs, and an output)



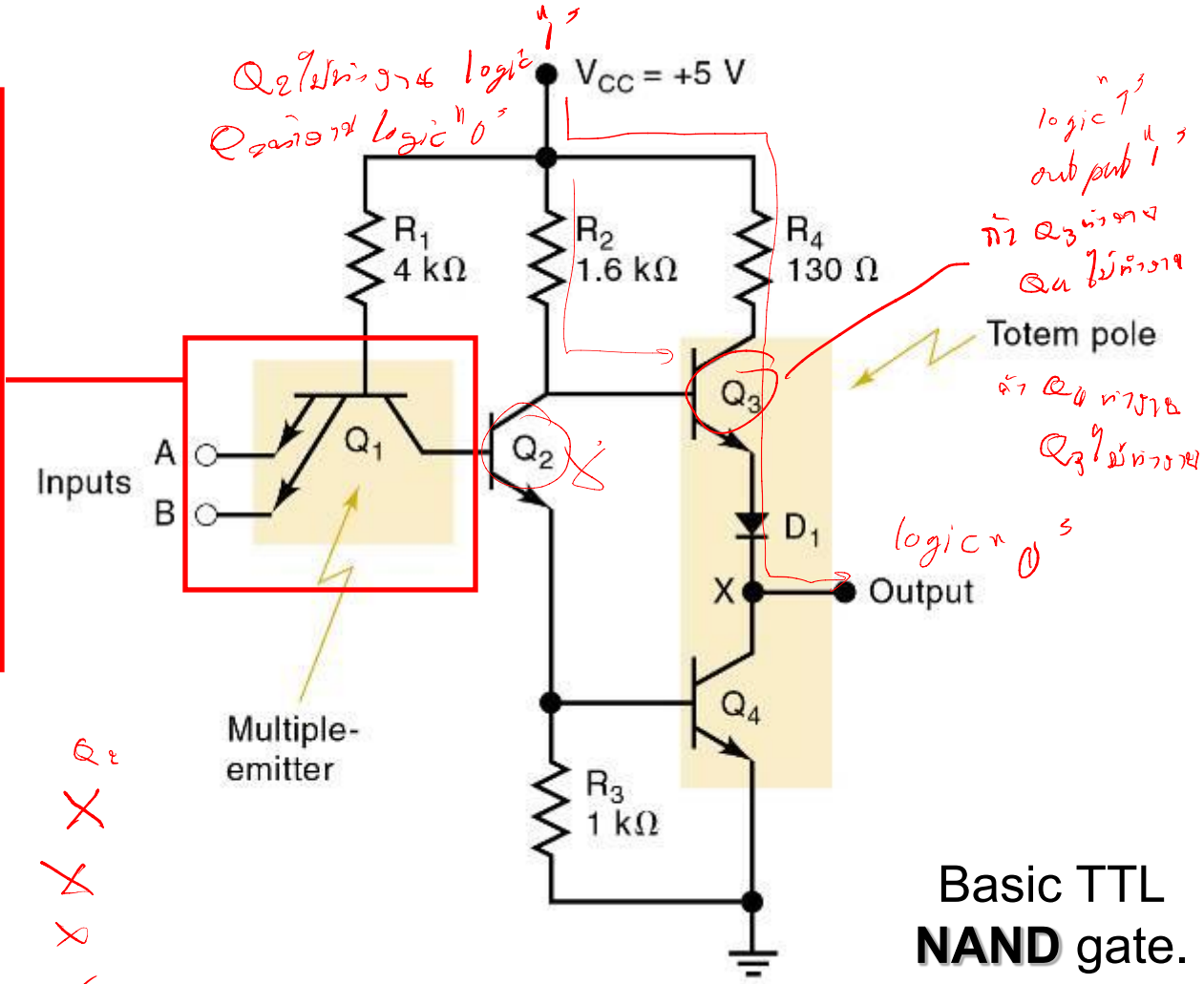
Abbreviation	Package Name	Height	Lead Pitch
DIP	Dual-in-line package	200 mils (5.1 mm)	100 mils (2.54 mm)
SOIC	Small outline integrated circuit	2.65 mm	50 mils (1.27 mm)
SSOP	Shrink small outline package	2.0 mm	0.65 mm
TSSOP	Thin shrink small outline package	1.1 mm	0.65 mm
TVSOP	Thin very small outline package	1.2 mm	0.4 mm
PLCC	Plastic leaded chip carrier	4.5 mm	1.27 mm
QFP	Quad flat pack	4.5 mm	0.635 mm
TQFP	Thin quad flat pack	1.6 mm	0.5 mm
LFBGA	Low-profile fine-pitch ball grid array	1.5 mm	0.8 mm
LGA	Land grid array	0.9 mm	0.8 mm

- Most TTL circuits have a similar structure
  - **NAND** and **AND** gates use multiple-emitter transistor or multiple diode junction inputs.
  - **NOR** and **OR** gates use separate input transistors.
- The input will be the cathode of a P-N junction
  - A HIGH input will turn off the junction.
    - Only a leakage current is generated.
  - A LOW input turns on the junction.
    - Relatively large current is generated.
- Most TTL circuits have some type of totem-pole output configuration.

The basic TTL logic circuit is the NAND gate.

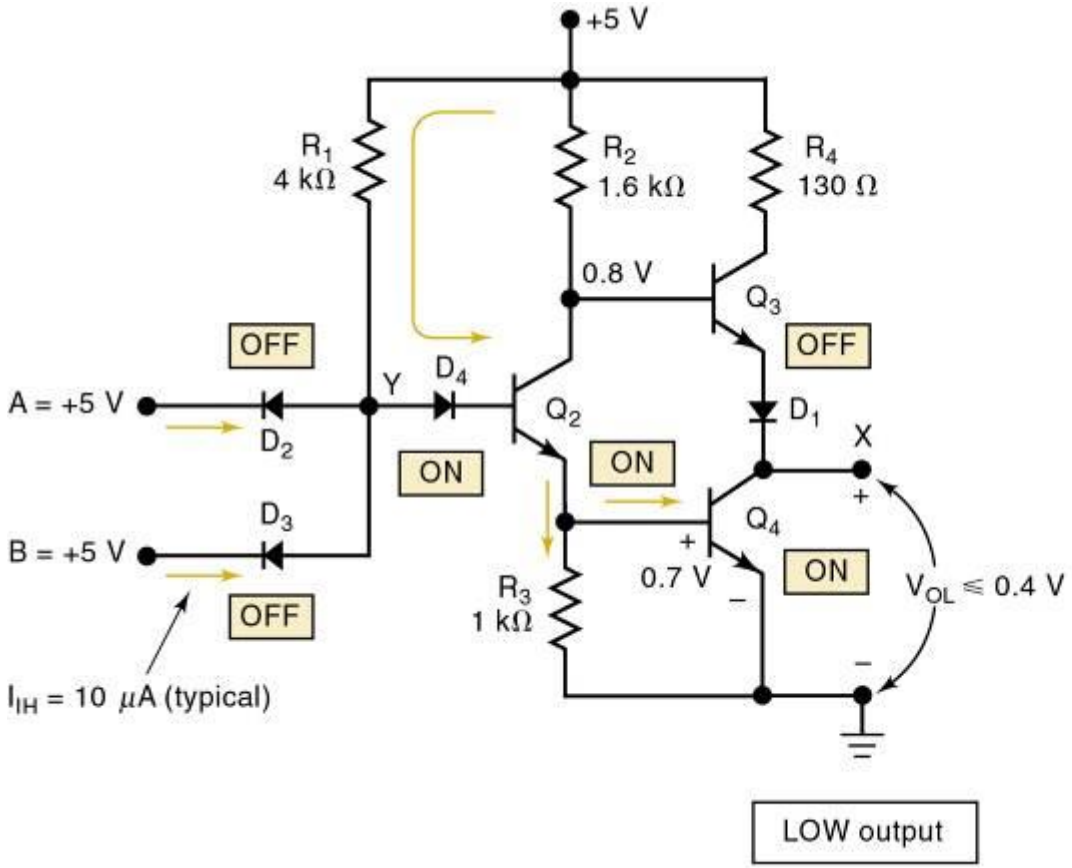


Diode equivalent for Q_1.



Basic TTL **NAND** gate.

TTL NAND gate LOW output

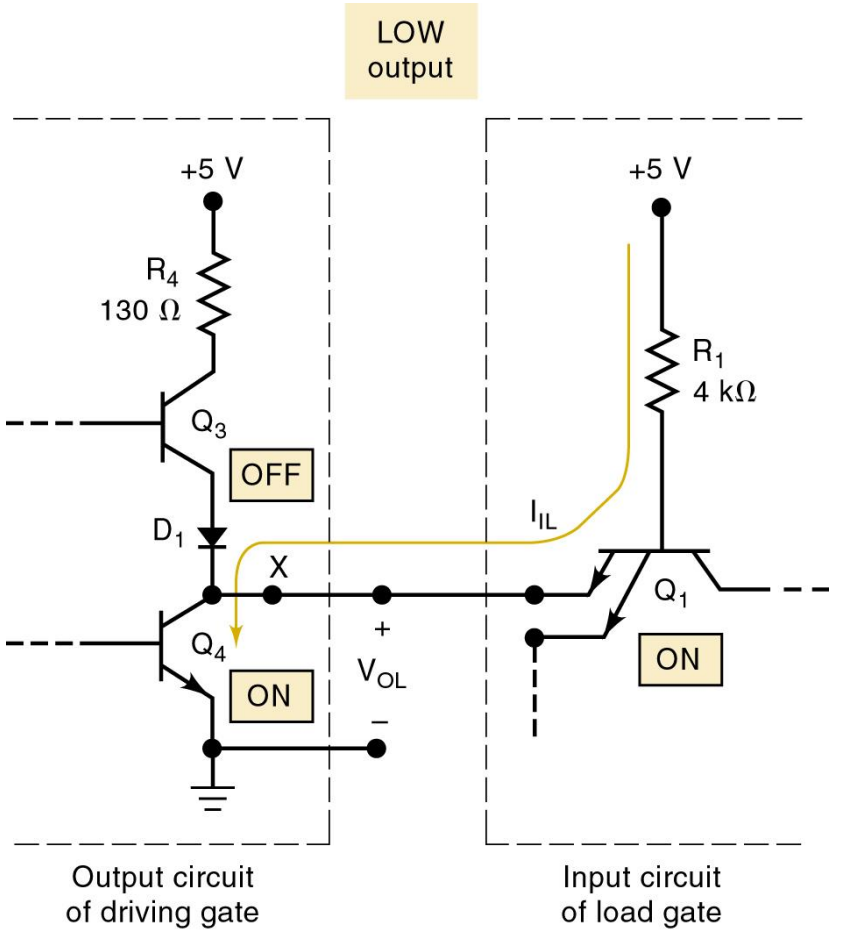


Input conditions	Output conditions
A and B are both HIGH ($\geq$ 2 V)	Q_3 OFF
Input currents are very low I_{IH} = 10 μA	Q_4 ON so that V_X is LOW ($\leq$ 0.4 V)

- A TTL output acts as a current sink in the LOW state because it *receives* current from the input of the gate that it is driving.

Transistor Q_4 of the driving gate is on and essentially "shorts" point *X* to ground.

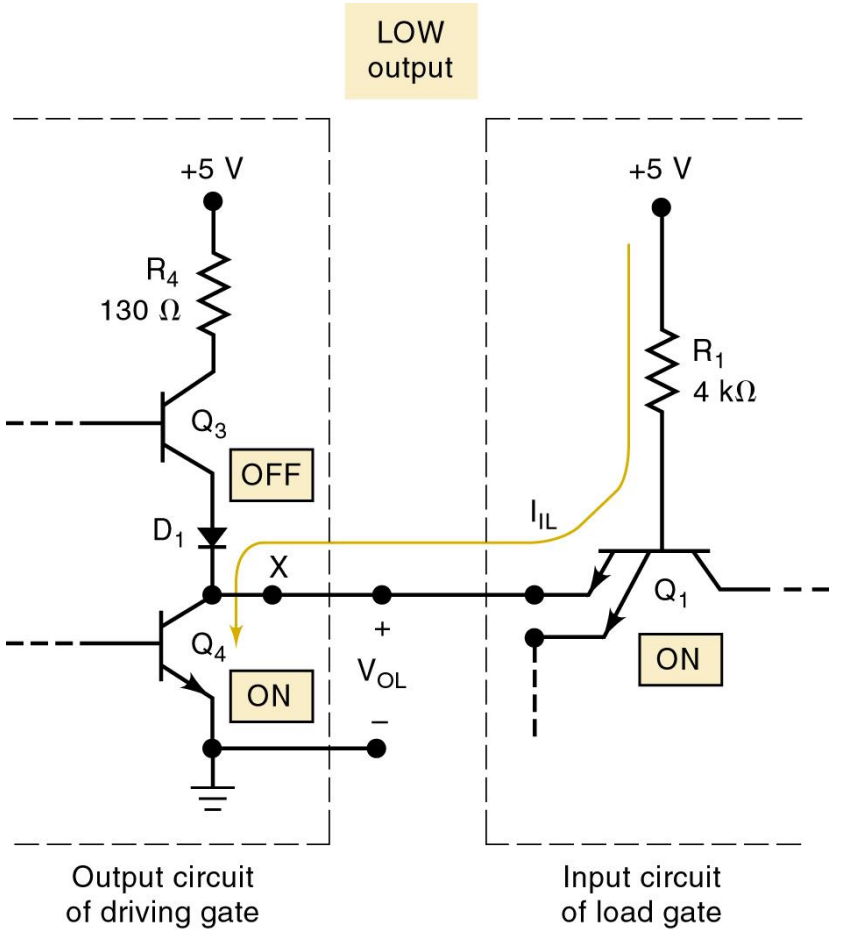
LOW voltage at *X* forward-biases the emitter–base junction of Q_1 & current flows back through Q_4.



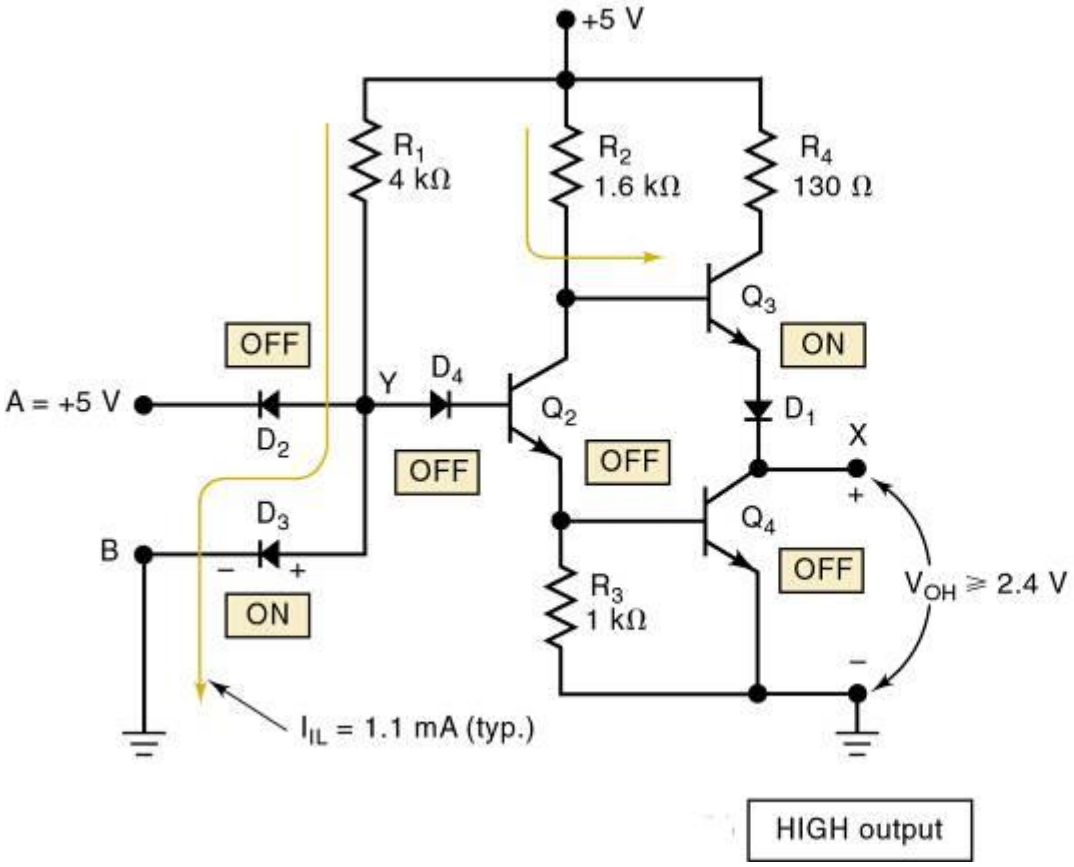
- A TTL output acts as a current sink in the LOW state because it *receives* current from the input of the gate that it is driving.

Q_4 is performing a current-sinking action—deriving its current from the input current (I_{IL}) of the load gate.

Q_4 is often called the **current-sinking transistor** or **pull-down transistor** because it brings the output voltage down to its LOW state.



TTL NAND gate HIGH output



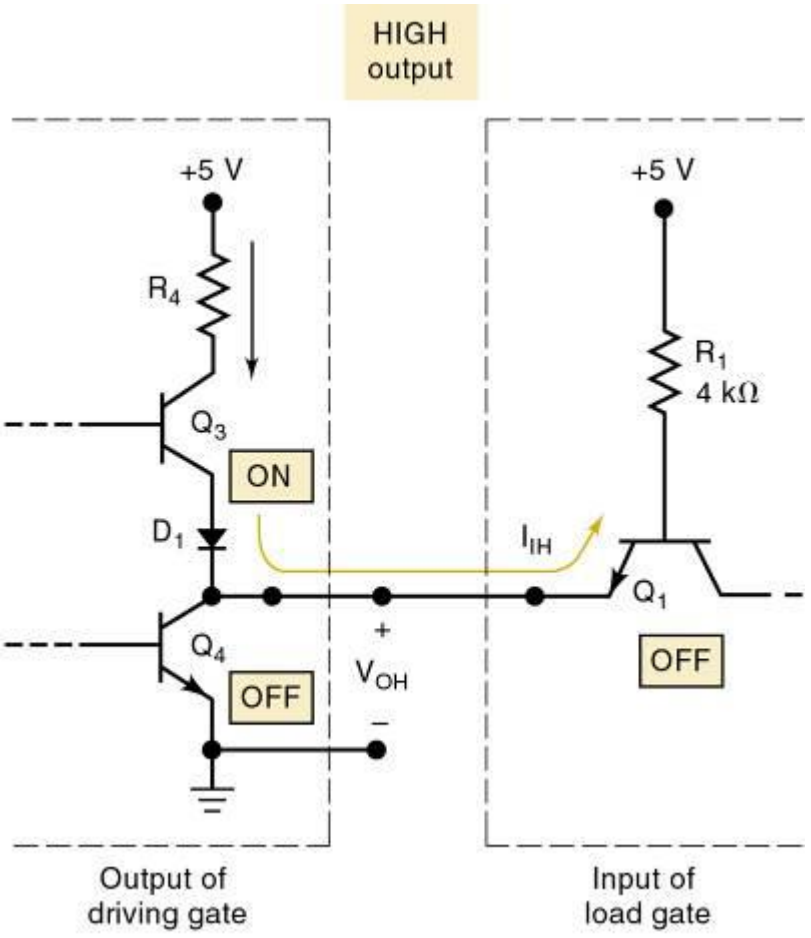
Input conditions	Output conditions
A or B or both are LOW ($\leq$ 0.8 V)	Q_4 OFF
Current flows back to ground through LOW input terminal. I_{IL} = 1.1 mA	Q_3 acts as emitter-follower and $V_{OH} \geq$ 2.4 V, typically 3.6 V

- A TTL output acts as a current source in the HIGH state—a small reverse-bias leakage current.

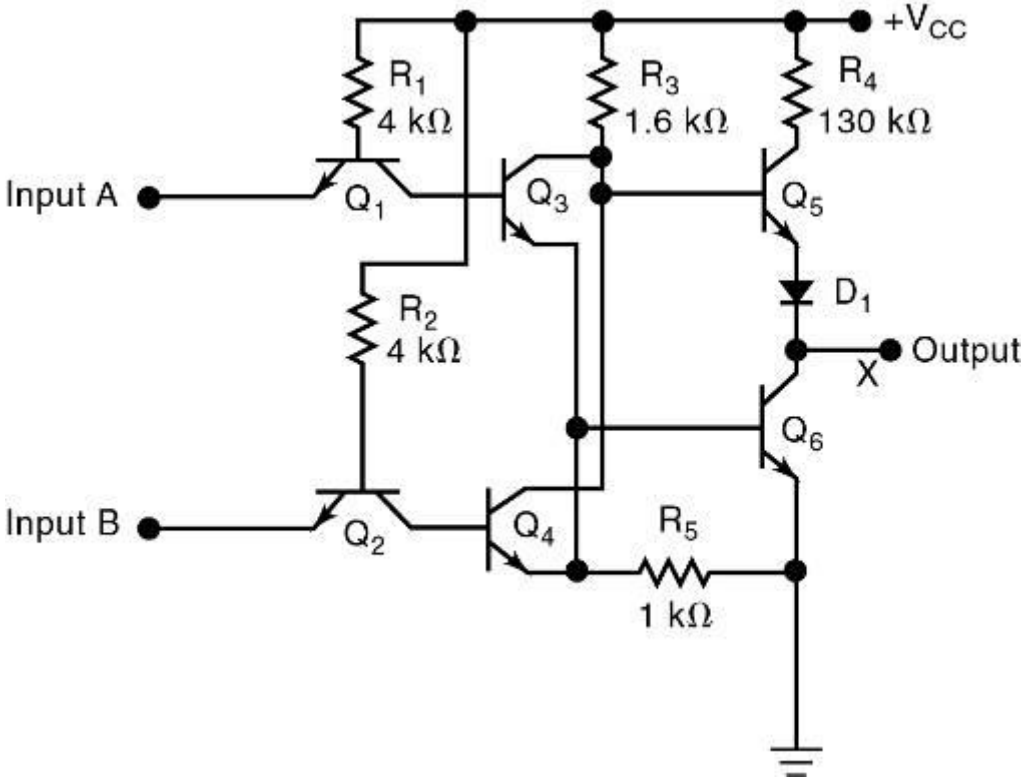
Transistor Q_3 is supplying the input current (I_{IH}) required by Q_1 of the load gate.

Q_3 is often called the **current-sourcing** or **pull-up transistor**.

In more modern TTL series, the pull-up circuit is made up of two transistors.



Internal circuit for a TTL NOR gate.



The **NOR** circuit does *not* use a multiple-emitter transistor.

Each input is applied to the emitter of a separate transistor.

The **NOR** circuit uses the same totem-pole arrangement as the **NAND** circuit on the output side

8-3 TTL Data Sheets

- The first line of TTL ICs was the 54/74 series from Texas Instruments—introduced in 1964.
- Manufacturers use the same numbering system.
  - Prefix indicates manufacturer.
    - SN – Texas Instruments.
    - DM – National Semiconductor.
    - S – Signetics.
  - DM7402, SN7402, S7402 perform the same function.
- Data sheets contain electrical characteristics, switching characteristics, and recommended operating conditions.

Data sheet for the 74ALS00 NAND gate IC

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C
§ Applies over temperature range 70°C to 125°C

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS00A		SN74ALS00A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	15	3	11	ns
t_{PHL}			2	9	2	8	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Data sheet for the 74ALS00 NAND gate IC

electrical characteristics over recommended operating free-air temperature range unless otherwise noted

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

74ALS series voltage levels.

	Minimum	Typical	Maximum
V_{OL} (V)	—	0.35	0.5
V_{OH} (V)	2.5	3.4	—
V_{IL} (V)	—	—	0.8
V_{IH} (V)	2.0	—	—

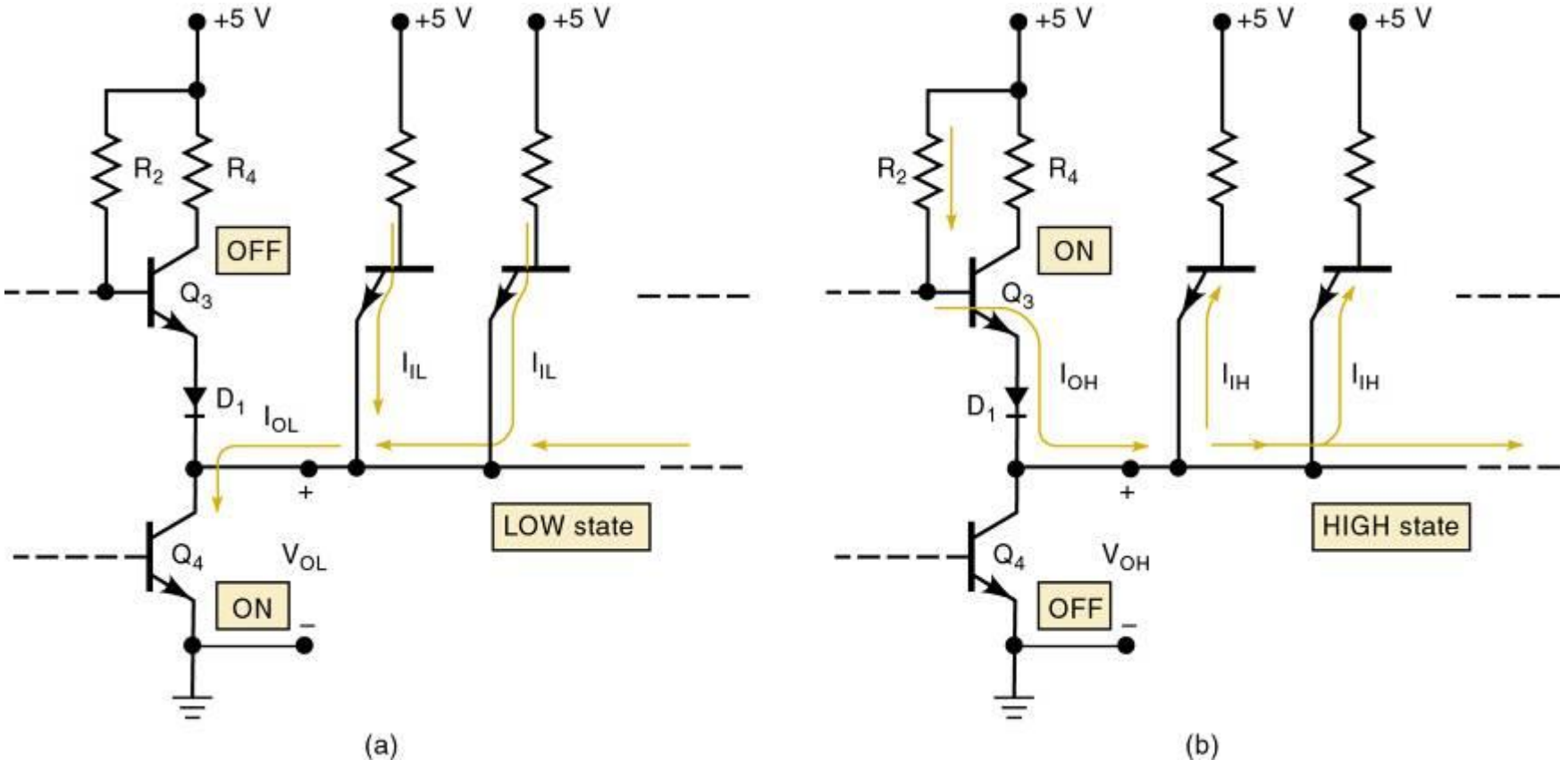
Typical TTL series characteristics.

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
V_{OH}(min) (V)	2.4	2.7	2.7	2.5	2.5	2.5
V_{OL}(max) (V)	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH}(min) (V)	2.0	2.0	2.0	2.0	2.0	2.0
V_{IL}(max) (V)	0.8	0.8	0.8	0.8	0.8	0.8

8-5 TTL Loading and Fan-Out

- Fan-out refers to the load drive capability of an IC output
  - A TTL output has a limit on how much current it can sink in the LOW state, or source in the HIGH state.
  - Exceeding these currents will result in output voltage levels outside specified ranges.
- Determining fan out
  - Add the I_{IH} for all inputs connected to an output.
    - Sum must be *less* than the output I_{OH} specification.
  - Add the I_{IL} for all inputs connected to an output.
    - Sum must be *less* than the output I_{OL} specification.

Currents when a TTL output is driving several inputs.

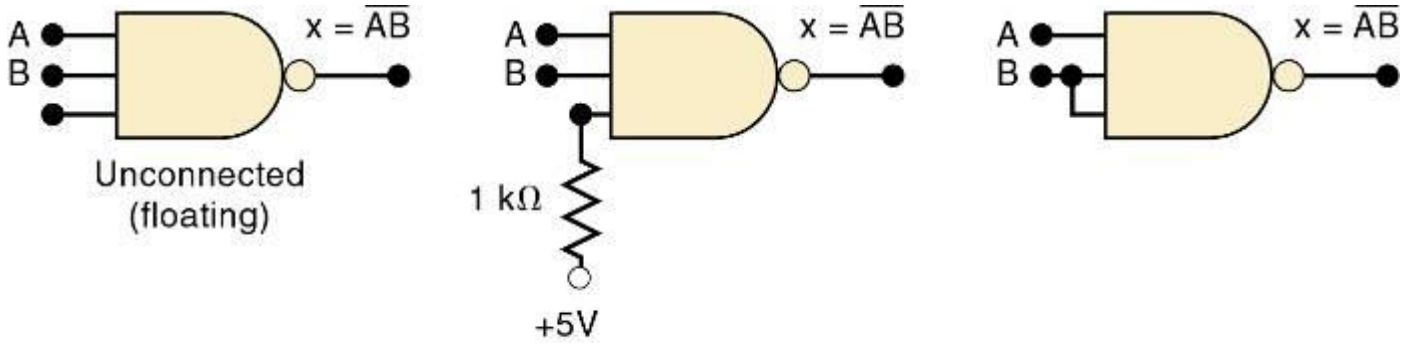


8-6 Other TTL Characteristics

- Unconnected (floating) inputs.
  - On *any* TTL IC, *all* of the inputs are 1s if they are not connected to some logic signal.
    - An input left unconnected, it is said to be **floatin**g.

8-6 Other TTL Characteristics – Unused Inputs

- Frequently, not all inputs on a TTL IC are being used in a particular application.
  - A common example is when not all the inputs to a logic gate are needed for the required logic function.
  - Unused input can be connected to +5V through a 1k-Ohm resistor, so the logic level is a 1.
  - A third possibility is where the unused input is tied to a used input.



Three ways to handle unused logic inputs.

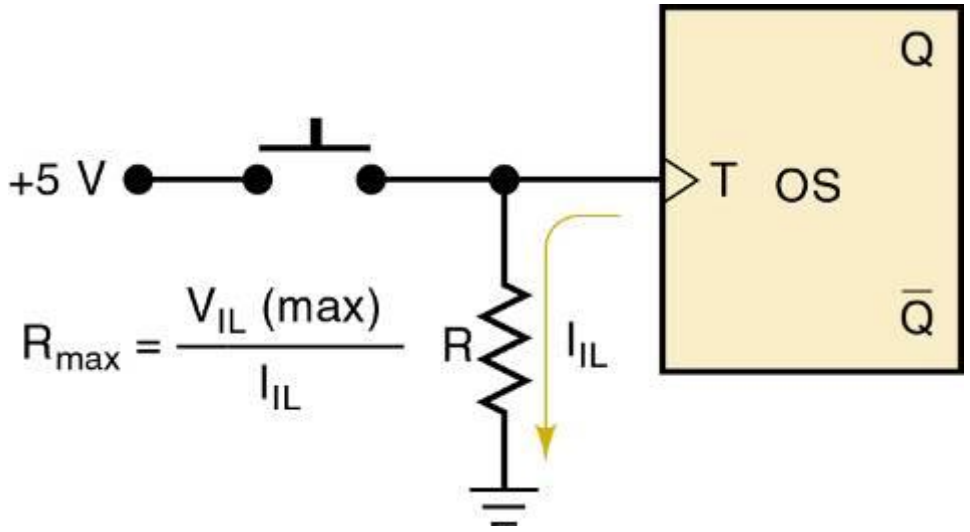
8-6 Other TTL Characteristics – Tied-Together Inputs

- Two (or more) TTL inputs on the same gate connected to form a common input will generally represent a load that is the sum of the load current rating of each individual input.
- The only exception is for **NAND** and **AND** gates.
  - The LOW-state input load will be the *same as a single input*—no matter how many inputs are tied together.

8-6 Other TTL Characteristics – Biasing TTL Inputs LOW

- Occasionally a TTL input must be held normally LOW and caused to go HIGH by actuation of a mechanical switch.
  - The one-shot triggers on a positive transition that occurs when the switch is momentarily closed.

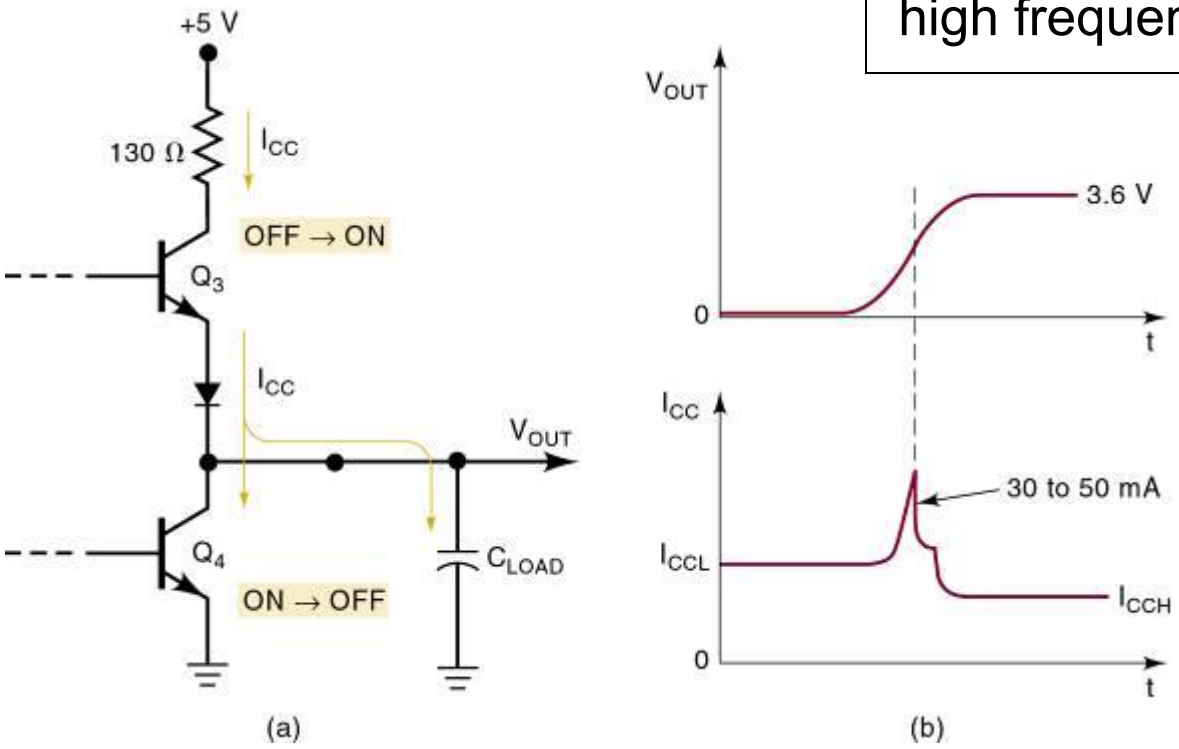
Resistor *R* keeps the *T* input LOW while the switch is open.



8-6 Other TTL Characteristics – Current Transients

- TTL logic circuits suffer from internally generated current transients or spikes due to the totem-pole output structure.

Ceramic disk capacitors (.01 or .1 μF) are used to short these high frequency spikes to ground.



8-7 MOS Technology

- MOS technology derives its name from the basic structure of a metal electrode, over an oxide insulator, over a semi-conductor substrate.
  - Transistors of MOS technology are field-effect transistors—called MOSFETs.

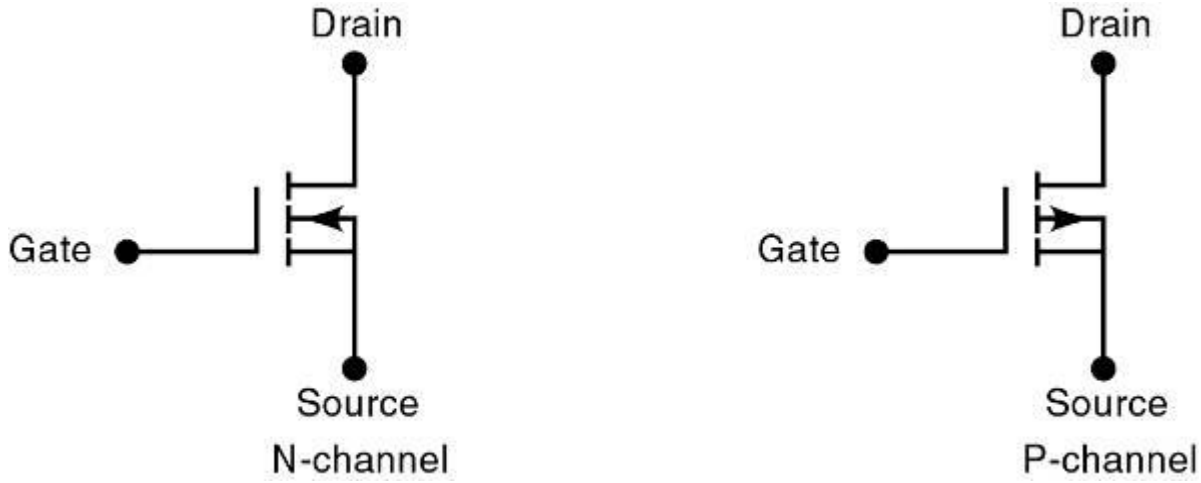
> The electric *field* on the *metal* electrode side of the *oxide* insulator has an *effect* on the resistance of the substrate.

- Most of the MOS digital ICs are constructed entirely of MOSFETs and no other components.
  - MOSFETs are relatively simple and inexpensive to fabricate, small, and consume very little power.

8-7 MOS Technology

- The principal disadvantage of MOS devices is their susceptibility to static-electricity damage.
  - Although minimized by proper handling, TTL is still more durable for laboratory experimentation.

- There are presently two general types of MOSFETs—*depletion* and *enhancement.*
  - MOS ICs use enhancement MOSFETs exclusively.



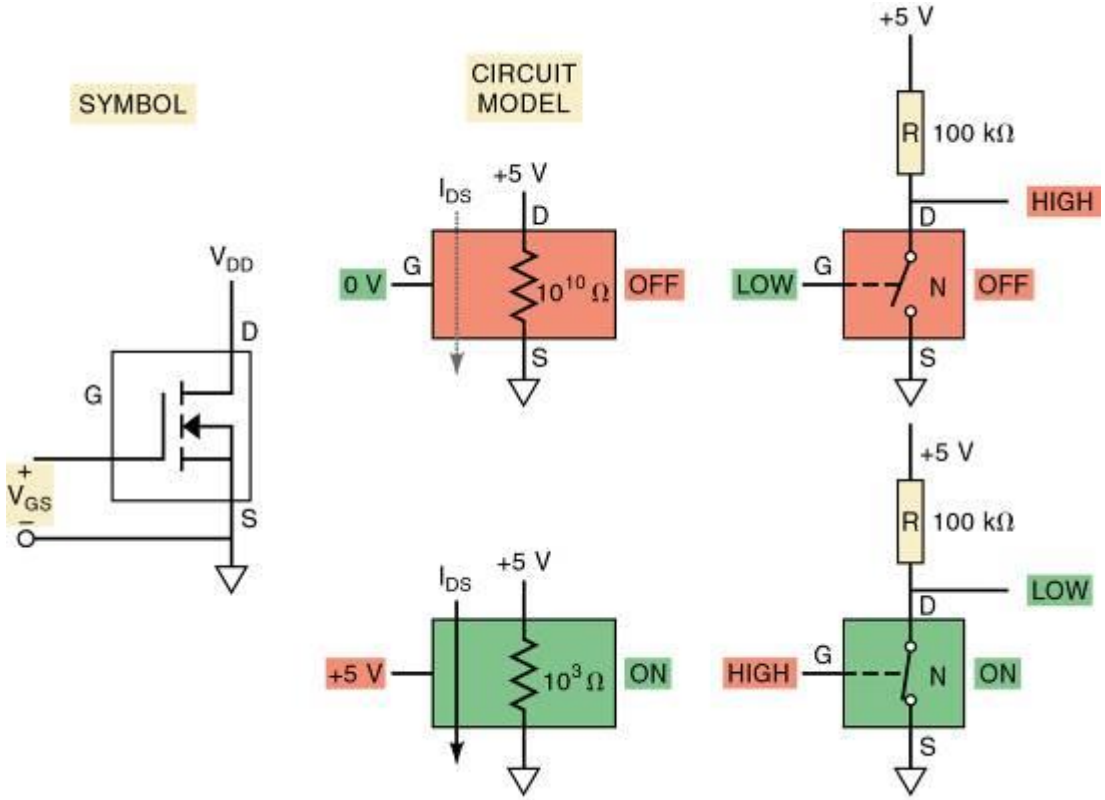
The direction of the arrow indicates either P- or N-channel. The symbols show a broken line between the *source* and the *drain* to indicate there is *normally* no conducting channel between these electrodes.

8-7 MOS Technology – Basic MOSFET Switch

- An N-channel MOSFET is the basic element in a family of devices known as **N-MOS**.
  - Drain is always biased positive relative to the source.

8-7 MOS Technology – Basic MOSFET Switch

- Gate-to-source voltage V_{GS} is the input voltage.
  - Used to control resistance between drain & source.
    - Determines whether the device is on or off.

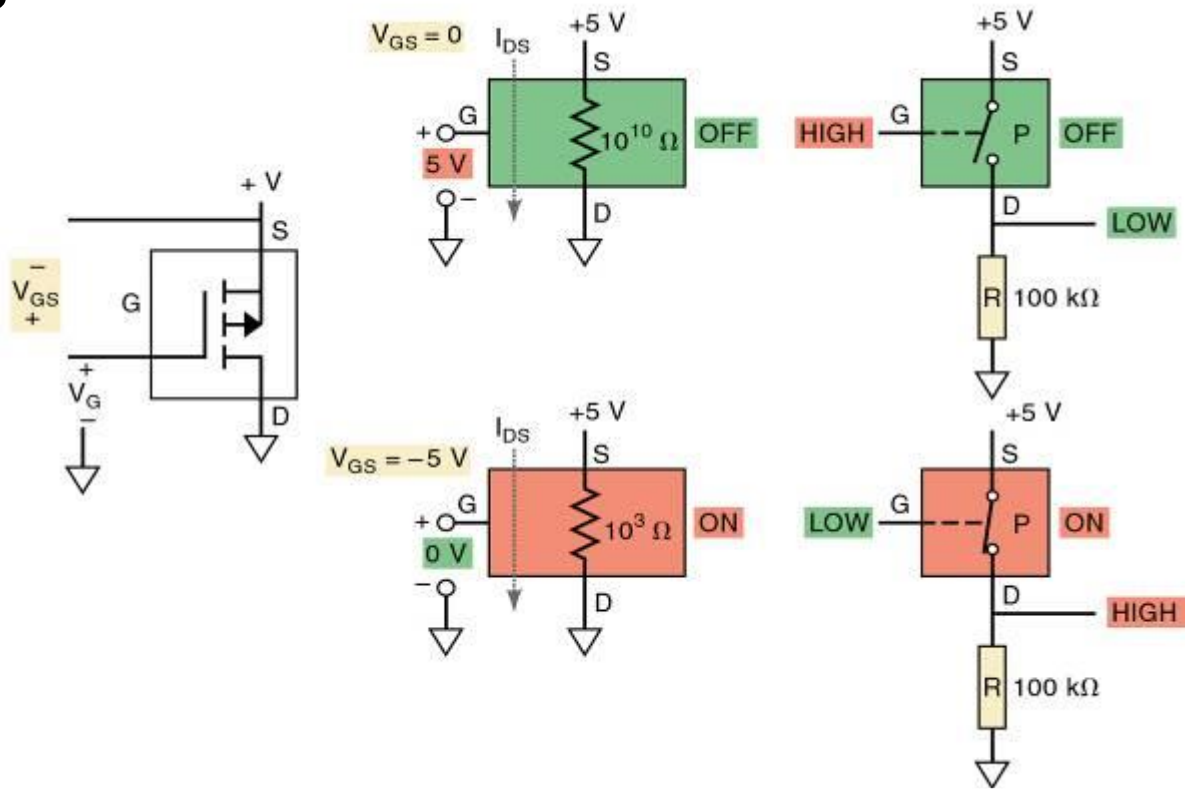


8-7 MOS Technology – Basic MOSFET Switch

- The P-channel MOSFET—**P-MOS**—operates in the same manner as the N-channel.
  - Except that it uses voltages of opposite polarity.
- The drain is connected to the lower side of the circuit so it is biased with a more negative voltage relative to the source.

8-7 MOS Technology – Basic MOSFET Switch

- To turn the P-MOSFET ON, a voltage *lower* than the source by V_T must be applied to the gate.
  - Voltage at the gate, relative to the source, must be negative.

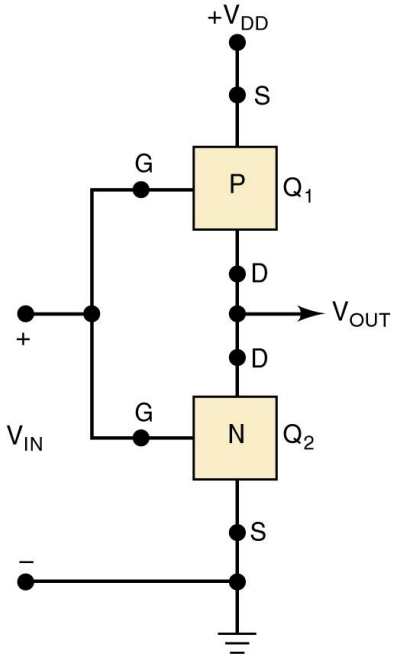


8-8 Complementary MOS Logic – CMOS Inverter

- P-MOS & N-MOS circuits began to dominate the LSI and VLSI markets in the 1970s and 1980s.
  - Use fewer components & are much simpler to manufacture than TTL circuits.
- During this era, technology emerged that used P-MOS & N-MOS transistors in the same circuit.
  - Complementary MOS, or **CMOS**, technology.

8-8 Complementary MOS Logic – CMOS Inverter

- The CMOS INVERTER has two MOSFETs in series.
  - The P-channel device source is connected to V_{DD} .
  - The N-channel device has its source connected to ground—usually labeled V_{SS}.



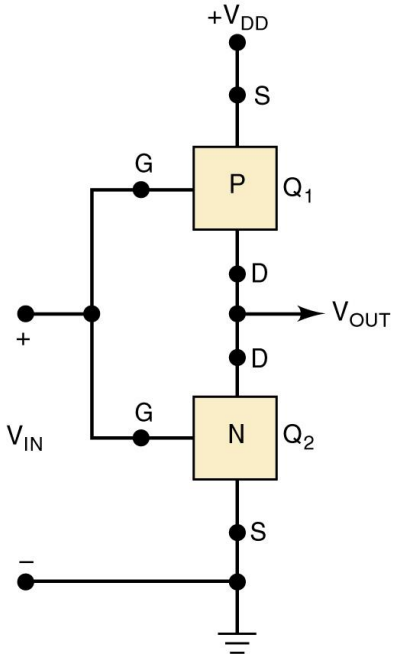
V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10}\ \Omega$	ON $R_{ON} = 1\ k\Omega$	$\simeq 0$ V
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	$\simeq +V_{DD}$

$V_{OUT} = \overline{V_{IN}}$

Basic CMOS INVERTER.

8-8 Complementary MOS Logic – CMOS Inverter

- The CMOS INVERTER has two MOSFETs in series.
  - Gates of the two devices are connected together as a common input.
  - Drains are connected together as common output.

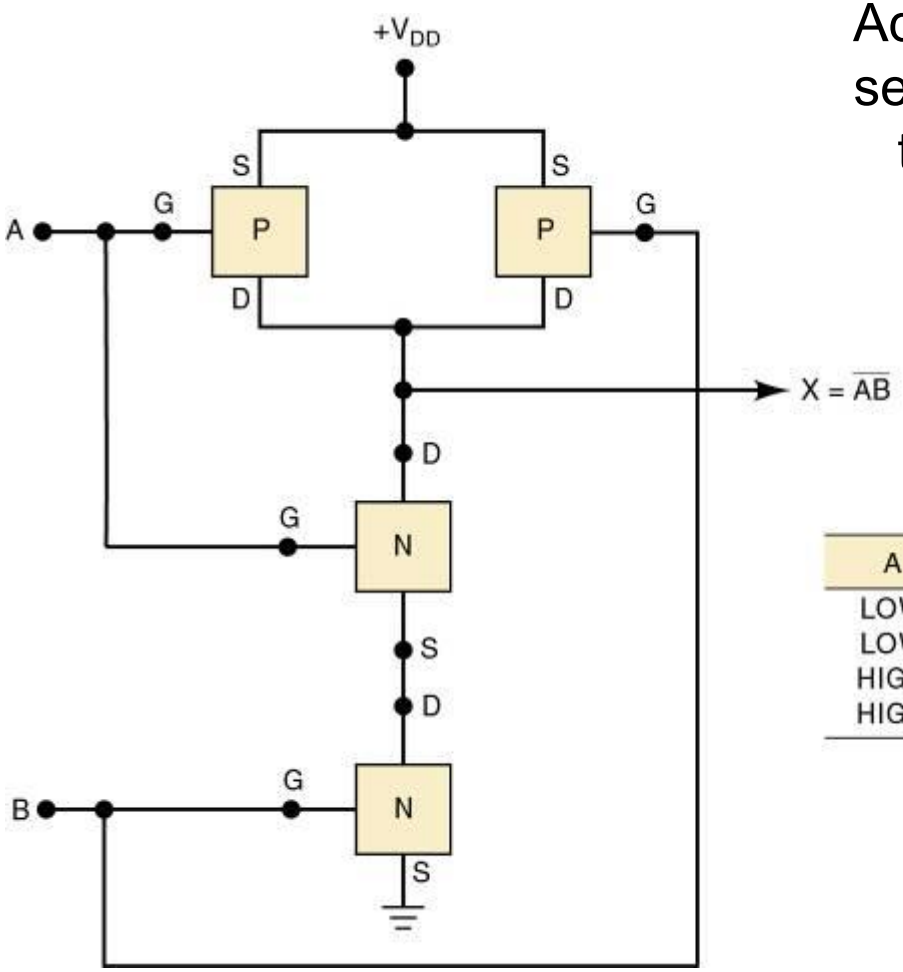


V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10}\ \Omega$	ON $R_{ON} = 1\ k\Omega$	$\simeq 0$ V
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	$\simeq +V_{DD}$

$V_{OUT} = \overline{V_{IN}}$

Basic CMOS INVERTER.

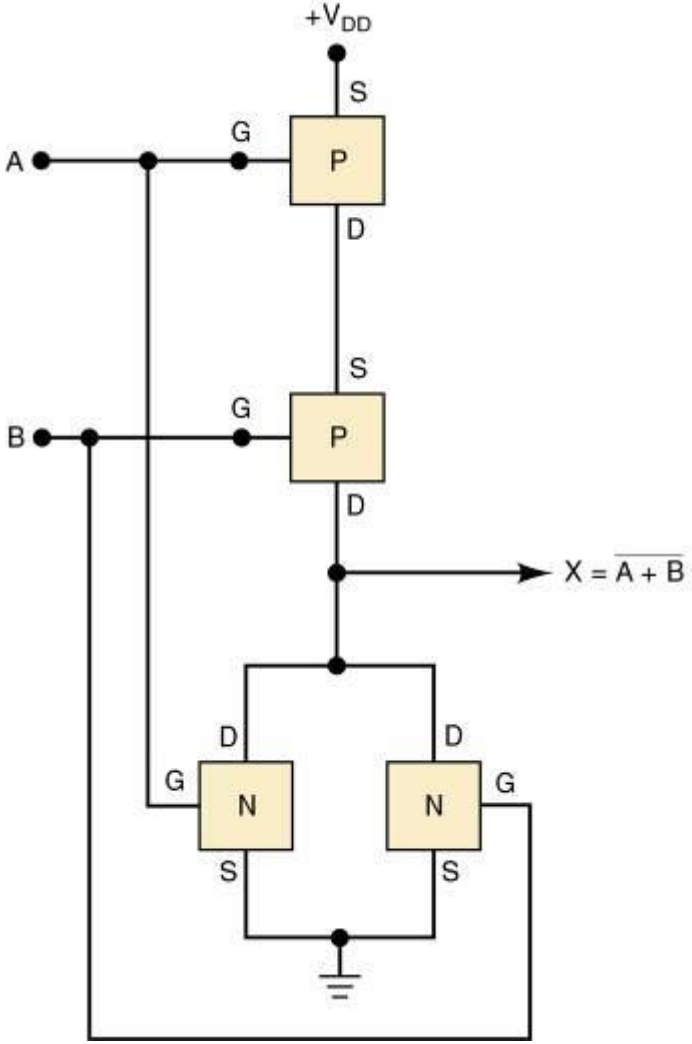
- A **NAND** gate is formed by modifying the basic INVERTER.



Adding parallel P-channel & series N-channel MOSFETs to the basic INVERTER.

A	B	X
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

- A CMOS **NOR** gate.



Formed by adding a series P-MOS and a parallel N-MOS to the basic INVERTER.

A	B	X
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

8-8 Complementary MOS Logic

- Two CMOS **NOR** gates or **NAND** gates can be cross-coupled to form a simple SET-RESET latch
  - Additional gating circuitry is used to convert the basic SET-RESET latch to clocked D and J-K flip-flops.

8-9 CMOS Series Characteristics - Terms

- CMOS ICs provide all TTL logic functions, and special-purpose functions not provided by TTL.
- Terms used when ICs from different families or series are to be used together or as replacements.
  - **Pin-compatible**—two ICs are pin-compatible when their pin configurations are the same.
  - **Functionally equivalent**—ICs are functionally equivalent when the logic functions they perform are exactly the same.
  - **Electrically compatible**—ICs are electrically compatible when they can be connected directly to each other without special measures to ensure proper operation.

8-9 CMOS Series Characteristics – IC Series

- The oldest CMOS series is the 4000 series by RCA—functionally equivalent to Motorola 14000.
  - Rarely used in new designs except when a special-purpose IC is not available in other series.
- The 74HC/HCT series has a 10-fold increase in switching speed, comparable to 74LS devices.
  - Pin-compatible with, functionally equivalent to TTL ICs with the same device number.
- The 74AC/ACT series is often referred to as ACL for advanced CMOS logic.
  - Functionally equivalent various TTL series, but *not* pin-compatible with TTL.

8-9 CMOS Series Characteristics – IC Series

- Series 74AHC/AHCT offers a natural migration path from the HC series to faster, lower-power, low-drive applications.
  - Three times faster, with similar noise immunity to HC without the over- under-shoot problems.
- BiCMOS combines the best of bipolar & CMOS
  - Characteristics are integrated to produce an extremely low-power, high-speed logic family.
    - Limited to functions used in microprocessor and bus interfacing applications.

8-9 CMOS Series Characteristics – Power

- When devices using different supply voltages are interconnected, special measures must be taken.
  - The 4000/14000 series and 74C series devices operate with V_{DD} values ranging from 3 to 15 V.
  - 74 series ICs operate over a much narrower range of supply voltages—typically between 2 and 6 V.
  - Lower-voltage series (2.5 or 3.3 V) are available.

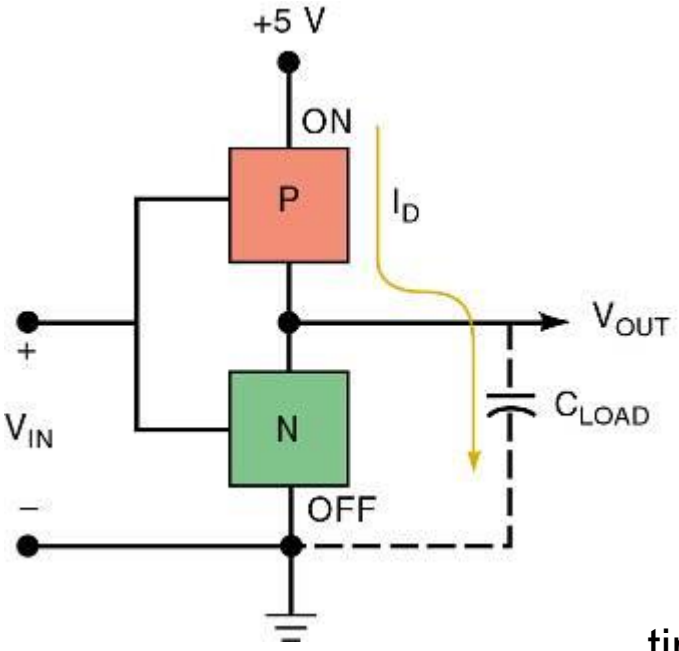
	CMOS							TTL			
Parameter	4000B	74HC	74HCT	74AC	74ACT	74AHC	74AHCT	74	74LS	74AS	74ALS
V_{IH}(min)	3.5	3.5	2.0	3.5	2.0	3.85	2.0	2.0	2.0	2.0	2.0
V_{IL}(max)	1.5	1.0	0.8	1.5	0.8	1.65	0.8	0.8	0.8	0.8	0.8
V_{OH}(min)	4.95	4.9	4.9	4.9	4.9	4.4	3.15	2.4	2.7	2.7	2.5
V_{OL}(max)	0.05	0.1	0.1	0.1	0.1	0.44	0.1	0.4	0.5	0.5	0.5
V_{NH}	1.45	1.4	2.9	1.4	2.9	0.55	1.15	0.4	0.7	0.7	0.7
V_{NL}	1.45	0.9	0.7	1.4	0.7	1.21	0.7	0.4	0.3	0.3	0.4

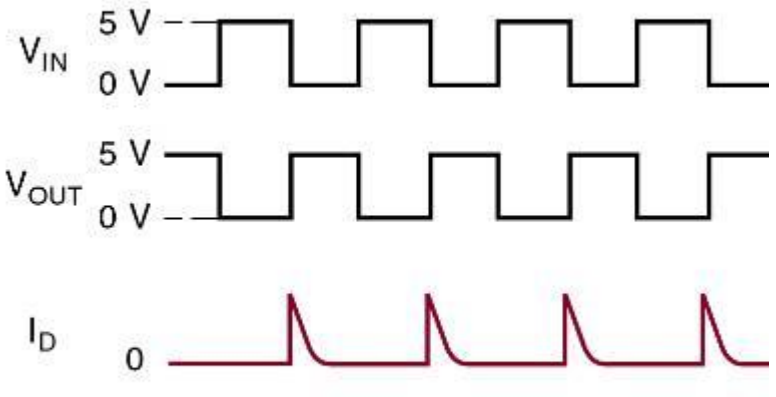
8-9 CMOS Series Characteristics – Power

- In general, CMOS devices have greater noise margins than TTL.
- When a CMOS logic circuit is in a static state—not changing—its power dissipation is extremely low.
  - Ideally suited for applications using battery power.
- Power dissipation of a CMOS IC will be very low as long as it is in a dc condition.
  - P_D will increase in proportion to the frequency at which the circuits are switching states.

8-9 CMOS Series Characteristics – Power Dissipation

- Each time a CMOS output switches from LOW to HIGH, a transient charging current must be supplied to the load capacitance.
  - The combined input capacitances of any loads being driven and the device's own output capacitance.





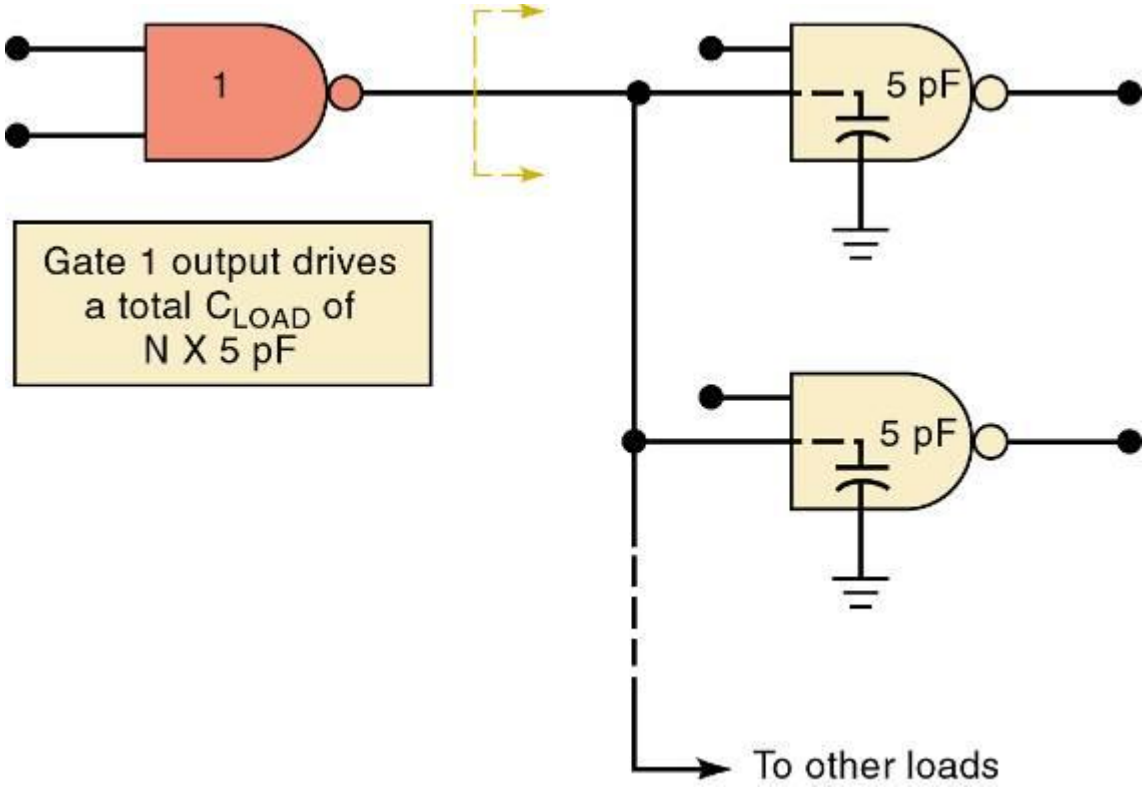
Current spikes are drawn from V_{DD} each time the output switches from LOW to HIGH.

8-9 CMOS Series Characteristics – Fan-Out

- CMOS inputs have an extremely large resistance that draws essentially no current from the source.
  - 10^{12} Ohms.

Each CMOS input, typically presents a 5-pF load to ground.

This input capacitance limits the number of CMOS inputs that one CMOS output can drive.



8-9 CMOS Series Characteristics – Switching Speed

- Although CMOS must drive relatively large load capacitances, switching speed is somewhat faster.
  - Due to low output resistance in each state.
- In the CMOS circuit, output resistance in the HIGH state is the R_{ON} of the P-MOSFET.
  - Typically 1-k Ohms or less.

8-9 CMOS Series Characteristics – Static Sensitivity

- All electronic devices, to varying degrees, are sensitive to damage by static electricity.
  - MOS logic families are especially susceptible.

8-9 CMOS Series Characteristics – Static Sensitivity

- Precautions against **Electrostatic discharge**:
  - Connect the chassis of all test instruments, soldering-iron tips, and your metal workbench to earth ground.
  - Connect yourself to ground with a special wrist strap.
  - Keep ICs in conductive foam or aluminum foil.
    - So no dangerous voltages develop between any pins.
  - Avoid touching IC pins—insert the IC into the circuit immediately after removing from the protective carrier.
  - Place shorting straps across the edge connectors of PC boards when the boards are carried/transported.
    - Avoid touching the edge connectors.
  - Do not leave any unused IC inputs unconnected.
    - Open inputs tend to pick up stray static charges.

8-9 CMOS Series Characteristics – Switching Speed

- Unavoidable existence of *parasitic* (unwanted) PNP and NPN transistors embedded in CMOS substrate can cause a condition called **latch-up**.
  - If triggered, they will latch-up (stay ON permanently), and a large current will destroy the IC.
- Most modern CMOS ICs are designed with protection circuitry that helps prevent latch-up
  - It can still occur when the device's maximum voltage ratings are exceeded.
  - Latch-up can be triggered by high-voltage spikes or ringing at the device inputs and outputs.

8-10 Low Voltage Technology

- Increased chip density has major benefits:
  - It allows more circuits to be packed onto the chip;
    - With the circuits closer together, the time for signals to propagate from one circuit to another will decrease.
- There are also drawbacks to higher chip density
  - When circuits are closer together, insulating material that isolates one circuit from another is narrower.
    - Decreases the amount of voltage that the device can withstand before dielectric breakdown occurs.
  - Chip power dissipation increases, which can raise chip temperature above maximum for reliable operation.
    - These drawbacks can be neutralized by operating the chip at lower volt-age levels,

8-10 Low Voltage Technology – CMOS

- Several low-voltage series are currently available:
  - *74LVC (Low-Voltage CMOS)* series contains the widest assortment of the familiar SSI gates and MSI functions of the 5-V families.
  - *74ALVC (Advanced Low-Voltage CMOS)* offers the highest performance.
  - *74LV (Low-Voltage)* series offers CMOS technology and many SSI gates/MSI logic functions, along with some popular octal buffers, latches, and flip-flops.
  - *74AVC (Advanced Very-Low-Voltage CMOS)* series is optimized for 2.5-V systems.
    - It has many of the bus interface features of the BiCMOS series that will make it useful in future generations.

8-10 Low Voltage Technology – CMOS

- Several low-voltage series are currently available:
  - *74AUC (Advanced Ultra-Low-Voltage CMOS)* series is optimized to operate at 1.8-V logic levels.
  - *74AUP* (Advanced Ultra-low Power) is the lowest-power logic series—used in battery-operated portable applications.
  - *74CBT (Cross Bar Technology)* series offers high-speed bus-interface circuits that can switch quickly.
    - *74CBTLV (Cross Bar Technology Low Voltage)* is the 3.3-V complement to the 74CBT series.
  - *74GTLP* (Gunning Transceiver Logic Plus) series is made for high-speed parallel backplane applications.

8-10 Low Voltage Technology – CMOS

- Several low-voltage series are currently available:
  - *74SSTV (Stub Series Terminated Logic)* is useful in high-speed advanced-memory systems.
  - *TS Switch* (TI Signal Switch) series is made for mixed-signal applications and offers some analog/digital switching & multiplexing solutions.
  - *74TVC (Translation Voltage Clamp)* series is used to protect the inputs and outputs of sensitive devices from voltage overshoot on the bus lines.

8-10 Low Voltage Technology – BiCMOS

- BiCMOS family:
  - The *74LVT (Low-Voltage BiCMOS Technology)* contains BiCMOS parts intended for 8- and 16-bit bus-interface applications.

	LV	ALVC	AVC	ALVT	ALB
V_{CC} (recommended)	2.7–3.6	2.3–3.6	1.65–3.6	2.3–2.7	3–3.6
t_{pd} (ns)	18	3	1.9	3.5	2
V_{IH} (V)	2 to V_{CC} + 0.5	2.0 to 4.6	1.2 to 4.6	2 to 7	2.2 to 4.6
V_{IL} (V)	0.8	0.8	0.7	0.8	0.6
I_{OH} (mA)	6	12	8	32	25
I_{OL} (mA)	6	12	8	32	25

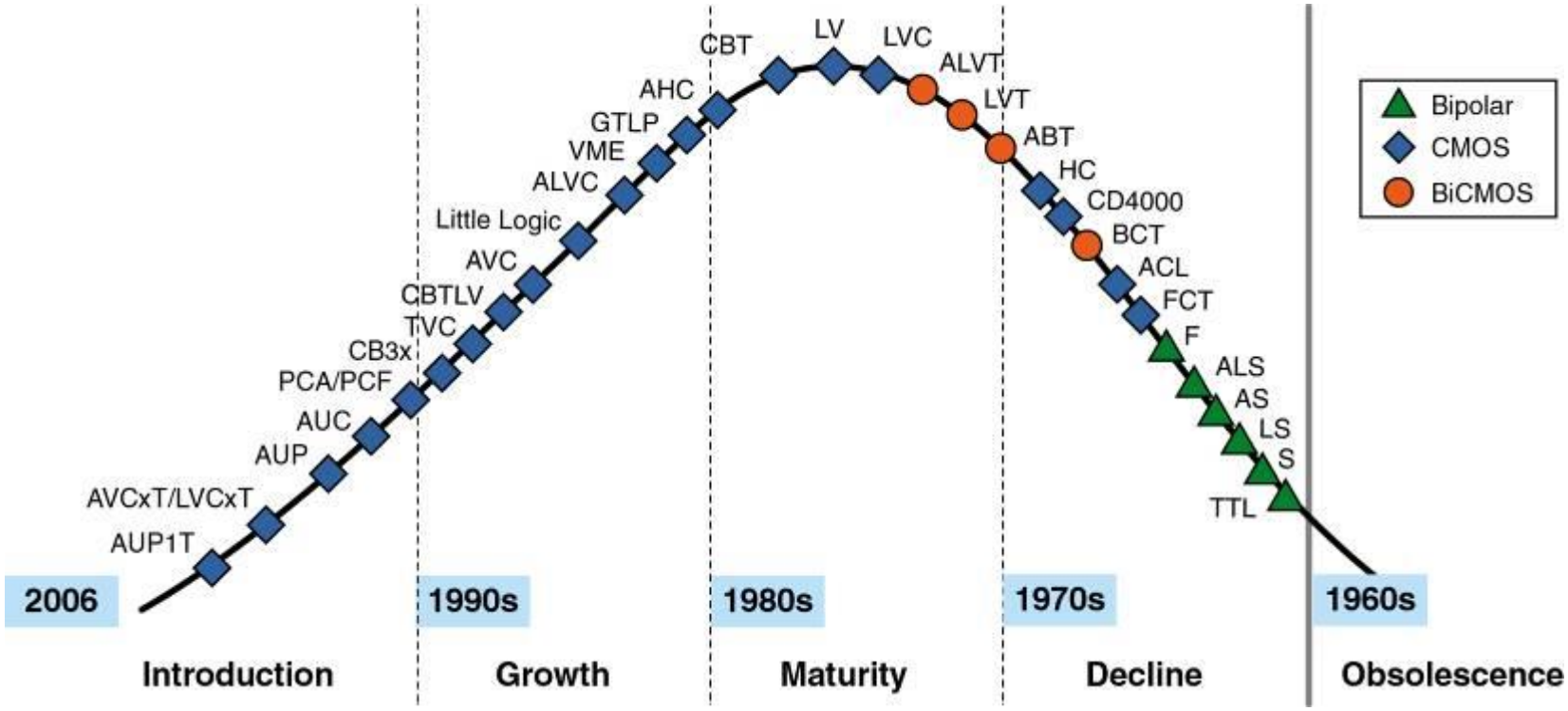
Because output levels [V_{OH} (min) and V_{OL} (max)] are equivalent to TTL levels, they are fully electrically compatible with TTL.

8-10 Low Voltage Technology

- BiCMOS family:
  - *74ALVT (Advanced Low-Voltage BiCMOS Technology)* series is an improvement over the LVT.
    - It offers 3.3-V or 2.5-V operation at 3 ns, pin-compatible with ABT and LVT, also intended for bus-interface uses.
  - *74ALB (Advanced Low-Voltage BiCMOS)* series is designed for 3.3-V bus-interface applications.
    - 25 mA output drive & propagation delays of only 2.2 ns.
  - *74VME (VERSA Module Eurocard*) series is designed to operate with the standard VME bus technology.

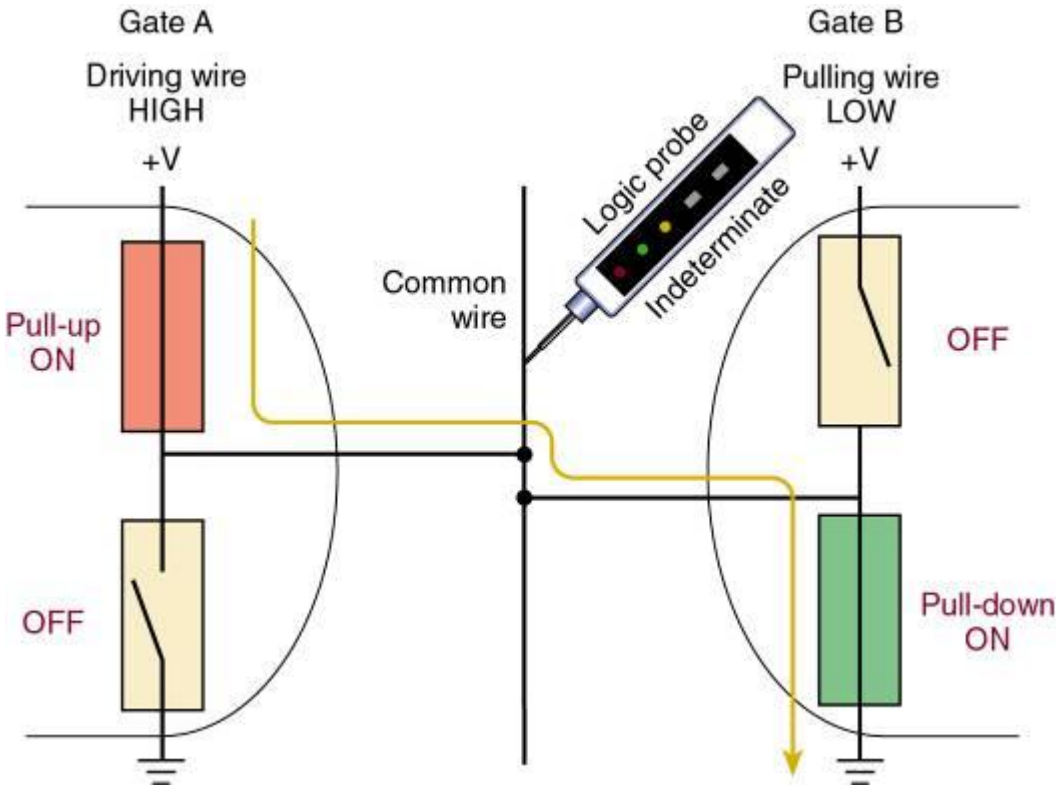
8-10 Low Voltage Technology

- Continued development of low-voltage technology promises a complete revolution from the original 5-V system, to pure 3.3-V, 2.5-V, or even lower-voltage digital systems.



8-11 Open Collector/Open Drain Outputs

Conventional CMOS or TTL totem pole outputs should *never* be connected to the same point.



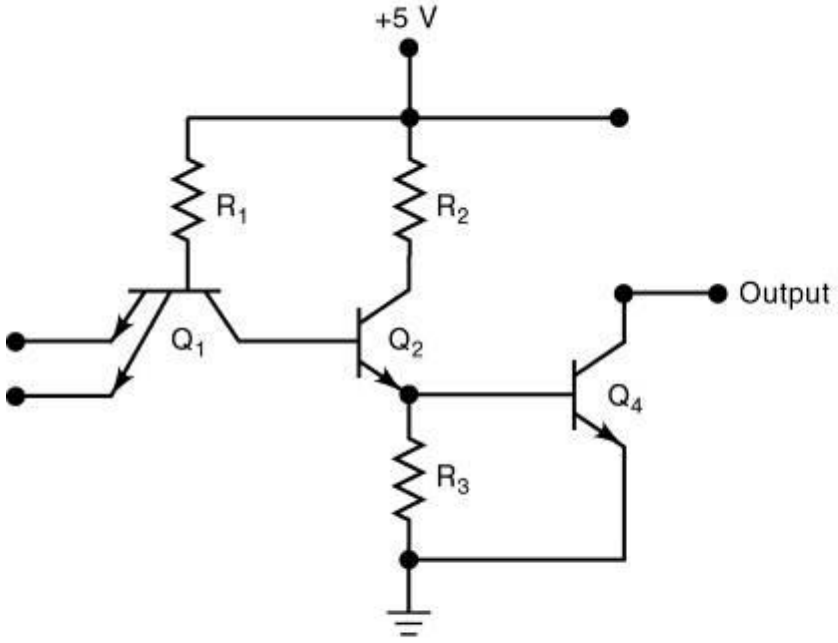
Two outputs contending for control of a wire.

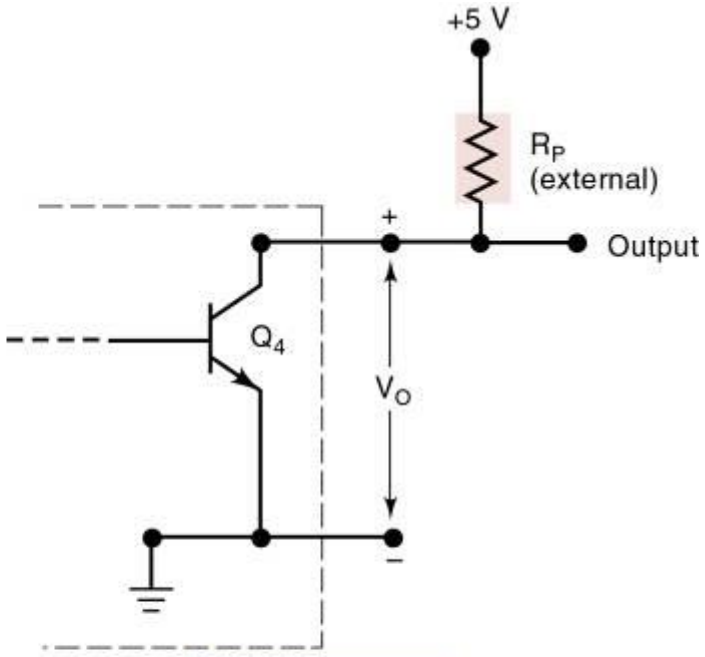
8-11 Open Collector/Open Drain Outputs

- One solution to the problem of sharing a common wire among gates is to remove the active pull-up transistor from each gate's output circuit.
  - In this way, none of the gates will ever try to assert a logic HIGH.

8-11 Open Collector/Open Drain Outputs

TTL outputs modified this way are called *open-collector* outputs.





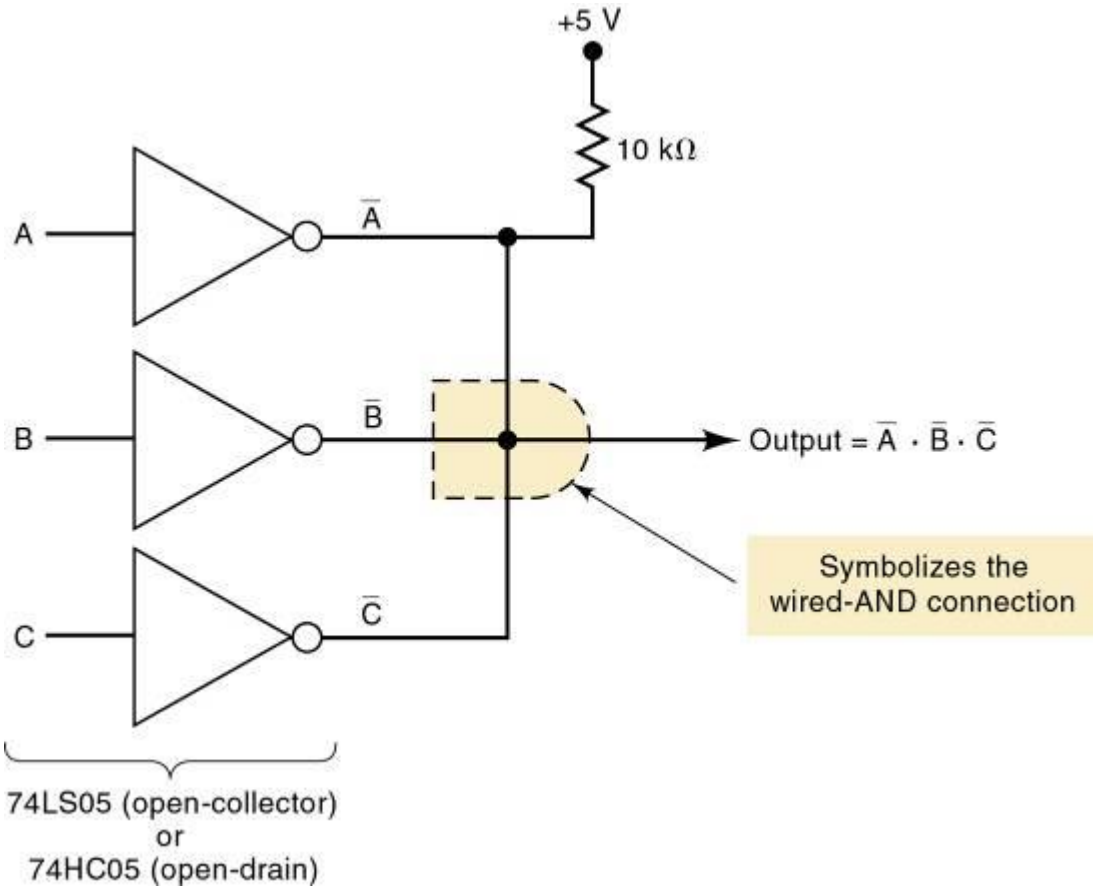
Operating states

Q_4 ON $\rightarrow V_O = V_{OL} \leq 0.4$ V
Q_4 OFF $\rightarrow V_O = V_{OH} = +5$ V

CMOS outputs modified this way are called *open-drain* outputs.

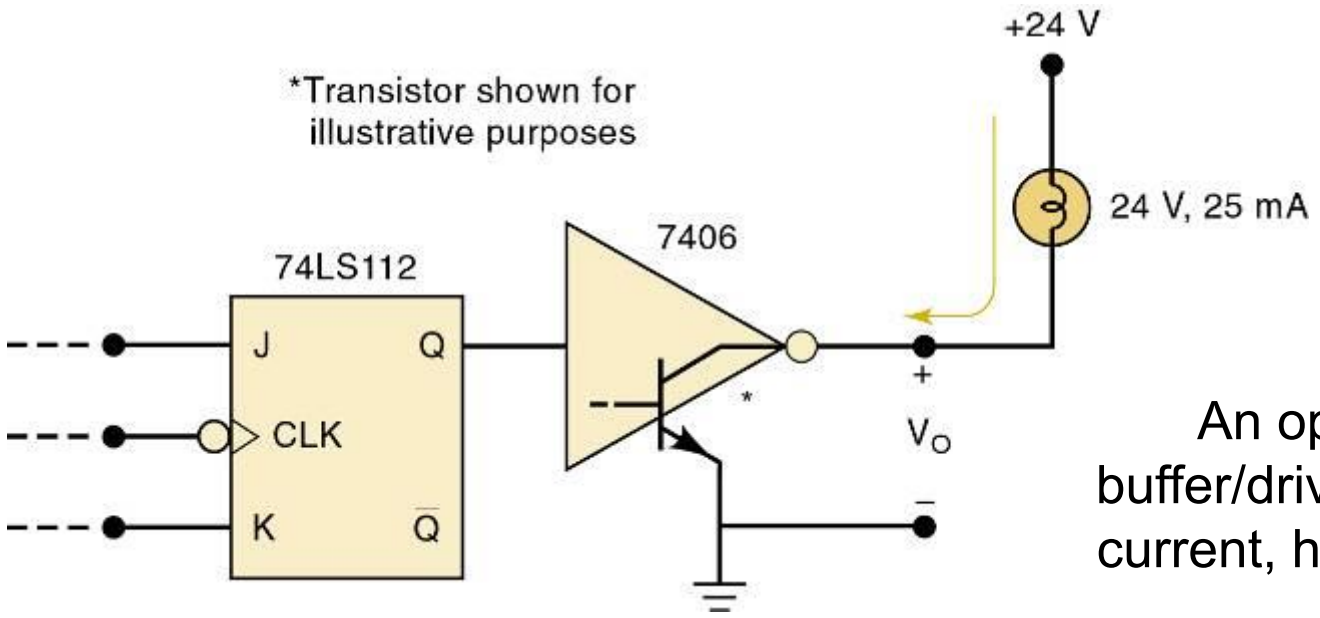
8-11 Open Collector/Open Drain Outputs

Wired-AND operation using open-collector gates.



8-11 Open Collector/Open Drain Outputs

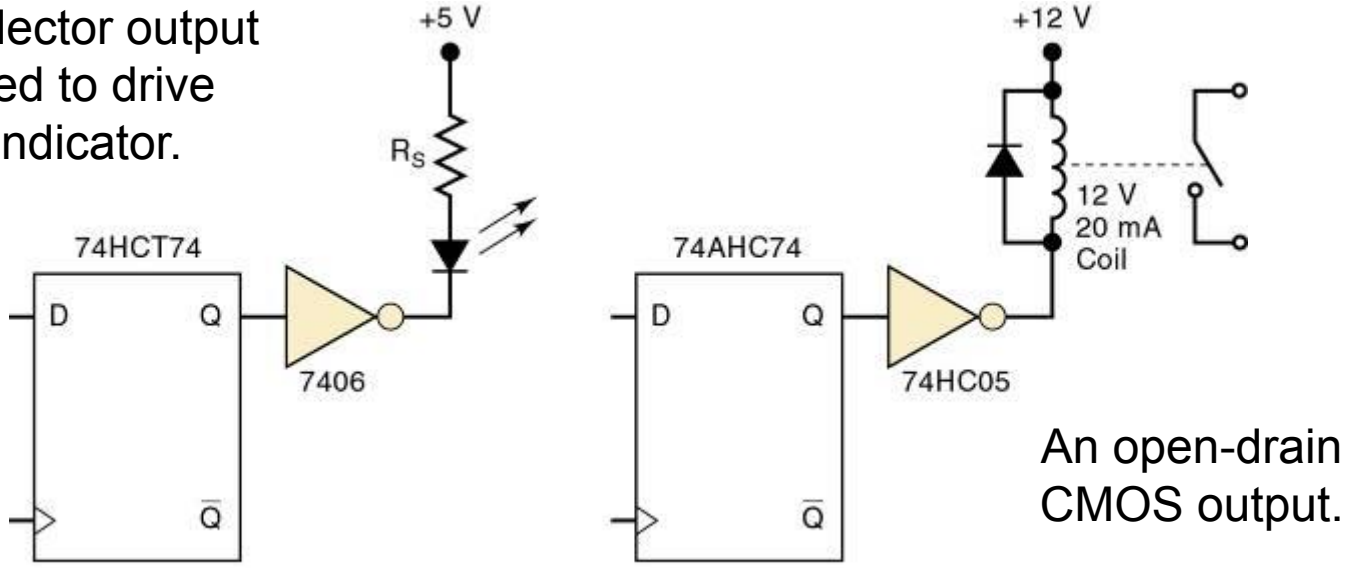
- A common use of open-collector/drain outputs is as a **buffer/driver**.
  - Logic circuit designed to have a greater output current and/or voltage capability than an ordinary logic circuit.
    - They allow a weaker output circuit to drive a heavy load.



An open-collector buffer/driver drives a high-current, high-voltage load.

Open-collector outputs are often used to drive indicator LEDs.

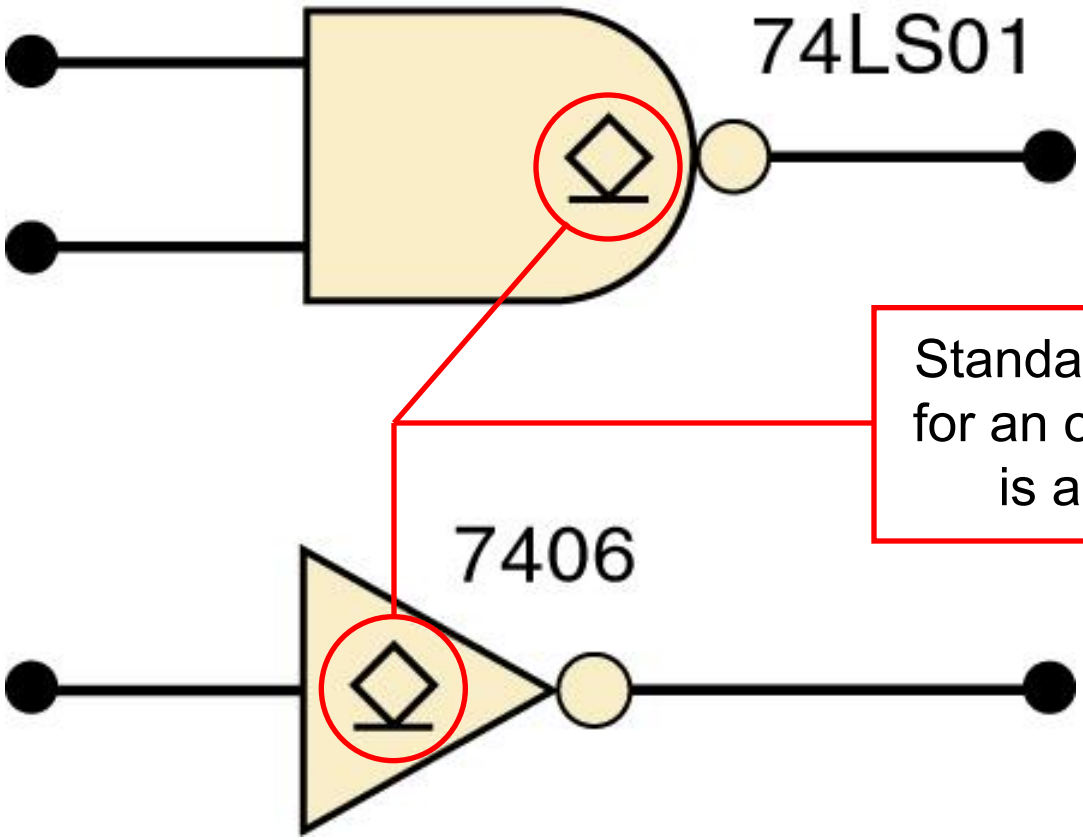
An open-collector output can be used to drive an LED indicator.



An open-drain CMOS output.

8-11 Open Collector/Open Drain Outputs

IEEE/ANSI symbology uses a distinctive notation to identify open-collector/drain outputs.



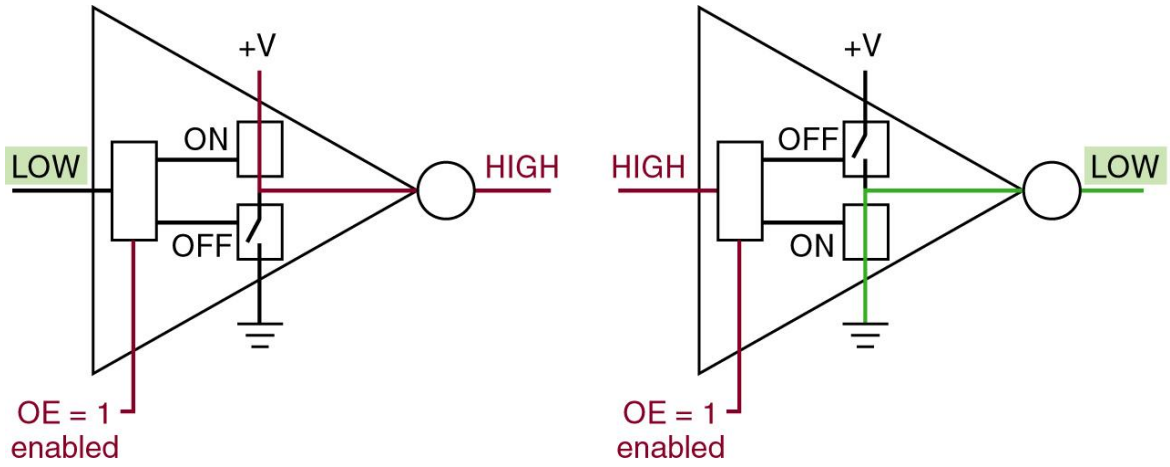
Standard IEEE/ANSI designation for an open-collector/drain output is an underlined diamond.

8-12 Tristate (Three-State) Logic Outputs

- The **tristate** configuration takes advantage of the high-speed operation of the pull-up/ pull-down output arrangement.
  - While allowing outputs to be connected together to share a common wire.
- Called tristate because it allows three possible output states:
  - HIGH, LOW, and high-impedance (Hi-Z).
- Hi-*Z* is a condition in which both pull-up & pull-down transistors are turned OFF.
  - The output terminal is a high impedance to both ground and the power supply.

8-12 Tristate (Three-State) Logic Outputs

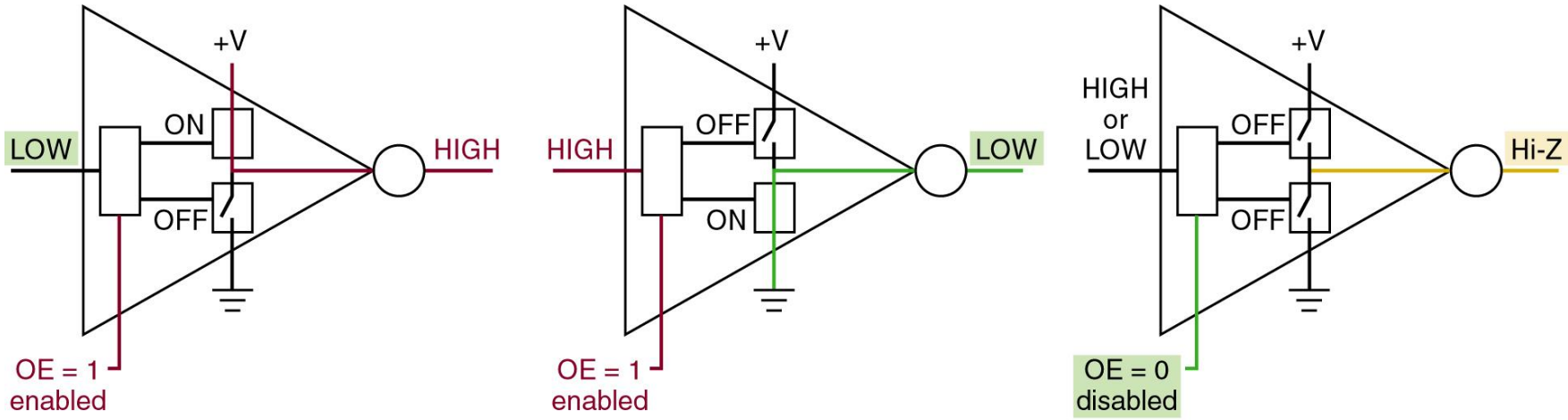
- Devices with tristate outputs have an *enable* input.
  - Often labeled *E* for enable or *OE* for output enable.



- When *OE* = 1, the circuit operates as a normal INVERTER because the HIGH logic level at *OE* enables the output.
  - Output will be either HIGH or LOW, depending on the input level.

8-12 Tristate (Three-State) Logic Outputs

- Devices with tristate outputs have an *enable* input.
  - Often labeled *E* for enable or *OE* for output enable.



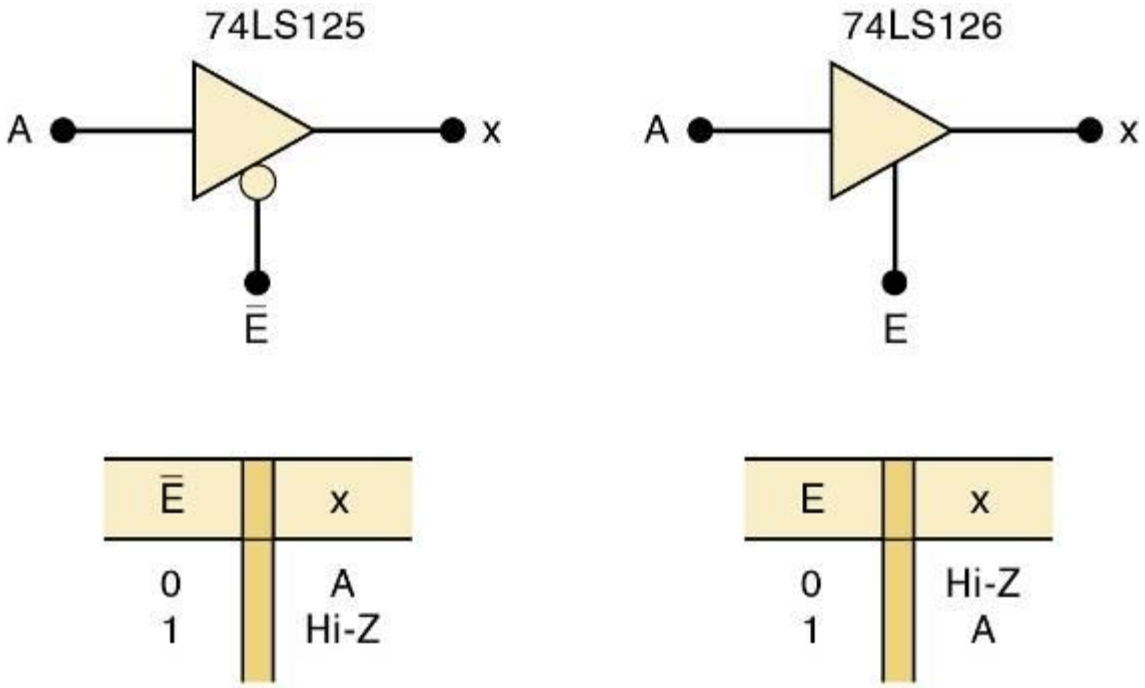
- When *OE* = 0, output is *disabled.* It goes into Hi-*Z* state with both transistors in nonconducting state.
  - In this state, the output terminal is essentially an open circuit (not connected to anything).

8-12 Tristate (Three-State) Logic Outputs

- Outputs of tristate ICs can be connected together without sacrificing switching speed.
  - When tristate outputs are connected together, only one of them should be enabled at one time.
    - Two active outputs could fight for control of the common wire.
- Many ICs are designed with tristate outputs.
  - 74LS374 is an octal D-type FF register IC with tristate outputs.

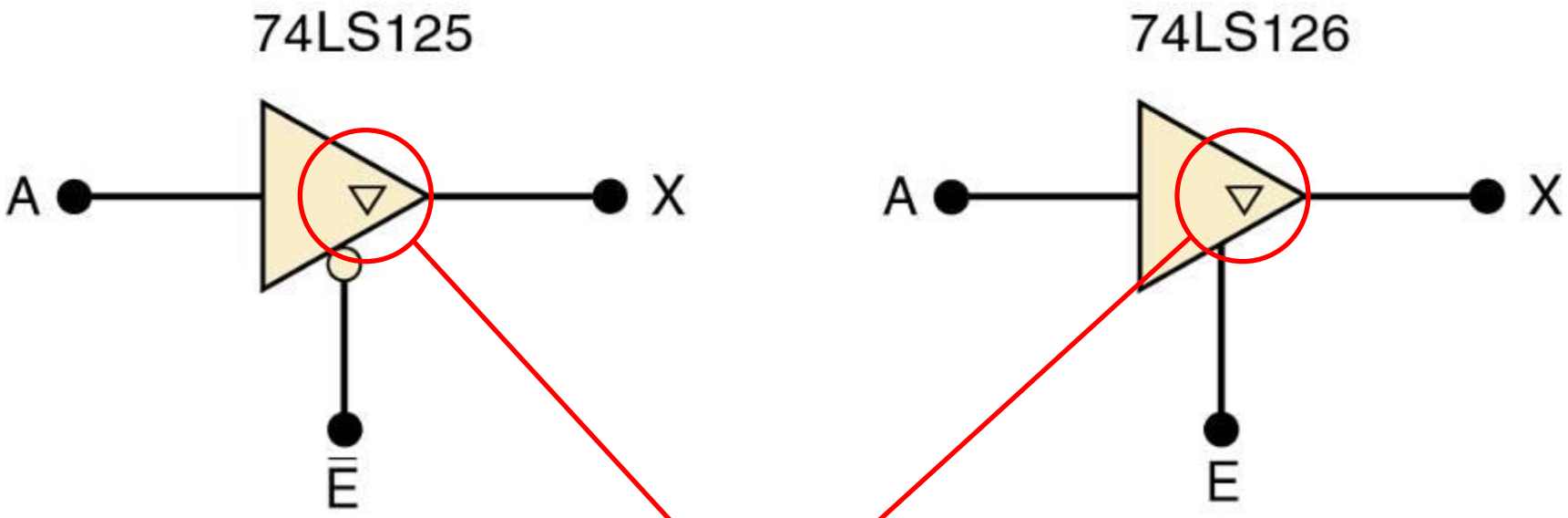
8-12 Tristate (Three-State) Logic Outputs

- A *tristate buffer* is a circuit used to control the passage of a logic signal from input to output
  - Some tristate buffers invert the signal as passes.



Tristate noninverting buffers.

IEEE/ANSI symbology to identify tristate outputs.

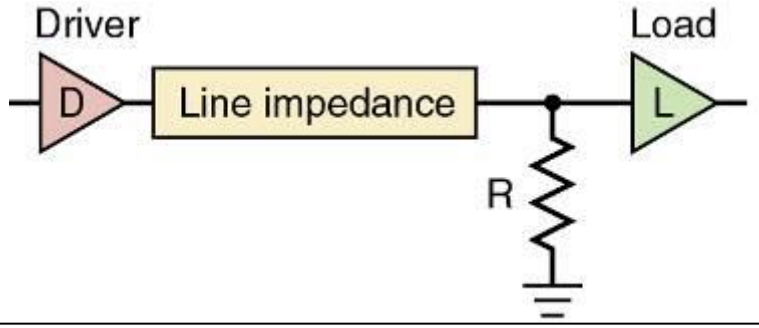


Standard IEEE/ANSI designation for tristate output is a triangle pointing downward.

8-13 High-Speed Bus Interface Logic

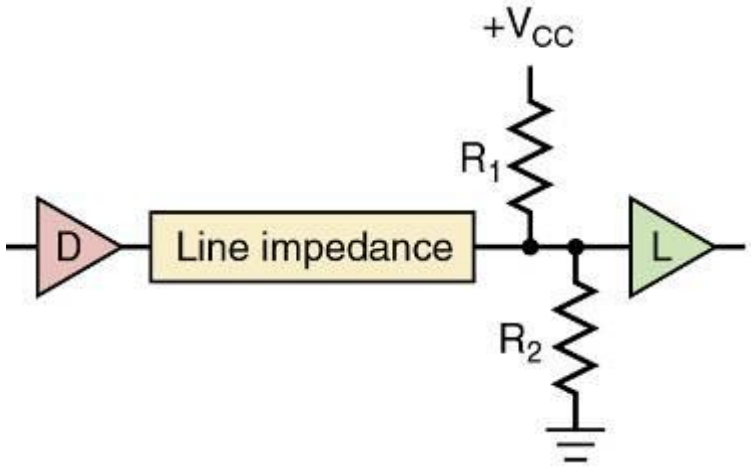
- At high frequencies, bus wires of more than about 4” in length act like transmission lines.
  - To prevent reflected pulse waves, the end of the bus must be terminated with a resistance equal to the line impedance—about 50 Ohms.

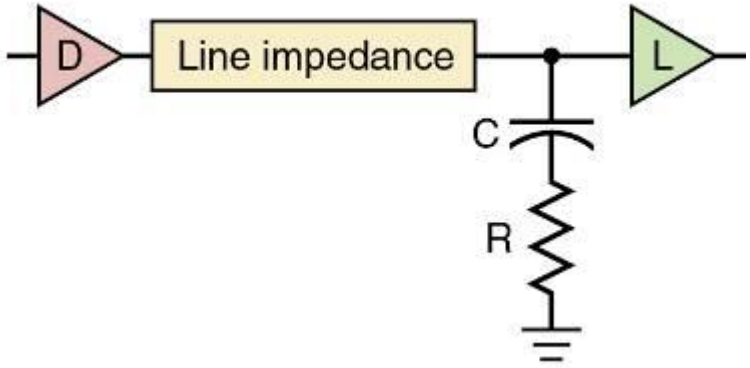
50 Ohm resistor.



Bus termination techniques.

Using a voltage divider with resistances larger than line impedance.

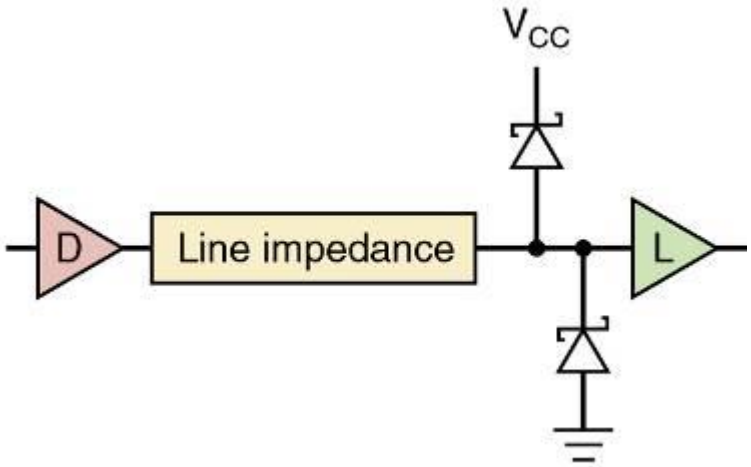


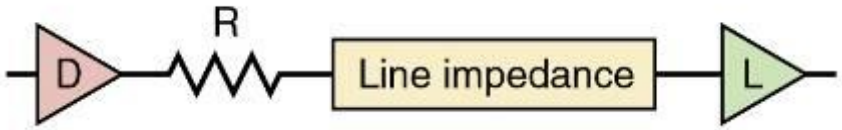


A capacitor blocks dc when the line is not changing—effectively appears as a resistor to the rising or falling pulse.

Bus termination techniques.

Diode termination clips off or clamps the overshoot/undershoot of the ringing caused by the reactive *LC* nature of the line.





Series termination at the source, slows down switching speed, reducing bus frequency limits, but substantially improving reliability of the bus signals.

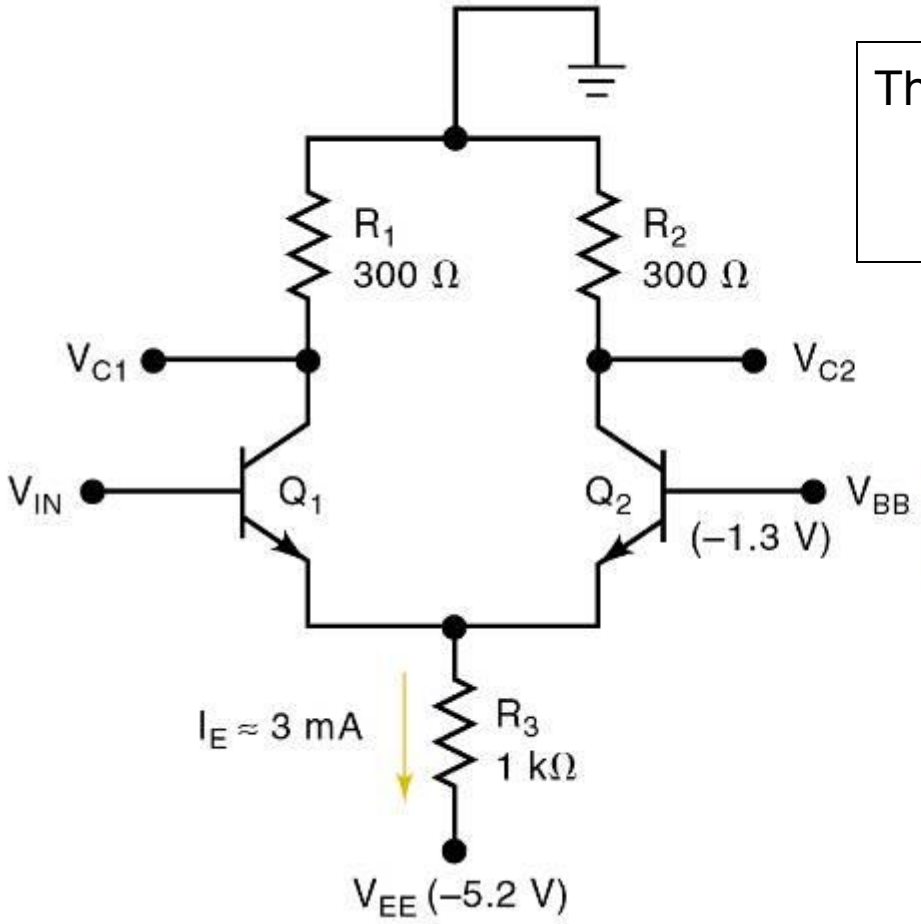
8-13 High-Speed Bus Interface Logic

- The GTLP (Gunning Transceiver Logic Plus) series of bus interface devices is specially designed to drive relatively long buses.
- **Low-voltage differential signaling (LVDS)** uses two wires for each signal.
  - Differential signaling means it responds to the difference between the two wires.

8-14 The ECL Digital IC Family

- The **emitter-coupled logic (ECL)** family operates on the principle of current switching whereby…
  - A fixed bias current less than I_C (sat) is switched from one transistor's collector to another.
    - Also referred to as *current-mode logic* (CML).

Basic ECL circuit – differential amplifier

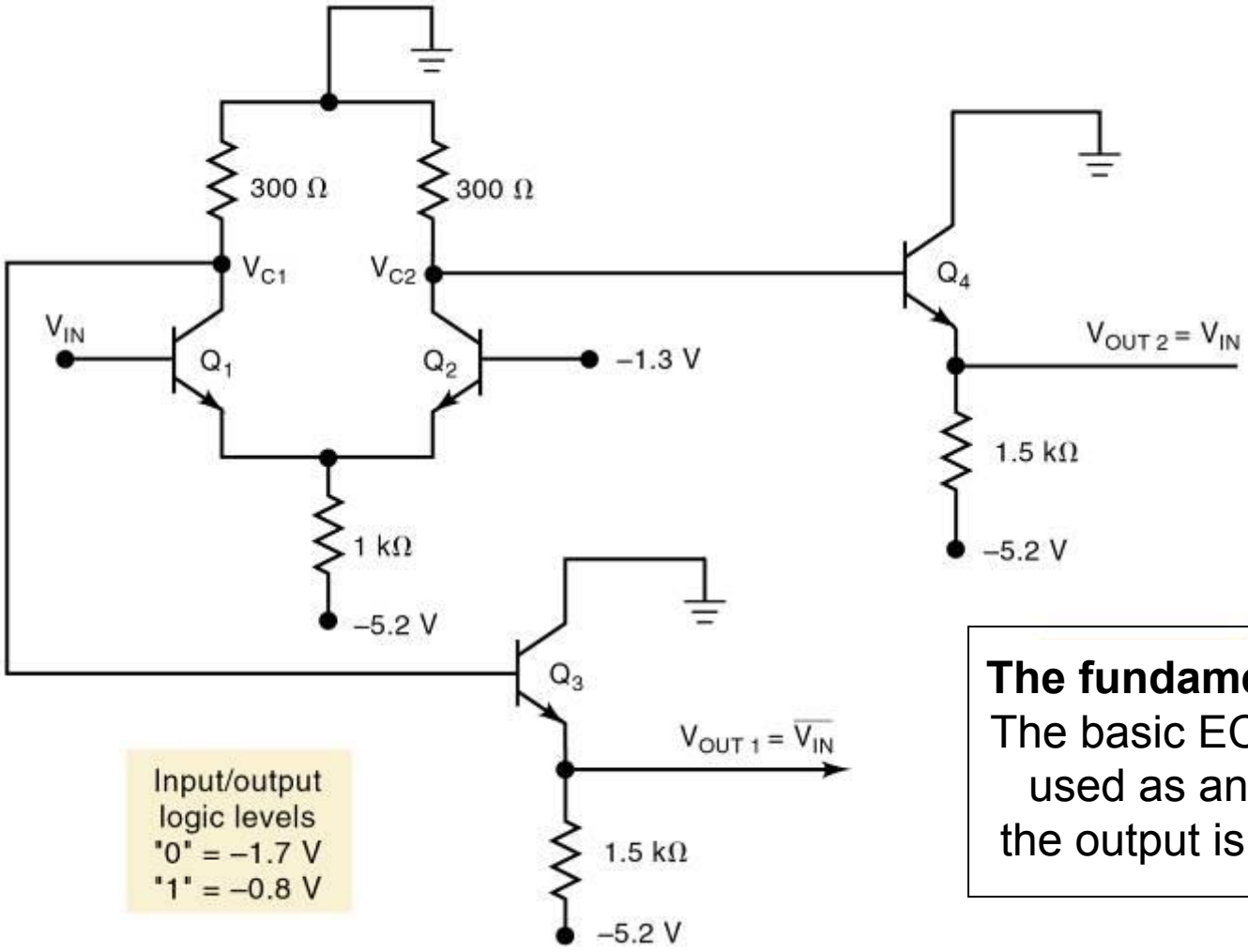


This circuit produces complementary outputs: V_{OUT1}, equal to $\overline{V_{IN}}$, and V_{OUT2}, equal to V_{IN}.

Operating States

V_{IN}	Outputs	
–1.7 V (logic 0)	V_{C1} = 0 V, V_{C2} = –0.9 V	Q_2 conducts
–0.8 V (logic 1)	V_{C1} = –0.9 V, V_{C2} = 0 V	Q_1 conducts

ECL OR/NOR Gate



The fundamental ECL gate. The basic ECL circuit can be used as an INVERTER if the output is taken at V_{OUT1}.

8-14 The ECL Digital IC Family

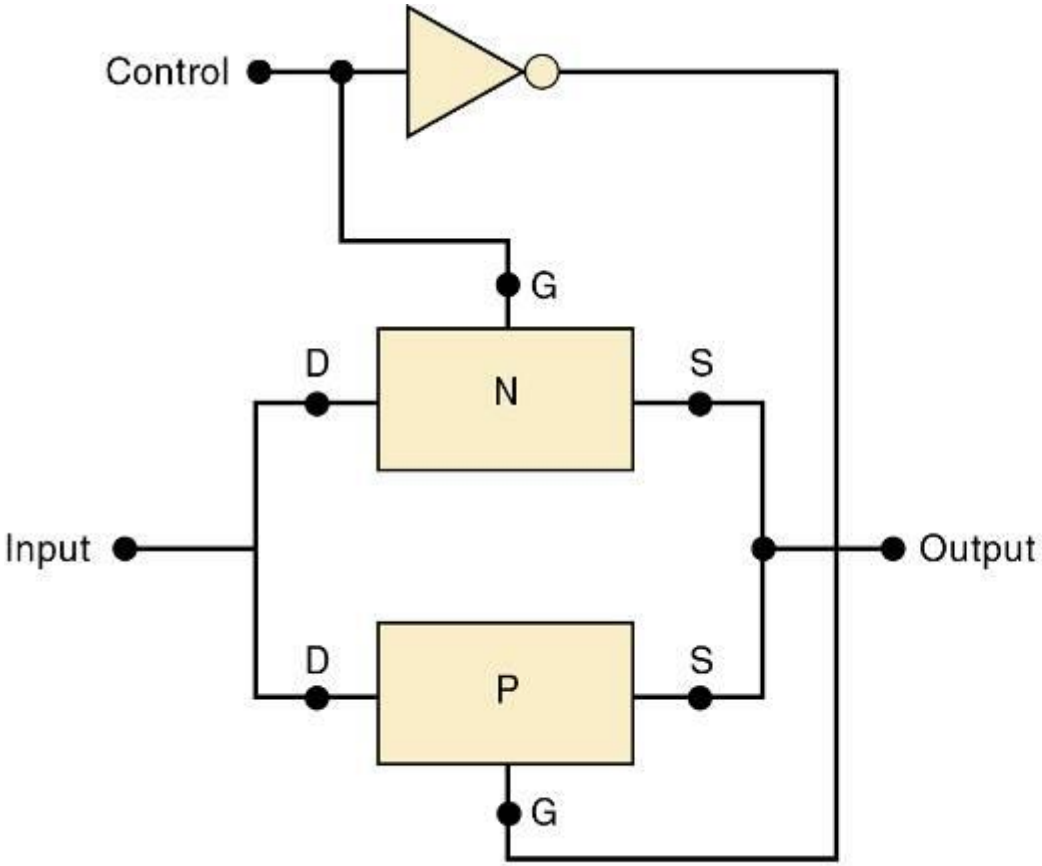
- ECL characteristics:
  - Very fast switching with typical propagation delay of 360 ps—faster than TTL or CMOS.
  - The standard ECL logic levels are nominally -0.8 V and 1.7 V for logical 1 and 0 respectively.
  - Worst-case noise margins approximately 150 mV.
  - ECL logic gates usually produce an output and its complement, eliminating the need for inverters.
  - Current flow remains constant, eliminating noise spikes

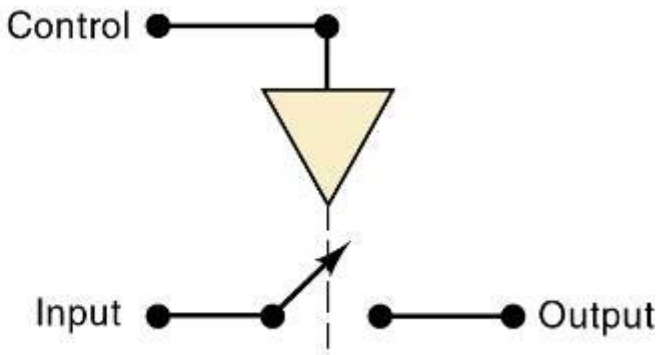
8-15 CMOS Transmission Gate (Bilateral Switch)

- A CMOS circuit with no TTL or ECL counterpart is the **transmission gate** or **bilateral switch**.
  - Essentially acts as a single-pole, single-throw switch controlled by an input logic level.
  - Passes signals in both directions—useful for digital and analog applications.
  - Input must be between 0 and V_{DD} volts.

8-15 CMOS Transmission Gate (Bilateral Switch)

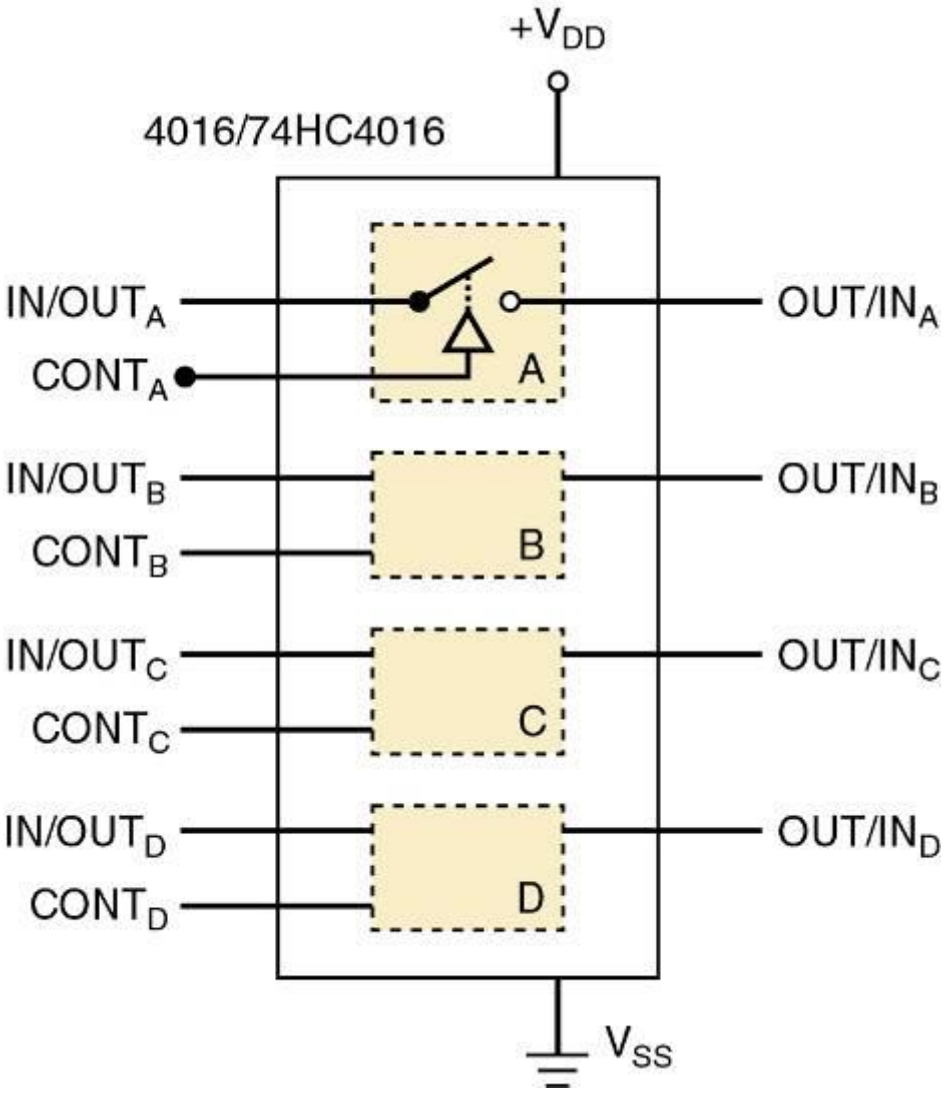
CMOS bilateral switch (transmission gate).





Control input	Switch
0 V	Open (OFF)
$+V_{DD}$	Closed (ON)

8-15 CMOS Transmission Gate (Bilateral Switch)



Logic diagram for a 4016 quad bilateral switch IC

The IC contains four bilateral switches.

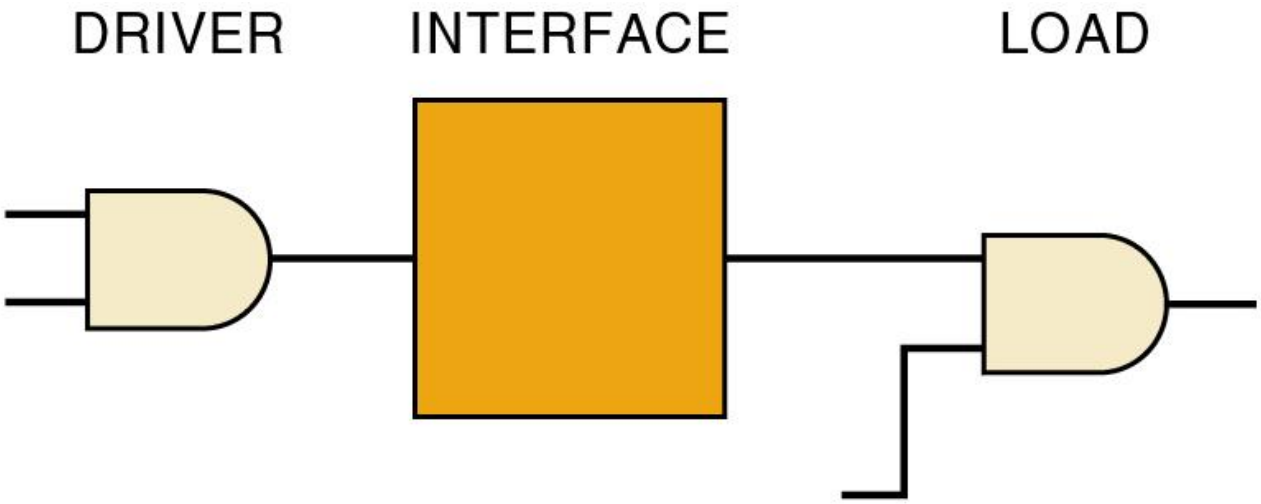
Each switch is independently controlled by its own control input.

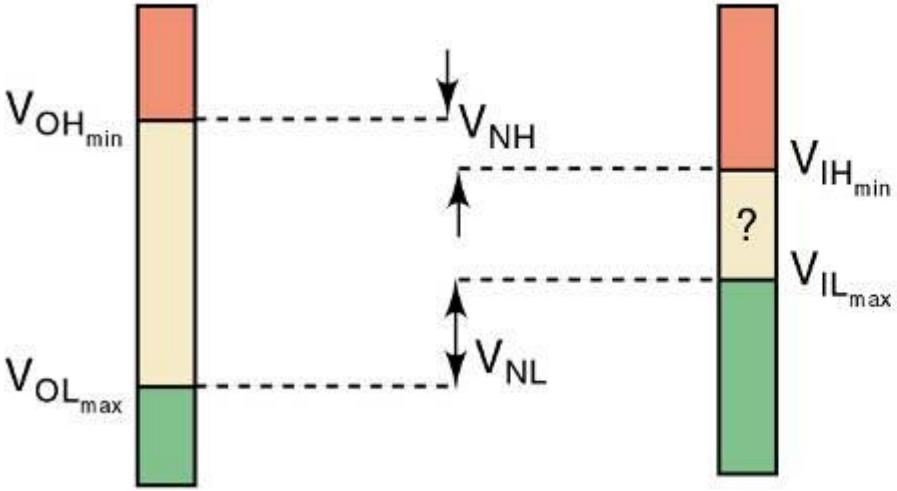
Because switches are bidirectional, either switch terminal can serve as input or output.

8-16 IC Interfacing

- **Interfacing** means connecting output(s) of one circuit/system to input(s) of another circuit/system.
- The simplest and most desirable interface circuit between a driver and a load is a direct connection.
  - Often a direct connection *cannot* be made due to a difference in electrical characteristics.
- An interface circuit is connected between the driver and the load, to condition the driver output signal so it is compatible with requirements of the load.

8-16 IC Interfacing



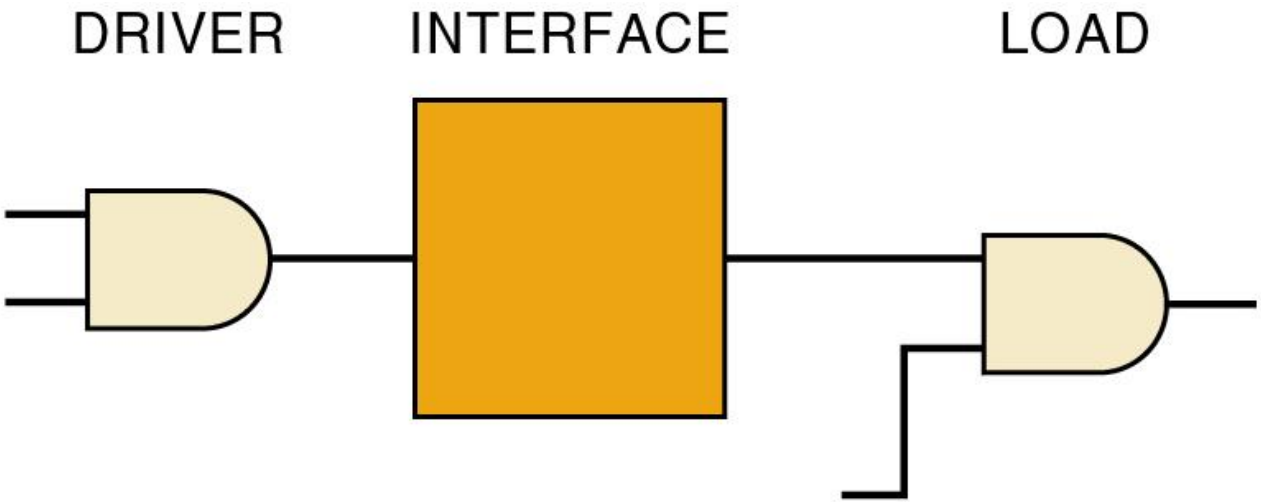


HIGHS are high enough
and
LOWS are low enough

NO INTERFACE NEEDED:
DIRECT CONNECT

(ASSUMING CURRENT LOADING
ACCEPTABLE)

8-16 IC Interfacing



HIGHS not high enough
or
LOWS not low enough

REQUIRES INTERFACE CIRCUIT

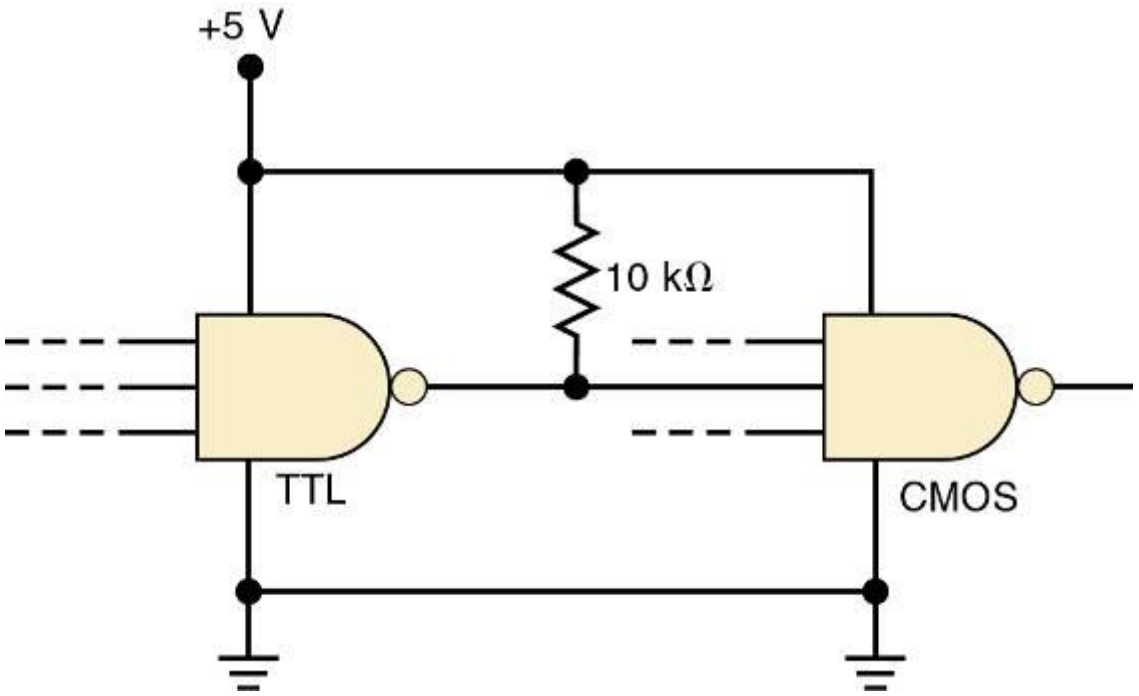
- Logic devices will be voltage-compatible, and no interface will be necessary under the following circumstances:

Driver	*Load*
$V_{OH}(\text{min})$	$> V_{IH}(\text{min}) + V_{NH}$
$V_{OL}(\text{max}) + V_{NL}$	$< V_{IL}(\text{max})$

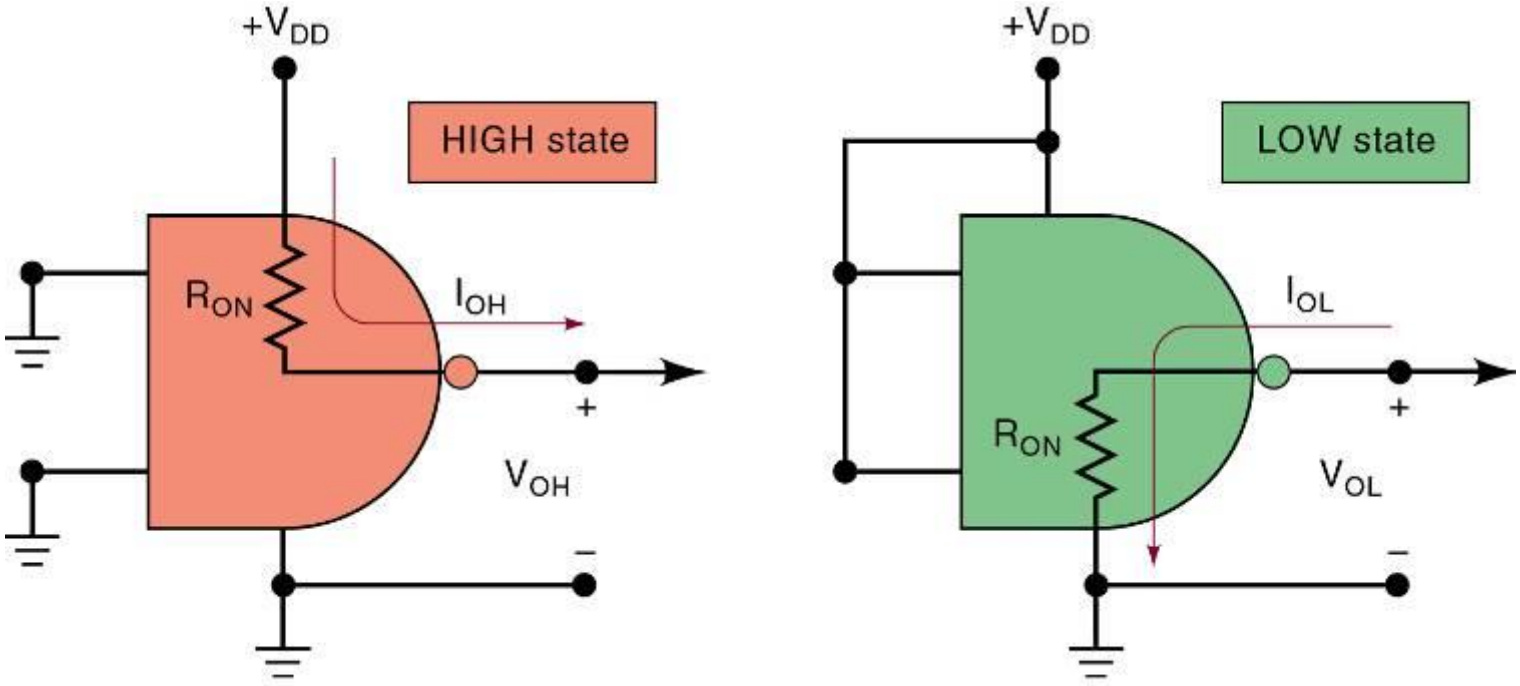
Nominal values for different families/series of digital devices.

	CMOS				TTL				
Parameter	4000B	74HC/HCT	74AC/ACT	74AHC/AHCT	74	74LS	74AS	74ALS	74F
I_{IH}(max)	1 μA	1 μA	1 μA	1 μA	40 A	20 μA	20 μA	20 μA	20 μA
I_{IL}(max)	1 μA	1 μA	1 μA	1 μA	1.6 mA	0.4 mA	0.5 mA	100 μA	0.6 mA
I_{OH}(max)	0.4 mA	4 mA	24 mA	8 mA	0.4 mA	0.4 mA	2 mA	400 mA	1.0 mA
I_{OL}(max)	0.4 mA	4 mA	24 mA	8 mA	16 mA	8 mA	20 mA	8 mA	20 mA

External pull-up resistor is used when TTL drives CMOS.

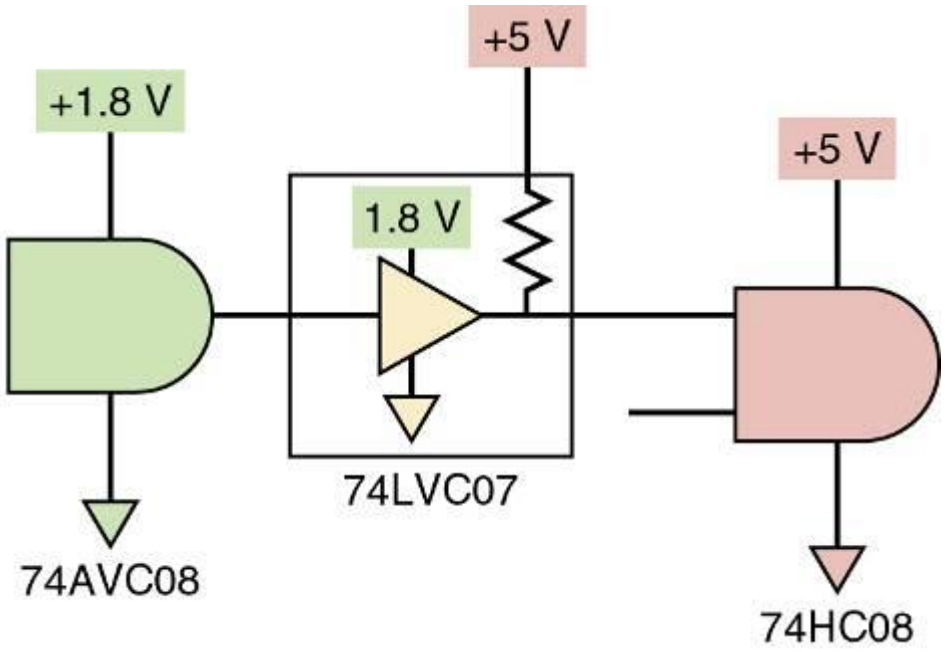


Equivalent CMOS output circuits for both logic states.



8-17 Mixed-Voltage Interfacing

- A substantial shift in voltage because driver & load operate on different supply voltages requires a **voltage-level translator** interface circuit.

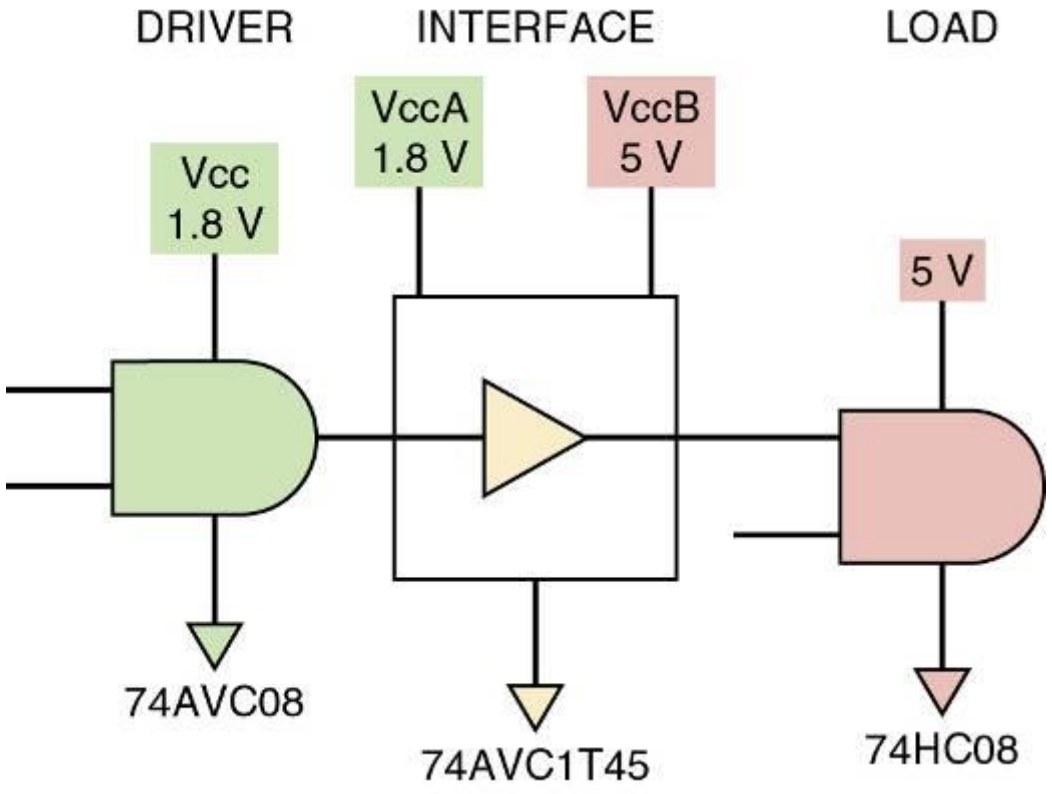


The simplest way to accomplish this is with a buffer that has an open drain—with a pull-up resistor.

8-17 Mixed-Voltage Interfacing

- A substantial shift in voltage because driver & load operate on different supply voltages requires a **voltage-level translator** interface circuit.

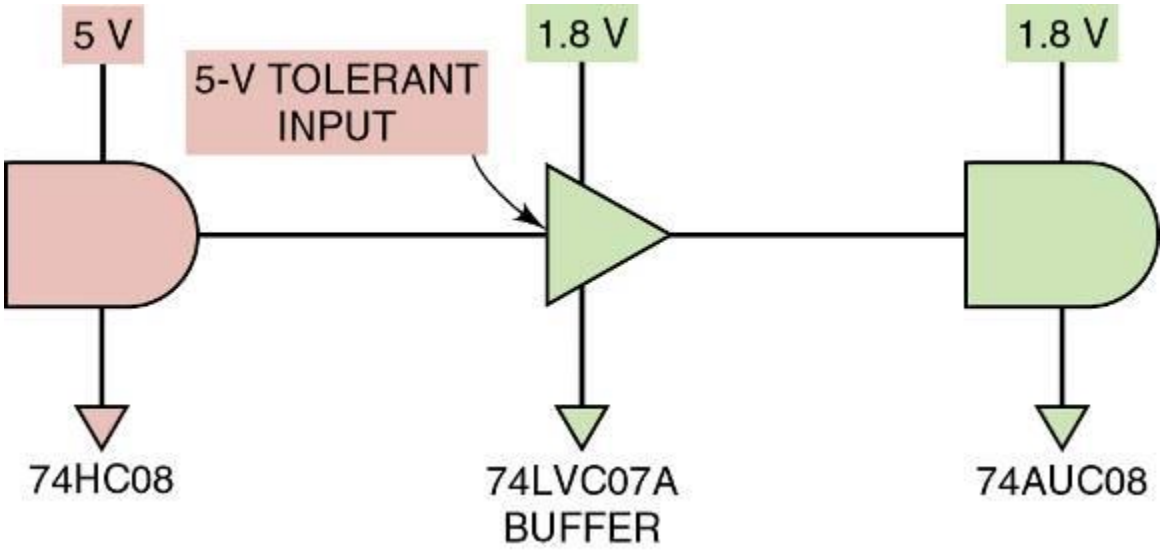
Another solution is a dual-supply-level translator circuit using two different supply voltages, one each for inputs & outputs, translating between the two levels.



8-17 Mixed-Voltage Interfacing

- A substantial shift in voltage because driver & load operate on different supply voltages requires a **voltage-level translator** interface circuit.

Another common solution is an interface using a buffer from a series that can withstand higher input.

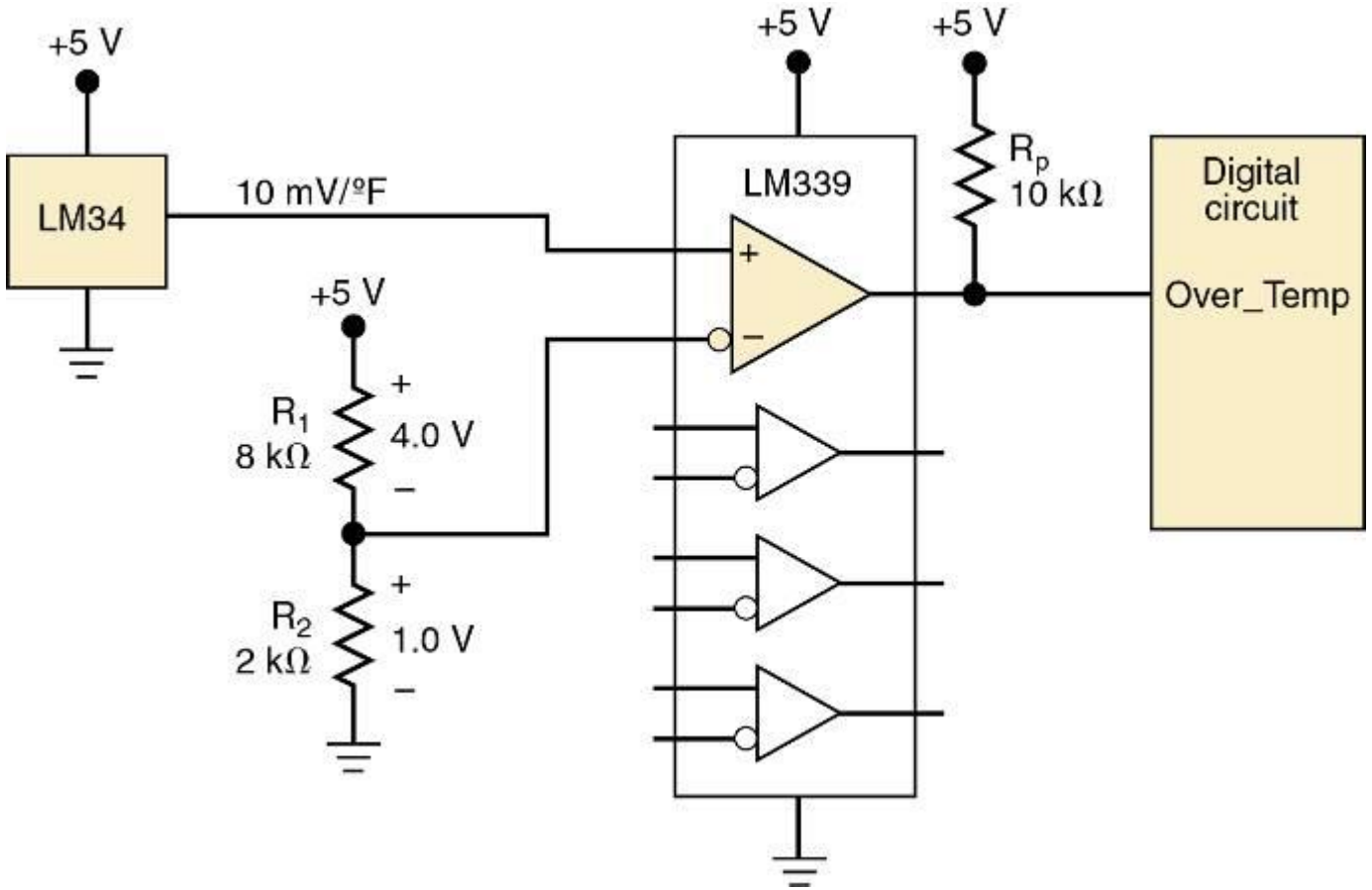


A low-voltage series with 5-V tolerant inputs as an interface.

8-18 Analog Voltage Comparators

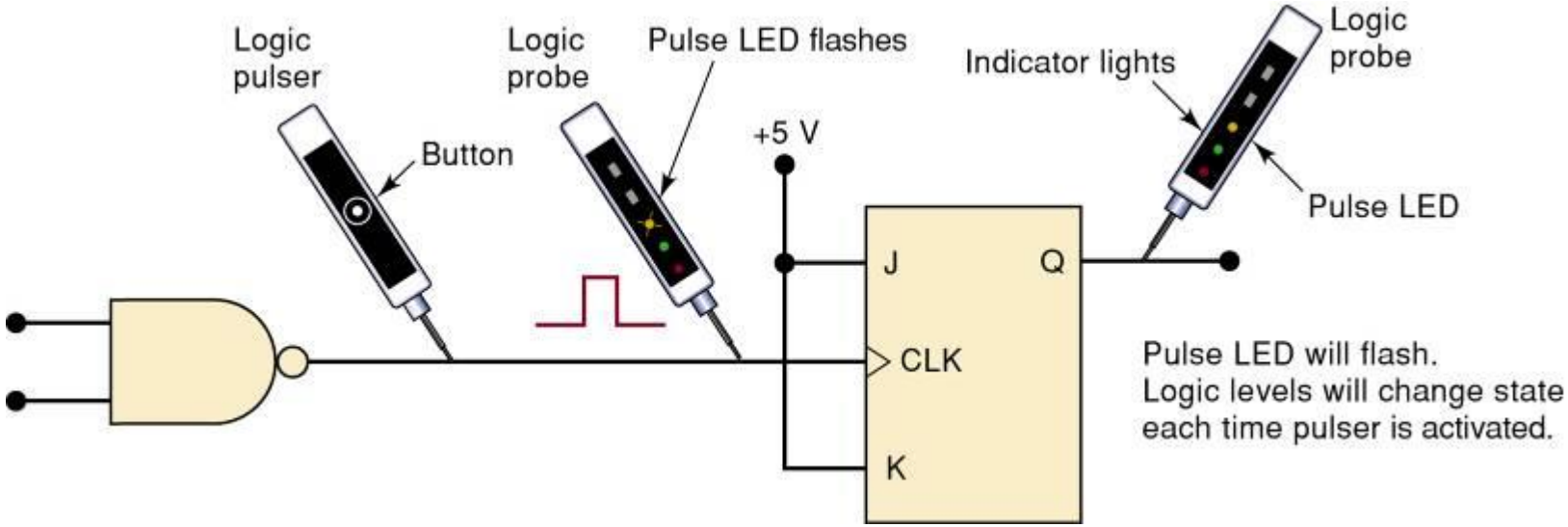
- Another very useful device for interfacing to digital systems is the **analog voltage comparator**.
  - An comparator compares two voltages.
    - If (+) input voltage is greater than (-) input voltage, the output is HIGH.
    - If (-) input voltage is greater than (+) input voltage, the output is LOW.
- Comparator inputs can be thought of as analog.
  - Output is digital—always either HIGH or LOW.
- The comparator is often referred to as a one-bit analog-to-digital (A/D) converter.

A temperature-limit detector using an LM339 analog voltage comparator.



8-19 Troubleshooting

- A **logic pulser** is a testing/troubleshooting tool that generates a short-duration pulse when actuated.
  - It senses existing voltage level at the node and produces a voltage pulse in the opposite direction.



A logic pulser can inject a pulse at any node not shorted directly to ground or V_{CC}.

8-20 Characteristics of an FPGA

- Consider the electrical and timing characteristics for the Altera Cyclone™ II family of devices.
  - A subcategory of PLD devices referred to as field programmable gate arrays (FPGAs).
- Two different power-supply voltages must be applied to a Cyclone II chip.
  - V_{CCINT} provides power for the internal logic of the chip.
    - The nominal value is 1.2 V
  - A separate supply voltage, V_{CCIO} , will power the input and output buffers of the Cyclone chips.

8-20 Characteristics of an FPGA

- Cyclone devices support a variety of input/output standards that gives flexibility in system design.

Parameter	I/O Standard				
	3.3-V LVTTL	3.3-V LVCMOS	2.5-V LVTTL & LVCMOS	1.8-V LVTTL & LVCMOS	1.5-V LVTTL & LVCMOS
V_{IL}(max) (V)	0.8	0.8	0.7	$0.35 \times V_{CCIO}$	$0.35 \times V_{CCIO}$
V_{IH}(min) (V)	1.7	1.7	1.7	$0.65 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
V_{OL}(max) (V)	0.45	0.2	0.4	0.45	$0.25 \times V_{CCIO}$
V_{OH}(min) (V)	2.4	$V_{CCIO} - 0.2$	2.0	$V_{CCIO} - 0.45$	$0.75 \times V_{CCIO}$

Altera Cyclone II characteristics using general-purpose I/O standards.

- In addition, the Cyclone family supports a number of differential I/O standards that can provide…
  - Improved noise immunity.
  - Lower electromagnetic interference (EMI) generation.
  - Reduced power consumption.

8-20 Characteristics of an FPGA

- The Cyclone II devices use CMOS, so power consumption will be low—power will be dependent on voltage level, frequencies & I/O signal loads.
- The Quartus II software has two tools to estimate the amount the power usage for an application
  - The PowerPlay Early Power Estimator is typically used during the early stages of design
  - The PowerPlay Power Analyzer is often used with sample test vectors, for more accurate estimate.

8-20 Characteristics of an FPGA

- The speed of an application will be dependent upon the application and how it is implemented in the programmable device.
  - Cyclone II chips are available in three different speed grades, called –6 (dash six), –7, and –8.

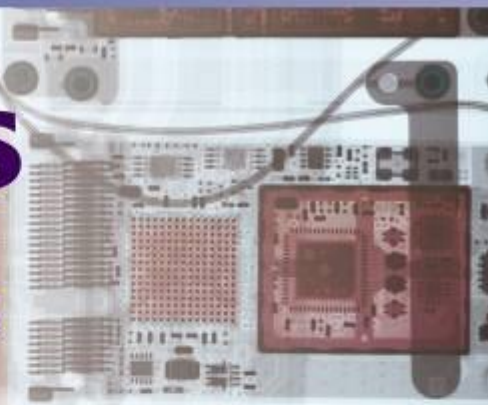
Application	–6 Speed grade	–7 Speed grade	–8 Speed grade
16-bit counter	401.6 MHz	349.4 MHz	310.65 MHz
64-bit counter	157.15 MHz	137.98 MHz	126.27 MHz

END

ELEVENTH EDITION

Digital Systems

Principles and Applications



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