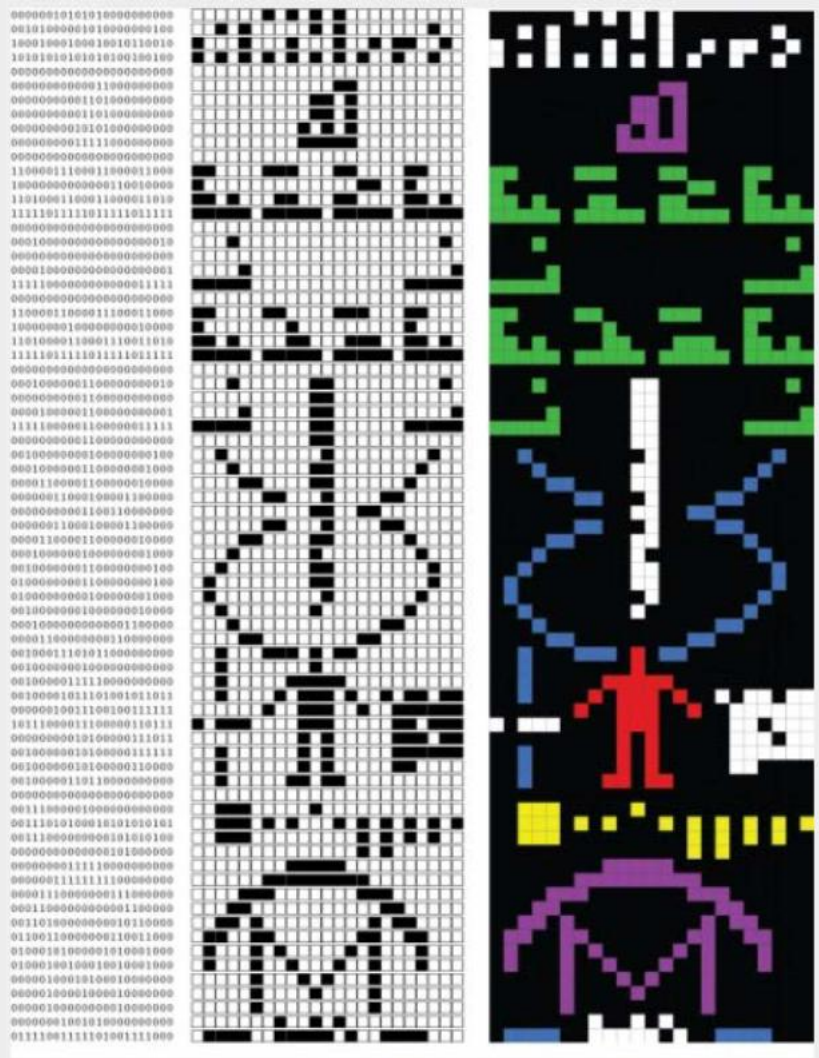
Digital Logic Design

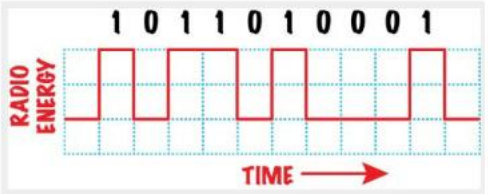
Lecture 1: Introduction to Digital Systems

Arecibo message



(L) The Arecibo Message string, arranged in 73 rows and 23 columns. Even in text, your eye can see patterns emerging. (C) The same message shown as a shaded grid, making the patterns more clear. (R) The same image colorized for discussion. [Images by S. Larson; R image from Wikimedia Commons]

(L) The 300 m Arecibo Radio Telescope, built into the landscape of Puerto Rico. (R) The globular cluster in Hercules, M13, located 24,000 lightyears from Earth.



In 1974, the astronomer named Frank Drake and his colleagues sent a message out to the aliens with the Arecibo radio telescope in Puerto Rico, the first deliberate message sent from Earth out to the stars.

The string of 1's and 0's was sent to a group of about 300,000 stars in called the Great Cluster in Hercules, Messier 13, about 24,000 light years away.

The message contained information about life-giving chemicals, DNA, a simple drawing of our solar system, and pictures of human beings and the Arecibo telescope.

Binary number system

The binary number system is a base-2 number system.

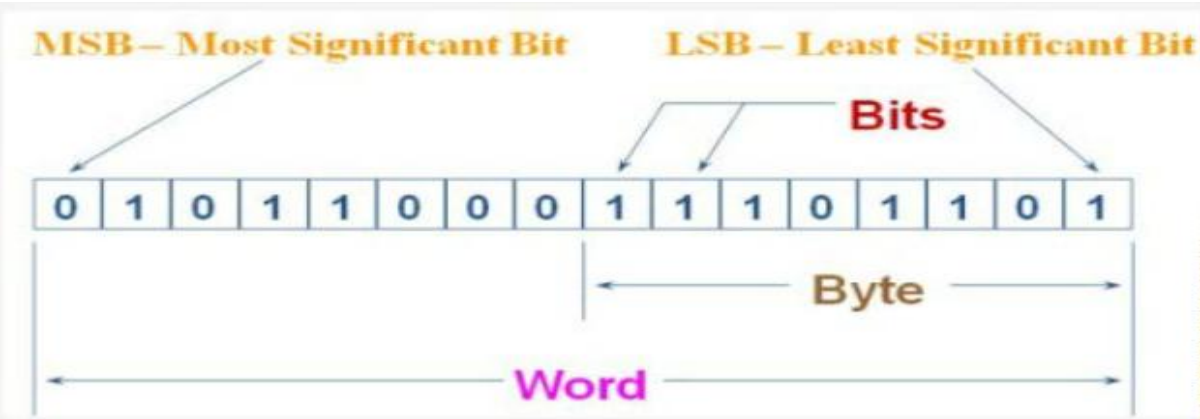
The system contains only two valid digits which are 0 and 1 to represent its numbers.

Example:

binary number $(11101110)_2 = 1x2^7 + 1x2^6 + 1x2^5 + 0x2^4 + 1x2^3 + 1x2^2 + 1x2^1 + 0x2^0$

$= 128 + 64 + 32 + 0 + 8 + 4 + 2 + 0$

$= 238$ decimal number



1 binary digit is a bit

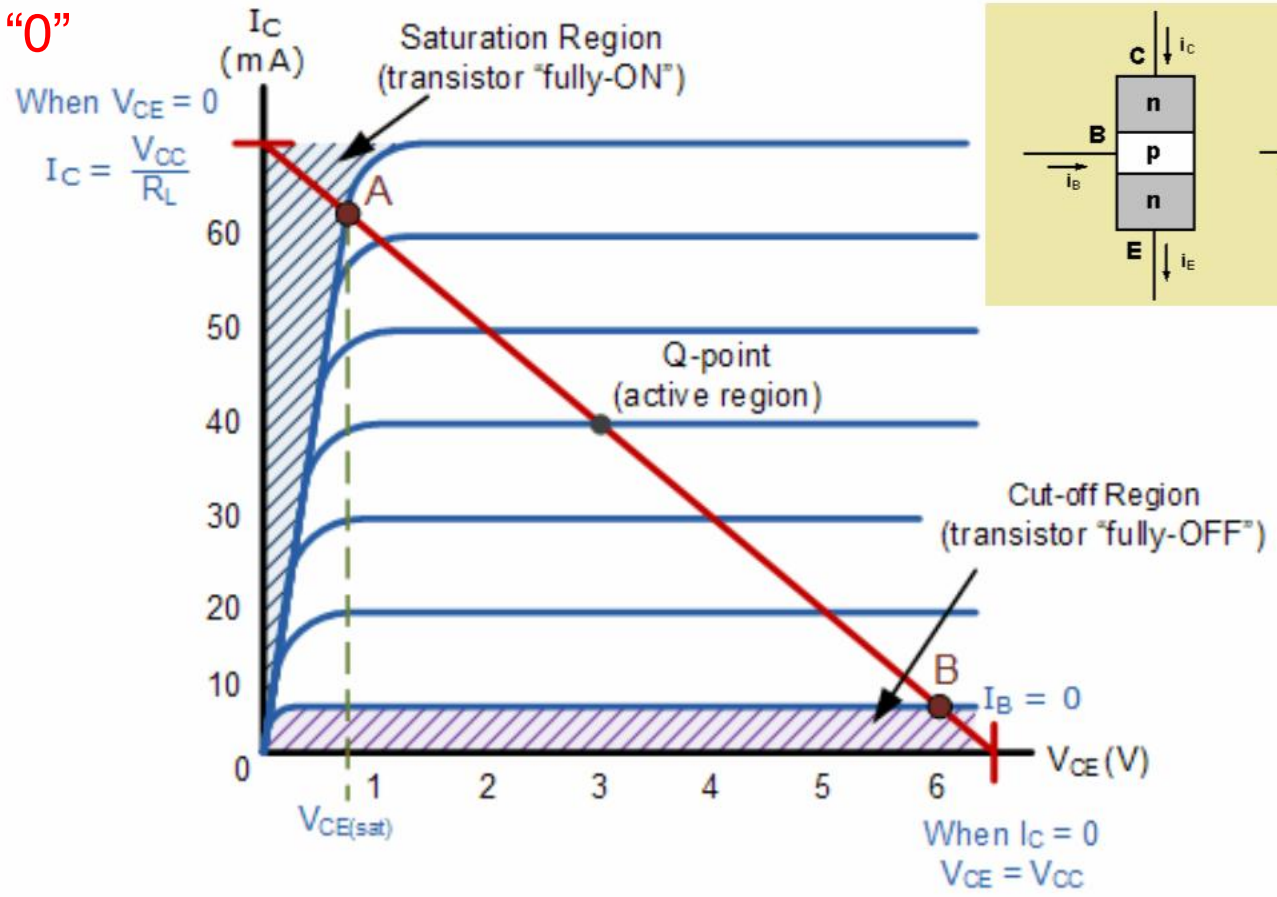
8-bits is a byte

16-bits is a word
(depending on the systems)

Transistor as a switch: operating regions

Switch: “ON”, “CLOSED”
Logic level: “LOW”
Binary digit: “0”

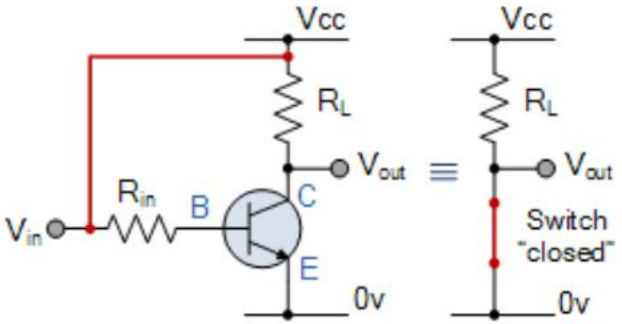
NPN BJT



Switch: “OFF”, “OPEN”
Logic level: “HIGH”
Binary digit: “1”

Transistor as a switch: saturation characteristics

Saturation Characteristics



- The input and Base are connected to V_{CC}
- Base-Emitter voltage $V_{BE} > 0.7v$
- Base-Emitter junction is forward biased
- Base-Collector junction is forward biased
- Transistor is "fully-ON" (saturation region)
- Max Collector current flows ($I_C = Vcc/R_L$)
- $V_{CE} = 0$ (ideal saturation)
- $V_{OUT} = V_{CE} =$ "0"
- Transistor operates as a "closed switch"

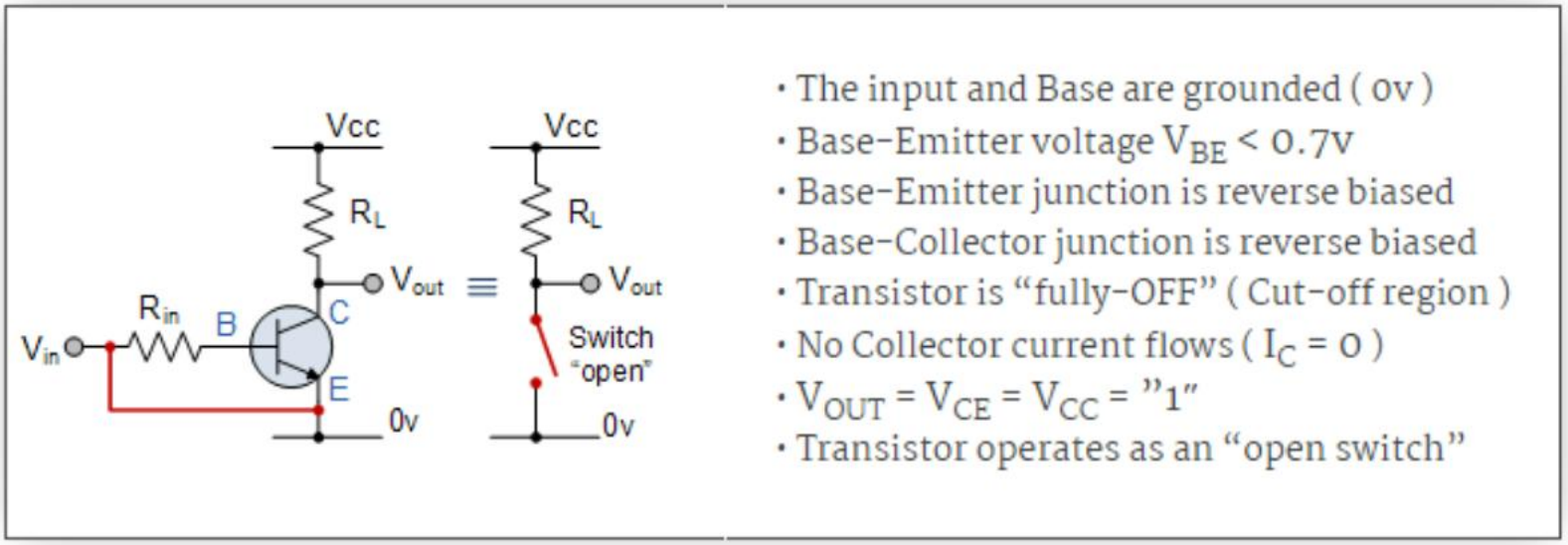
Switch: "ON", "CLOSED"

Logic level: "LOW"

Binary digit: "0"

Transistor as a switch: cutoff characteristics

Cut-off Characteristics



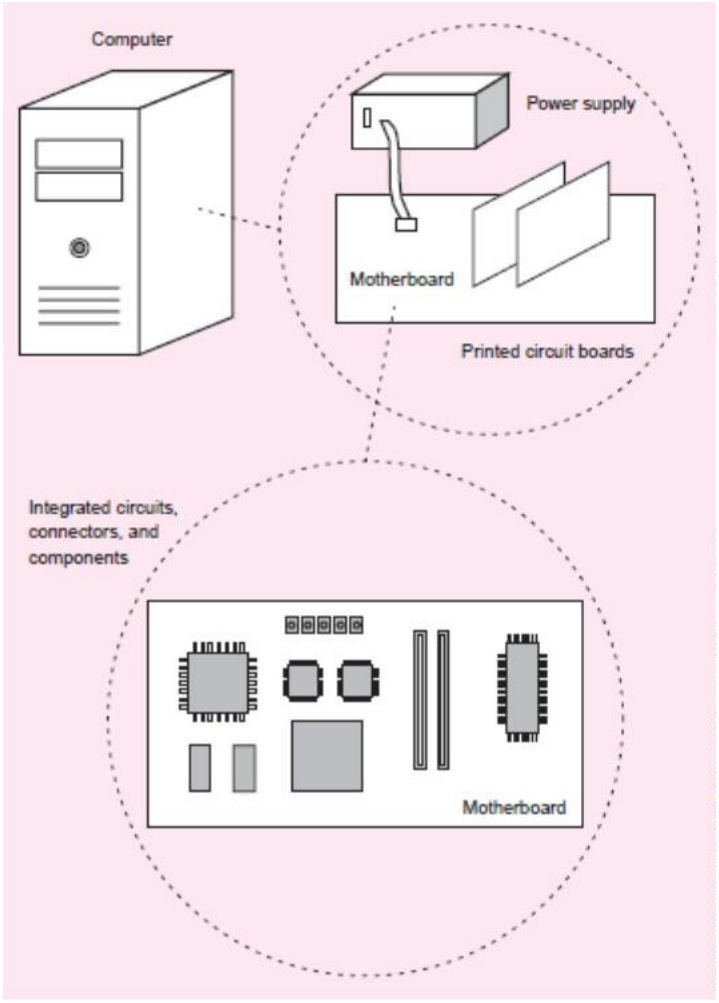
- The input and Base are grounded (0v)
- Base-Emitter voltage $V_{BE} < 0.7v$
- Base-Emitter junction is reverse biased
- Base-Collector junction is reverse biased
- Transistor is "fully-OFF" (Cut-off region)
- No Collector current flows ($I_C = 0$)
- $V_{OUT} = V_{CE} = V_{CC} =$ "1"
- Transistor operates as an "open switch"

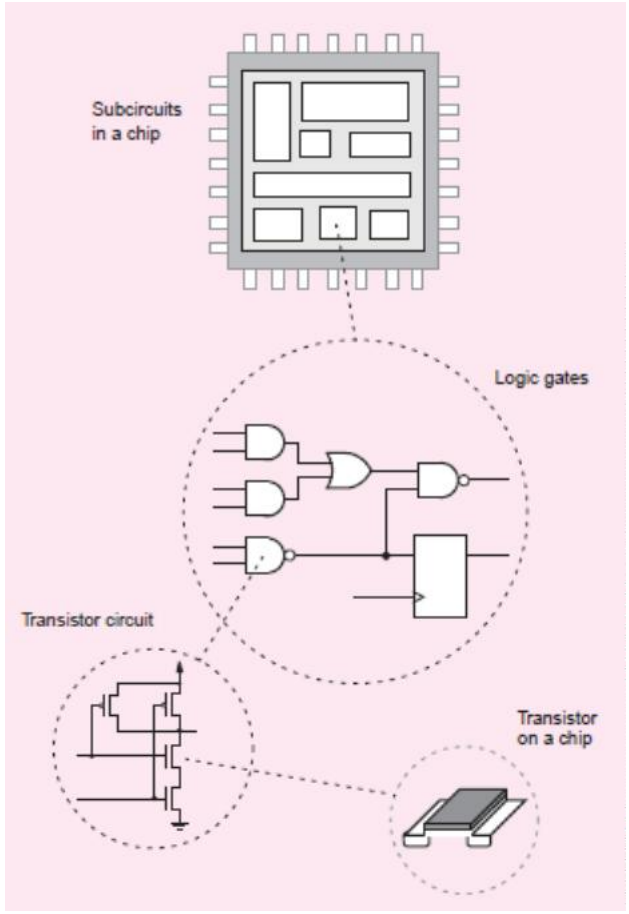
Switch: "OFF", "OPEN"

Logic level: "HIGH"

Binary digit: "1"

Structure of a computer

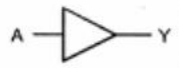
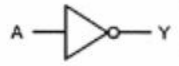
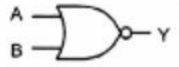




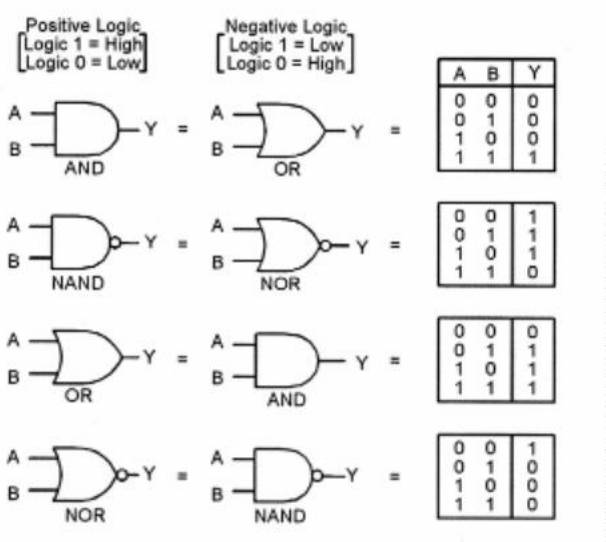
An integrated circuit chip
comprises a number of subcircuits, which are logic circuits interconnected to build the complete circuit.
Examples of subcircuits are those that perform arithmetic operations, store data, or control the flow of data.

A logic circuit comprises
a network of connected logic gates.
A logic gate is constructed from a transistor circuit.

Logic gates

Logic function	Logic symbol	Truth table	Boolean expression
Buffer		A Y 0 0 1 1	Y = A
Inverter (NOT gate)		A Y 0 1 1 0	$Y = \overline{A}$
2-input AND gate		A B Y 0 0 0 0 1 0 1 0 0 1 1 1	Y = A•B
2-input NAND gate		A B Y 0 0 1 0 1 1 1 0 1 1 1 0	$Y = \overline{A \cdot B}$
2-input OR gate		A B Y 0 0 0 0 1 1 1 0 1 1 1 1	Y = A + B
2-input NOR gate		A B Y 0 0 1 0 1 0 1 0 0 1 1 0	$Y = \overline{A + B}$
2-input EX-OR gate		A B Y 0 0 0 0 1 1 1 0 1 1 1 0	$Y = A \oplus B$
2-input EX-NOR gate		A B Y 0 0 1 0 1 0 1 0 0 1 1 1	$Y = \overline{A \oplus B}$

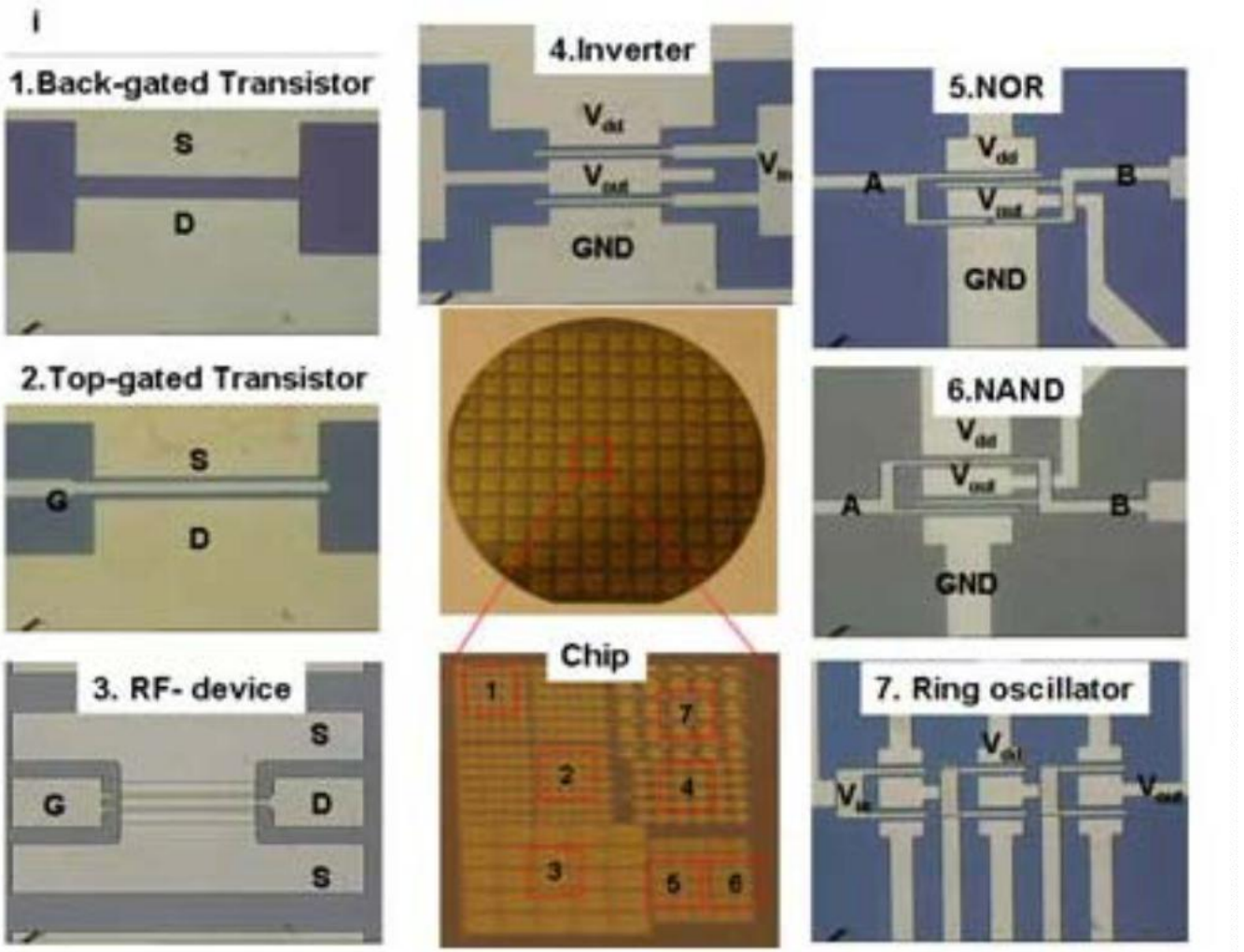
Symbols, truth tables, and Boolean expressions for the eight basic types of logic gates



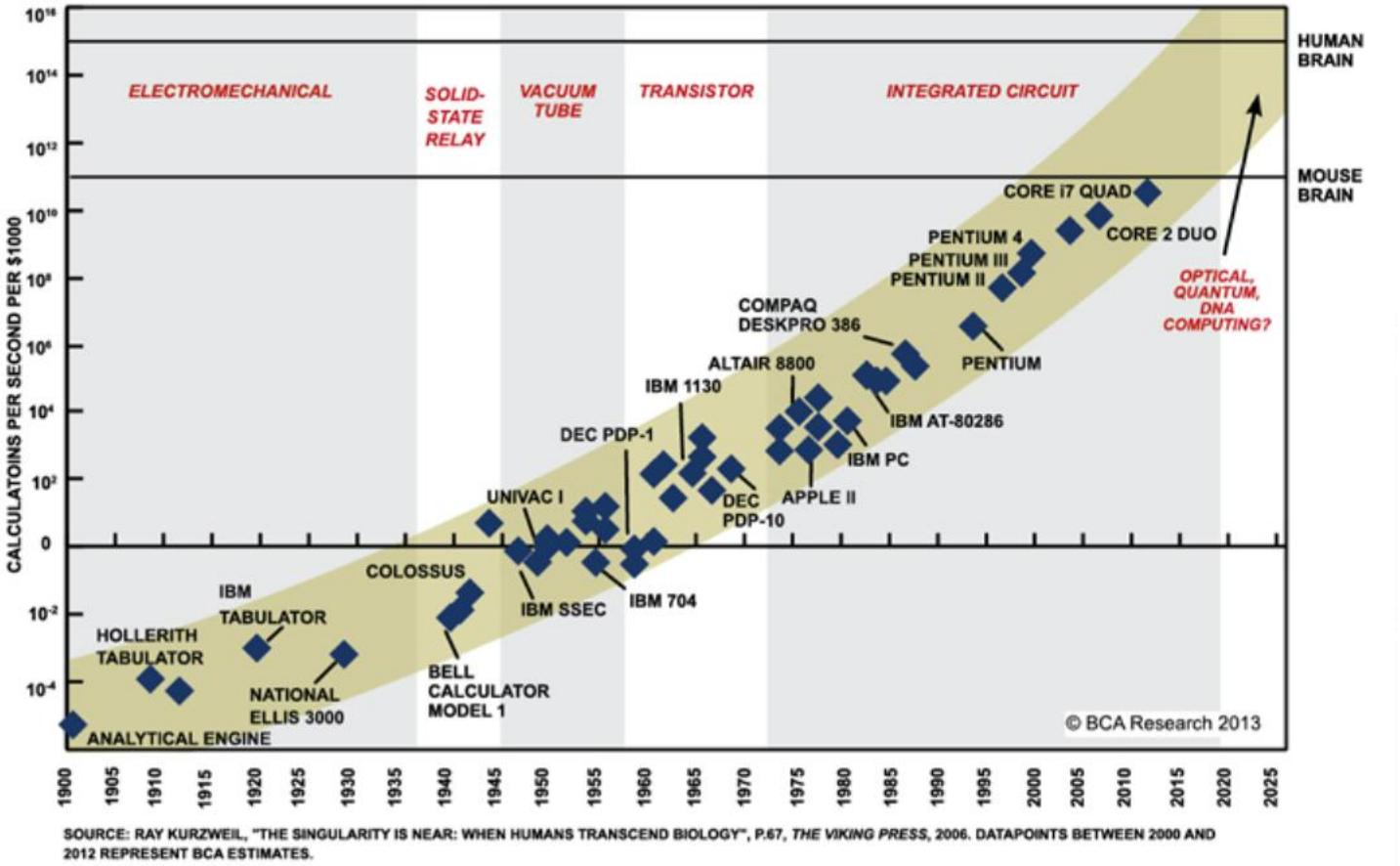
Basic sets of two-input positive and negative
logic equivalents

Any AND or OR gate can be used as a
non-inverting buffer element

Transistors on a Si chip



Moore's Law



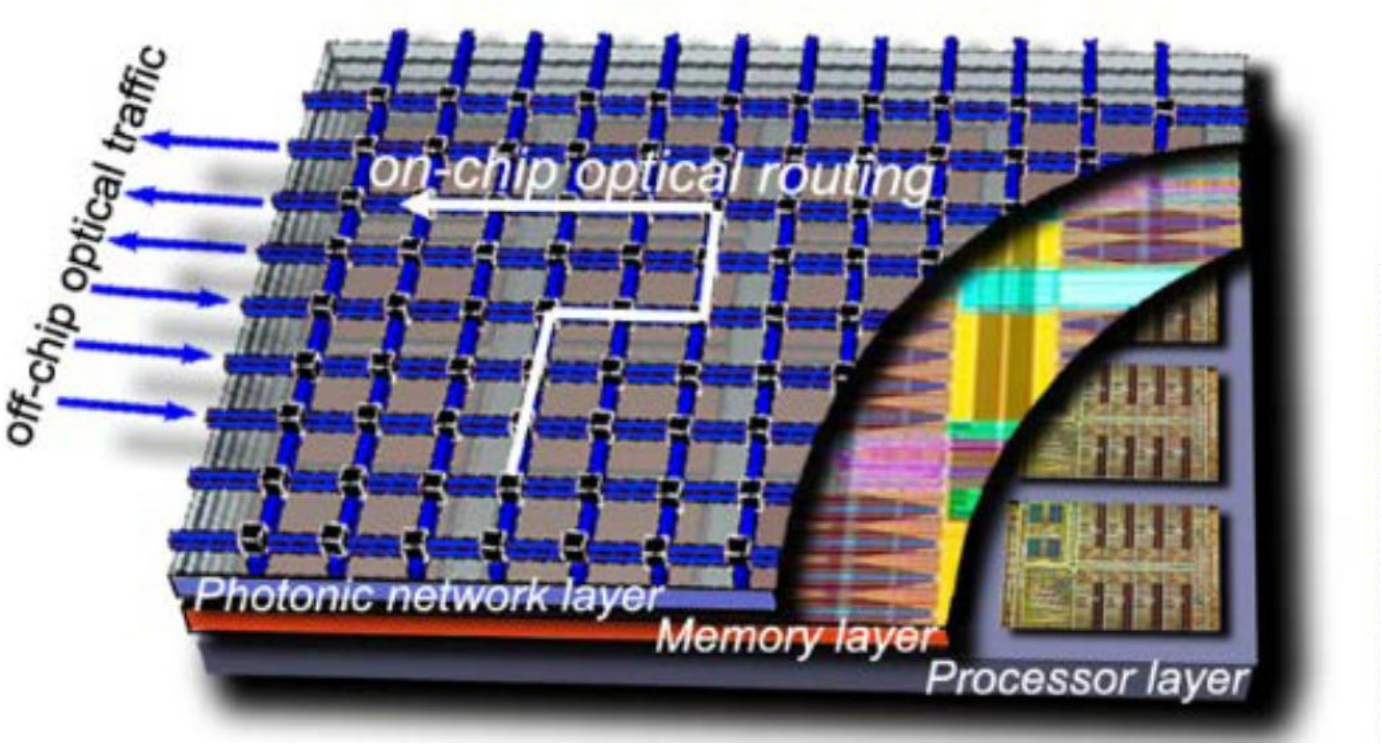
SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, *THE VIKING PRESS*, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Moore's law states that the number of transistors on a microprocessor chip will double every two years.

This means the processor speeds, or overall processing power for computers will double every two years.

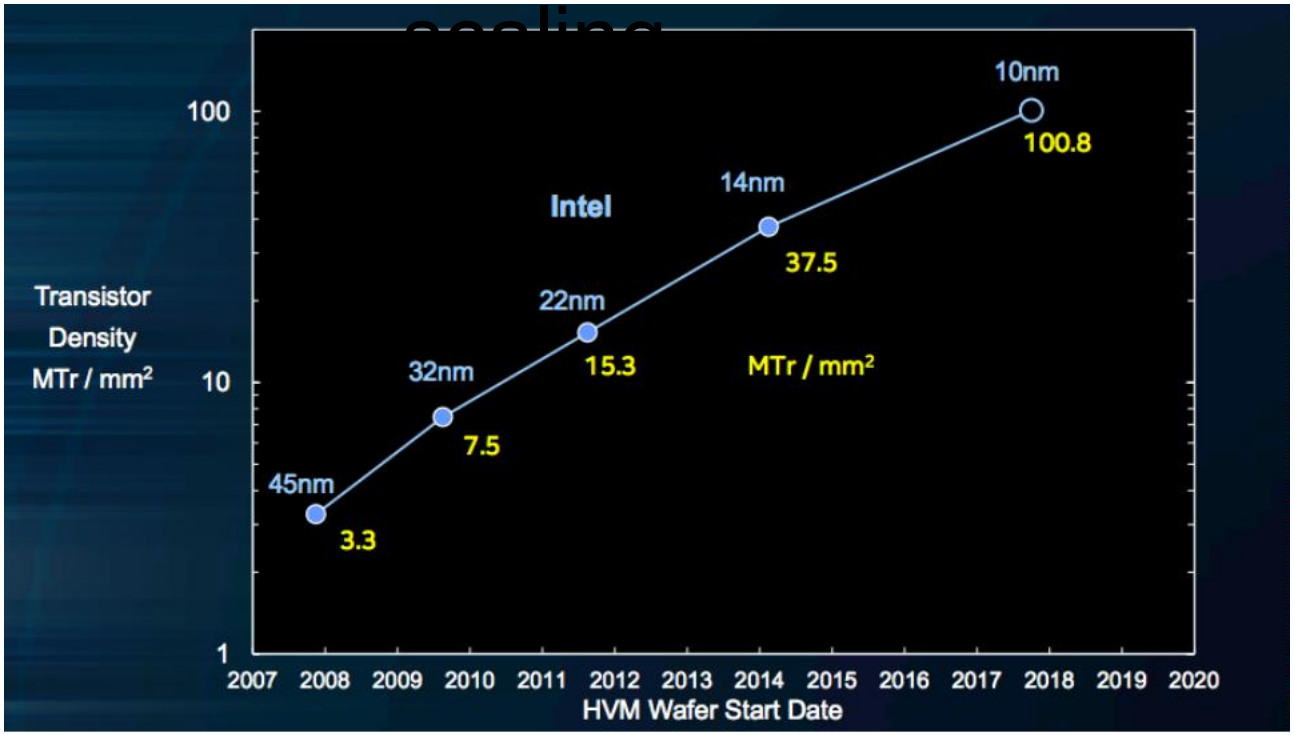
Where is Moore's Law Headed Now?

A lot of people who know about these things have predicted that in 2022 Moore's Law will reach its logical end.



There are technologies being explored now that could surpass Moore's Law, at least for any given two-year period. For example, 3D circuit boards that employ nanotechnology and optical components. These have the power to advance computing power and speed an order of magnitude.

Transistor technology scaling

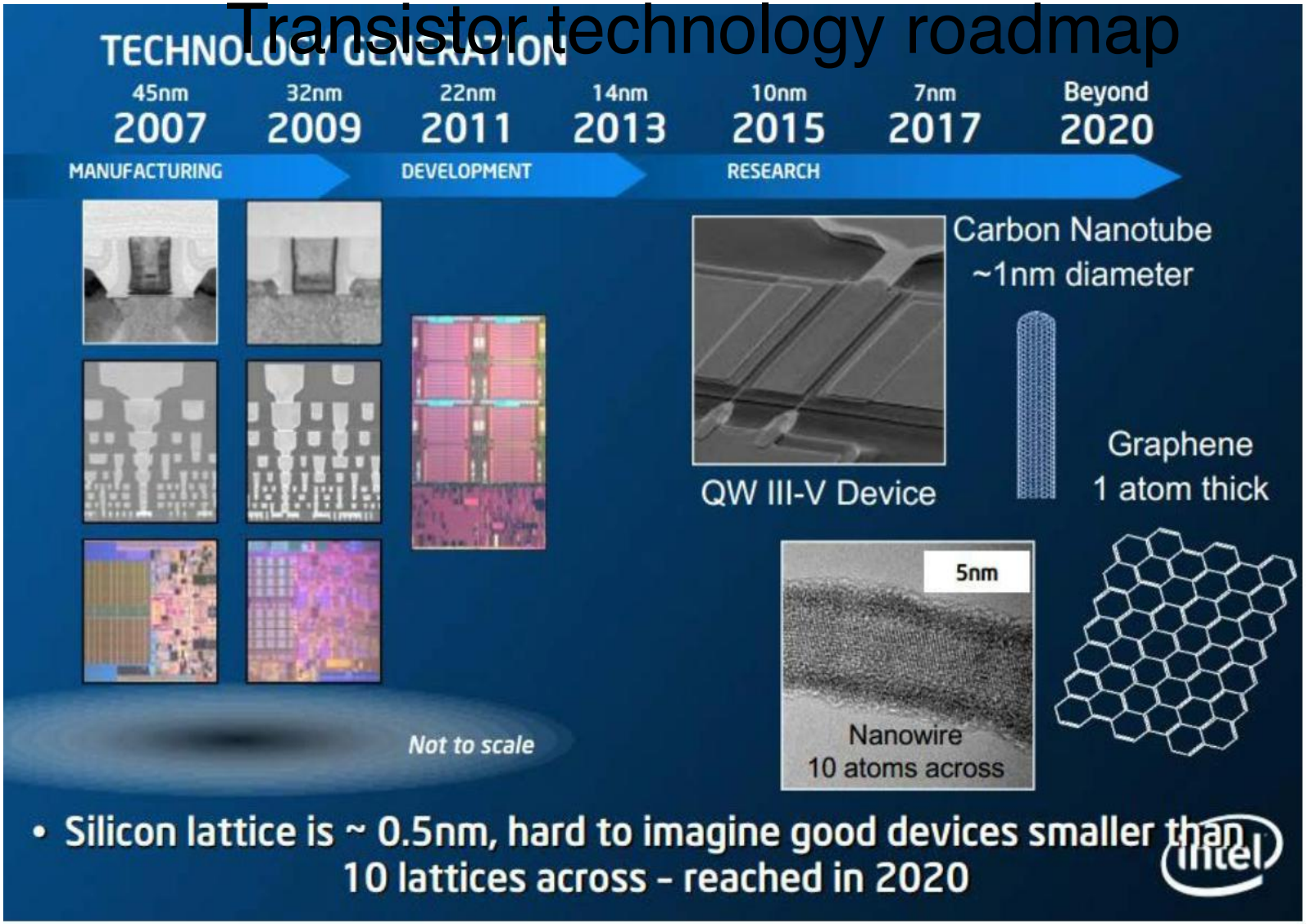


Intel now packs 100 million transistors in each square millimeter.

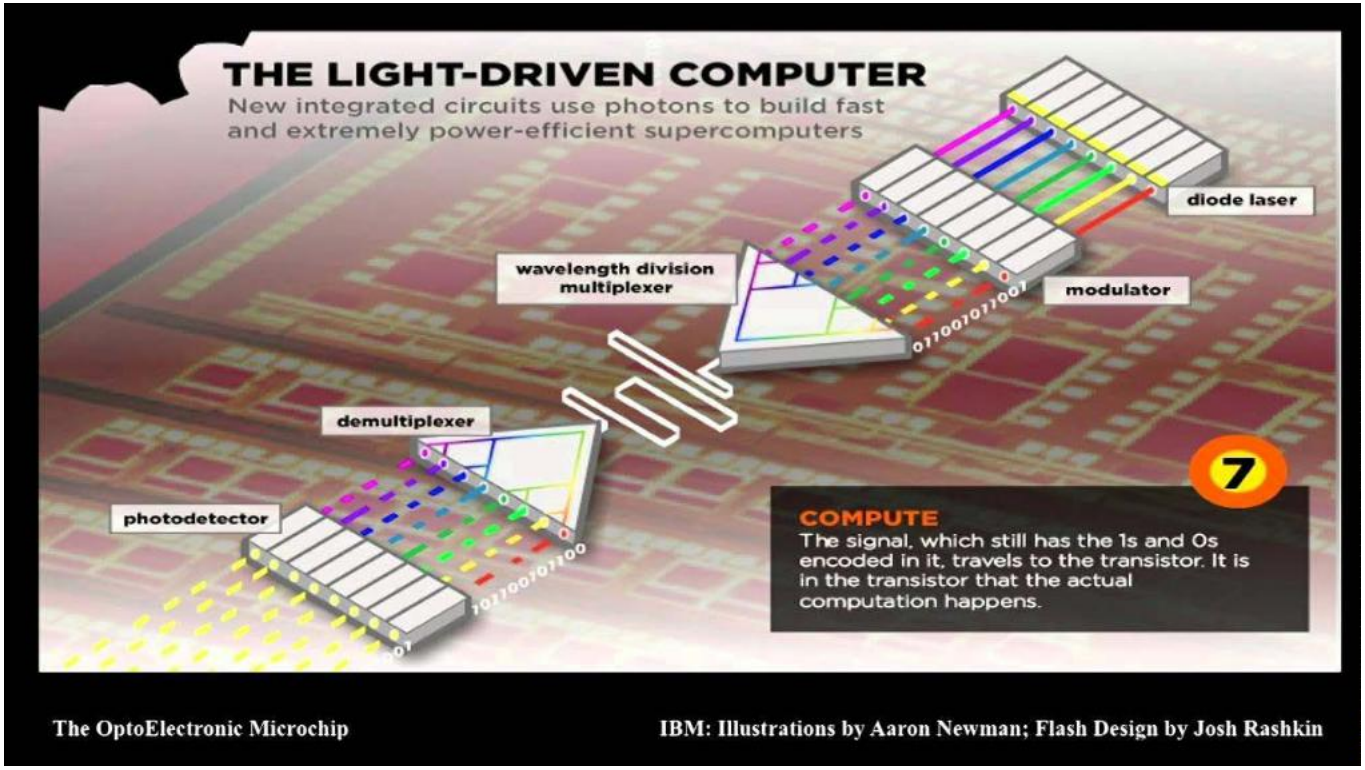
The issue with transistors is that they now exist at the scale of a few nanometers in size—only a few silicon atoms thick. They can't practically be made any smaller than they are now.

If they get any smaller, the electrical current flowing through the transistor easily leaks out into other components nearby or deforms the transistor due to heat, rendering it useless. You need a minimum number of atoms to make the transistor work and we've functionally reached that limit.

Transistor technology roadmap

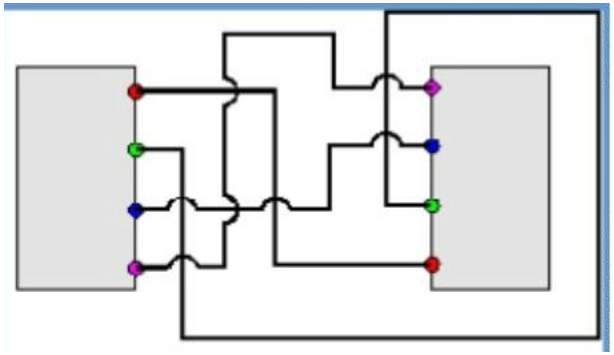


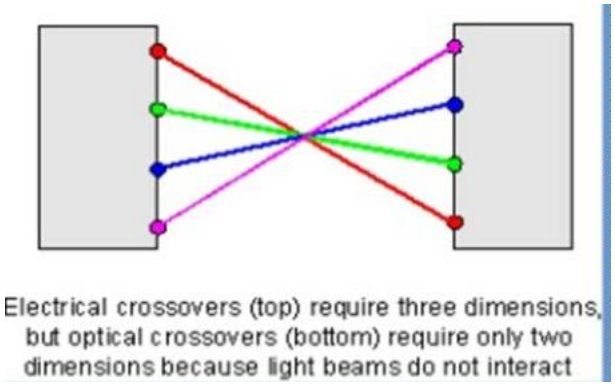
Optical computer



An optical computer is a device that uses photons in visible light or infrared beams, rather than electric current, to perform digital computations.

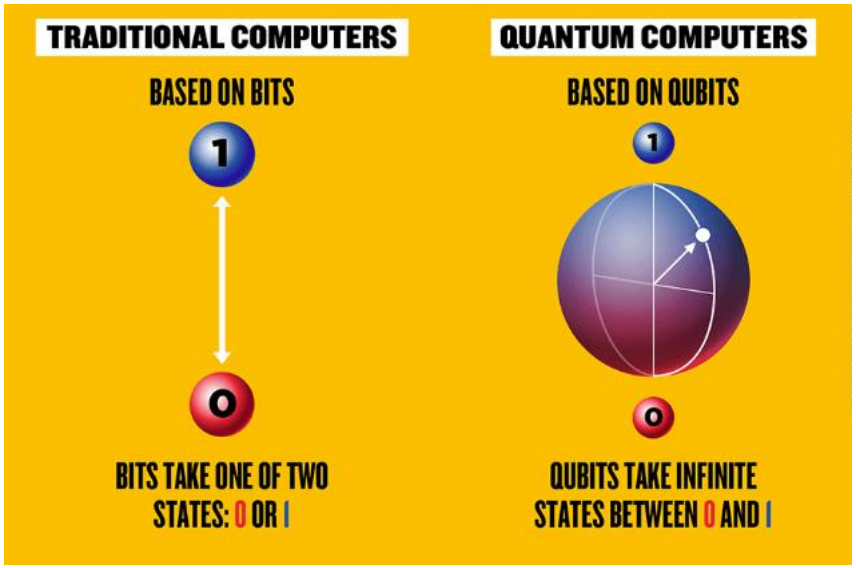
Computers used to work in millisecond, then moved up to microseconds, and now are approaching nanoseconds for logic operations and picosecond or femtosecond for the switches and gates in the chip.

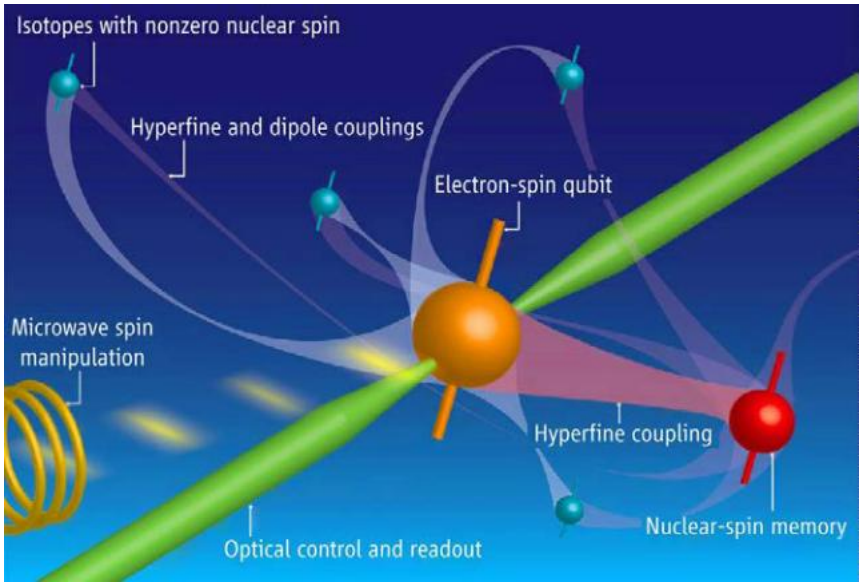




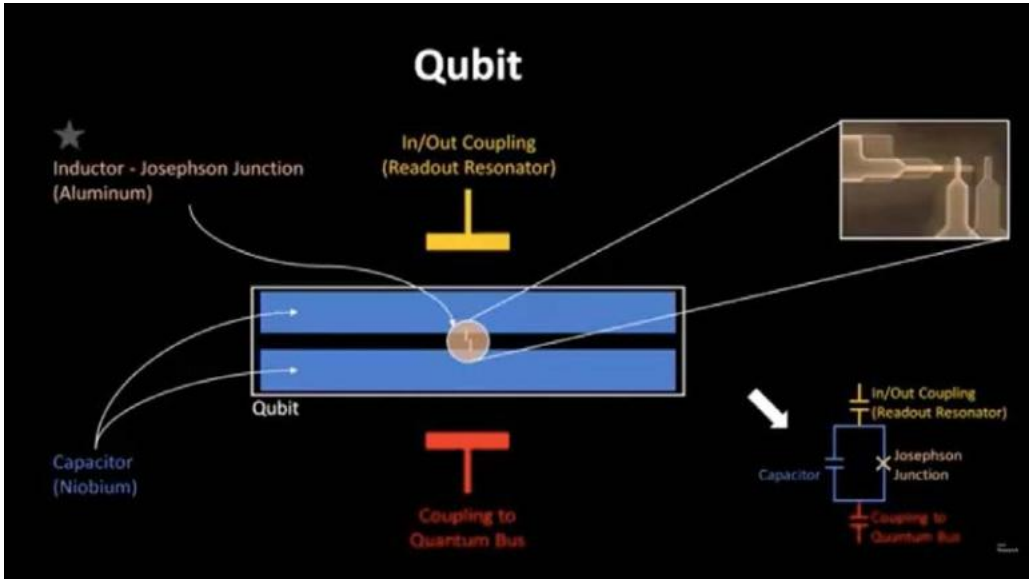
Electrical crossovers (top) require three dimensions, but optical crossovers (bottom) require only two dimensions because light beams do not interact

Quantum computer



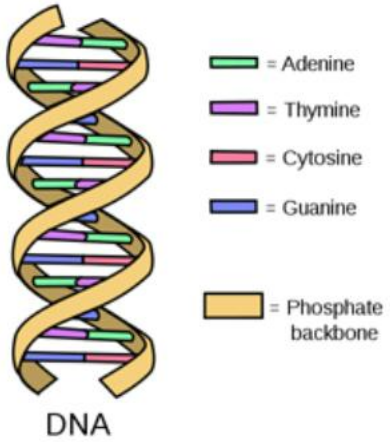


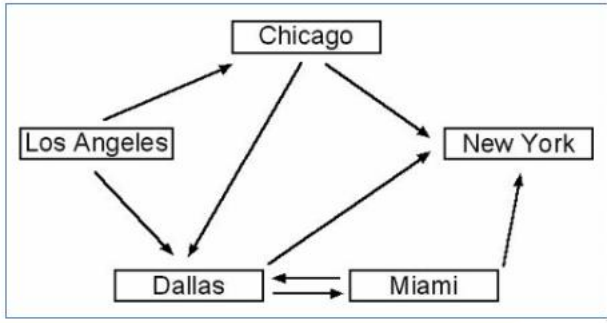
Superconducting Circuits for making of Qbits



Qbits or quantum bits exist in a state of superposition, meaning they can be in two states at once, rather being restricted to a single binary state. This allows quantum computing systems to be exponentially more powerful thanclassical computers and could potentially solve computing challenges that are far beyond thereach of today's fastest supercomputers.

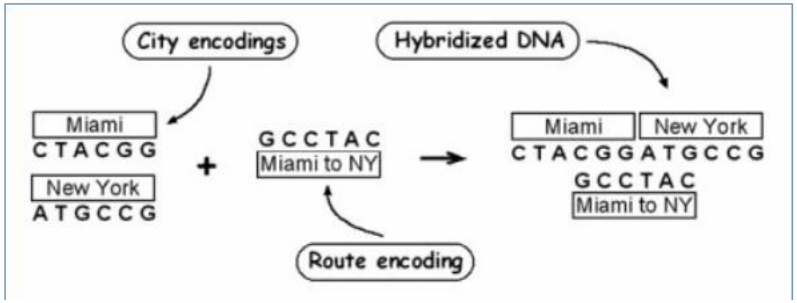
DNA computer

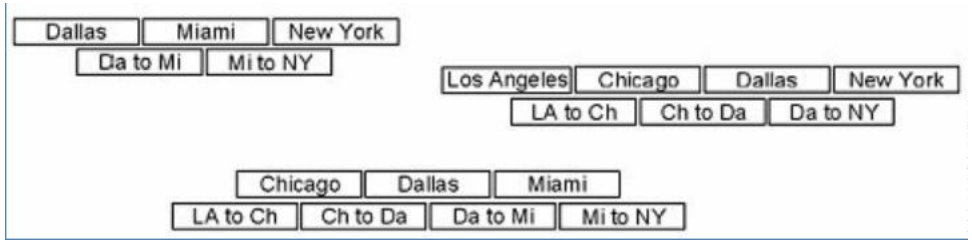


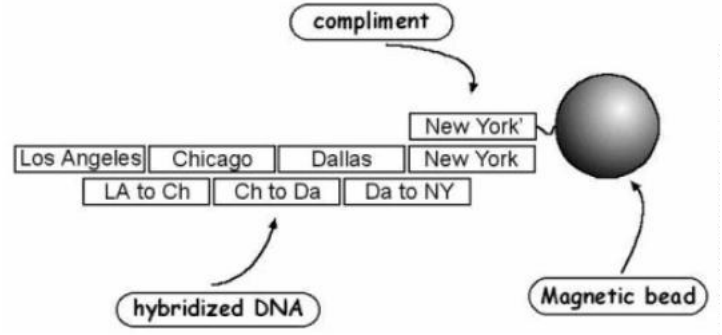


DNA based computer uses DNA (deoxyribonucleic acids) to store information and simultaneously perform complex calculations with low power consumption.

DNA computing was first proposed by Leonard Adelman in 1994, to solve what is known as the "travelling salesman problem" -determining the shortest path that joins a number of geographically separated locations.

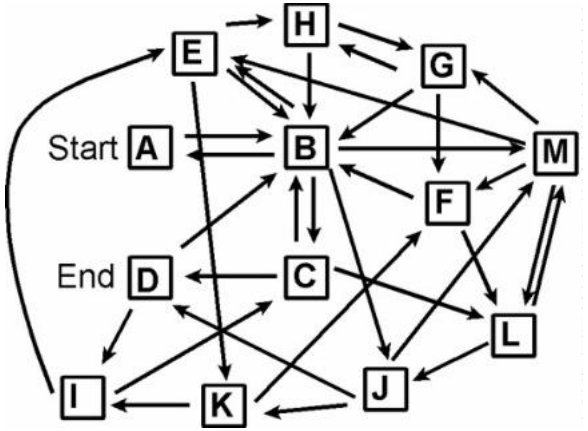






A very complex Hamiltonian path problem (NP-hard problem)

Can you go from node A to node D using only the paths shown such that you visit all the nodes exactly once?

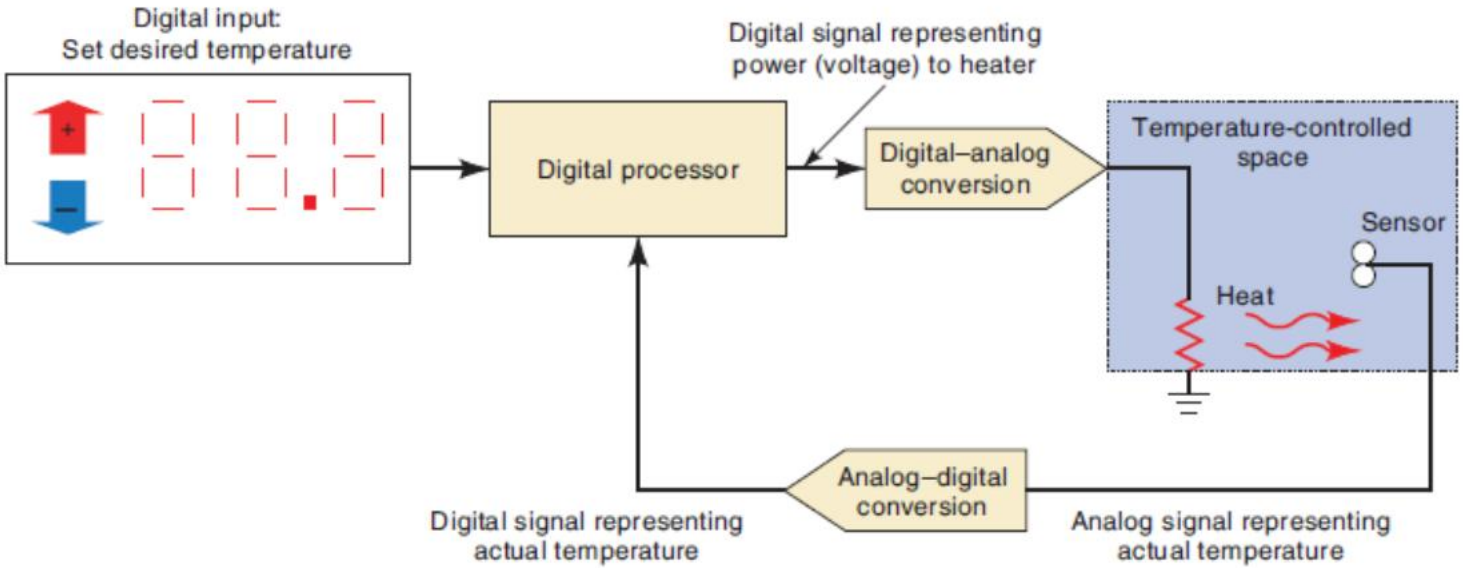


Digital system techniques

1. Convert the physical variable to an electrical signal (analog).
2. Convert the electrical (analog) signal into digital form.
3. Process (operate on) the digital information.
4. Convert the digital outputs back to real-world analog form.

Limitations:

1. The real world is analog and digitizing always introduces some error.
2. Processing digitized signals takes time.

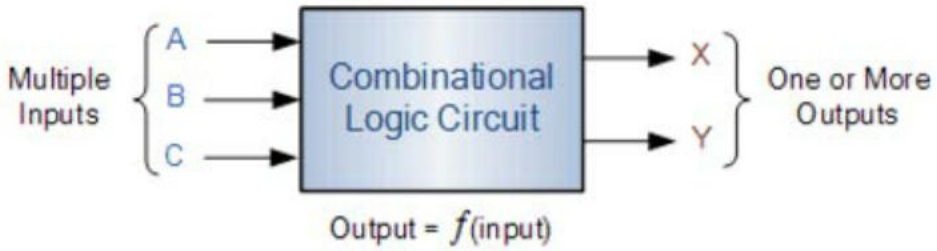


A digital temperature control system

Neal S. Widmer, Gregory L. Moss, and Ronald J. Tocci. Digital Systems: Principles and Applications, 12th ed. Pearson Education, Inc. 2017.

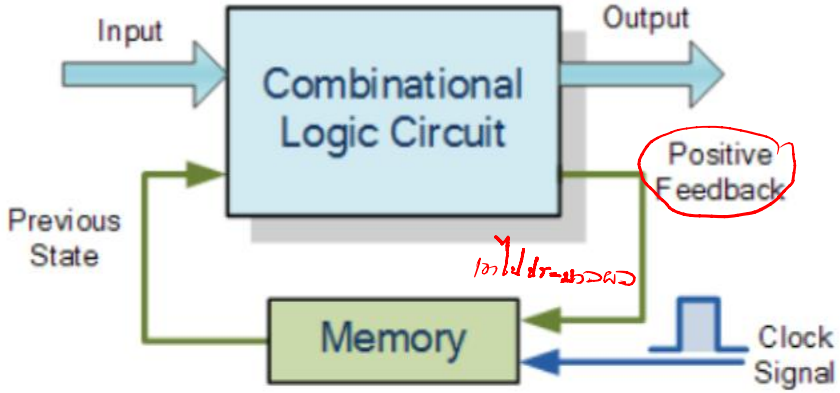
Combinational and Sequential logic circuits

Combinational logic circuits



The outputs are only determined by the logical function of their <u>current input</u> state, logic “0” or logic “1”, at any given instant in time.

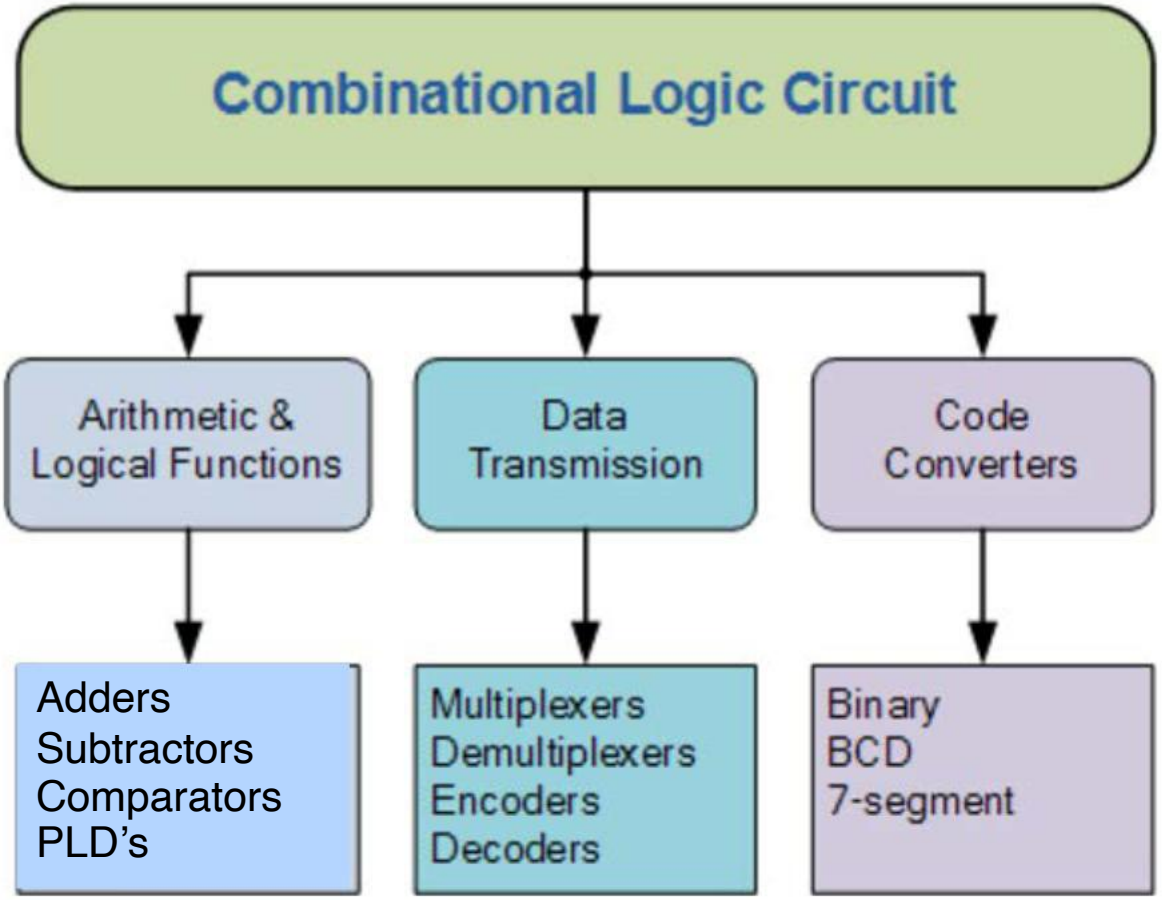
Sequential logic circuits



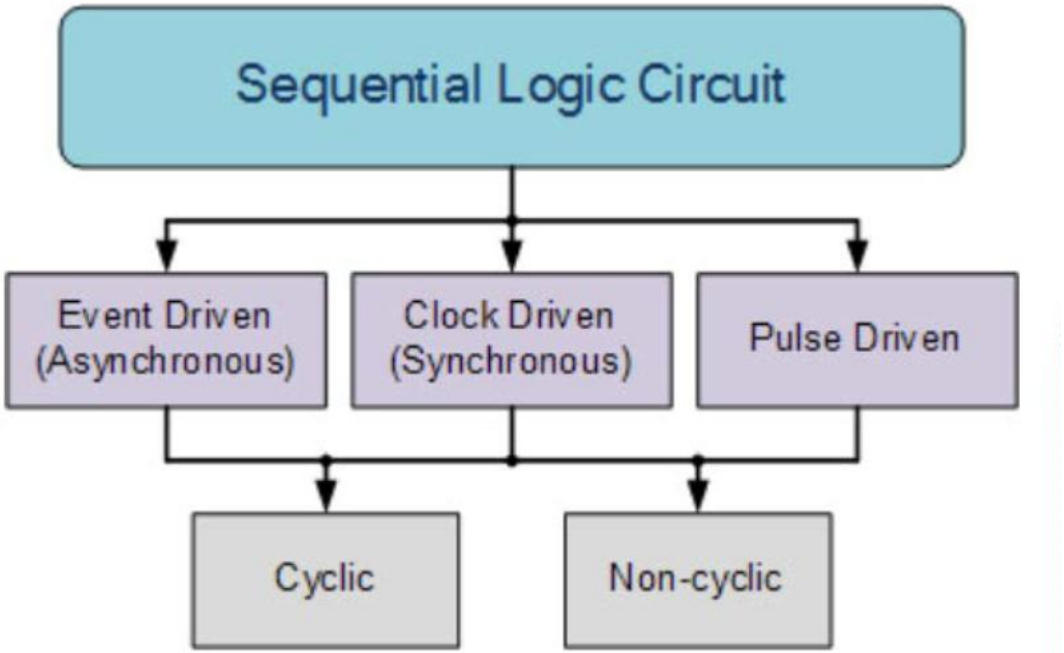
The outputs are dependent on both their <u>present inputs</u> and their <u>previous output</u> state giving them some form of memory.

The clock signal determines when things will happen next.

Classification of combinational logic circuits



Classification of sequential logic circuits



Event Driven: asynchronous circuits that change state immediately when enabled.

Clock Driven: synchronous circuits that are synchronized to a specific clock signal.

Pulse Driven: a combination of the two that responds to triggering pulses.

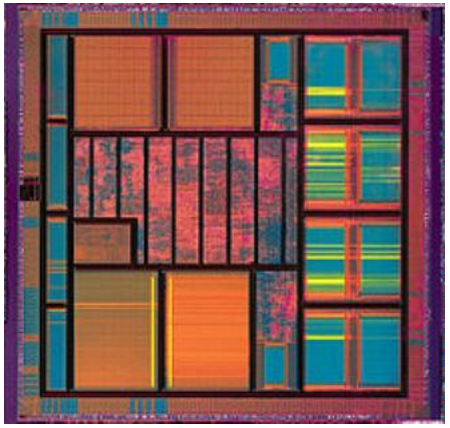
Sequential logic circuits return back to their original steady state once reset.

Sequential circuits with loops or feedback paths are said to be “cyclic” in nature.

Digital integrated circuits (ICs)

Digital ICs are a collection of resistors, diodes, and transistors fabricated on a single piece of semiconductor material (usually silicon) called a substrate, which is commonly referred to as a chip.

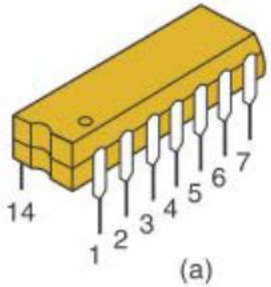
The chip is enclosed in a protective plastic or ceramic package from which pins extend for connecting the IC to other devices.



A VLSI integrated-circuit die

Complexity	Gates per Chip
Small-scale integration (SSI)	Fewer than 12
Medium-scale integration (MSI)	12–99
Large-scale integration (LSI)	100–9999
Very large-scale integration (VLSI)	10,000–99,999
Ultra large-scale integration (ULSI)	100,000–999,999
Giga-scale integration (GSI)	1,000,000 or more

Dual-in-line package (DIP)



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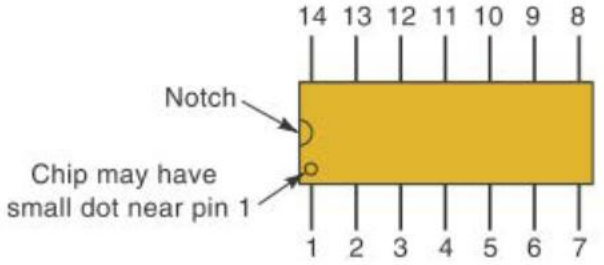
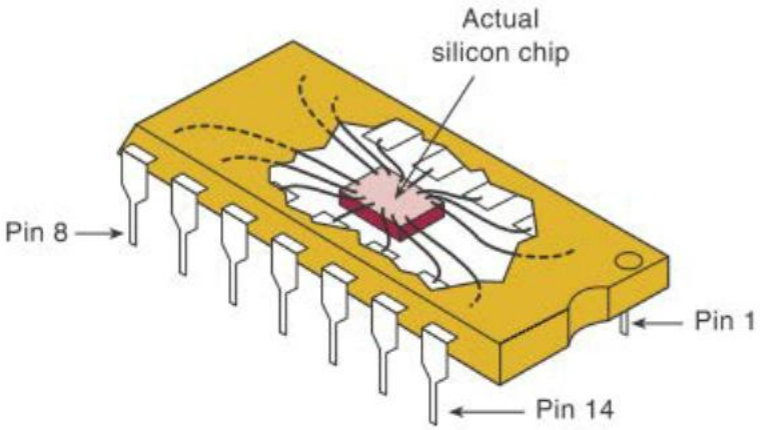
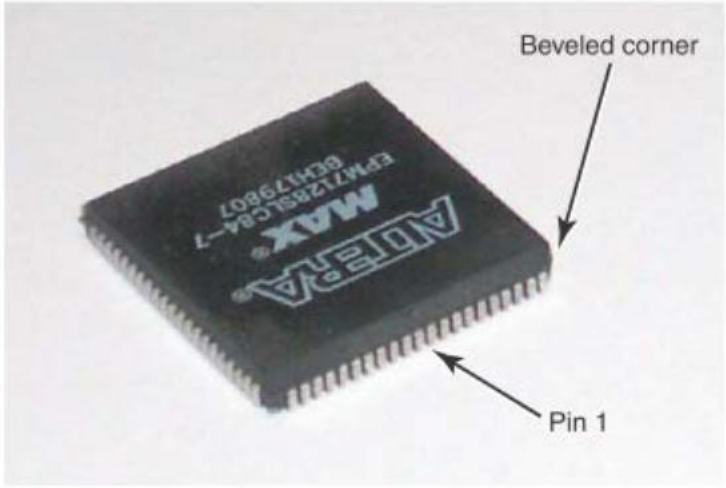


(b)





Transistor technologies for digital circuits

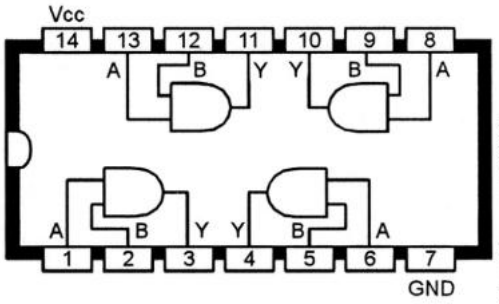
Today the most common technology used to implement digital circuits (including the vast majority of computer hardware) is complementary metal-oxide semiconductor (CMOS).

The other technology uses bipolar junction transistors (BJTs). The major logic family that sprung from bipolar technology is

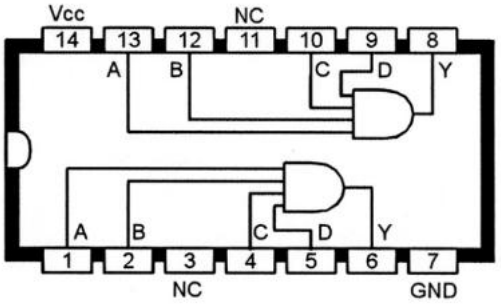
referred to as TTL (transistor/transistor logic).

Seven popular AND gate ICs.

Device	Type	Description
74LS08	LS TTL	Quad 2-input AND gate
74HC08	CMOS	Quad 2-input AND gate
4081B	CMOS	Quad 2-input AND gate
74LS11	LS TTL	Triple 3-input AND gate
4073B	CMOS	Triple 3-input AND gate
74LS21	LS TTL	Dual 4-input AND gate
4082B	CMOS	Dual 4-input AND gate

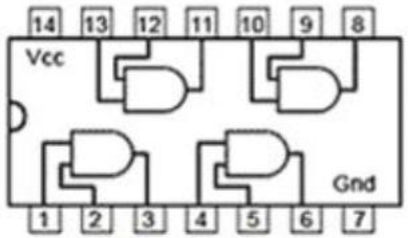


4081B

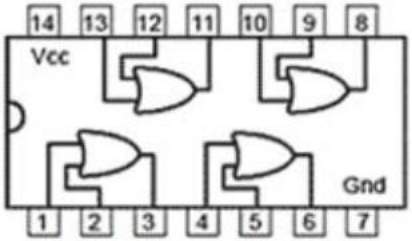


74LS21

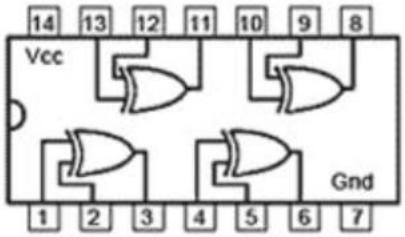
Logic gates from the 7400-series TTL IC Family



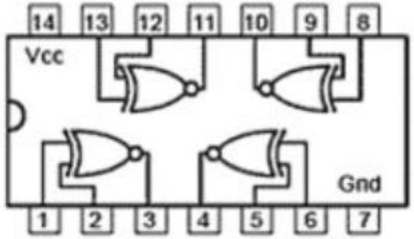
7408 Quad 2 input AND Gates



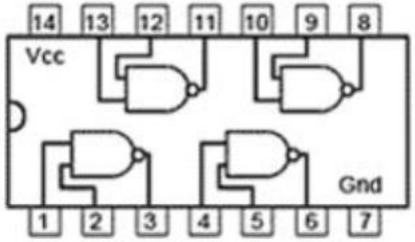
7432 Quad 2 input OR Gates



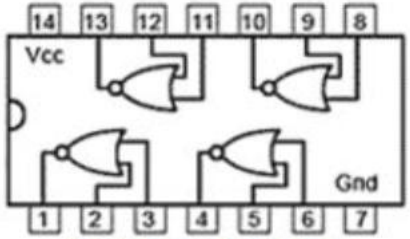
7486 Quad 2 input XOR Gates



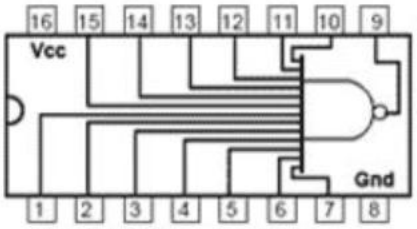
747266 Quad 2 input XNOR Gates



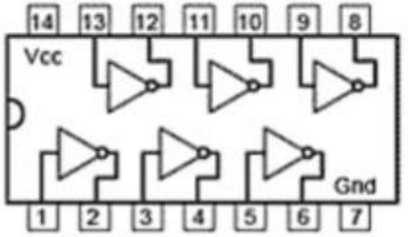
7400 Quad 2 input NAND Gates



7402 Quad 2 input NOR Gates

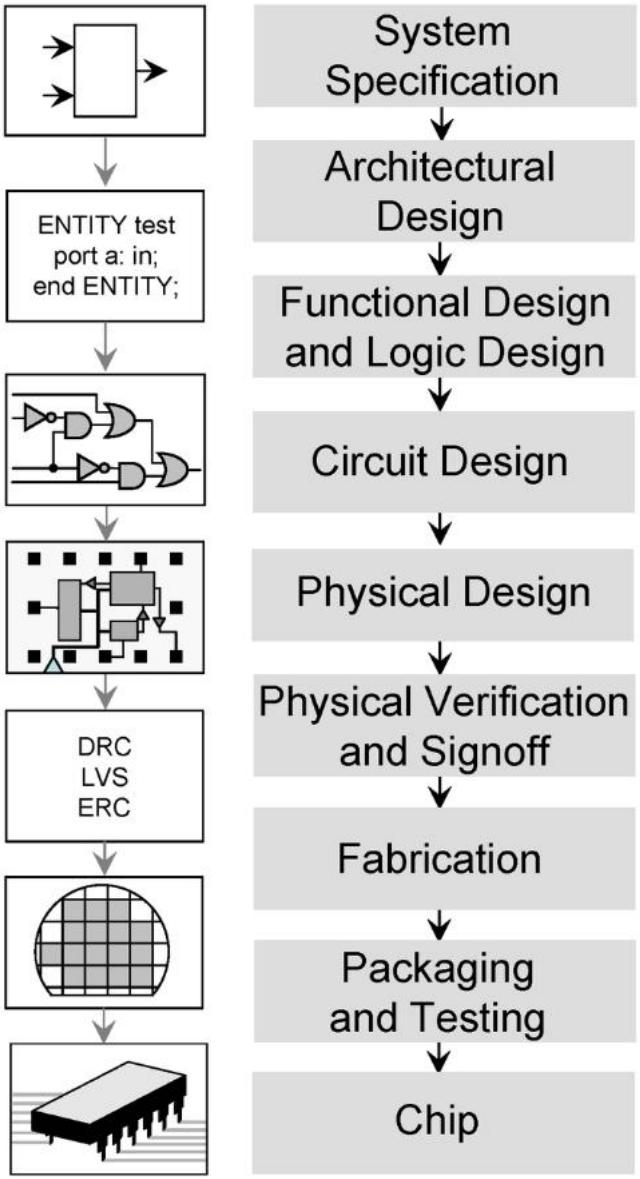


74133 Single 13 input NAND Gate



7404 Hex NOT Gates (Inverters)

Major steps in IC design

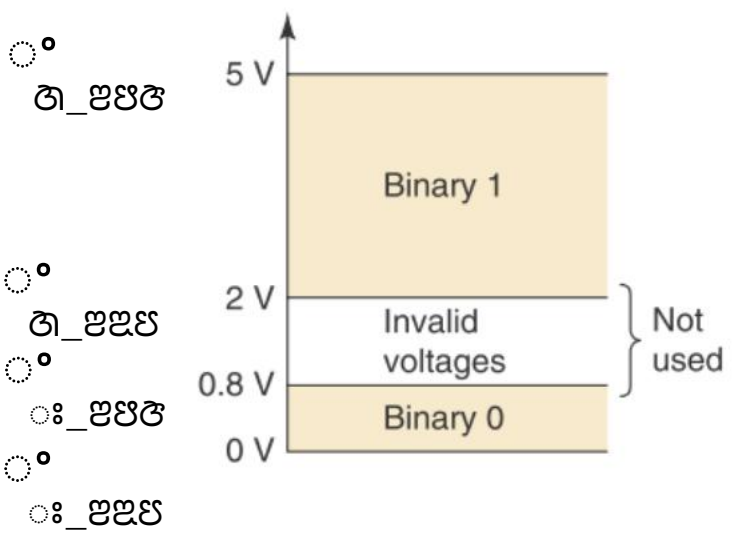


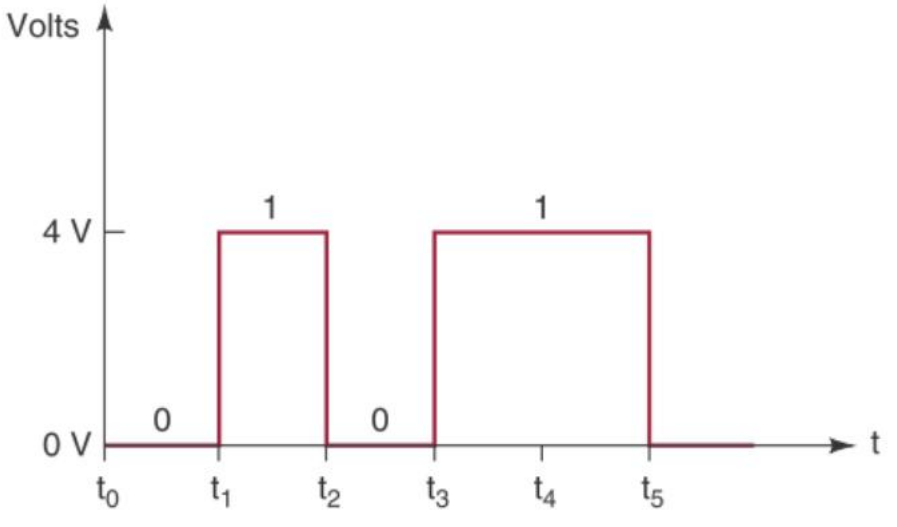
Introduction to 1's and 0's

Digital circuits observe the state of each component and make a "logical" decision. These conditions are often referred to as logic states.

For a positive logic system, logic 0 is represented by the LOW voltage (close to 0 V) levels and logic 1 is represented by the HIGH voltage levels.

Defined threshold voltages





Example: A 5-V logic system based on BJT technology

Positive and negative logic systems

V_{x_1}	V_{x_2}	V_f
L	L	L
L	H	L
H	L	L
H	H	H

(a) Voltage levels

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

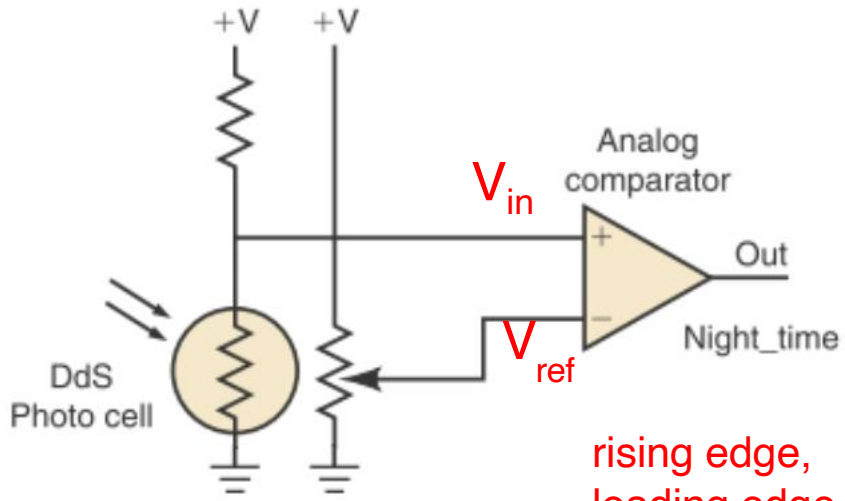
(b) Positive logic

x_1	x_2	f
1	1	1
1	0	1
0	1	1
0	0	0

(c) Negative logic

Digital signals

Example of a digital system: a light sensor that is intended to turn on the streetlights at night



Light = Low
Dark = High

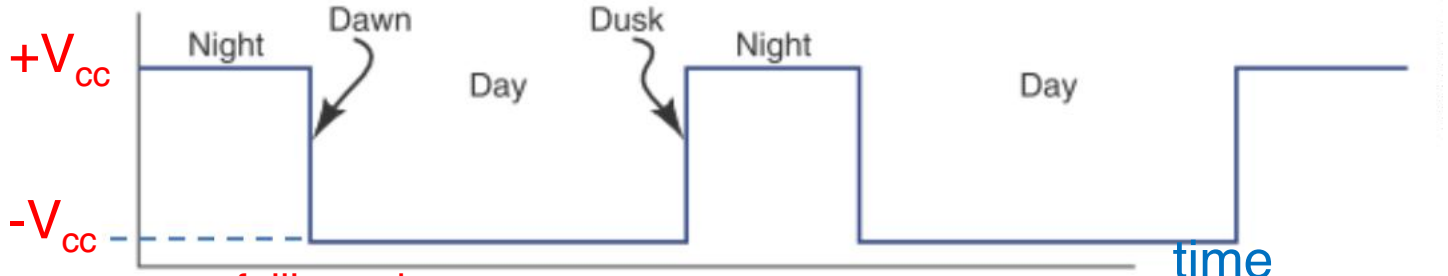
Logic 0 (LOW)

Logic 1 (HIGH)

(a)

rising edge, leading edge, positive edge

voltage or logic level



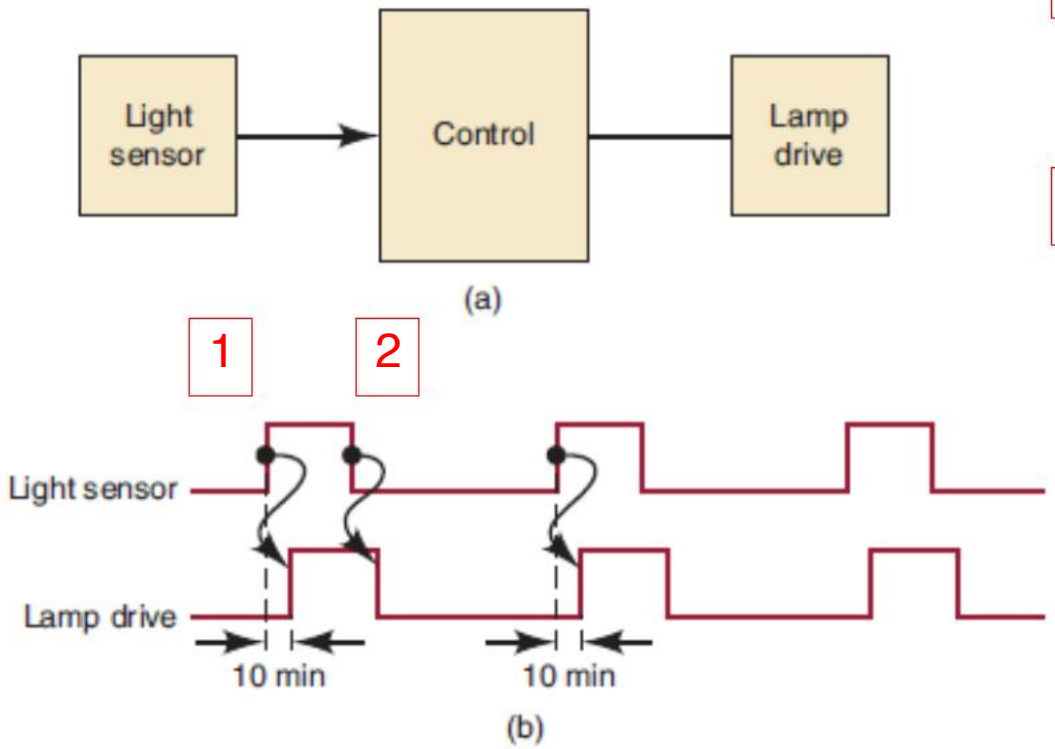
falling edge, trailing edge, negative edge

(b) "The timing diagram"

Timing diagrams with input and output

The logic states must be observed over time.

Timing diagrams show the relationship between changes at the input and changes at the output in order to demonstrate the operation of the system over time.



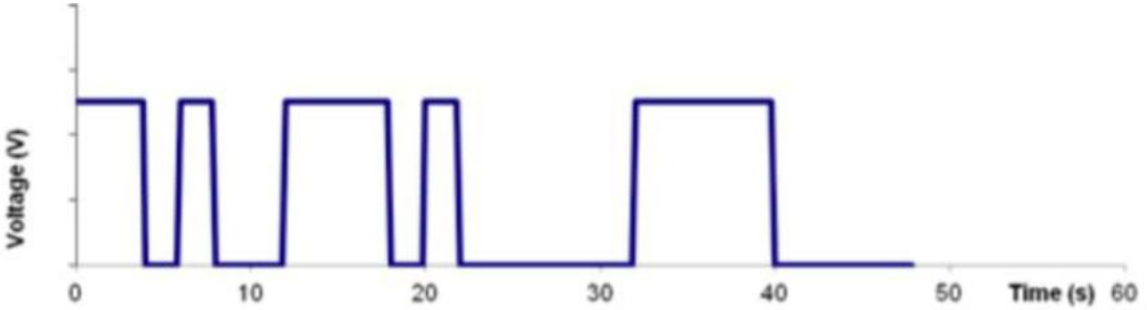
1 detects the “edge” at dusk
à waits 10 min
à turns on the streetlamp

2 detects the “edge” at dawn
à waits 10 min
à turns off the streetlamp

The curvy arrows are used to indicate the cause-and-effect relationship between input and output signals.

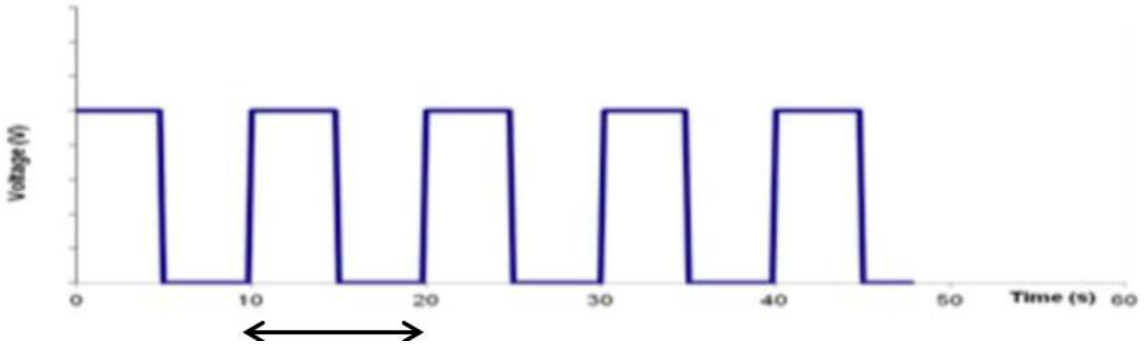
Types of digital waveforms and parameters

An aperiodic digital signal:



A periodic digital signal:

The signal repeats itself at regular intervals.



T: period

In a periodic signal, each repetition is called a cycle.

$$f = \frac{1}{T}$$

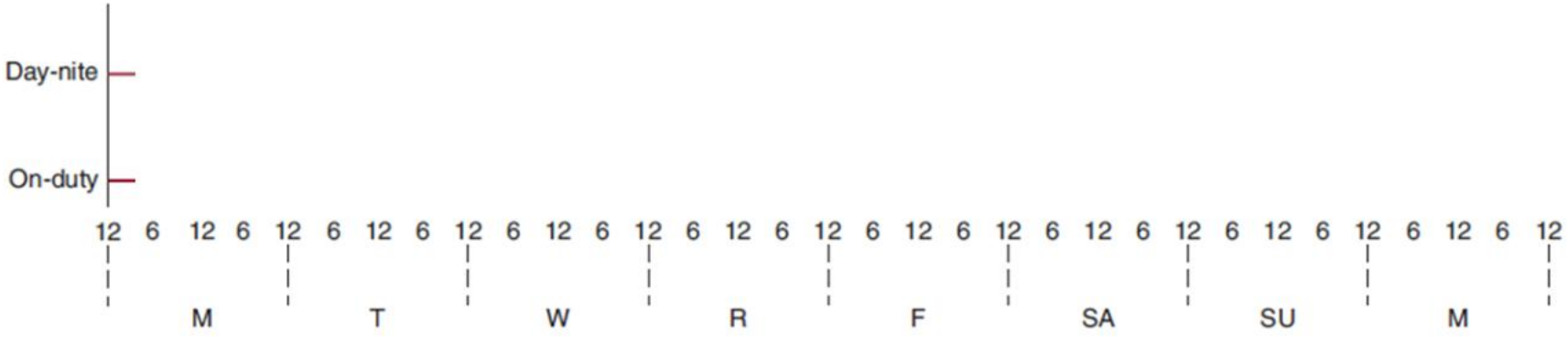
The time requires for one cycle is called a signal's period.

A signal's frequency is the number of cycles that occur in one second.

Example: periodic/aperiodic

1. Draw a timing diagram showing when a person is “on duty” over an entire week. Begin on Monday morning. The diagram will have one input representing the day/night cycle (assume equinox where length of day = length of night dawn 6:00 am, dusk 6:00 pm) and one output which goes HIGH representing when a person in “on duty.” Assume they work a typical 8am – 5pm job Monday to Friday with Saturday and Sunday off.

Answer:

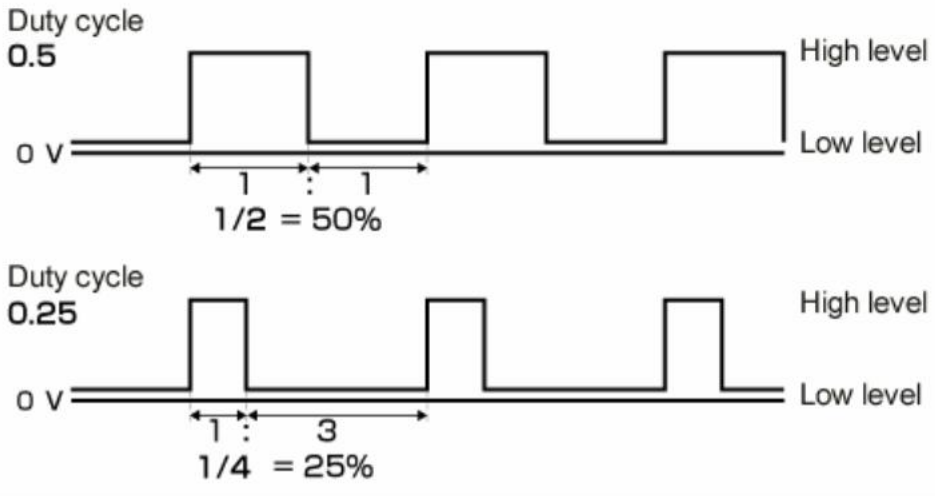


2. Determine the types (periodic/aperiodic) of the “day-nite” and “on_duty” digital waveforms.

Answer:

Duty cycle

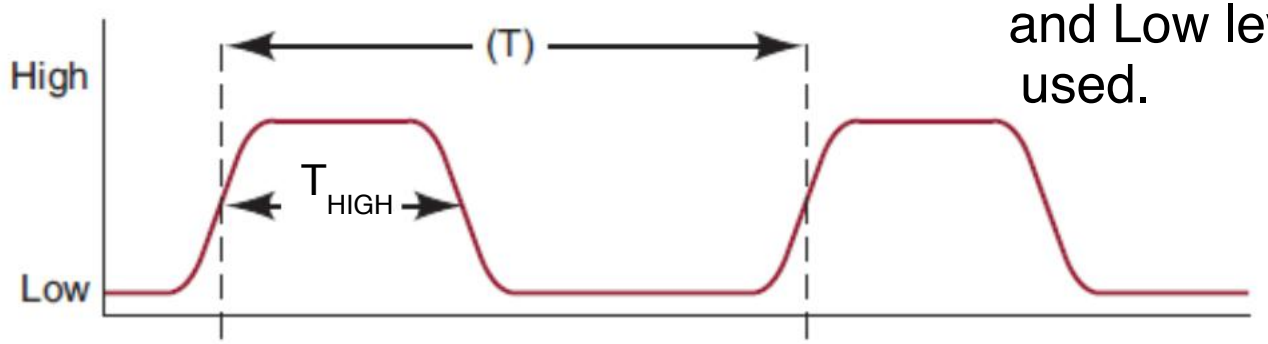
The duty cycle is used to indicate how much of the time a digital signal is in its "active" state.



Considering active HIGH:

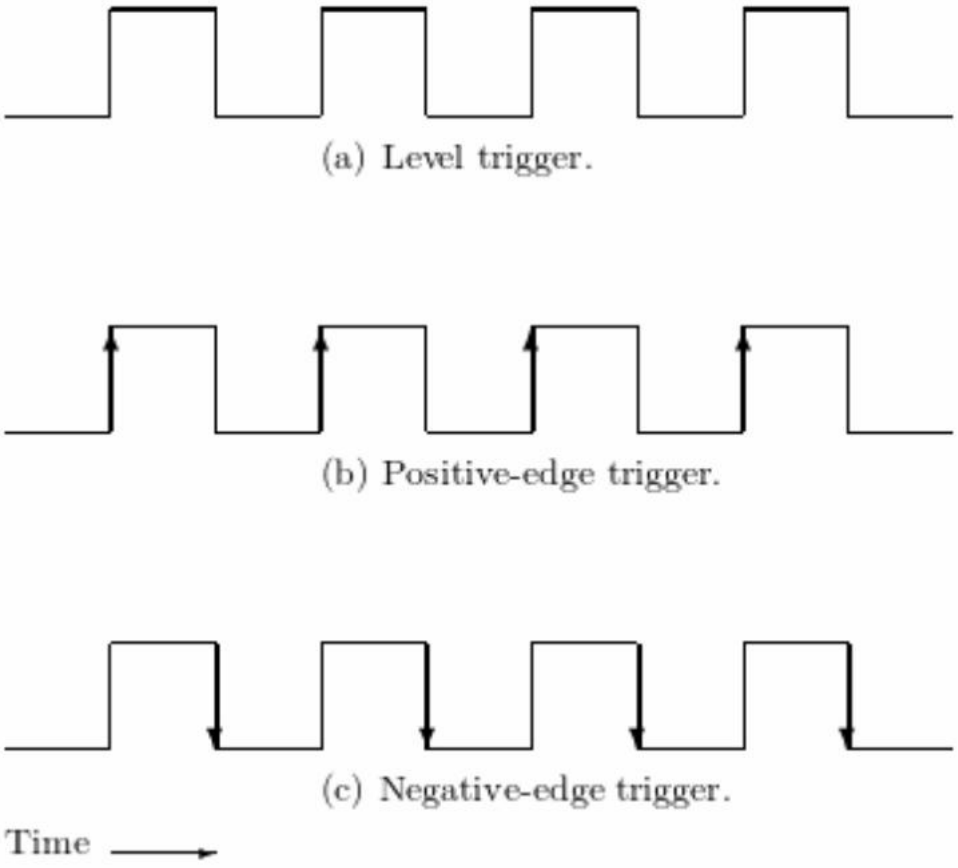
$$\text{Duty cycle (\%)} = \frac{T_{HIGH}}{T} \times 100$$

When there is some transition time, 50% point between High and Low level of the signal is used.



50% point

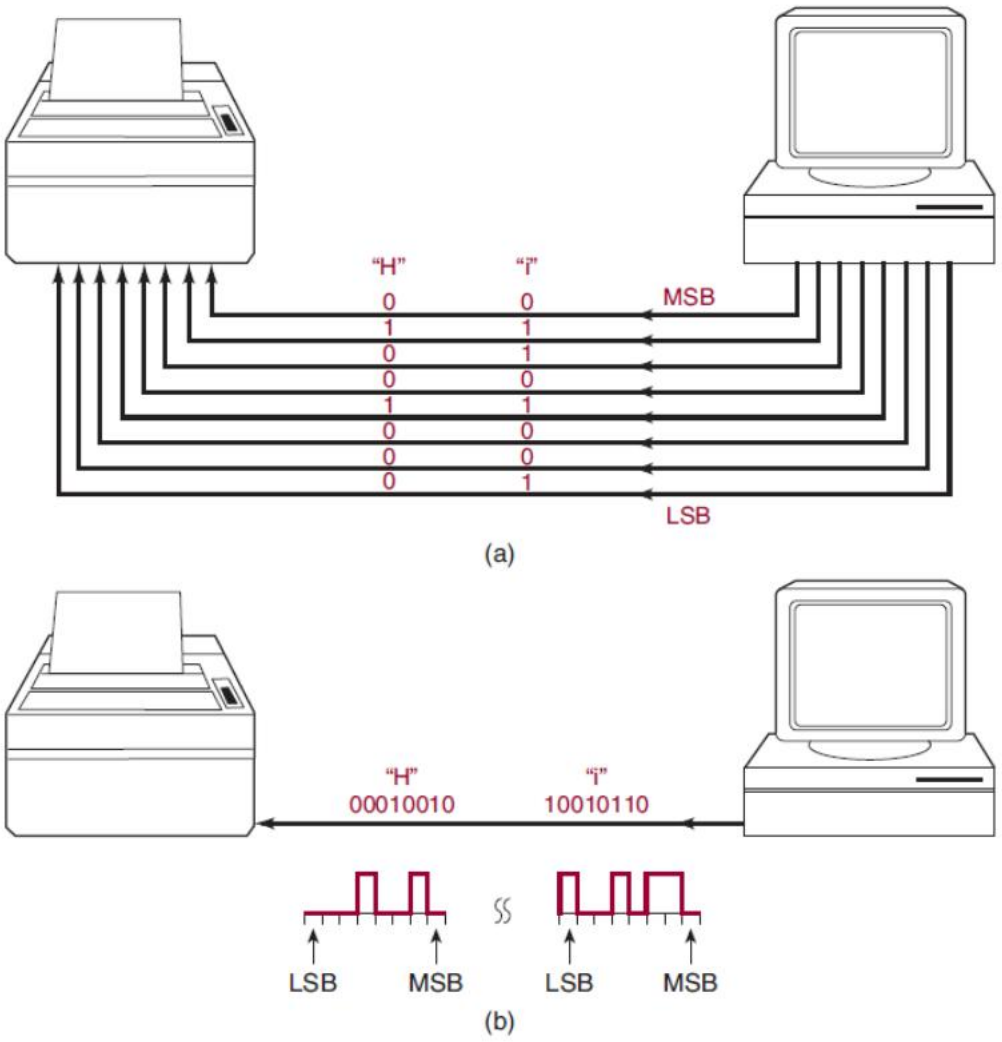
Trigger modes



Level trigger

Edge trigger

Parallel and serial transmission



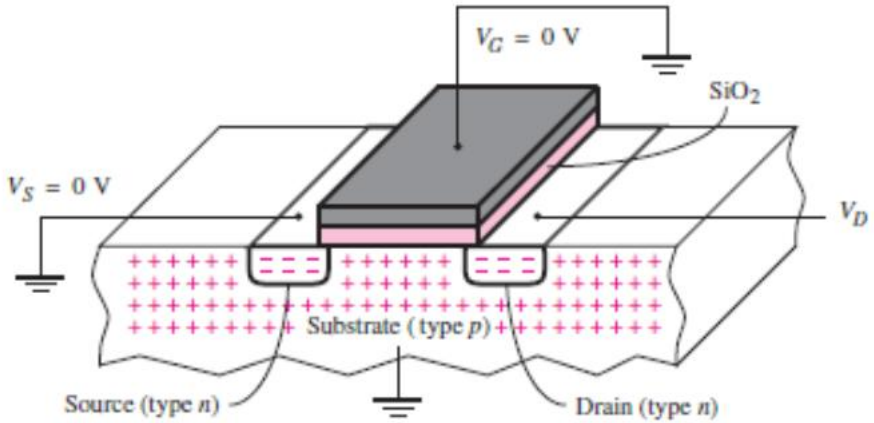
Parallel transmission

uses one connecting line per bit, and all bits are transmitted simultaneously.

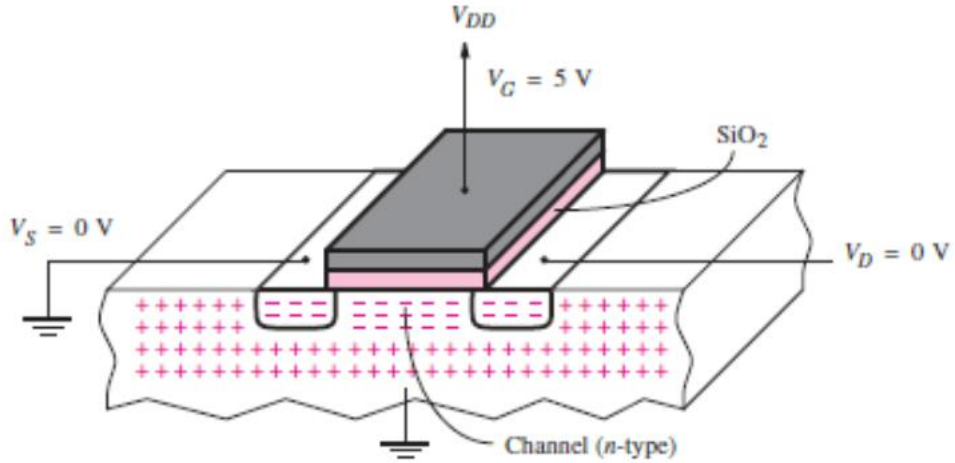
Serial transmission

uses only one signal line, and the individual bits are transmitted serially (one at a time).

Physical structure of an NMOS transistor



(a) When $V_{GS} = 0$ V, the transistor is off

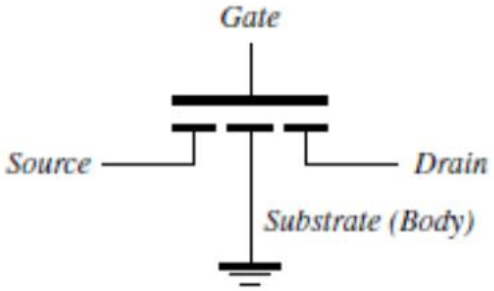


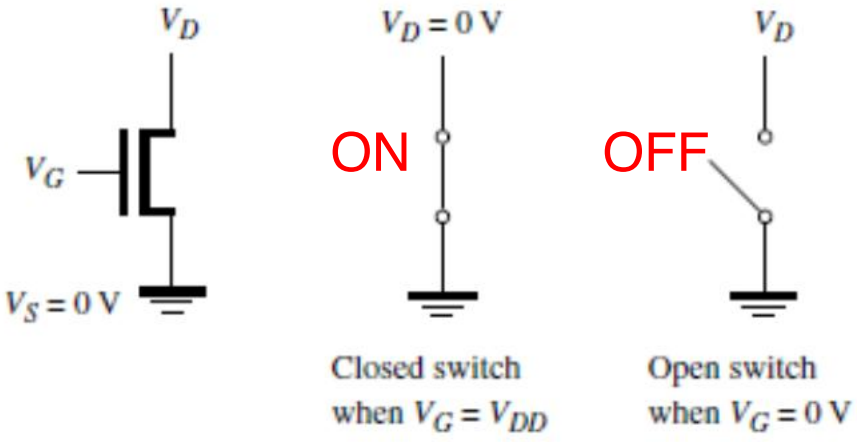
(b) When $V_{GS} = 5$ V, the transistor is on

The behavior of PMOS transistors is the same as for NMOS except that all voltages and currents are reversed.

Transistor switches

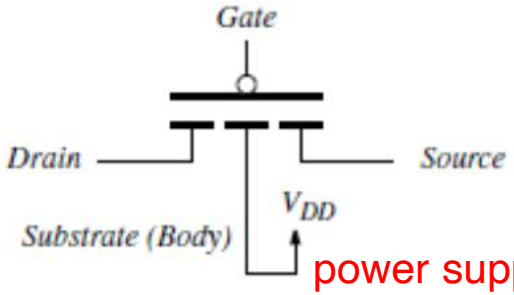
NMOS transistor



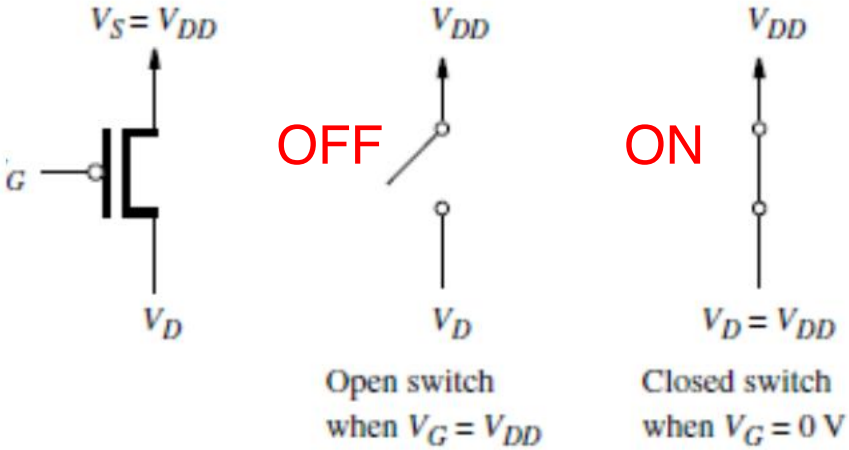


When the NMOS transistor is turned ON, is turned ON, its drain is pulled down to ground.

PMOS transistor

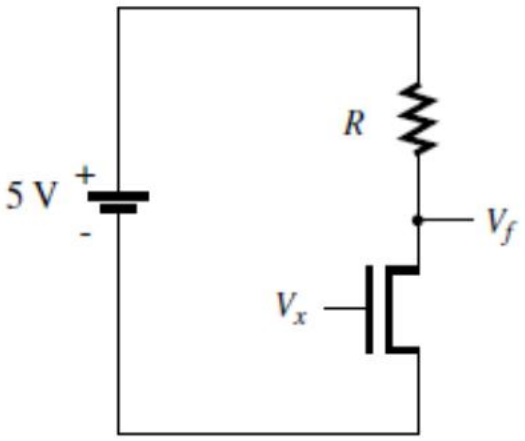


power supply voltage

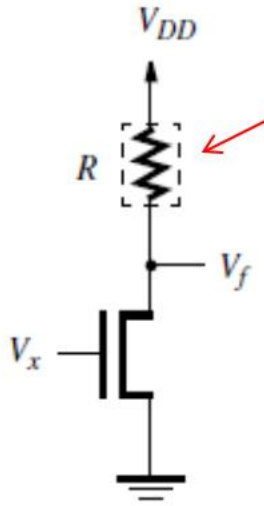


When the PMOS transistor ts drain is pulled up to V_{DD}.

NMOS logic gates: NOT gate or inverter



(a) Circuit diagram



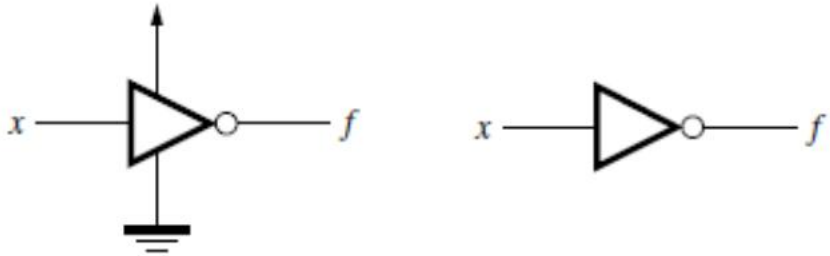
(b) Simplified circuit diagram

used to limit the amount of current that flows

$V_x = 0\ \text{V} \longrightarrow V_f = 5\ \text{V}$

$V_x = 5\ \text{V} \longrightarrow V_f \approx 0\ \text{V}$

power terminal



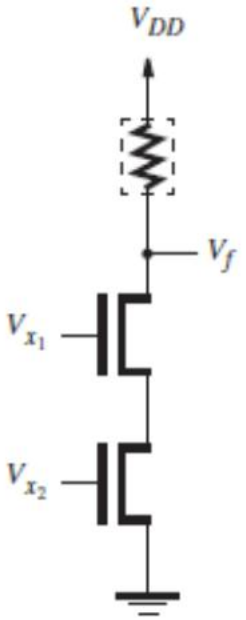
(c) Graphical symbols

Boolean expression:

$$f = \bar{x}$$

Figure B.5 A NOT gate built using NMOS technology.

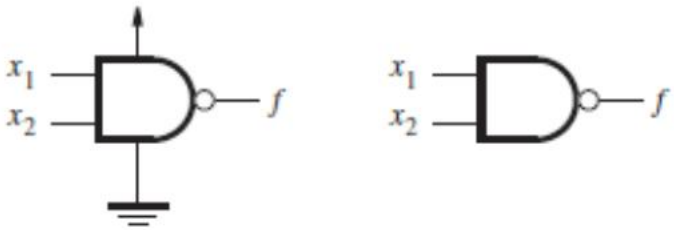
NMOS logic gates: NAND gate



(a) Circuit

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table



(c) Graphical symbols

Figure B.6 NMOS realization of a NAND gate.

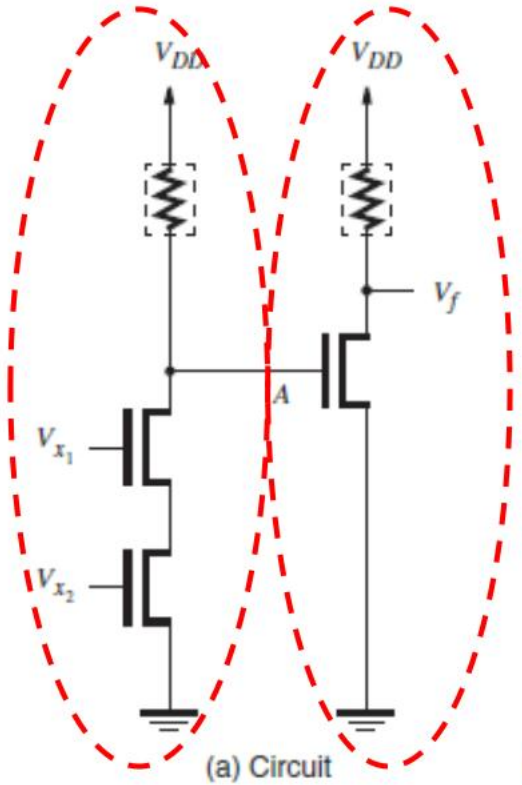
Boolean expression:

$$f = \overline{x_1 x_2}$$

NMOS logic gates: AND gate

NAND

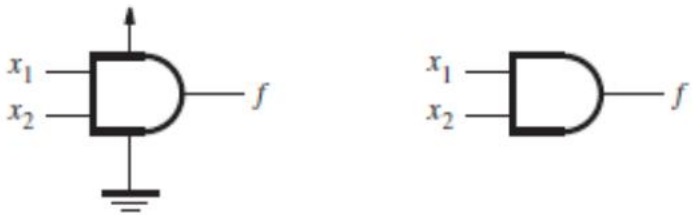
NOT



(a) Circuit

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



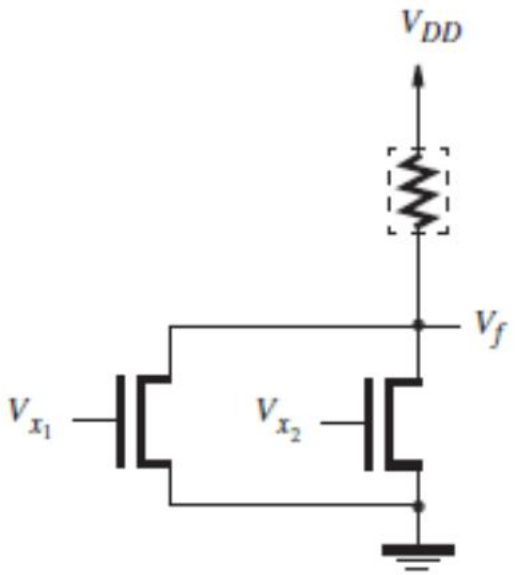
(c) Graphical symbols

Boolean expression:

$$f = x_1 x_2$$

Figure B.8 NMOS realization of an AND gate.

NMOS logic gates: NOR gate



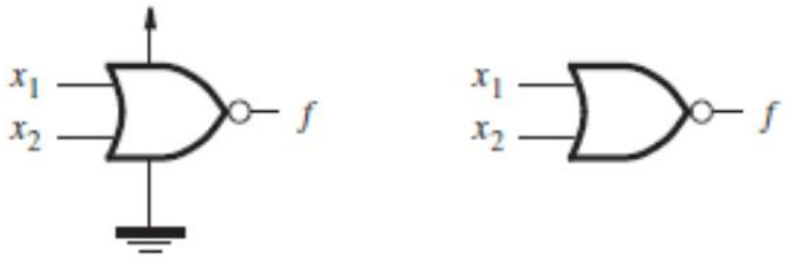
(a) Circuit

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table

Boolean expression:

$$f = \overline{x_1 + x_2}$$



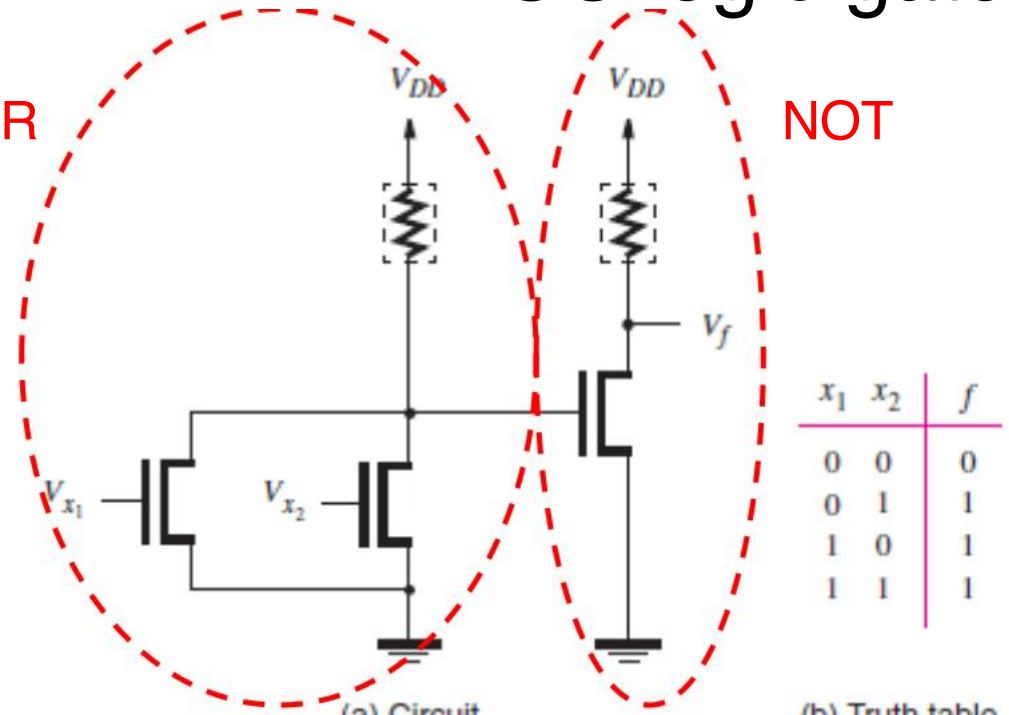
(c) Graphical symbols

Figure B.7 NMOS realization of a NOR gate.

NMOS logic gates: OR gate

NOR

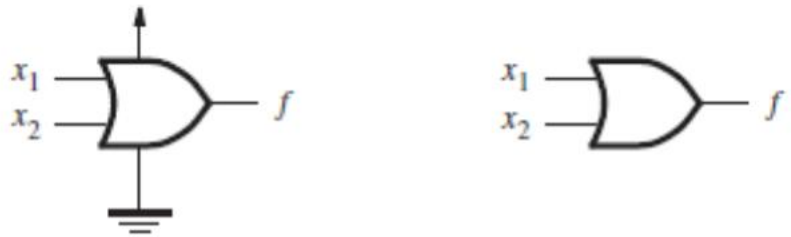
NOT



(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



(c) Graphical symbols

Figure B.9 NMOS realization of an OR gate.

Boolean expression:

$$f = x_1 + x_2$$

Complementary MOS (CMOS) transistor logic gate circuits

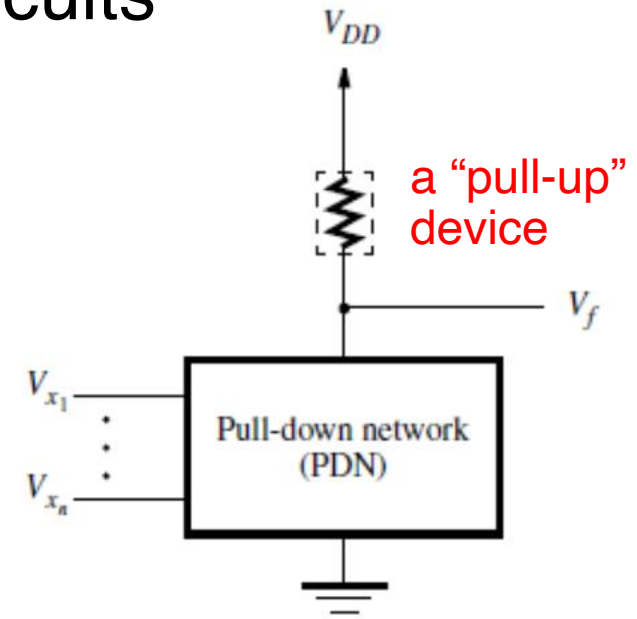


Figure B.10 Structure of an NMOS circuit.

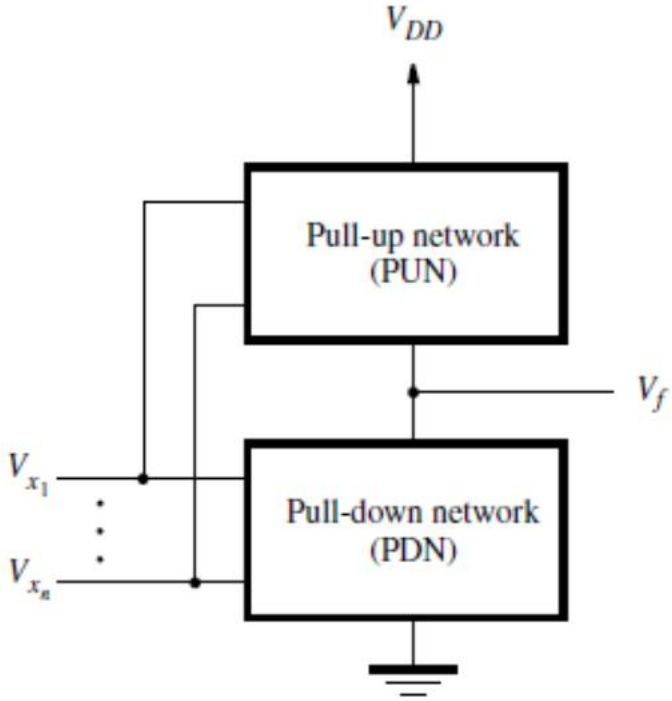


Figure B.11 Structure of a CMOS circuit.

The concept of CMOS circuits is based on replacing the pull-up device with a pull-up network (PUN) that is built using PMOS transistors, such that the functions realized by the PDN and PUN networks are complements of each other.

For any given valuation of the input signals, either the PDN pulls V_f down to Gnd or the PUN pulls V μp to V_{DD}

Structure of a CMOS logic circuit

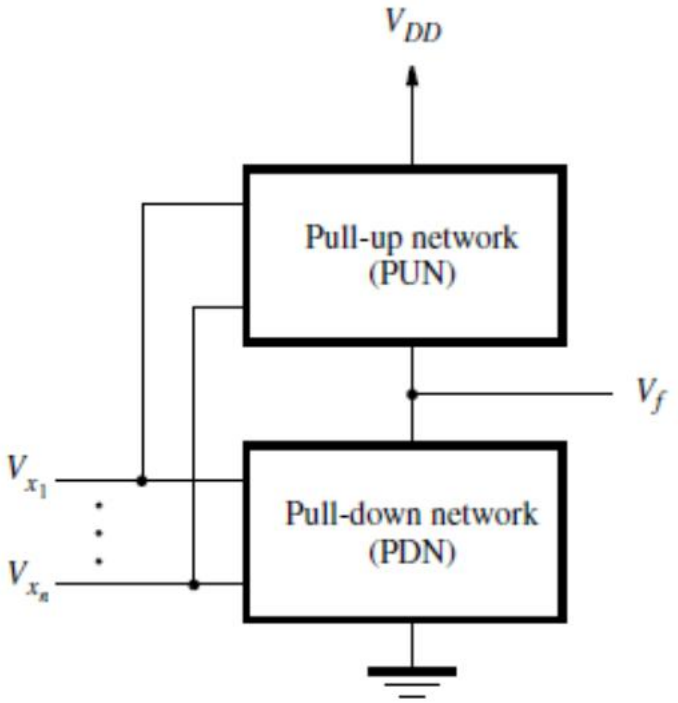


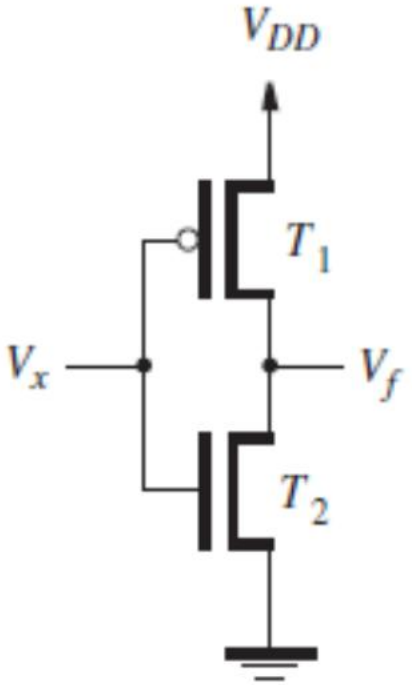
Figure B.11 Structure of a CMOS circuit.

Criteria for CMOS logic circuit construction:

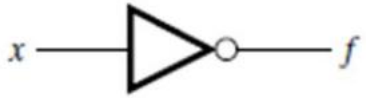
1. The PDN and the PUN must have equal numbers of transistors, which are arranged so that the two networks are duals of one another.

2. Wherever the PDN has NMOS transistors in series, the PUN has PMOS transistors in parallel, and vice versa. (The two networks are complements of each other.)

CMOS logic gates: NOT gate



(a) Circuit



Note that no current flows in a CMOS inverter
when the input is either low or high.

x	T_1	T_2	f
0	on	off	1
1	off	on	0

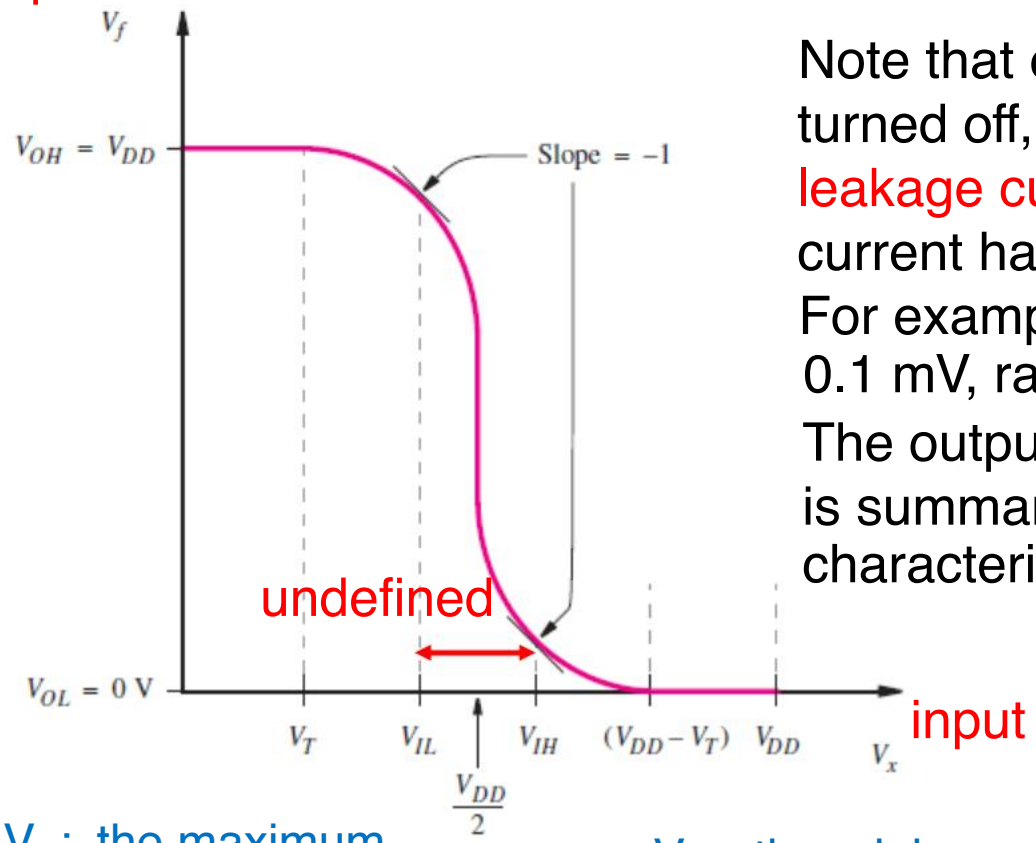
(b) Truth table and transistor states

Consider for all ideal CMOS circuits; no current flows, and hence no power is dissipated under steady state conditions.

This property has led to CMOS becoming the most popular technology in use today for building logic circuits.

The voltage transfer characteristic of the CMOS inverter

output



input

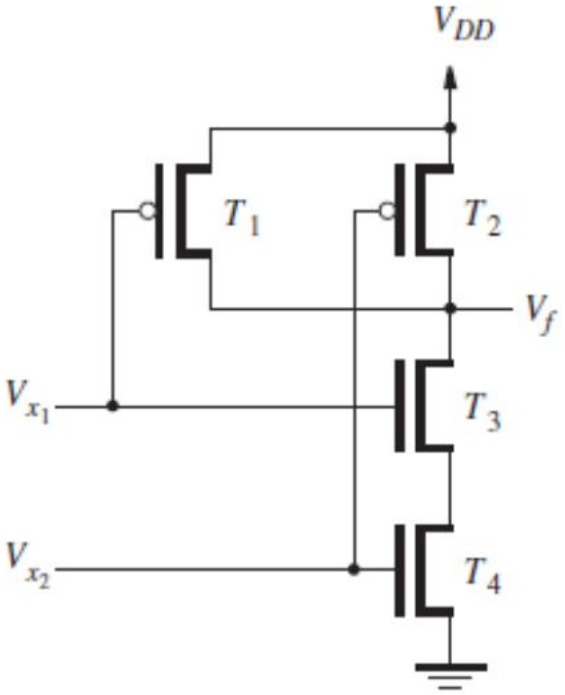
Note that even when a transistor is turned off, a small current, called the leakage current, may flow through it. This current has a slight effect on V_{OH} and V_{OL} . For example, a typical value of V_{OL} is 0.1 mV, rather than 0 V

The output-input voltage relationship is summarized by the voltage transfer characteristic.

V_{IL}: the maximum input voltage level that the inverter will interpret as LOW, hence producing a HIGH output

V_{IH}: the minimum input voltage level that the inverter will interpret as HIGH, hence producing a LOW output

CMOS logic gates: NAND gate

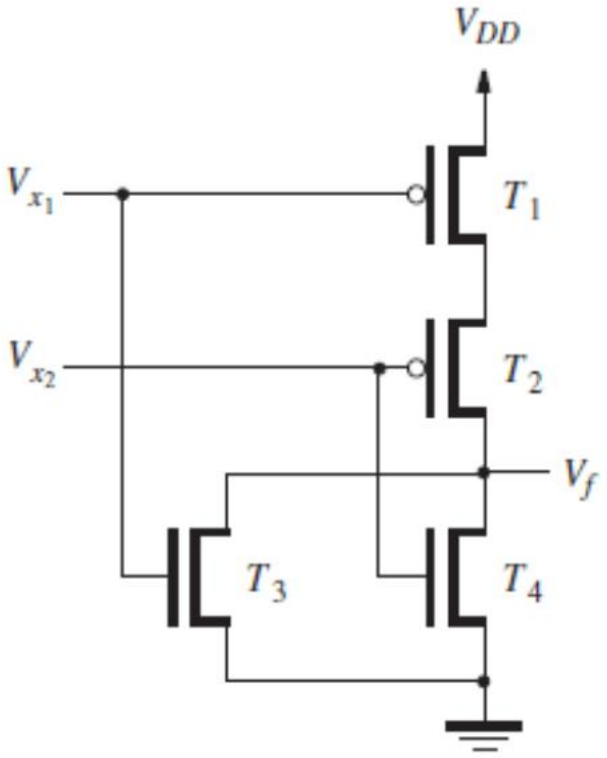


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

CMOS logic gates: NOR gate



(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states