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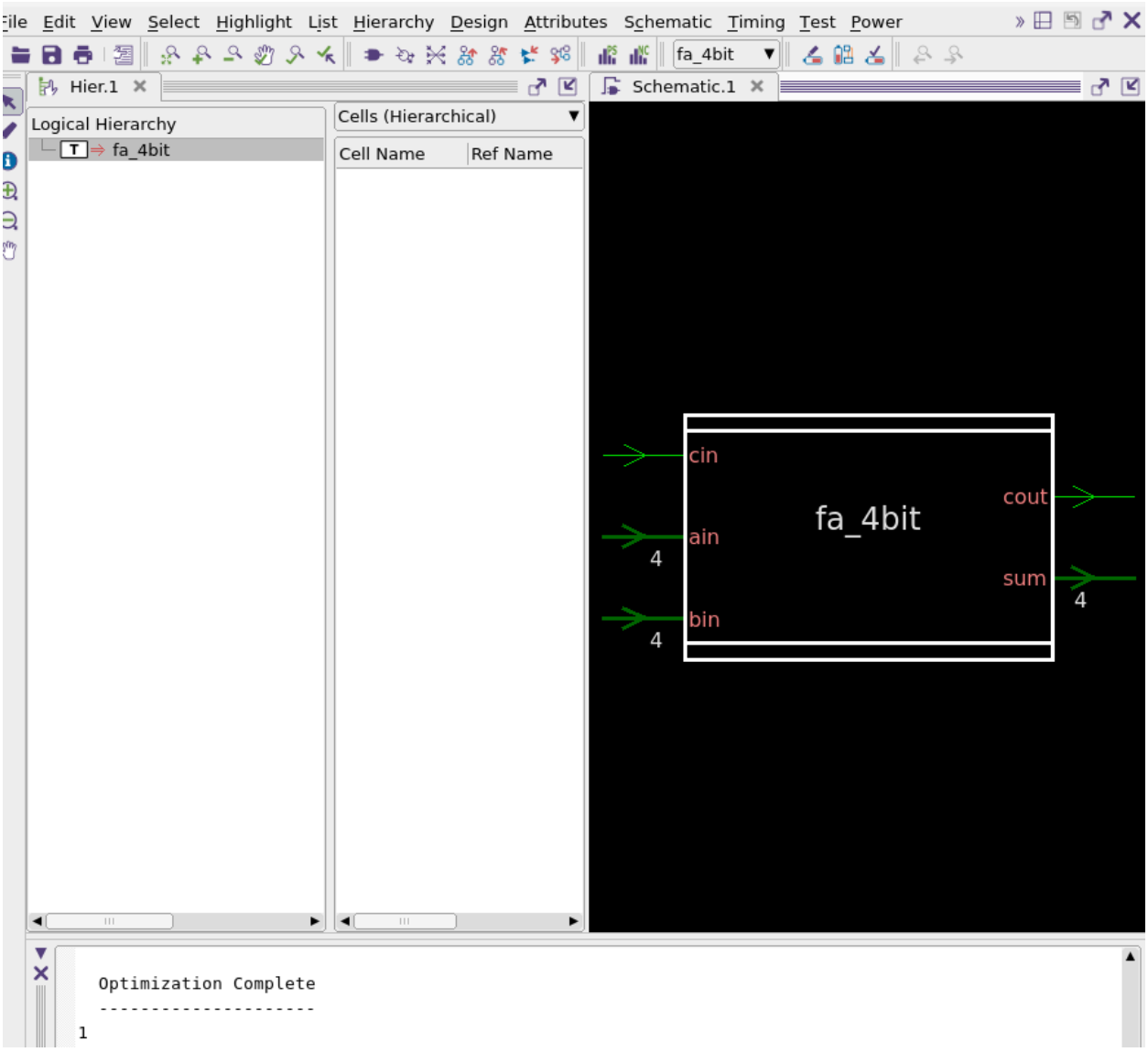
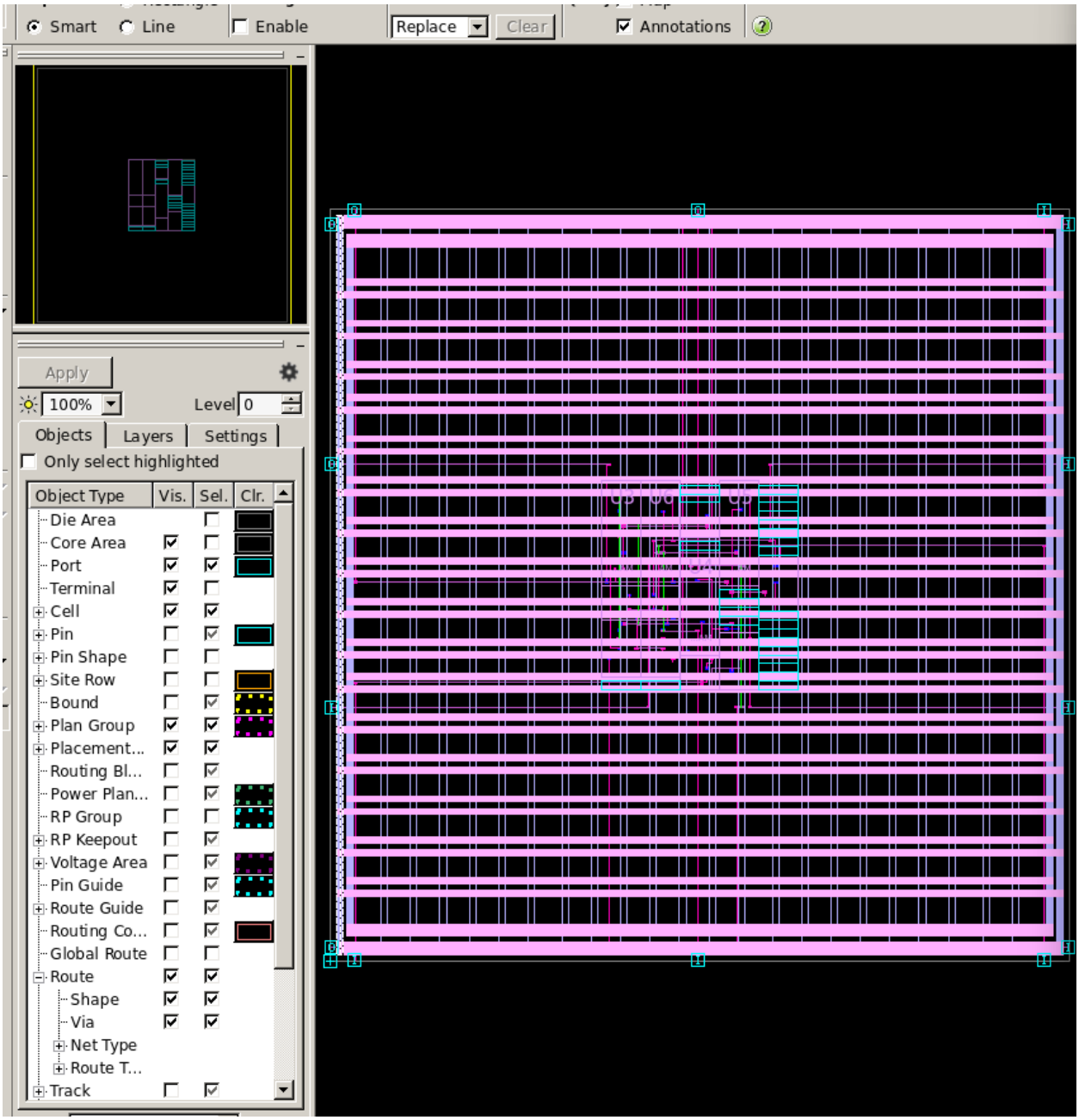
Session 021
Frosales
Frosa009

Summary: For Lab 4 we use Design compiler and IC compiler to simulate Verilog code. WE learn how to setup each environment to accept the files and how to convert them into visual representations of the code. In this lab we create a 4bit full adder and a GCD circuit using this method of simulation.

```
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -m32 -m32 -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-
rpath=./simv.daidir -Wl,-rpath=/usr/local/synopsys/vcs/T-2022.06-1/linux/lib -L/
usr/local/synopsys/vcs/T-2022.06-1/linux/lib  -Wl,-rpath-link=./   objs/amcQw_d.
o   _130469_archive_1.so  SIM_1.o       rmapats_mop.o rmapats.o rmar.o rmar_nd.o
  rmar_llvm_0_1.o rmar_llvm_0_0.o           -lvirsim -lerrorinf -lsnpsmalloc -lv
fs    -lvcsnew -lsimprofile -luclinative /usr/local/synopsys/vcs/T-2022.06-1/lin
ux/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive
   /usr/local/synopsys/vcs/T-2022.06-1/linux/lib/vcs_save_restore_new.o /usr/loc
al/synopsys/vcs/T-2022.06-1/linux/lib/ctype-stubs_32.a -ldl  -lc -lm -lpthread -
ldl
../simv up to date
CPU time: .334 seconds to compile + .283 seconds to elab + .353 seconds to link
bender /home/cemaj/frosales/eecs168/lab4-rtl/counter $ ./simv
Chronologic VCS simulator copyright 1991-2022
Contains Synopsys proprietary information.
Compiler version T-2022.06-1; Runtime version T-2022.06-1;  Mar 14 15:42 2023
time=    0 ns, clk=0, reset=0, out=xxxx
time=   10 ns, clk=1, reset=0, out=xxxx
time=   11 ns, clk=1, reset=1, out=xxxx
time=   20 ns, clk=0, reset=1, out=xxxx
time=   30 ns, clk=1, reset=1, out=xxxx
time=   31 ns, clk=1, reset=0, out=0000
time=   40 ns, clk=0, reset=0, out=0000
time=   50 ns, clk=1, reset=0, out=0000
time=   51 ns, clk=1, reset=0, out=0001
time=   60 ns, clk=0, reset=0, out=0001
time=   70 ns, clk=1, reset=0, out=0001
time=   71 ns, clk=1, reset=0, out=0010
time=   80 ns, clk=0, reset=0, out=0010
time=   90 ns, clk=1, reset=0, out=0010
time=   91 ns, clk=1, reset=0, out=0011
time=  100 ns, clk=0, reset=0, out=0011
time=  110 ns, clk=1, reset=0, out=0011
time=  111 ns, clk=1, reset=0, out=0100
time=  120 ns, clk=0, reset=0, out=0100
time=  130 ns, clk=1, reset=0, out=0100
time=  131 ns, clk=1, reset=0, out=0101
time=  140 ns, clk=0, reset=0, out=0101
time=  150 ns, clk=1, reset=0, out=0101
time=  151 ns, clk=1, reset=0, out=0110
time=  160 ns, clk=0, reset=0, out=0110
time=  170 ns, clk=1, reset=0, out=0110
All tests completed sucessfully


$finish called from file "counter_tb.v", line 55.
$finish at simulation time  171.0 ns
           V C S   S i m u l a t i o n   R e p o r t
Time: 171000 ps
CPU Time:      0.490 seconds;       Data structure size:   0.0Mb
Tue Mar 14 15:42:45 2023
bender /home/cemaj/frosales/eecs168/lab4-rtl/counter $
```

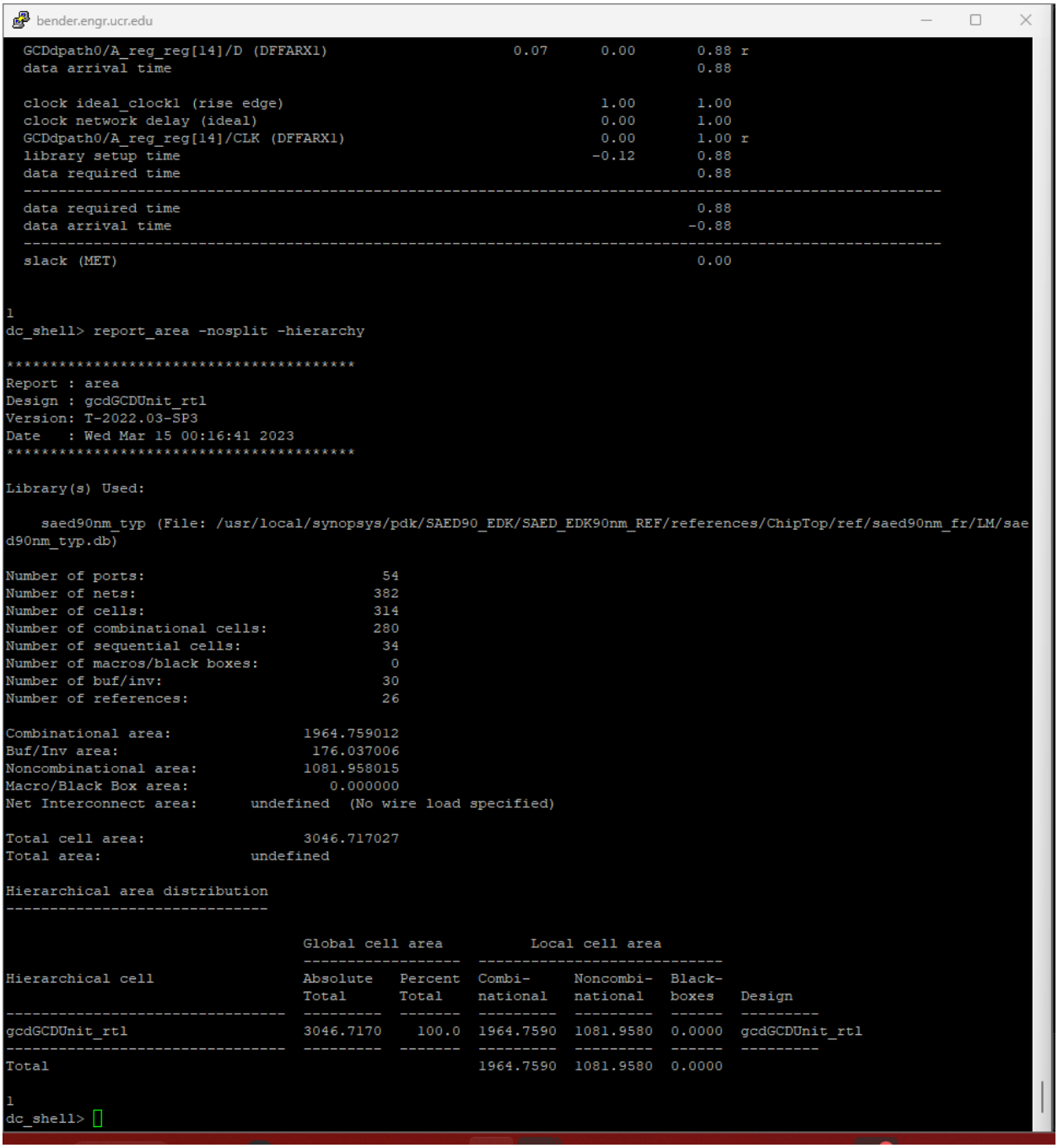

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power
fa_4bit
Hier.1
Schematic.1
Logical Hierarchy
fa_4bit
Cells (Hierarchical)
Cell Name
Ref Name
cin
ain
4
bin
4
fa_4bit
cout
sum
4
Optimization Complete
1

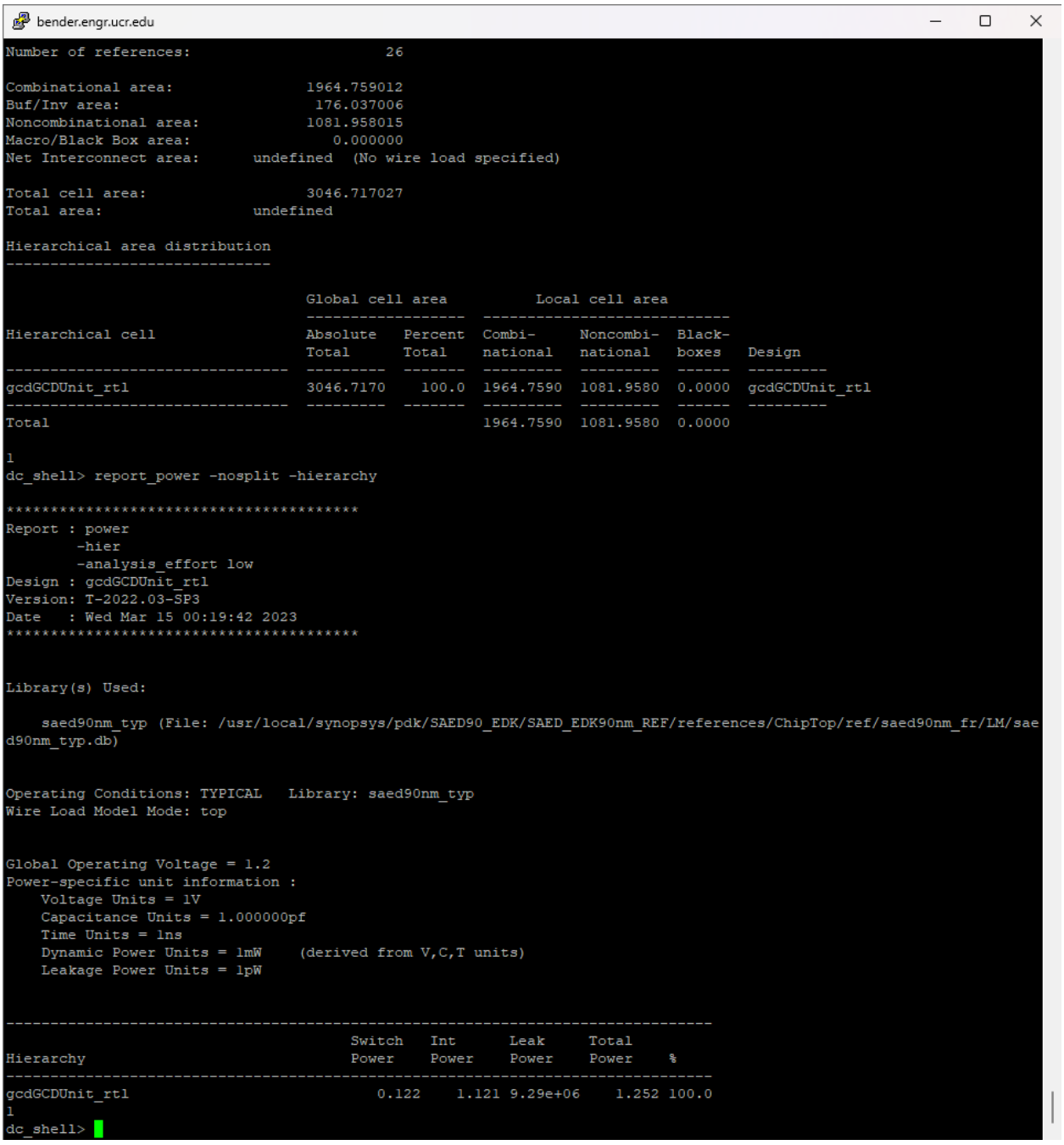

Smart
Line
Enable
Replace
Clear
Annotations
Apply
100%
Level
0
Objects
Layers
Settings
Only select highlighted
Object Type
Vis.
Sel.
Clr.
Die Area
Core Area
Port
Terminal
Cell
Pin
Pin Shape
Site Row
Bound
Plan Group
Placement...
Routing Bl...
Power Plan...
RP Group
RP Keepout
Voltage Area
Pin Guide
Route Guide
Routing Co...
Global Route
Route
Shape
Via
Net Type
Route T...
Track

```
****************************************
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 1
        -transition_time
Design : gcdGCDUnit_rtl
Version: T-2022.03-SP3
Date   : Wed Mar 15 00:14:57 2023
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

  Startpoint: GCDdpath0/A_reg_reg[9]
              (rising edge-triggered flip-flop clocked by ideal_clock1)
  Endpoint: GCDdpath0/A_reg_reg[14]
            (rising edge-triggered flip-flop clocked by ideal_clock1)
  Path Group: ideal_clock1
  Path Type: max

Attributes:
    d - dont_touch
    u - dont_use
   mo - map_only
   so - size_only
    i - ideal_net or ideal_network
  inf - infeasible path

  Point                                Fanout     Trans      Incr       Path      Attributes
  ----------------------------------------------------------------------------------------------------
  clock ideal_clock1 (rise edge)                                0.00       0.00
  clock network delay (ideal)                                   0.00       0.00
  GCDdpath0/A_reg_reg[9]/CLK (DFFARX1)                          0.00       0.00       0.00 r
  GCDdpath0/A_reg_reg[9]/Q (DFFARX1)                            0.04       0.24       0.24 f
  result_bits_data[9] (net)                    4                0.00       0.24 f
```

U228/QN (NOR2X0)		0.08	0.05	0.29 r
n312 (net)	3	0.00		0.29 r
U139/QN (NOR2X0)		0.05	0.05	0.33 f
n142 (net)	1	0.00		0.33 f
U133/QN (NOR2X0)		0.07	0.04	0.38 r
n321 (net)	3	0.00		0.38 r
U157/QN (INVX0)		0.03	0.03	0.41 f
n157 (net)	1	0.00		0.41 f
U128/QN (NAND2X1)		0.04	0.03	0.43 r
n163 (net)	1	0.00		0.43 r
U248/QN (NAND2X1)		0.04	0.03	0.46 f
n206 (net)	2	0.00		0.46 f
U304/QN (INVX0)		0.05	0.04	0.50 r
n345 (net)	4	0.00		0.50 r
U314/Q (OA21X1)		0.04	0.09	0.59 r
n218 (net)	1	0.00		0.59 r
U315/Q (OA21X1)		0.04	0.09	0.68 r
n220 (net)	1	0.00		0.68 r
U317/Q (XNOR2X1)		0.04	0.12	0.80 r
n221 (net)	1	0.00		0.80 r
U318/QN (NAND2X0)		0.06	0.04	0.84 f
n225 (net)	1	0.00		0.84 f
U322/QN (NAND4X0)		0.07	0.04	0.88 r
n100 (net)	1	0.00		0.88 r
GCDdpath0/A_reg_reg[14]/D (DFFARX1)			0.07	0.00 0.88 r
data arrival time			0.88	
clock ideal_clock1 (rise edge)			1.00	1.00
clock network delay (ideal)			0.00	1.00
GCDdpath0/A_reg_reg[14]/CLK (DFFARX1)				0.00 1.00 r
library setup time			-0.12	0.88
data required time			0.88	
---				
data required time			0.88	
data arrival time			-0.88	
---				
slack (MET)			0.00	

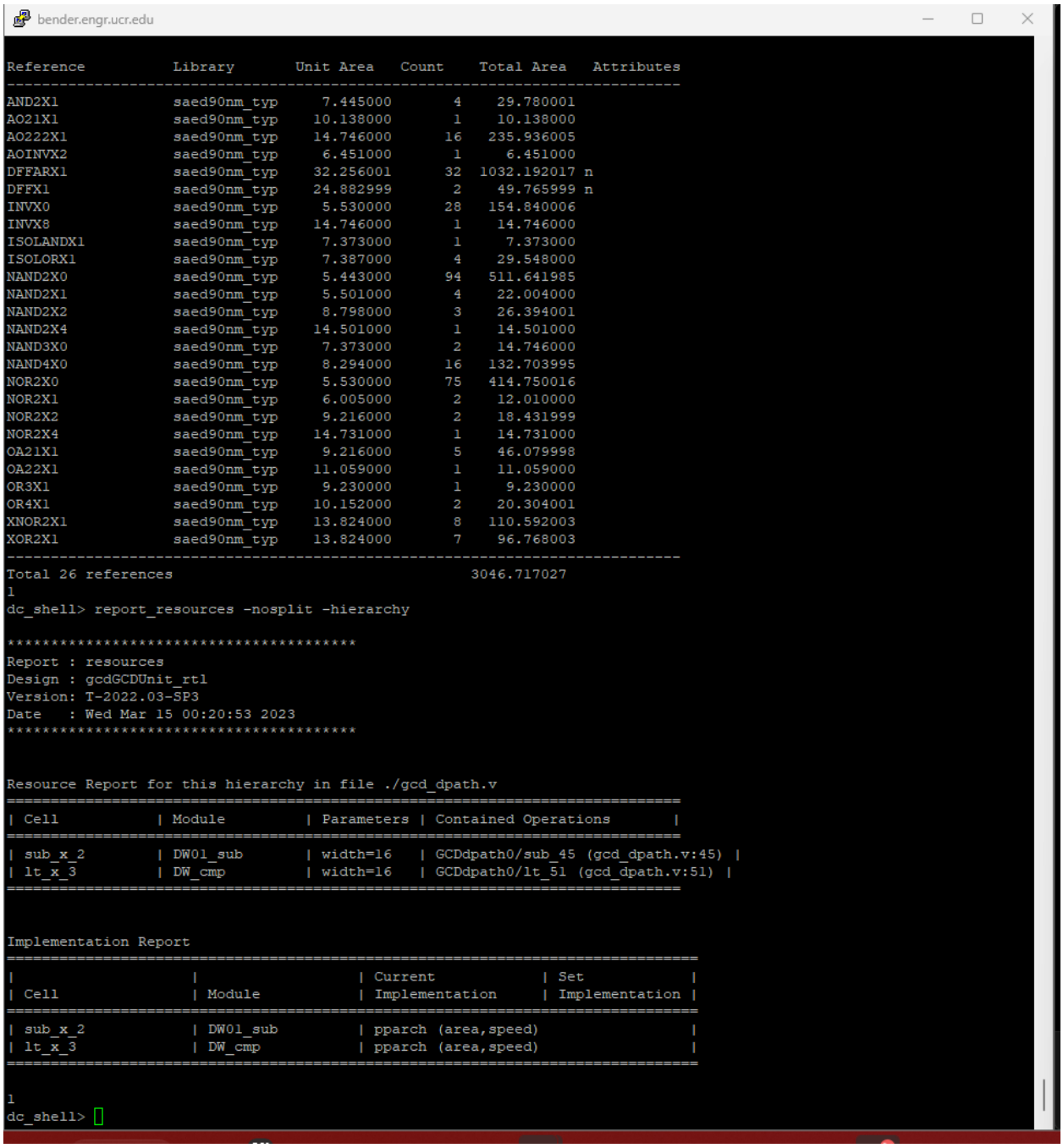
```
             (rising edge-triggered flip-flop clocked by ideal_clock1)
  Endpoint: GCDdpath0/A_reg_reg[14]
            (rising edge-triggered flip-flop clocked by ideal_clock1)
  Path Group: ideal_clock1
  Path Type: max

Attributes:
    d - dont_touch
    u - dont_use
   mo - map_only
   so - size_only
    i - ideal_net or ideal_network
  inf - infeasible path

  Point                                    Fanout     Trans      Incr       Path      Attributes
  ----------------------------------------------------------------------------------------------
  clock ideal_clock1 (rise edge)                                0.00       0.00
  clock network delay (ideal)                                   0.00       0.00
  GCDdpath0/A_reg_reg[9]/CLK (DFFARX1)                  0.00    0.00       0.00 r
  GCDdpath0/A_reg_reg[9]/Q (DFFARX1)                    0.04    0.24       0.24 f
  result_bits_data[9] (net)                        4                0.00    0.24 f
  U228/QN (NOR2X0)                                      0.08    0.05       0.29 r
  n312 (net)                                       3                0.00    0.29 r
  U139/QN (NOR2X0)                                      0.05    0.05       0.33 f
  n142 (net)                                       1                0.00    0.33 f
  U133/QN (NOR2X0)                                      0.07    0.04       0.38 r
  n321 (net)                                       3                0.00    0.38 r
  U157/QN (INVX0)                                       0.03    0.03       0.41 f
  n157 (net)                                       1                0.00    0.41 f
  U128/QN (NAND2X1)                                     0.04    0.03       0.43 r
  n163 (net)                                       1                0.00    0.43 r
  U248/QN (NAND2X1)                                     0.04    0.03       0.46 f
  n206 (net)                                       2                0.00    0.46 f
  U304/QN (INVX0)                                       0.05    0.04       0.50 r
  n345 (net)                                       4                0.00    0.50 r
  U314/Q (OA21X1)                                       0.04    0.09       0.59 r
  n218 (net)                                       1                0.00    0.59 r
  U315/Q (OA21X1)                                       0.04    0.09       0.68 r
  n220 (net)                                       1                0.00    0.68 r
  U317/Q (XNOR2X1)                                      0.04    0.12       0.80 r
  n221 (net)                                       1                0.00    0.80 r
  U318/QN (NAND2X0)                                     0.06    0.04       0.84 f
  n225 (net)                                       1                0.00    0.84 f
  U322/QN (NAND4X0)                                     0.07    0.04       0.88 r
  n100 (net)                                       1                0.00    0.88 r
  GCDdpath0/A_reg_reg[14]/D (DFFARX1)                   0.07    0.00       0.88 r
  data arrival time                                                        0.88

  clock ideal_clock1 (rise edge)                                1.00       1.00
  clock network delay (ideal)                                   0.00       1.00
  GCDdpath0/A_reg_reg[14]/CLK (DFFARX1)                         0.00       1.00 r
  library setup time                                           -0.12       0.88
  data required time                                                       0.88
  ----------------------------------------------------------------------------------------------
  data required time                                                       0.88
  data arrival time                                                       -0.88
  ----------------------------------------------------------------------------------------------
  slack (MET)                                                              0.00


1
dc_shell>
```

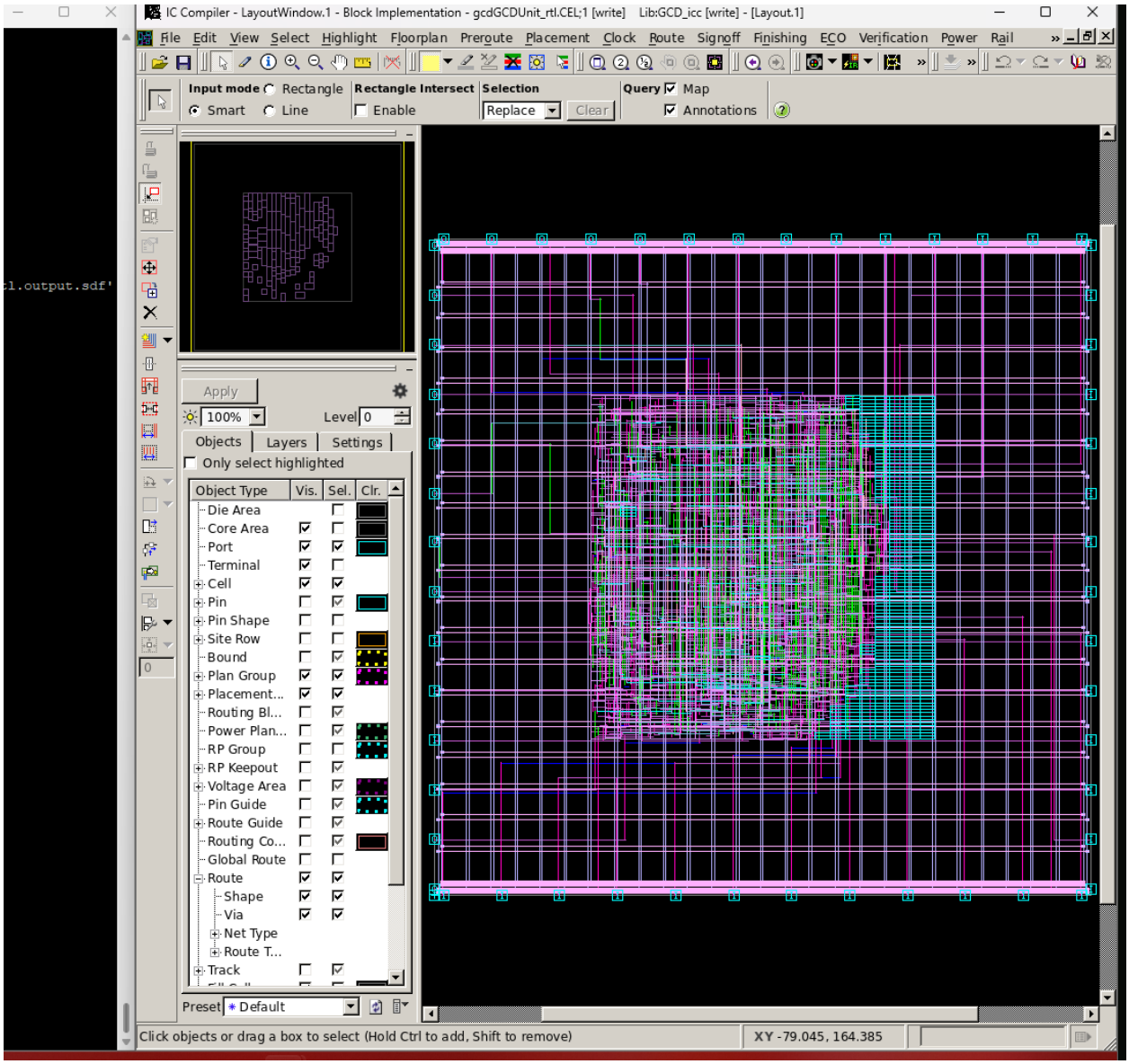

bender.engr.ucr.edu
GCDdpath0/A_reg_reg[14]/D (DFFARX1) 0.07 0.00 0.88 r
data arrival time 0.88
clock ideal_clock1 (rise edge) 1.00 1.00
clock network delay (ideal) 0.00 1.00
GCDdpath0/A_reg_reg[14]/CLK (DFFARX1) 0.00 1.00 r
library setup time -0.12 0.88
data required time 0.88
data required time 0.88
data arrival time -0.88
slack (MET) 0.00
1
dc_shell> report_area -nosplit -hierarchy
Report : area
Design : gcdGCDUnit_rtl
Version: T-2022.03-SP3
Date : Wed Mar 15 00:16:41 2023
Library(s) Used:
saed90nm_typ (File: /usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db)
Number of ports: 54
Number of nets: 382
Number of cells: 314
Number of combinational cells: 280
Number of sequential cells: 34
Number of macros/black boxes: 0
Number of buf/inv: 30
Number of references: 26
Combinational area: 1964.759012
Buf/Inv area: 176.037006
Noncombinational area: 1081.958015
Macro/Black Box area: 0.000000
Net Interconnect area: undefined (No wire load specified)
Total cell area: 3046.717027
Total area: undefined
Hierarchical area distribution
Global cell area
Local cell area
Hierarchical cell
Absolute Total
Percent Total
Combi-national
Noncombi-national
Black-boxes
Design
gcdGCDUnit_rtl 3046.7170 100.0 1964.7590 1081.9580 0.0000 gcdGCDUnit_rtl
Total 1964.7590 1081.9580 0.0000
1
dc_shell>


bender.engr.ucr.edu
Number of references: 26
Combinational area: 1964.759012
Buf/Inv area: 176.037006
Noncombinational area: 1081.958015
Macro/Black Box area: 0.000000
Net Interconnect area: undefined (No wire load specified)
Total cell area: 3046.717027
Total area: undefined
Hierarchical area distribution
Global cell area Local cell area
Hierarchical cell Absolute Total Percent Total Combi-national Noncombi-national Black-boxes Design
gcdGCDUnit_rtl 3046.7170 100.0 1964.7590 1081.9580 0.0000 gcdGCDUnit_rtl
Total 1964.7590 1081.9580 0.0000
1
dc_shell> report_power -nosplit -hierarchy
Report : power
-hier
-analysis_effort low
Design : gcdGCDUnit_rtl
Version: T-2022.03-SP3
Date : Wed Mar 15 00:19:42 2023
Library(s) Used:
saed90nm_typ (File: /usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db)
Operating Conditions: TYPICAL Library: saed90nm_typ
Wire Load Model Mode: top
Global Operating Voltage = 1.2
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V,C,T units)
Leakage Power Units = 1pW
Hierarchy Switch Power Int Power Leak Power Total Power %
gcdGCDUnit_rtl 0.122 1.121 9.29e+06 1.252 100.0
1
dc_shell>

bender.engr.ucr.edu

```
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------------------
                                  Switch   Int      Leak     Total
Hierarchy                         Power    Power    Power    Power    %
--------------------------------------------------------------------------------
gcdGCDUnit_rtl                       0.122    1.121 9.29e+06    1.252 100.0
1
dc_shell> report_reference -nosplit -hierarchy

****************************************
Report : reference
Design : gcdGCDUnit_rtl
Version: T-2022.03-SP3
Date   : Wed Mar 15 00:20:18 2023
****************************************

Attributes:
    b - black box (unknown)
   bo - allows boundary optimization
    d - dont_touch
   mo - map_only
    h - hierarchical
    n - noncombinational
    r - removable
    s - synthetic operator
    u - contains unmapped logic

Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
AND2X1             saed90nm_typ     7.445000       4    29.780001
AO21X1             saed90nm_typ    10.138000       1    10.138000
AO222X1            saed90nm_typ    14.746000      16   235.936005
AOINVX2            saed90nm_typ     6.451000       1     6.451000
DFFARX1            saed90nm_typ    32.256001      32  1032.192017 n
DFFX1              saed90nm_typ    24.882999       2    49.765999 n
INVX0              saed90nm_typ     5.530000      28   154.840006
INVX8              saed90nm_typ    14.746000       1    14.746000
ISOLANDX1          saed90nm_typ     7.373000       1     7.373000
ISOLORX1           saed90nm_typ     7.387000       4    29.548000
NAND2X0            saed90nm_typ     5.443000      94   511.641985
NAND2X1            saed90nm_typ     5.501000       4    22.004000
NAND2X2            saed90nm_typ     8.798000       3    26.394001
NAND2X4            saed90nm_typ    14.501000       1    14.501000
NAND3X0            saed90nm_typ     7.373000       2    14.746000
NAND4X0            saed90nm_typ     8.294000      16   132.703995
NOR2X0             saed90nm_typ     5.530000      75   414.750016
NOR2X1             saed90nm_typ     6.005000       2    12.010000
NOR2X2             saed90nm_typ     9.216000       2    18.431999
NOR2X4             saed90nm_typ    14.731000       1    14.731000
OA21X1             saed90nm_typ     9.216000       5    46.079998
OA22X1             saed90nm_typ    11.059000       1    11.059000
OR3X1              saed90nm_typ     9.230000       1     9.230000
OR4X1              saed90nm_typ    10.152000       2    20.304001
XNOR2X1            saed90nm_typ    13.824000       8   110.592003
XOR2X1             saed90nm_typ    13.824000       7    96.768003
--------------------------------------------------------------------------------
Total 26 references                                  3046.717027
1
dc_shell>
```


bender.engr.ucr.edu
Reference Library Unit Area Count Total Area Attributes
AND2X1 saed90nm_typ 7.445000 4 29.780001
AO21X1 saed90nm_typ 10.138000 1 10.138000
AO222X1 saed90nm_typ 14.746000 16 235.936005
AOINVX2 saed90nm_typ 6.451000 1 6.451000
DFFARX1 saed90nm_typ 32.256001 32 1032.192017 n
DFFX1 saed90nm_typ 24.882999 2 49.765999 n
INVX0 saed90nm_typ 5.530000 28 154.840006
INVX8 saed90nm_typ 14.746000 1 14.746000
ISOLANDX1 saed90nm_typ 7.373000 1 7.373000
ISOLORX1 saed90nm_typ 7.387000 4 29.548000
NAND2X0 saed90nm_typ 5.443000 94 511.641985
NAND2X1 saed90nm_typ 5.501000 4 22.004000
NAND2X2 saed90nm_typ 8.798000 3 26.394001
NAND2X4 saed90nm_typ 14.501000 1 14.501000
NAND3X0 saed90nm_typ 7.373000 2 14.746000
NAND4X0 saed90nm_typ 8.294000 16 132.703995
NOR2X0 saed90nm_typ 5.530000 75 414.750016
NOR2X1 saed90nm_typ 6.005000 2 12.010000
NOR2X2 saed90nm_typ 9.216000 2 18.431999
NOR2X4 saed90nm_typ 14.731000 1 14.731000
OA21X1 saed90nm_typ 9.216000 5 46.079998
OA22X1 saed90nm_typ 11.059000 1 11.059000
OR3X1 saed90nm_typ 9.230000 1 9.230000
OR4X1 saed90nm_typ 10.152000 2 20.304001
XNOR2X1 saed90nm_typ 13.824000 8 110.592003
XOR2X1 saed90nm_typ 13.824000 7 96.768003
Total 26 references 3046.717027
1
dc_shell> report_resources -nosplit -hierarchy
Report : resources
Design : gcdGCDUnit_rtl
Version: T-2022.03-SP3
Date : Wed Mar 15 00:20:53 2023
Resource Report for this hierarchy in file ./gcd_dpath.v
Cell Module Parameters Contained Operations
sub_x_2 DW01_sub width=16 GCDdpath0/sub_45 (gcd_dpath.v:45)
lt_x_3 DW_cmp width=16 GCDdpath0/lt_51 (gcd_dpath.v:51)
Implementation Report
Cell Module Current Implementation Set Implementation
sub_x_2 DW01_sub pparch (area,speed)
lt_x_3 DW_cmp pparch (area,speed)
1
dc_shell>



ISSUES: Overall there were no major issues this lab. Most of the simulations and commands went smoothly. The only issues occurred during 2 commands. Both times when using the insert_stdcell_filler this command would make a small error appear but overall I do not believe it affected the lab majorly. Other than that no other errors occurred during the lab assignment.