



Figure 1- Imported Layout

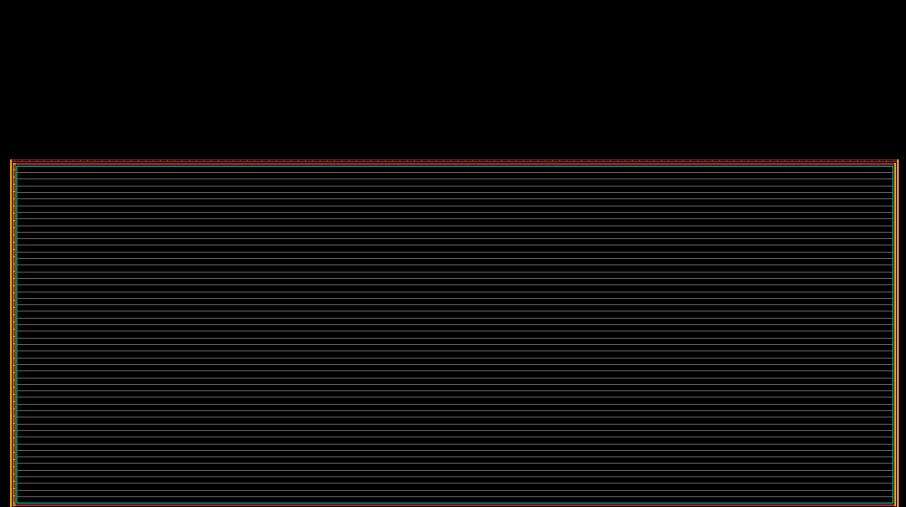
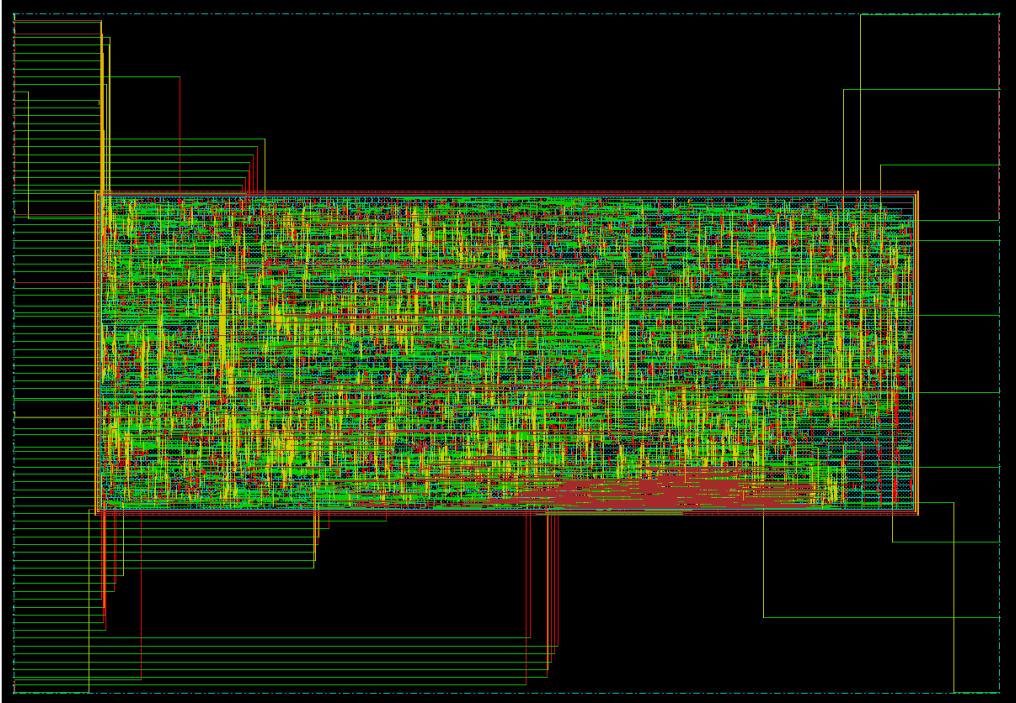


Figure 2-Ring power is added



*Figure 4- Placement Result*



*Figure 3- trail route*

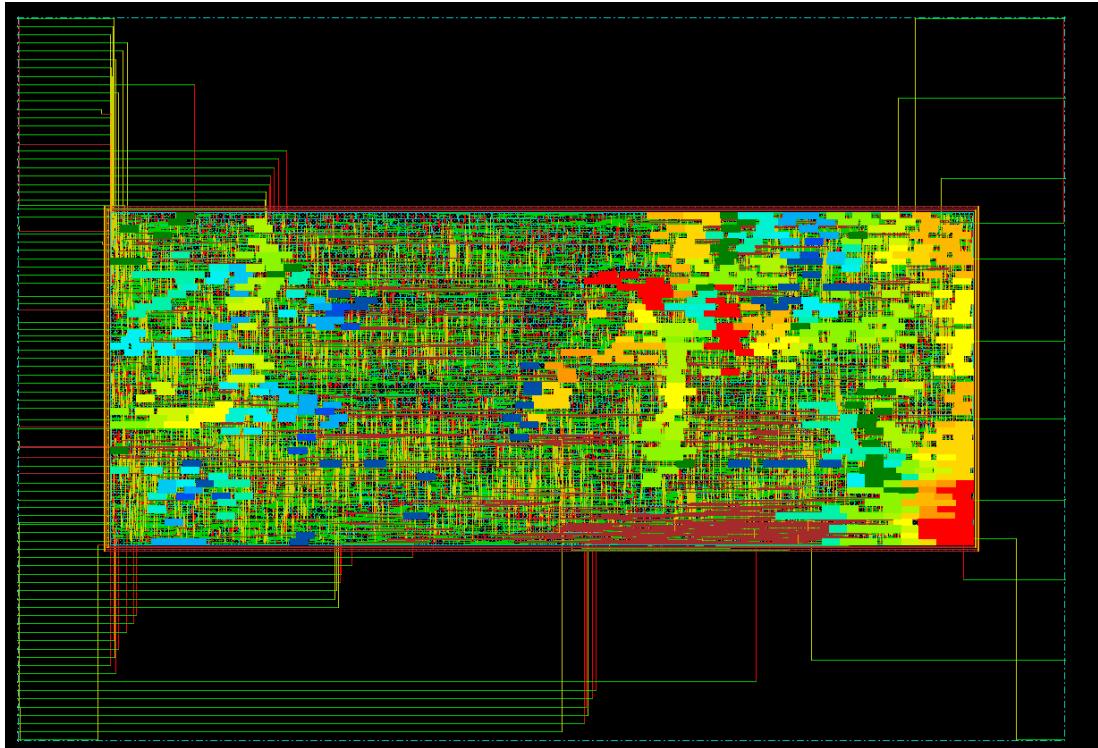


Figure 6- Clock delay

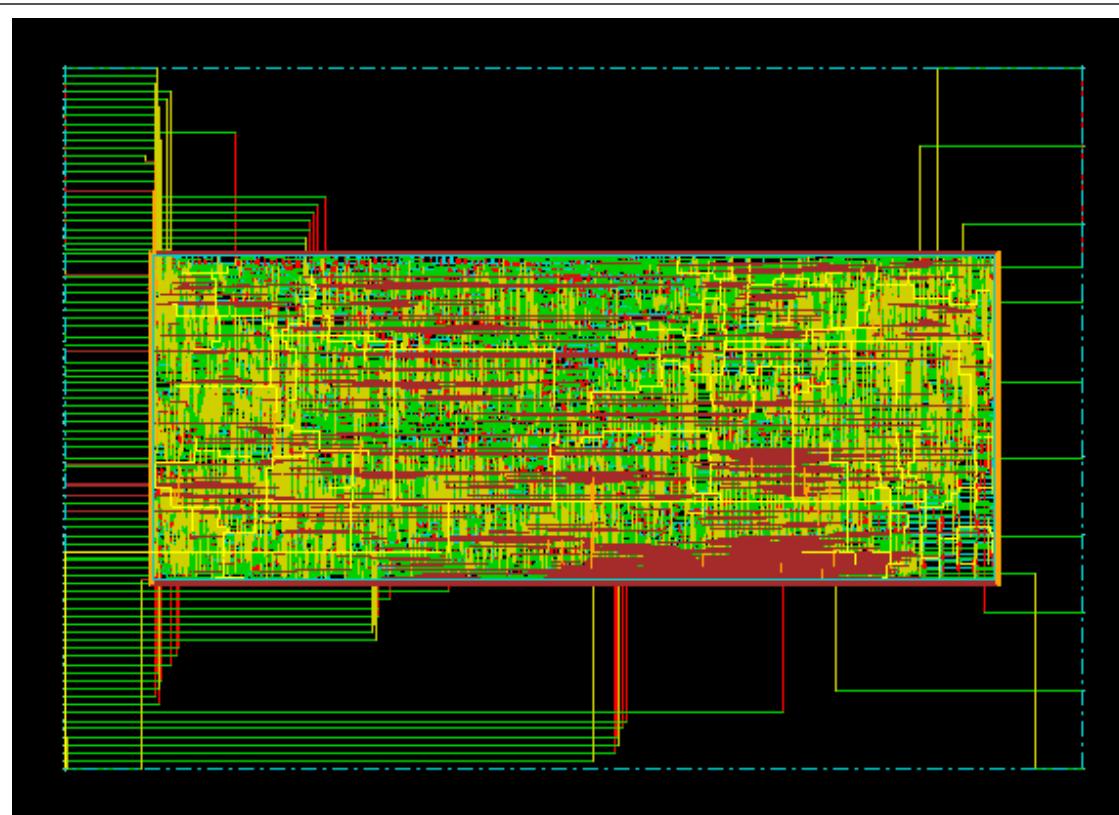


Figure 5- Clock tree

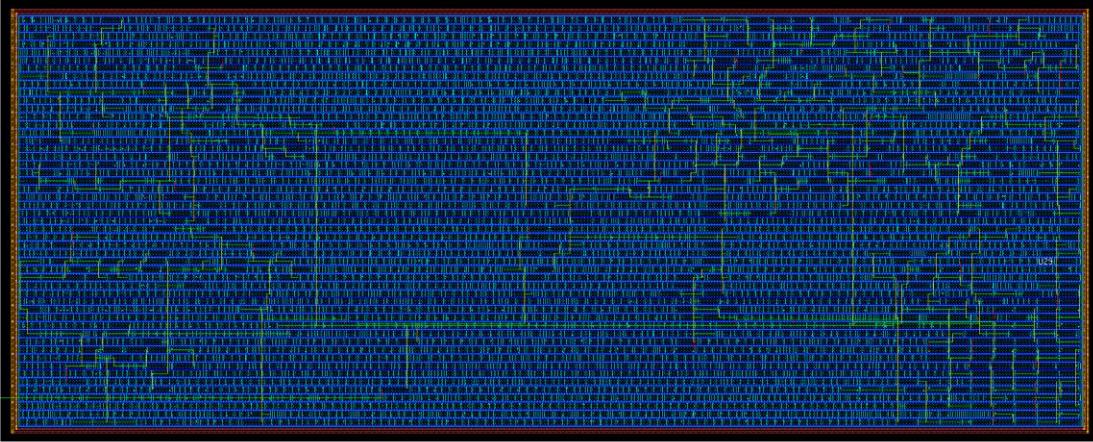


Figure 8- Routing

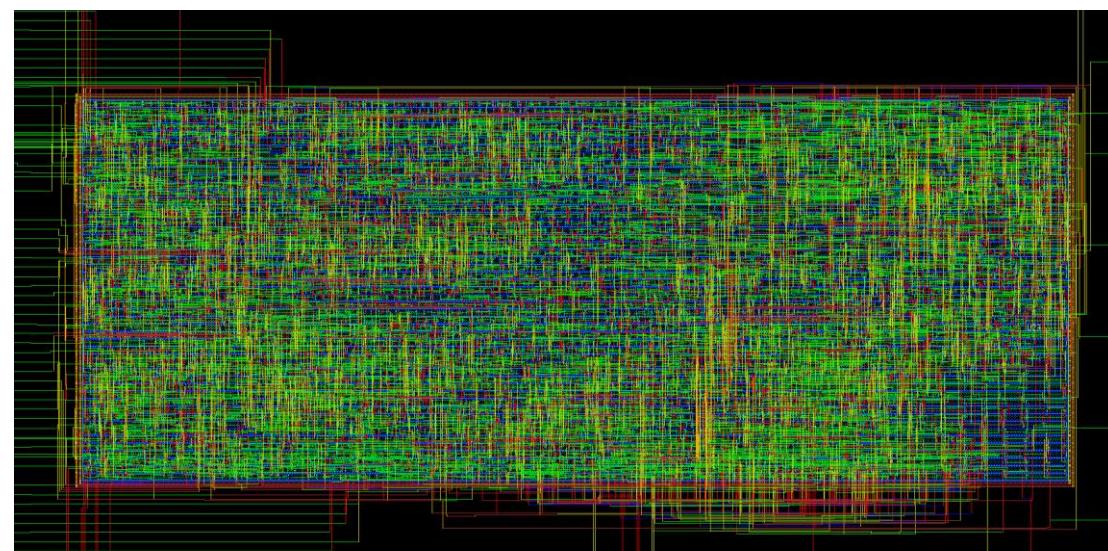


Figure 7- Nano route plus Filled layout

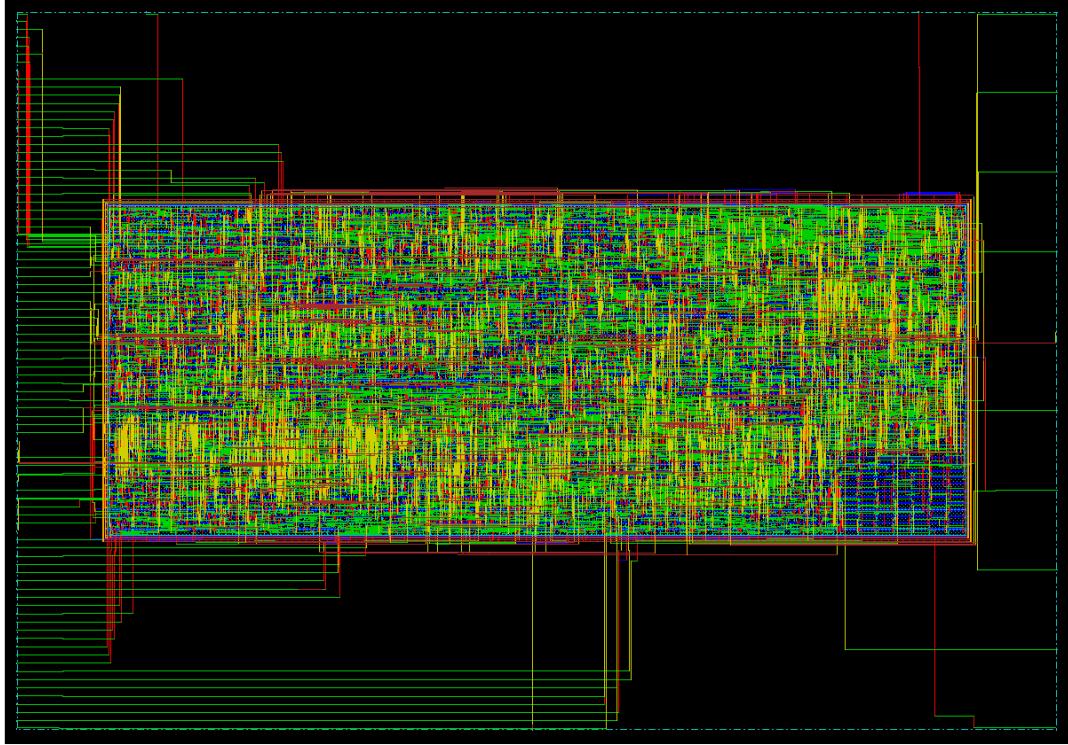


Figure 9- Final Layout

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Wed Apr 25 17:52:20 2018

Design Name: biquad_filter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (807.0650, 557.6800)
Error Limit = 1000; Warning Limit = 50
Check all nets
Net clk: Found a geometry with bounding box (-0.14,0.00) (0.14,0.28) outside design boundary.
Violations for such geometries will be reported.
Net en: Found a geometry with bounding box (806.93,557.40) (807.21,557.68) outside design boundary.
Violations for such geometries will be reported.
Net reset: Found a geometry with bounding box (-0.14,557.40) (0.14,557.68) outside design boundary.
Violations for such geometries will be reported.
Net parameter_A1_mul[0]: Found a geometry with bounding box (0.00,-0.14) (0.28,0.14) outside design boundary.
Violations for such geometries will be reported.
Net input_signal[7]: Found a geometry with bounding box (0.00,557.53) (0.28,557.81) outside design boundary.
Violations for such geometries will be reported.
Net output_signal[7]: Found a geometry with bounding box (806.78,557.53) (807.07,557.82) outside design boundary.
Violations for such geometries will be reported.
Net change_input: Found a geometry with bounding box (806.78,-0.14) (807.07,0.14) outside design boundary.
Violations for such geometries will be reported.
**** 17:52:20 **** Processed 5000 nets (Total 8124)
Time Elapsed: 0:00:00.0

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Apr 25 17:52:20 2018
***** End: VERIFY CONNECTIVITY *****
  Verification Complete: 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:00.8  MEM: 0.500M)
```

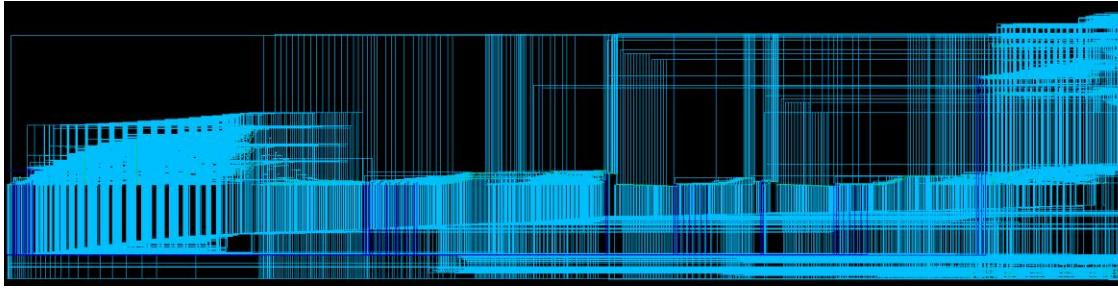
Figure 10- Connectivity Verification

```
encounter 4> *** Starting Verify Geometry (MEM: 395.9) ***  
VERIFY GEOMETRY ..... Starting Verification  
VERIFY GEOMETRY ..... Initializing  
VERIFY GEOMETRY ..... Deleting Existing Violations  
VERIFY GEOMETRY ..... Creating Sub-Areas  
..... bin size: 8320  
VERIFY GEOMETRY ..... SubArea : 1 of 1  
VERIFY GEOMETRY ..... Cells : 0 Viols.  
VERIFY GEOMETRY ..... SameNet : 0 Viols.  
VERIFY GEOMETRY ..... Wiring : 0 Viols.  
VERIFY GEOMETRY ..... Antenna : 0 Viols.  
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.  
VG: elapsed time: 5.00  
Begin Summary ...  
Cells : 0  
SameNet : 0  
Wiring : 0  
Antenna : 0  
Short : 0  
Overlap : 0  
End Summary  
Verification Complete : 0 Viols. 0 Wrngs.  
*****End: VERIFY GEOMETRY*****  
*** verify geometry (CPU: 0:00:04.2 MEM: 92.8M)
```

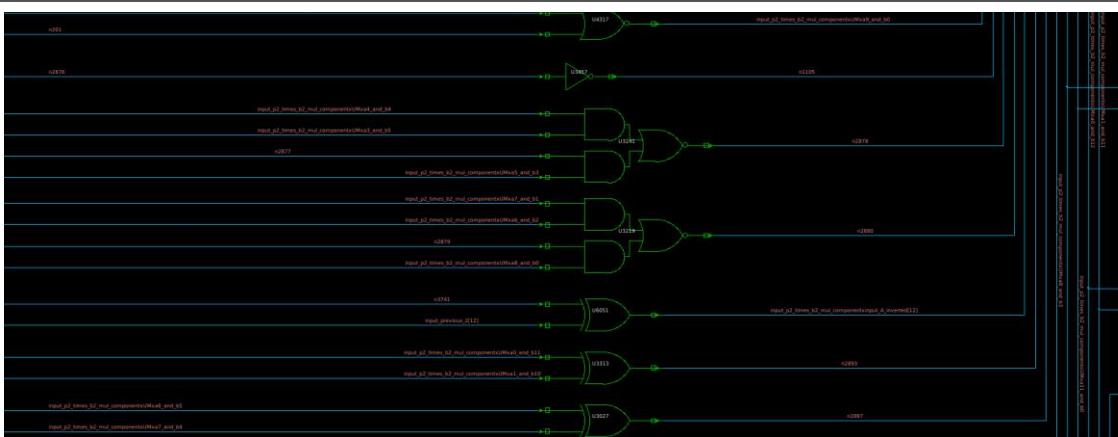
Figure 11- Geometry verification result

```
***** START VERIFY ANTENNA *****  
Report File: biquad_filter.antenna.rpt  
LEF Macro File: biquad_filter_antenna.lef  
5000 nets processed: 0 violations  
Verification Complete: 0 Violations  
***** DONE VERIFY ANTENNA *****  
(CPU Time: 0:00:00.8 MEM: 0.000M)
```

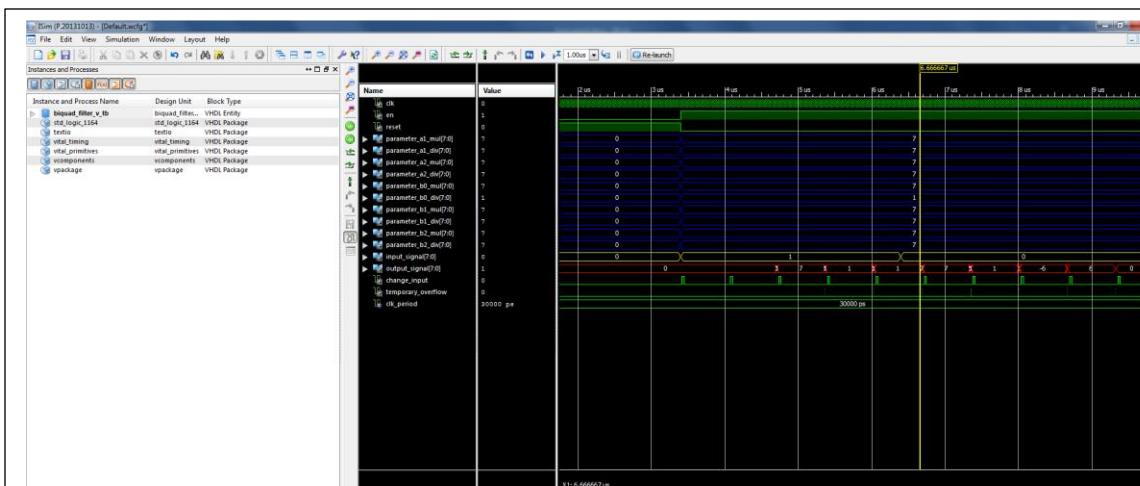
Figure 12- Process and antenna verification Result



*Figure 13- Top level of design vision output*



*Figure 14- Zoom into top-level module*



*Figure 15- Post route simulation result*

