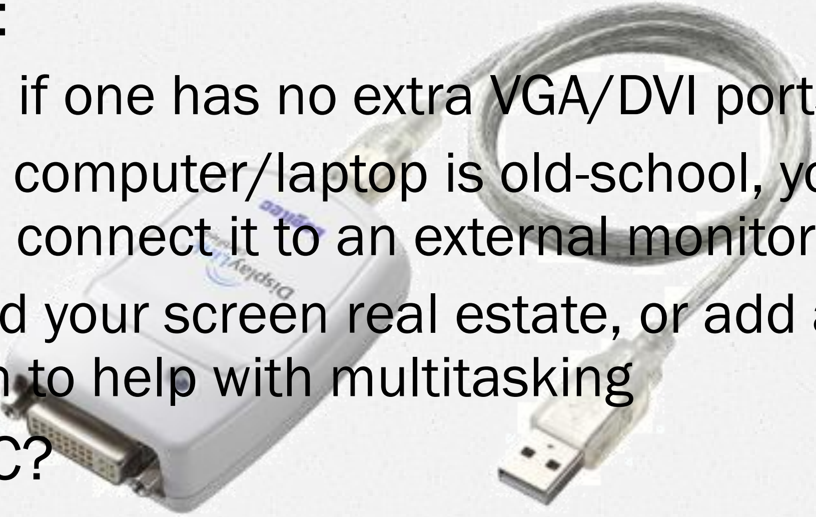
USB to DVI converter

- Matthew Barga
- Alex Reyes
- Harsimranjit Singh

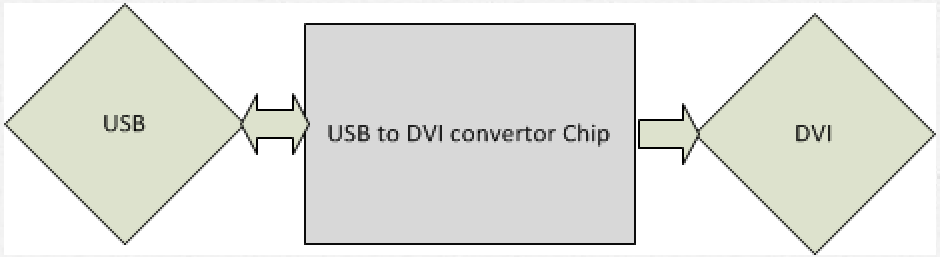
Overview

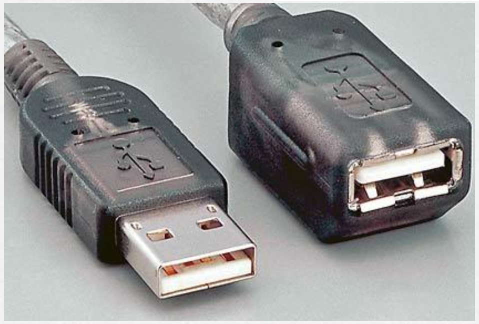
USB to DVI converter

- One end plugs into the USB port on a notebook or desktop computer, and the other end plugs into the DVI port on an external monitor
- Benefits:
  - Useful if one has no extra VGA/DVI ports
  - If your computer/laptop is old-school, you have a way to connect it to an external monitor
  - Expand your screen real estate, or add another screen to help with multitasking
- Why ASIC?
  - Reduced cost when mass-producing an ASIC design
  - High pin count (around 40)



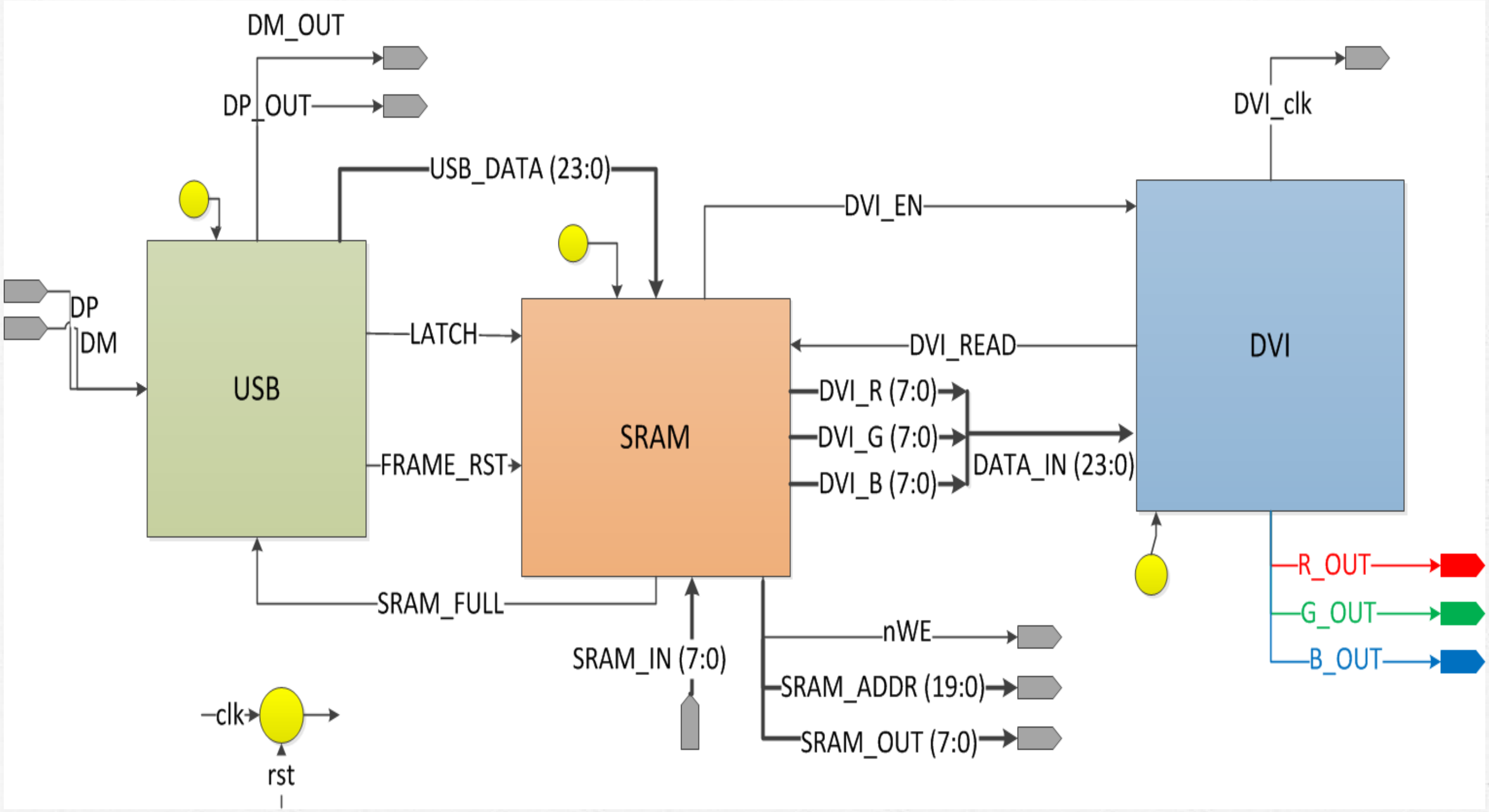
System Level Diagram



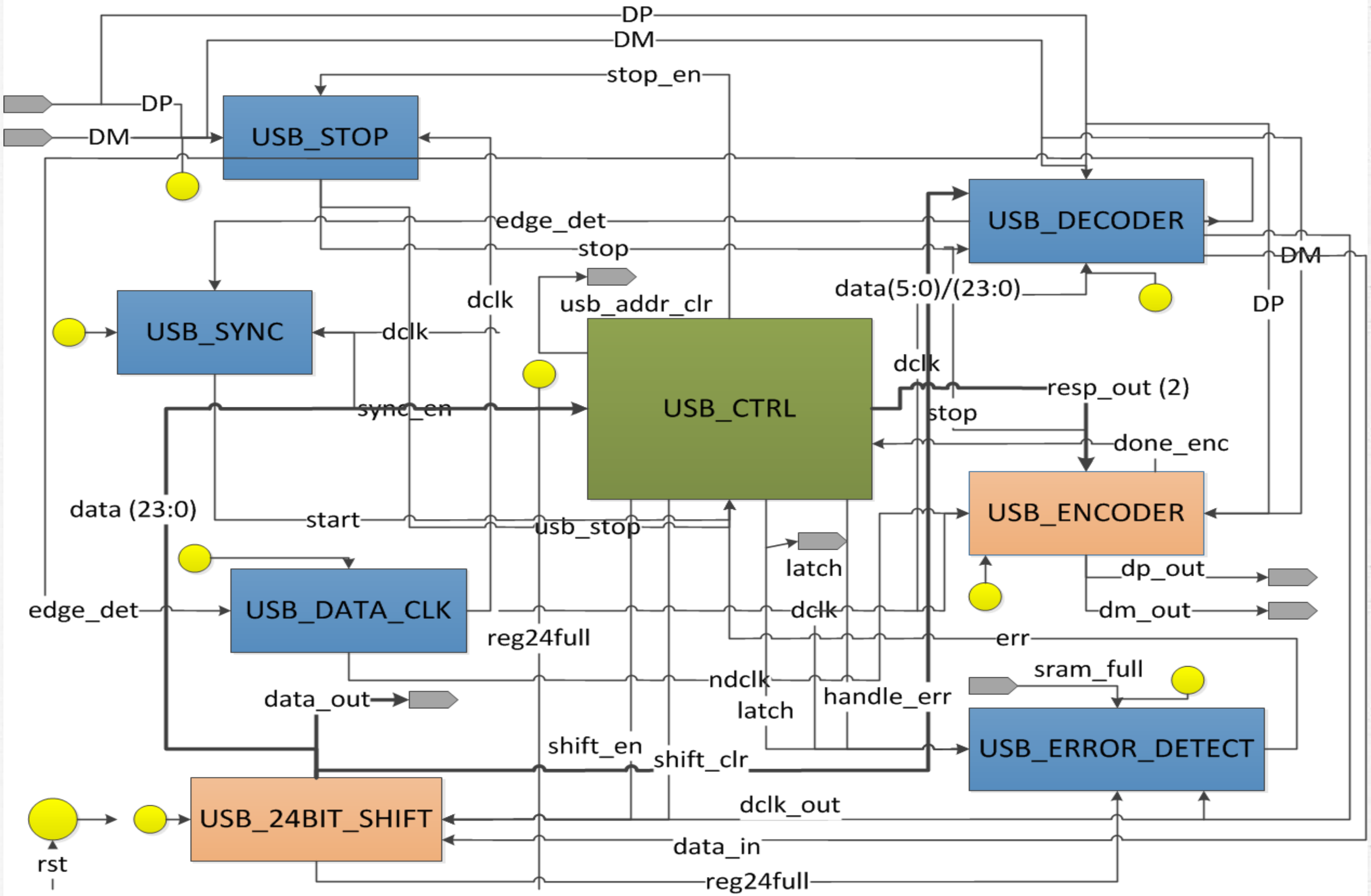


System Design

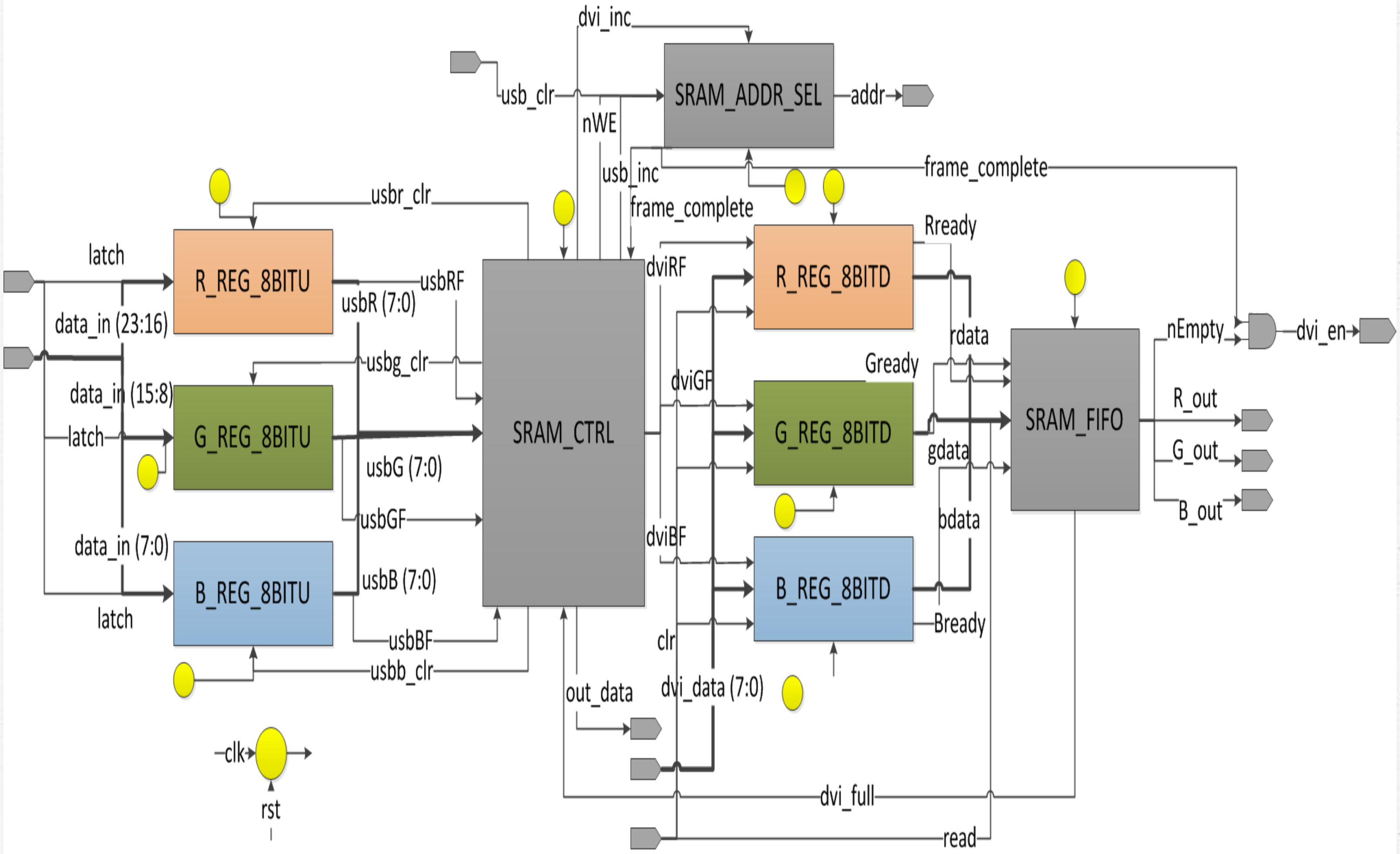
Top Level Block Diagram



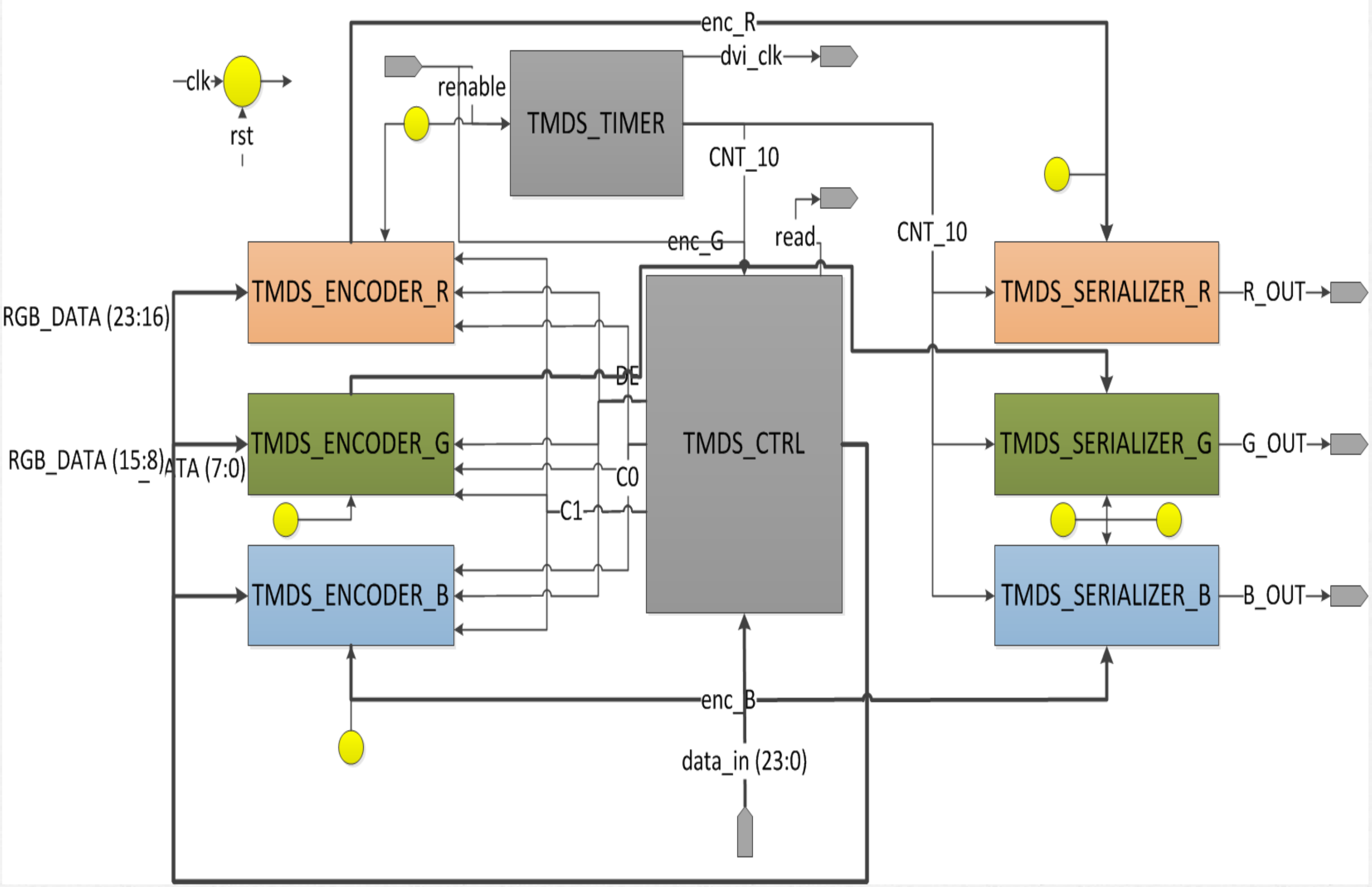
USB Top Level Block Diagram



SRAM Top Level Block Diagram



DVI Top Level Block Diagram



Top Level Signals

Signal Name	Type	No. of Bits	Data Format or Active High/Low	Description, Timing Constraints
RST_N	In	1	Active Low	Asynchronous Reset
CLK	In	1	50% duty cycle	Chip Clock, 4ns period (250 MHz)
DP	In	1	-	USB Data + Line
DM	In	1	-	USB Data – Line
DP_Out	Out	1	-	USB Data + Line Out
DM_Out	Out	1	-	USB Data – Line Out
Sram_In	In	8	Binary Data	SRAM Data Port In
Sram_Out	Out	8	Binary Data	SRAM Data Port Out
Addr	Out	20	Unsigned Binary	SRAM Address
nWE	Out	1	Active Low	SRAM Write Enable

Top Level Signals (contd..)

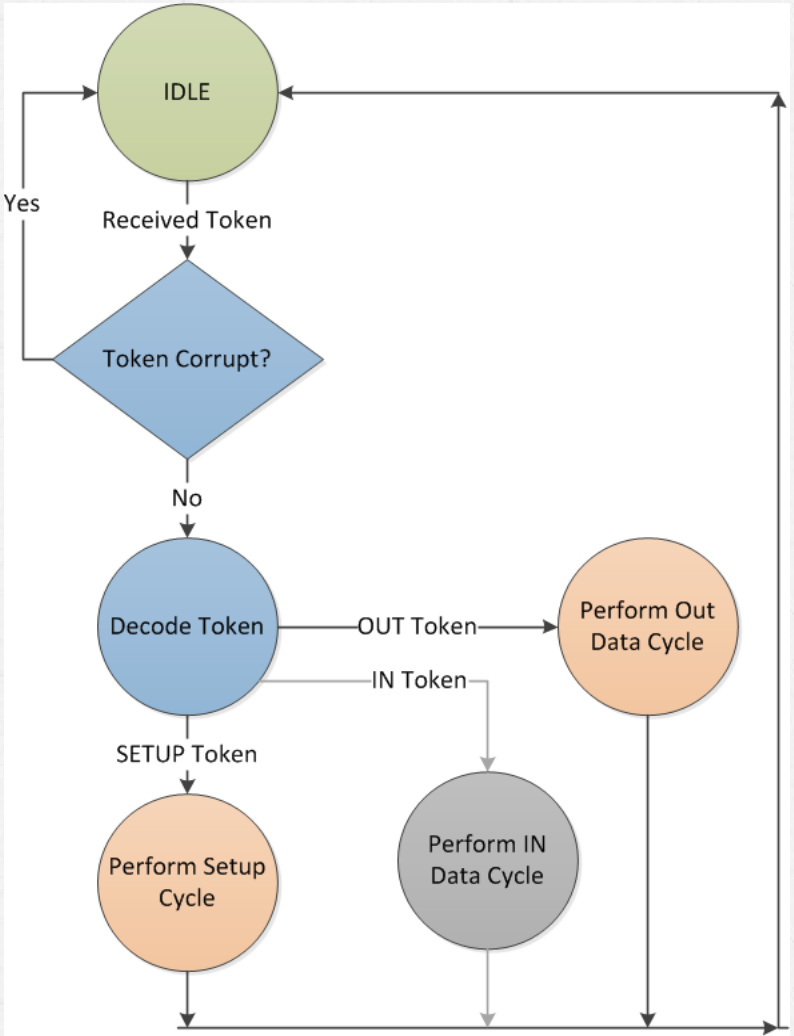
Signal Name	Type	No. of Bits	Data Format or Active High/Low	Description, Timing Constraints
R_Out	Out	1	Active High	Serial Output registers in parallel
G_Out	Out	1		
B_Out	Out	1		
DVI_clk	Out	1	50% Duty Cycle	Output clock divided to 25 MHz

Design Decisions

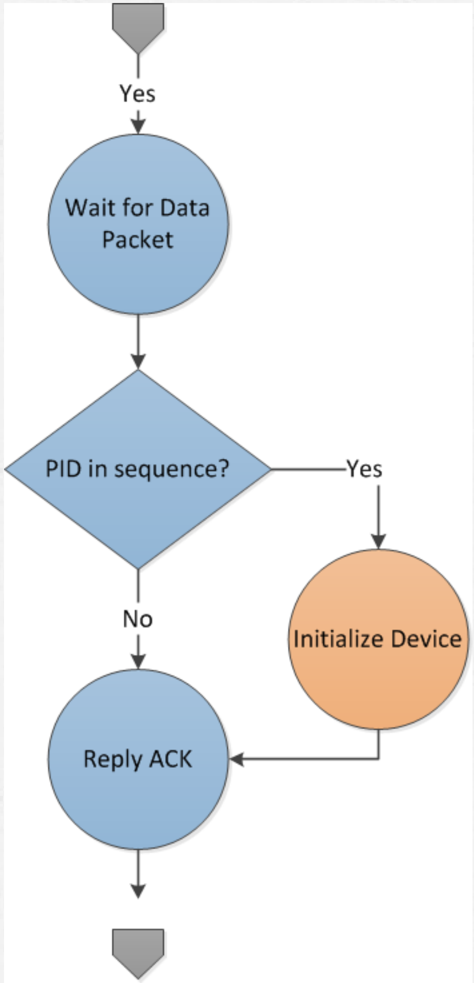
- Memory Interface
  - Use SRAM for frame repetition
- USB Protocol
  - Used 1.1 Protocol

Operational Characteristics

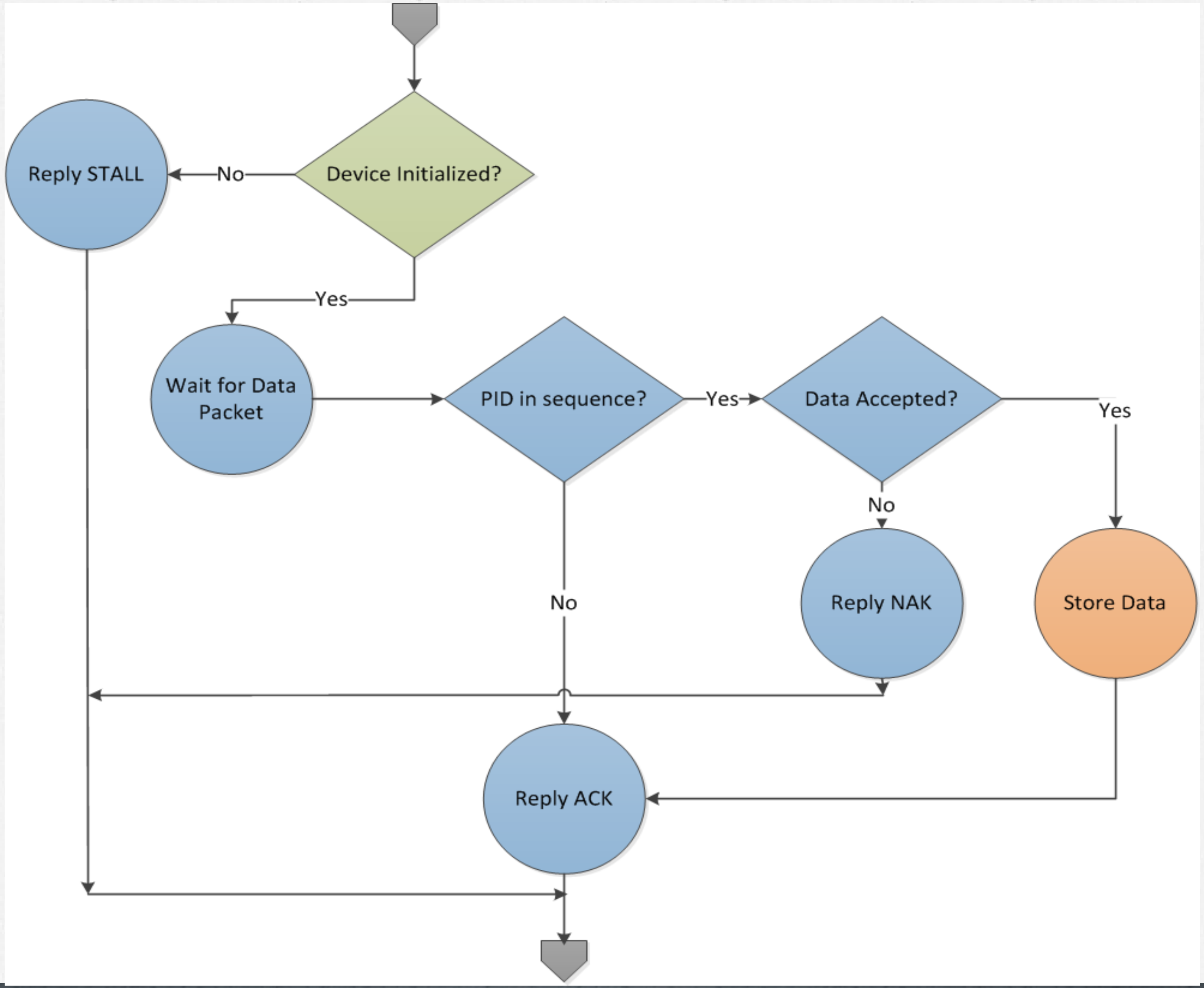
USB Core Main Loop



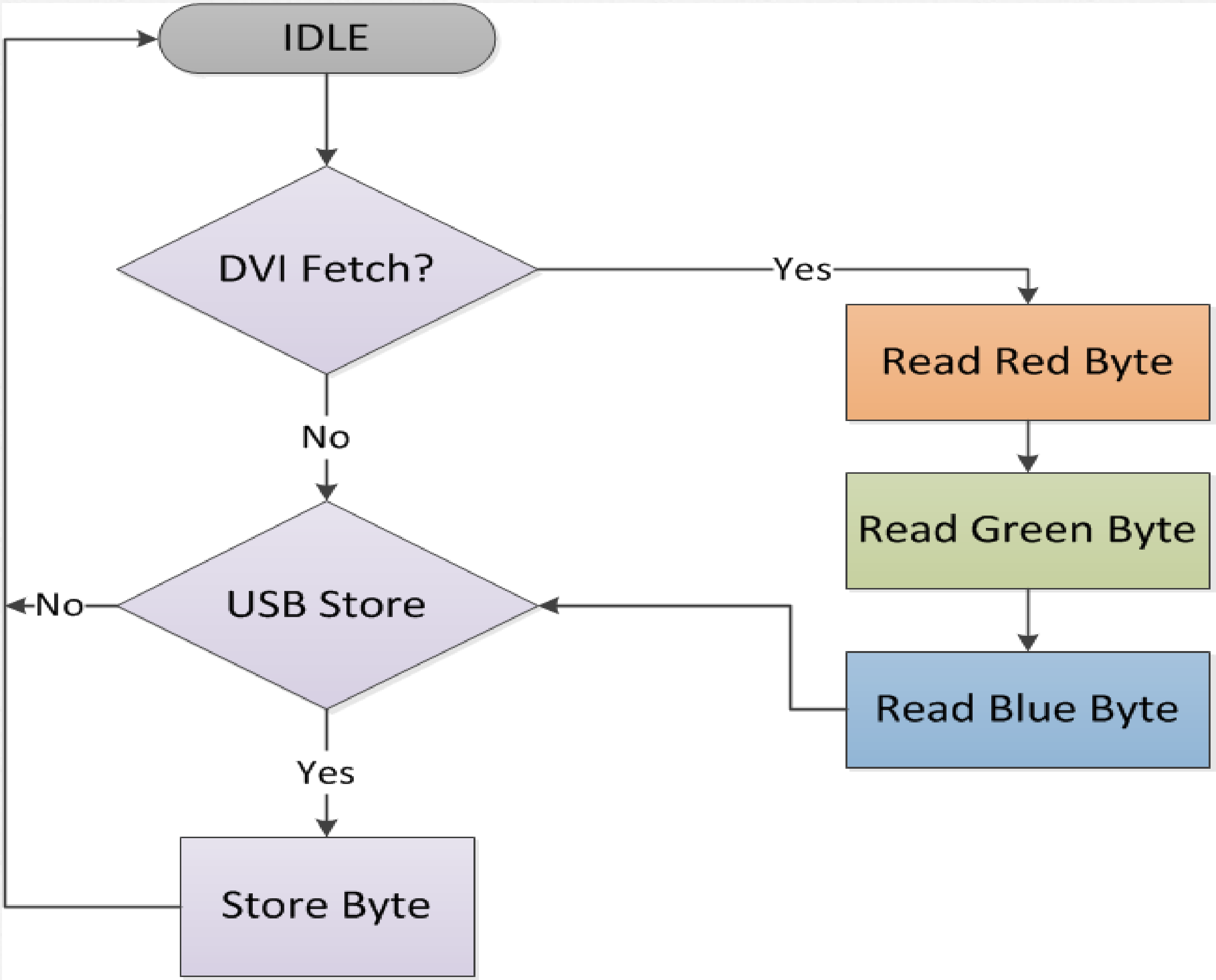
Setup Cycle USB



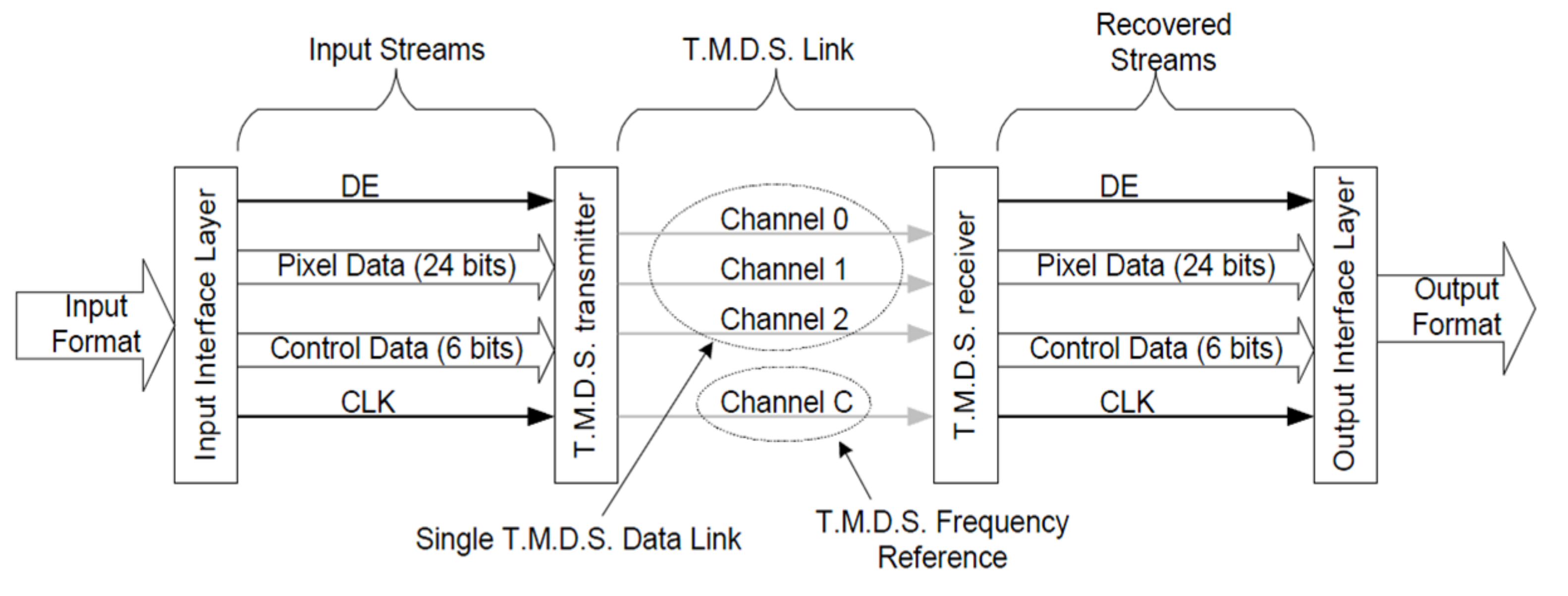
OUT Data Cycle USB



SRAM

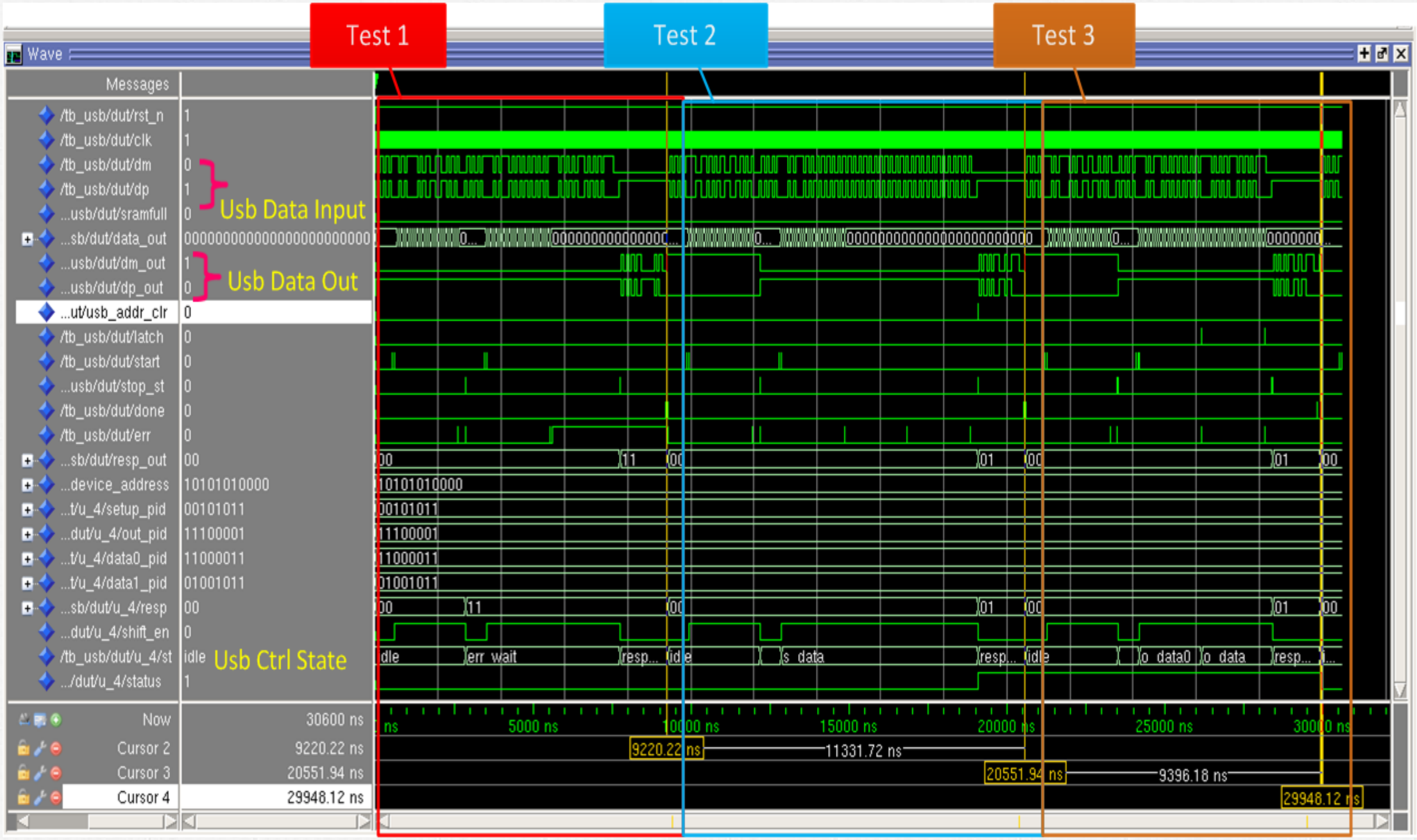

IDLE
DVI Fetch?
Yes
Read Red Byte
Read Green Byte
Read Blue Byte
No
USB Store
No
Yes
Store Byte

DVI


Input Streams
T.M.D.S. Link
Recovered Streams
Input Format
Input Interface Layer
DE
Pixel Data (24 bits)
Control Data (6 bits)
CLK
T.M.D.S. transmitter
Channel 0
Channel 1
Channel 2
Channel C
T.M.D.S. receiver
DE
Pixel Data (24 bits)
Control Data (6 bits)
CLK
Output Interface Layer
Output Format
Single T.M.D.S. Data Link
T.M.D.S. Frequency Reference

Results

USB Source Simulation



Test 1

Test 2

Test 3

Wave

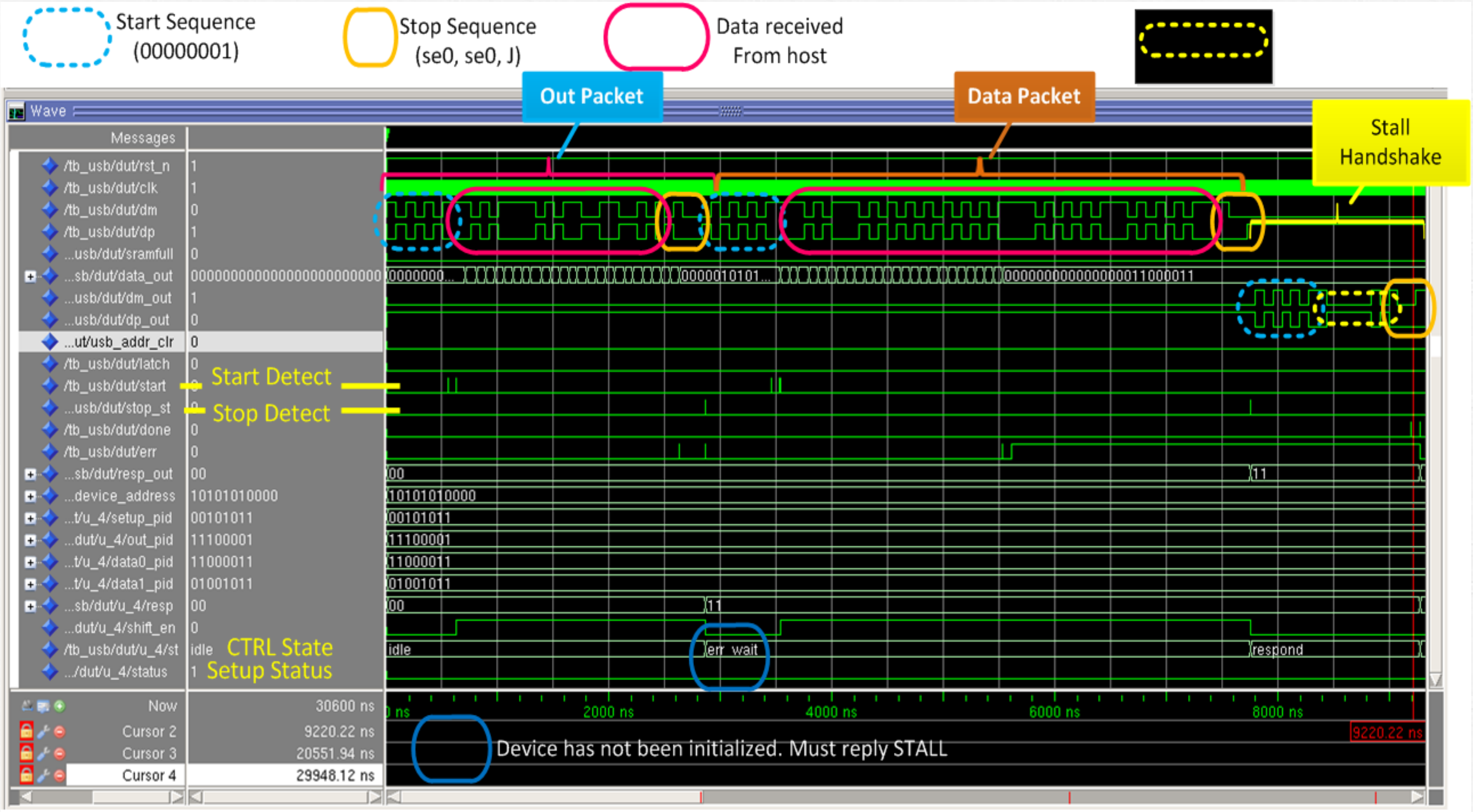
Messages	
/tb_usb/dut/rst_n	1
/tb_usb/dut/clk	1
/tb_usb/dut/dm	0
/tb_usb/dut/dp	1
...usb/dut/sramfull	0
...sb/dut/data_out	000000000000000000000000
...usb/dut/dm_out	1
...usb/dut/dp_out	0
...ut/usb_addr_clr	0
/tb_usb/dut/latch	0
/tb_usb/dut/start	0
...usb/dut/stop_st	0
/tb_usb/dut/done	0
/tb_usb/dut/err	0
...sb/dut/resp_out	00
...device_address	10101010000
...t/u_4/setup_pid	00101011
...dut/u_4/out_pid	11100001
...t/u_4/data0_pid	11000011
...t/u_4/data1_pid	01001011
...sb/dut/u_4/resp	00
...dut/u_4/shift_en	0
/tb_usb/dut/u_4/st	idle
.../dut/u_4/status	1
Now	30600 ns
Cursor 2	9220.22 ns
Cursor 3	20551.94 ns
Cursor 4	29948.12 ns

Usb Data Input

Usb Data Out

Usb Ctrl State

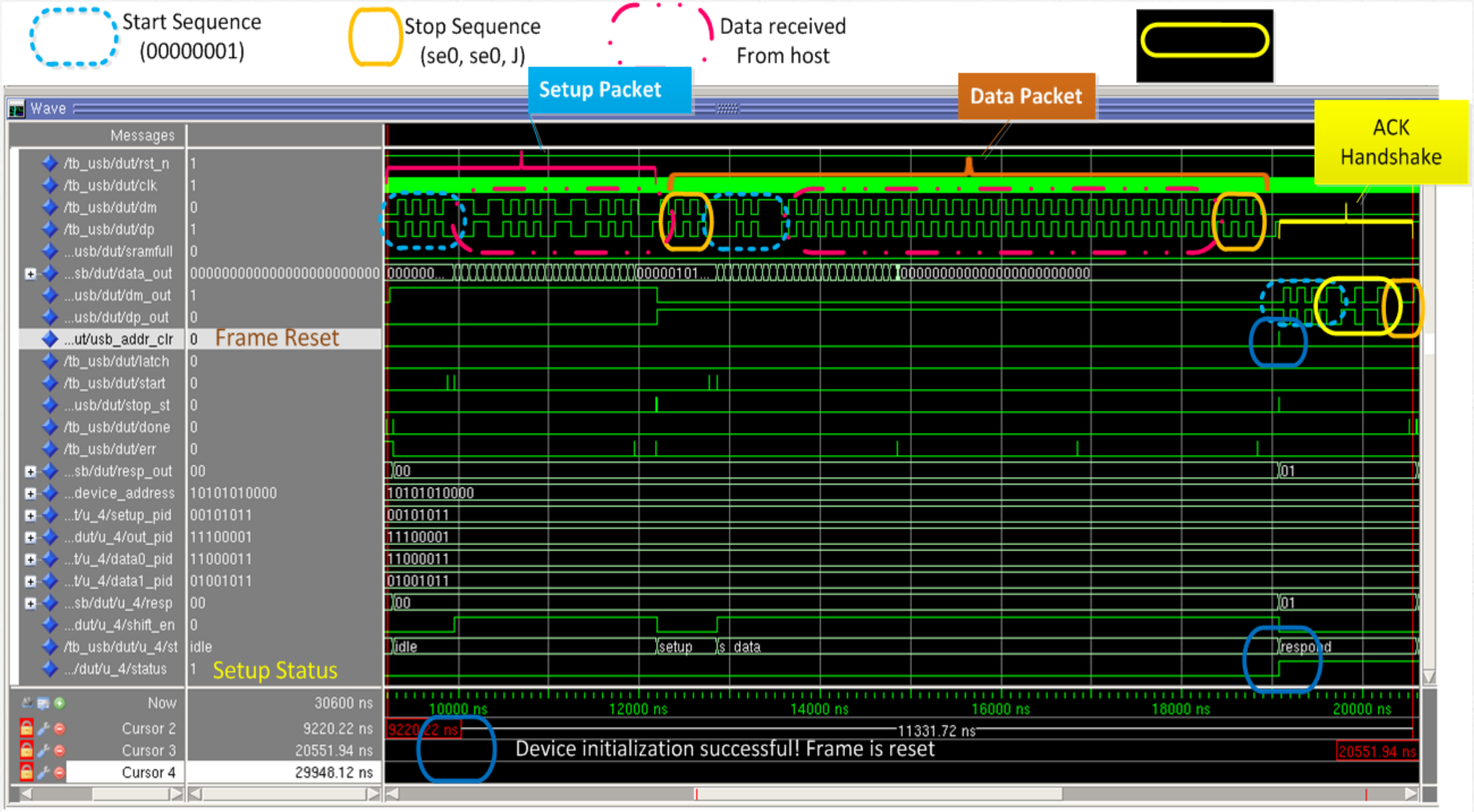
USB Source Simulation: Test 1



Messages	
/tb_usb/dut/rst_n	1
/tb_usb/dut/clk	1
/tb_usb/dut/dm	0
/tb_usb/dut/dp	1
...usb/dut/sramfull	0
...sb/dut/data_out	000000000000000000000000
...usb/dut/dm_out	1
...usb/dut/dp_out	0
...ut/usb_addr_clr	0
/tb_usb/dut/latch	0
/tb_usb/dut/start	0
...usb/dut/stop_st	0
/tb_usb/dut/done	0
/tb_usb/dut/err	0
...sb/dut/resp_out	00
...device_address	10101010000
...t/u_4/setup_pid	00101011
...dut/u_4/out_pid	11100001
...t/u_4/data0_pid	11000011
...t/u_4/data1_pid	01001011
...sb/dut/u_4/resp	00
...dut/u_4/shift_en	0
/tb_usb/dut/u_4/st	idle
.../dut/u_4/status	1
Now	30600 ns
Cursor 2	9220.22 ns
Cursor 3	20551.94 ns
Cursor 4	29948.12 ns

Device has not been initialized. Must reply STALL

USB Source Simulation: Test 2



Start Sequence (00000001)

Stop Sequence (se0, se0, J)

Data received From host

Setup Packet

Data Packet

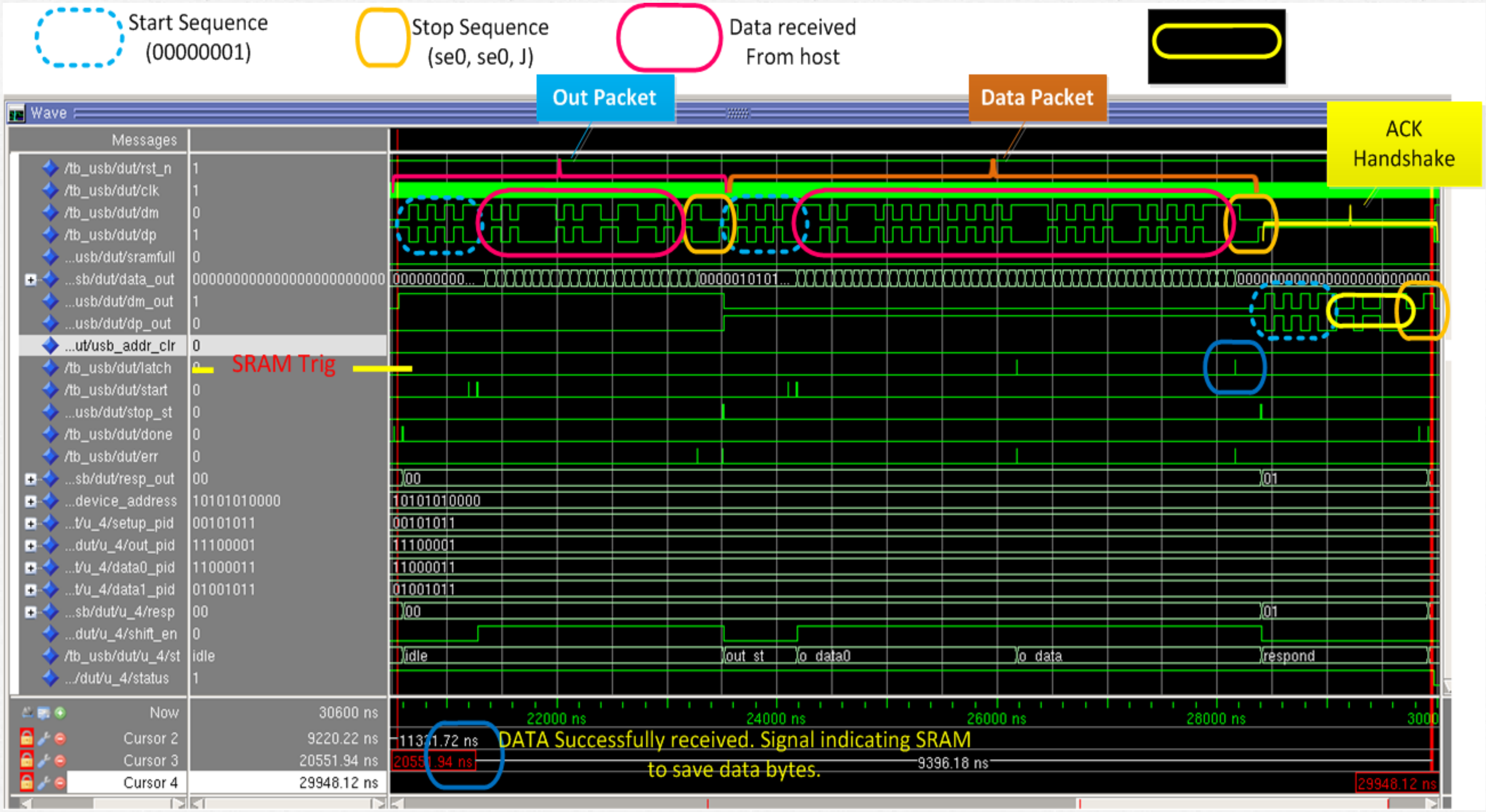
ACK Handshake

Wave

Messages	
/tb_usb/dut/rst_n	1
/tb_usb/dut/clk	1
/tb_usb/dut/dm	0
/tb_usb/dut/dp	1
...usb/dut/sramfull	0
...sb/dut/data_out	000000000000000000000000
...usb/dut/dm_out	1
...usb/dut/dp_out	0
...ut/usb_addr_clr	0 Frame Reset
/tb_usb/dut/latch	0
/tb_usb/dut/start	0
...usb/dut/stop_st	0
/tb_usb/dut/done	0
/tb_usb/dut/err	0
...sb/dut/resp_out	00
...device_address	10101010000
...t/u_4/setup_pid	00101011
...dut/u_4/out_pid	11100001
...t/u_4/data0_pid	11000011
...t/u_4/data1_pid	01001011
...sb/dut/u_4/resp	00
...dut/u_4/shift_en	0
/tb_usb/dut/u_4/st	idle
.../dut/u_4/status	1 Setup Status
Now	30600 ns
Cursor 2	9220.22 ns
Cursor 3	20551.94 ns
Cursor 4	29948.12 ns

Device initialization successful! Frame is reset

USB Source Simulation: Test 3



Start Sequence (00000001)

Stop Sequence (se0, se0, J)

Data received From host

Out Packet

Data Packet

ACK Handshake

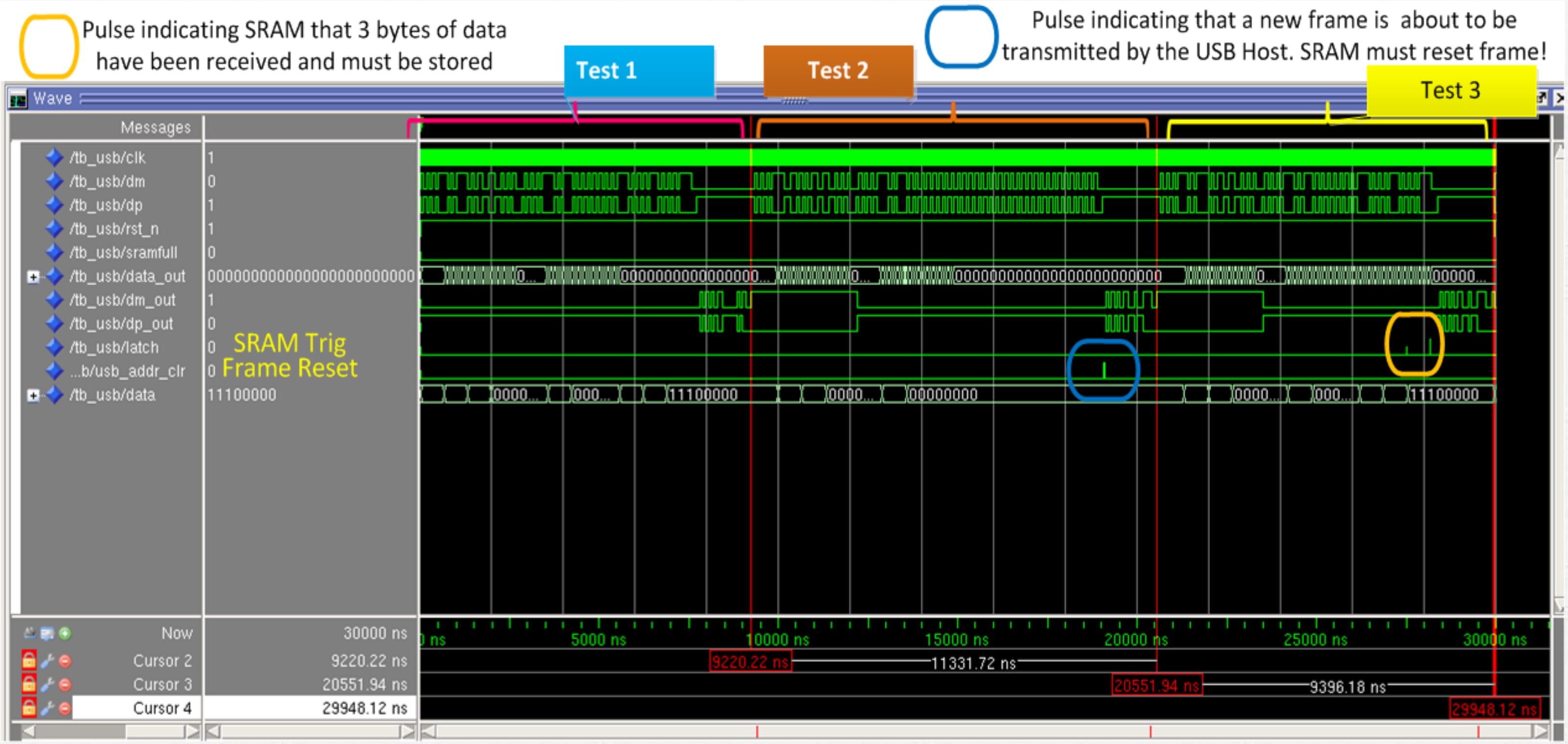
SRAM Trig

DATA Successfully received. Signal indicating SRAM to save data bytes.

```
Messages
/tb_usb/dut/rst_n        1
/tb_usb/dut/clk          1
/tb_usb/dut/dm           0
/tb_usb/dut/dp           1
...usb/dut/sramfull      0
...sb/dut/data_out       000000000000000000000000
...usb/dut/dm_out        1
...usb/dut/dp_out        0
...ut/usb_addr_clr       0
/tb_usb/dut/latch        0
/tb_usb/dut/start        0
...usb/dut/stop_st       0
/tb_usb/dut/done         0
/tb_usb/dut/err          0
...sb/dut/resp_out       00
...device_address        10101010000
...t/u_4/setup_pid       00101011
...dut/u_4/out_pid       11100001
...t/u_4/data0_pid       11000011
...t/u_4/data1_pid       01001011
...sb/dut/u_4/resp       00
...dut/u_4/shift_en      0
/tb_usb/dut/u_4/st       idle
.../dut/u_4/status       1

Now                      30600 ns
Cursor 2                 9220.22 ns
Cursor 3                 20551.94 ns
Cursor 4                 29948.12 ns
```

USB Mapped Simulation



Pulse indicating SRAM that 3 bytes of data have been received and must be stored

Pulse indicating that a new frame is about to be transmitted by the USB Host. SRAM must reset frame!

Test 1

Test 2

Test 3

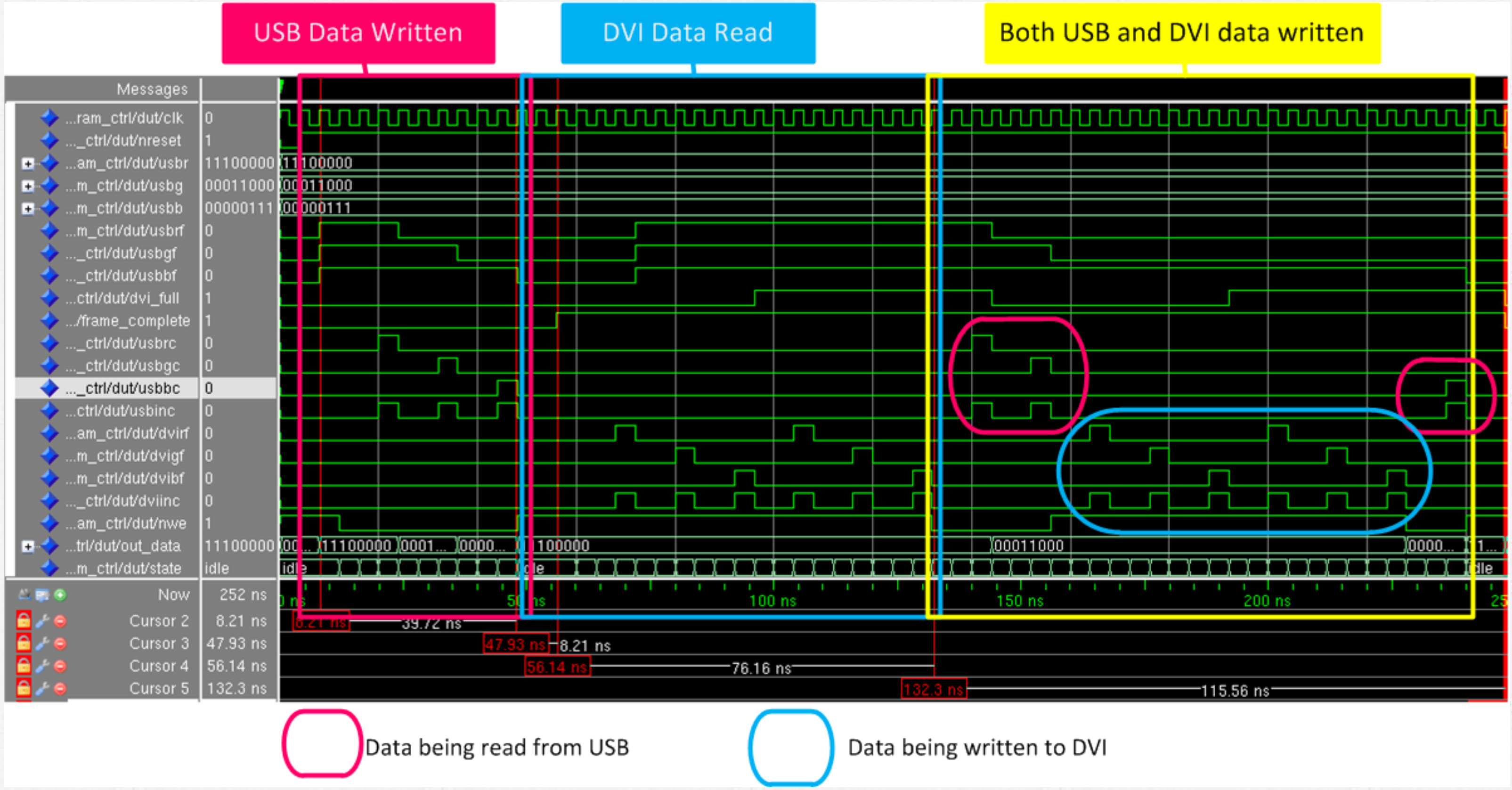
SRAM Trig

Frame Reset

```
Messages
/tb_usb/clk            1
/tb_usb/dm             0
/tb_usb/dp             1
/tb_usb/rst_n          1
/tb_usb/sramfull       0
/tb_usb/data_out       000000000000000000000000
/tb_usb/dm_out         1
/tb_usb/dp_out         0
/tb_usb/latch          0
...b/usb_addr_clr      0
/tb_usb/data           11100000

Now        30000 ns
Cursor 2   9220.22 ns
Cursor 3   20551.94 ns
Cursor 4   29948.12 ns
```

SRAM Simulation: CTRL



USB Data Written

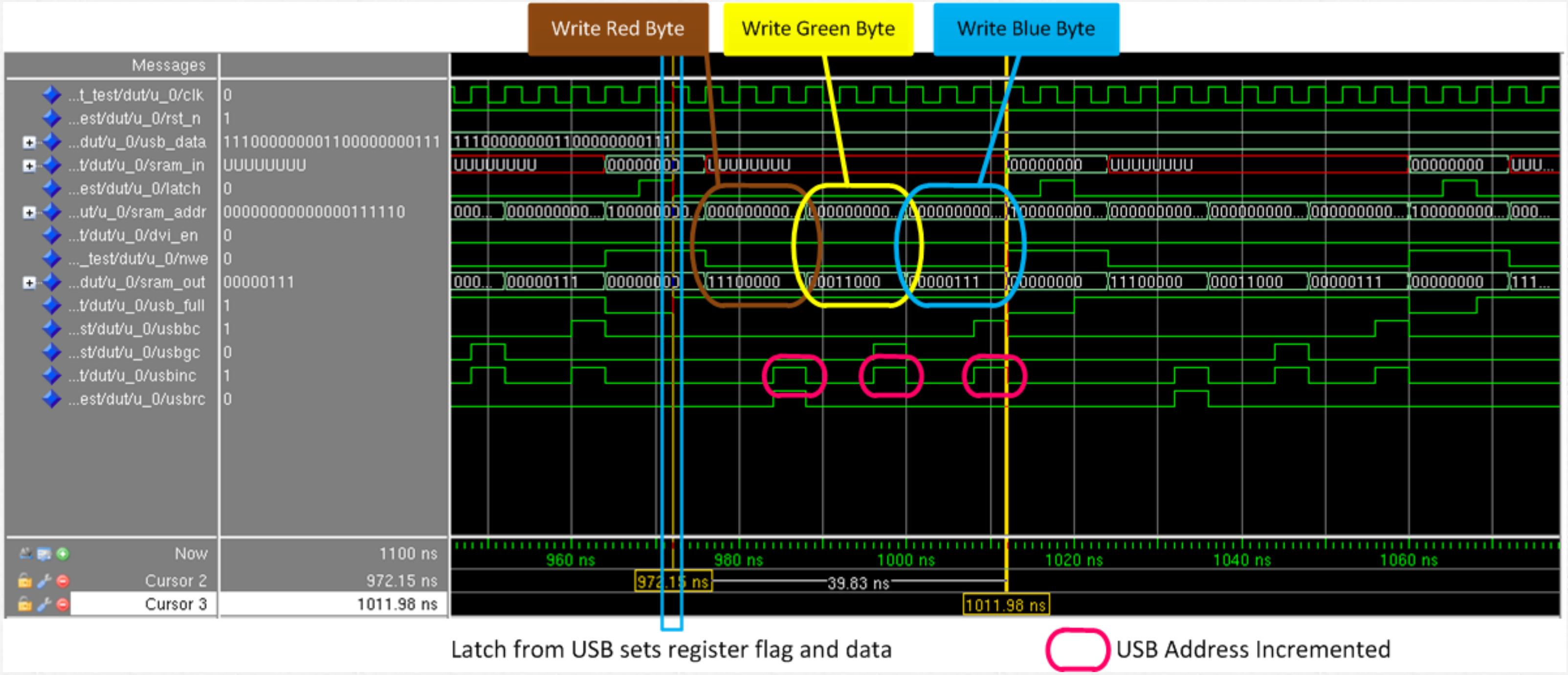
DVI Data Read

Both USB and DVI data written

Data being read from USB

Data being written to DVI

SRAM Simulation: Interface

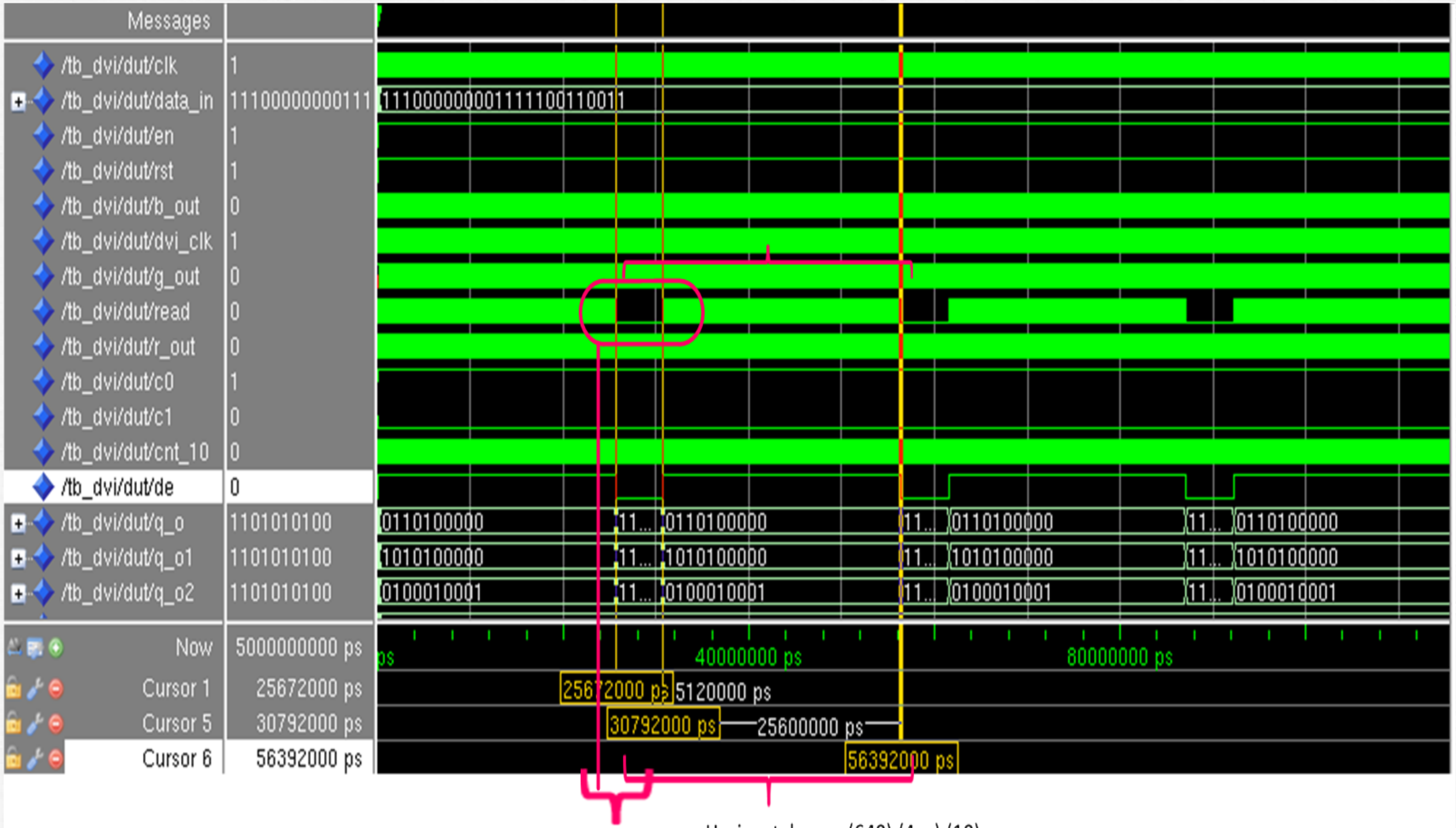


Messages	
...t_test/dut/u_0/clk	0
...est/dut/u_0/rst_n	1
...dut/u_0/usb_data	111000000001100000000111
...t/dut/u_0/sram_in	UUUUUUUU
...est/dut/u_0/latch	0
...ut/u_0/sram_addr	00000000000000111110
...t/dut/u_0/dvi_en	0
..._test/dut/u_0/nwe	0
...dut/u_0/sram_out	00000111
...t/dut/u_0/usb_full	1
...st/dut/u_0/usbbc	1
...st/dut/u_0/usbgc	0
...t/dut/u_0/usbinc	1
...est/dut/u_0/usbrc	0
Now	1100 ns
Cursor 2	972.15 ns
Cursor 3	1011.98 ns

Latch from USB sets register flag and data

USB Address Incremented

DVI Simulation: Periodic Cues



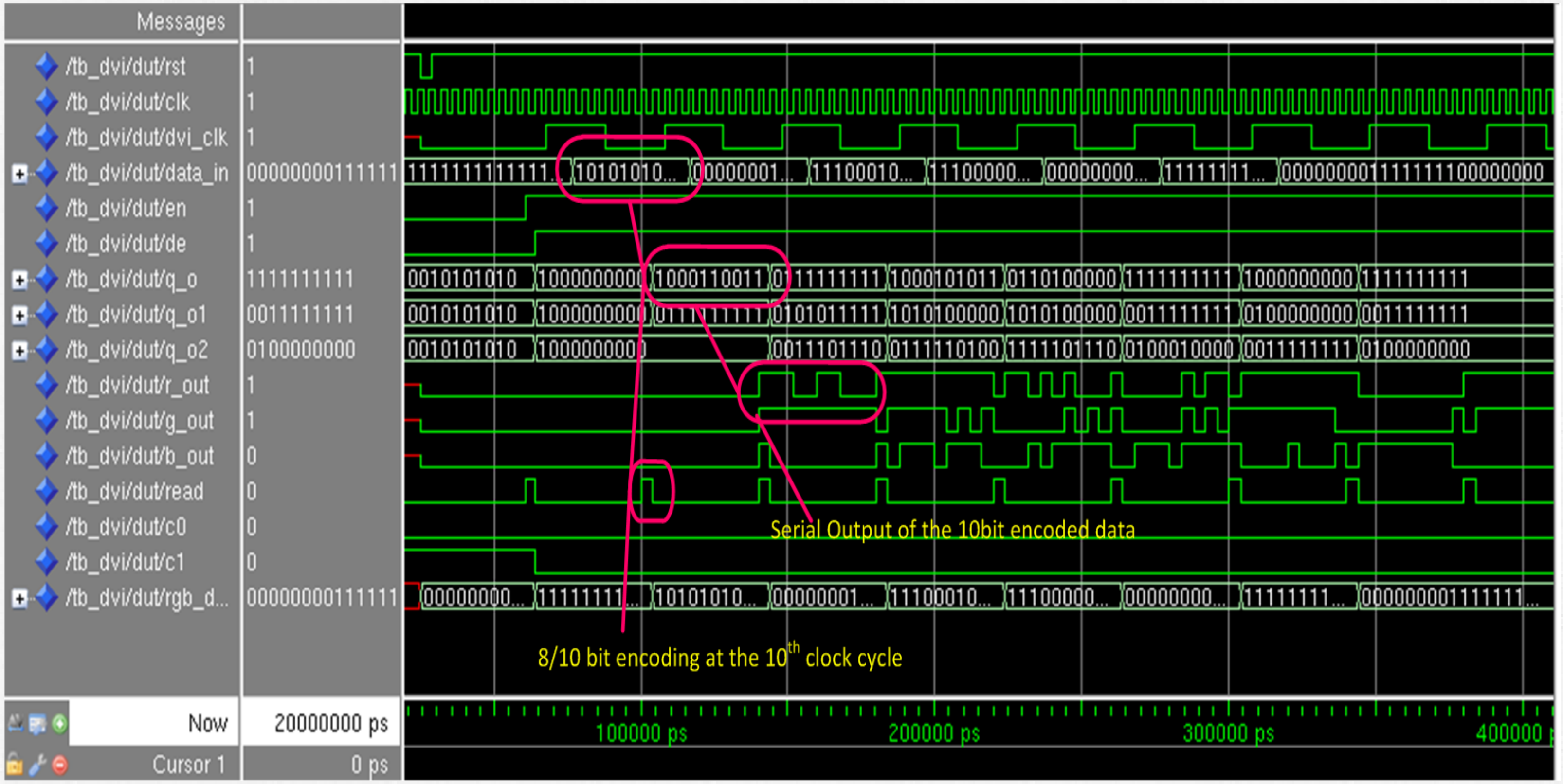
Messages	
/tb_dvi/dut/clk	1
/tb_dvi/dut/data_in	11100000000111
/tb_dvi/dut/en	1
/tb_dvi/dut/rst	1
/tb_dvi/dut/b_out	0
/tb_dvi/dut/dvi_clk	1
/tb_dvi/dut/g_out	0
/tb_dvi/dut/read	0
/tb_dvi/dut/r_out	0
/tb_dvi/dut/c0	1
/tb_dvi/dut/c1	0
/tb_dvi/dut/cnt_10	0
/tb_dvi/dut/de	0
/tb_dvi/dut/q_o	1101010100
/tb_dvi/dut/q_o1	1101010100
/tb_dvi/dut/q_o2	1101010100
Now	5000000000 ps
Cursor 1	25672000 ps
Cursor 5	30792000 ps
Cursor 6	56392000 ps

(128).(4ns).(10)

Horizontal sync: (640).(4ns).(10)

The TMDS data stream provides periodic cues for the decoder synchronization

DVI Simulation: 8/10 encoding (TMDS)



Messages	
/tb_dvi/dut/rst	1
/tb_dvi/dut/clk	1
/tb_dvi/dut/dvi_clk	1
/tb_dvi/dut/data_in	00000000111111
/tb_dvi/dut/en	1
/tb_dvi/dut/de	1
/tb_dvi/dut/q_o	1111111111
/tb_dvi/dut/q_o1	0011111111
/tb_dvi/dut/q_o2	0100000000
/tb_dvi/dut/r_out	1
/tb_dvi/dut/g_out	1
/tb_dvi/dut/b_out	0
/tb_dvi/dut/read	0
/tb_dvi/dut/c0	0
/tb_dvi/dut/c1	0
/tb_dvi/dut/rgb_d...	00000000111111
Now	20000000 ps
Cursor 1	0 ps

Serial Output of the 10bit encoded data

8/10 bit encoding at the 10th clock cycle

8/10 Bit TMDS Encoding

DATA = 10101010 .. No. of 1’s = 4 and D(0) = 0

```
q_m:    q_m (0) = D (0) = 0
        for 1 to 7
        q_m (i) = q_m (i-1) x Nor D(i)
        end i
        q_m (8) = 0;
        = 011001100
```

= 011001100

```
Cnt = 0
        q_m (8) = 0
        Q_0 = not q_m (8) & q_m (8) & q_m (7:0)’
```

= 1000110011

Summary and Conclusions

Chip Layout

- **Synthesis Results:**

Block	Area
Top Level	1.316394 mm^2
USB	0.203760 mm^2
SRAM	0.475515 mm^2
DVI	0.840879 mm^2

Block	Timing
Top Level	3.75 ns
USB	4.60 ns
SRAM	3.75 ns
DVI	3.54 ns

- **Budget Estimates:**
  - Area: ~1.3mm^2
  - Timing: 3.7ns
- **Total Pin Count: 39**

Success Criteria

- Successfully receiving a packet of data from USB bus according to USB 1.1 protocol. *(2)* – DONE!
- Successful transmission of Handshake packets by device according to USB 1.1 protocol. *(1.5)* – DONE!
- Successful 8/10 bit encoding for TMDS transmission. *(2)* – DONE!
- Successful transmission of encoded data and intermittent control signals according to TMDS specifications. *(1.5)* – DONE!
- Successful management of SRAM to allow for simultaneous storage of data from USB and reading of data for DVI transmission. *(1)* – DONE!

Conclusions

- **Challenges:**
  - Timing – Frequency rate of DVI and USB
    - 12 Mbps for USB, 600 Mbps for DVI
  - Memory Interfacing – Frame Repetition
    - SRAM choice: 2 Mb, 10 ns

- **Second Run and Improvements:**
  - Possibly USB 2.0
  - Incorporate a more extensive SETUP and IN cycle for USB
  - I2C Implementation in DVI

Thank You!