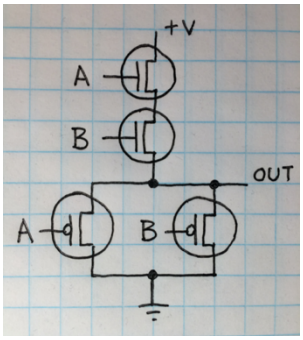
CS 250 Final Exam SOLUTION A
Spring 2017
Purdue University

Questions 3 through 52 scored at 3 points each.

1. **I have bubbled Test Form A next to the Date field on my bubble sheet** AND I have checked that my exam document has all 10 pages.
   A True
   B False

2. I will neither give nor receive aid on this exam. [Please abide by this policy.]
   A True
   B False

3. Consider this circuit with inputs A and B, output OUT, a +V supply voltage and a connection to ground.

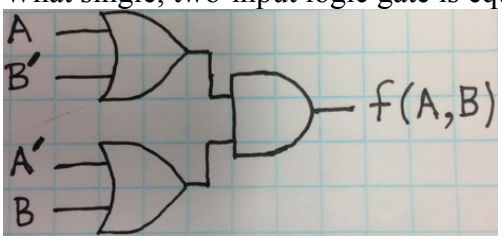


   How many different pairs of (A,B) voltage values correspond to an OUT voltage of ground, or 0 (zero) volts?
   A 0 **B** 1 **C** 2 **D** 3 **E** 4
   Answer: D 3; all of (A,B) that are elements of {(0,0), (0,1), (1,0)}.

4. Which circuit has an output that is a function of its inputs and past history of inputs?
   A Inverter
   B Adder
   C Decoder
   D Latch
   E None of the above
   Answer: D; all other choices listed are combinatorial devices, no history.

5. How many different input conditions for a full adder correspond to a Sum = 1 output?
   A 1 **B** 2 **C** 3 **D** 4 **E** 5
   Answer: D. Sum =1 when the sum of all three bits – Augend, Addend, and Carry In – is odd. There are 3 ways to have the total equal 1 and 1 way for the total to equal 3. (There is one way for the total to equal zero, and three ways for 2.)

6. What single, two-input logic gate is equivalent to the following circuit?



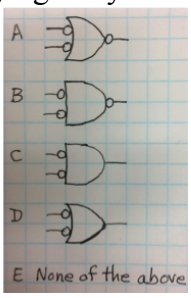
A AND **B** NAND **C** XOR **D** XNOR **E** NOR
Answer: XNOR

7. The logic values of inputs A and A' for the circuit in Question 6 are changed. How long must we wait before using the signal f(A,B)?
   A f(A,B) is always present, no need to wait
   B 30 nanoseconds
   C 3 gate delays
   D Insufficient information given to allow one of the above answers to be considered correct.
   E None of the above
   Answer: E. f(A,B) needs time to transition. 30 ns may be correct but exceeds information given to be considered correct. Gate delays is a unit that could be considered correct, but 3 is not the correct number; that would be 2. We can always count delay in terms of units of gate delay.

8. The most important logic gate parameter for the prevention of error is the
   A width of the voltage band representing logic 1
   B width of the voltage band representing logic 0
   C power supply voltage
   D gap between the highest logic 1 voltage and the lowest logic 0 voltage
   E gap between the lowest logic 1 voltage and the highest logic 0 voltage
   Answer: E. This is the gap region between the logic 1 and logic 0 voltage bands.

9. Which one of the logic gate symbols corresponds to the truth table?

X	Y	f(X,Y)
0	0	0
0	1	1
1	0	1
1	1	1



Answer: The truth table is of an OR gate, which is depicted by choice B.

10. Which of the following does not belong with the others?
    A Hexadecimal
    B 1's complement
    C IEEE 754 floating point

D Packed BCD
E Signed digit
Answer: Hexadecimal. All the others are number representations. Hexadecimal is only shorthand for writing meaningless binary strings.

11. Which part of a machine language instruction specifies the data type(s) of the operands?
A Data types only exist in programming languages such as C, C++ and higher and not in assembly language or machine language
B The opcode field
C The register field(s)
D The offset field
E All machine language instruction fields must be examined to determine operand data type(s)
Answer: B. Hardware has native data types that typically include integer and floating point, and nothing else. Registers can hold either of these types, as well as meaningless bit strings, hence these fields say nothing. The offset field is only one of the perhaps several operand fields. The opcode field defines how all the operands are used and interpreted.

12. An example of a C language statement that will cause replacement of the default_next_instruction_pointer address in the processor with a different address is
A while (j < 10) { j = j * j; }
B if (x == 0) { j = 5; }
C for (int j = 0; j < 10; ++j) { array[j] = j * j; }
D break;
E All of the above
Answer: E. At some time during their execution all of these program constructs branch to an instruction that is not the default next instruction.

13. Operation of the processor circuit of Figure 6.9 is controlled in part by the three multiplexers M1, M2, and M3 as they are commanded to select from their upper and lower inputs. (The "upper input" for each multiplexer is the input that is closer to the top of Figure 6.9.) Which of the following is used to execute a STORE instruction?
A M1 selects upper, M2 selects upper, and M3 selects upper
B M1 selects lower, M2 selects upper, and M3 selects upper
C M1 selects upper, M2 selects lower, and M3 selects lower
D M1 selects lower, M2 selects lower, and M3 selects lower
E None of the above is correct
Answer: D. M1 is lower because the next instruction after a STORE is the instruction at the default location, M2 is lower because the STORE needs to add the offset value to the base address from its register operand, and while M3 control is "don't care," lower will get the job done.

14. According to Figure 6.2, 00001001101000010000101110101111 means
A Nothing, bit strings are meaningless

B r3 ← r4 + r2
C r3 ← r2 + r4
D r3 ← r4 + r2 + 0x0BAF
E None of the above are correct
Answer: E. r2 ← r3 + r4 is the meaning per Figure 6.2.

15. Consider the very simple processor of Figure 6.9 and its instruction set in Figure 6.2 and its associated definitions of the four instructions (see exam cover pages). Which of the following, if any, will not affect the correct operation of this simple processor?
A Wiring the control signal for M3 to either ground or Vdd
B Changing the 32-bit adder upper input to 8
C Making the instr. decoder operation output always be the 5-bit opcode for the add instruction
D Enabling data_in to write to the register unit at all times
E All of the above will cause the processor to operate incorrectly in some way
Answer: C. Every one of the four instructions needs the ALU to perform an integer add. So, OK, hardwiring this would work, if the control of the multiplexers is not disrupted from what it was. Choice A, hardwiring M3 breaks the difference between LOAD and ADD, for example. Choice B breaks the ability to fetch the default next instruction. Choice D means that the JUMP address from ALU output will be written to the register matching the address in the "unused" dst_reg field. Yikes! Because C, not E.

16. The instruction format of Figure 6.2 is sufficient to access any location in a memory containing 2^{32} locations for how many of the five addressing modes shown in Figure 7.6?
A 1 **B** 2 **C** 3 **D** 4 **E** 5
Answer: B. Modes 4 and 5, or indirect through a register and indirect memory reference, can address all 2^32 locations.

17. The diagram of Figure 6.9 is at what level of abstraction?
A Transistor
B Gate
C Function unit
D Computer
E None of the above
Answer: C.

18. What type or types of hazard can be eliminated by prediction?
A Structural hazard
B Control hazard
C Data hazard
D Both B and C
E None of the above
Answer: B, as in branch prediction. The structural hazard cure is more (intelligently chosen) hardware. Some data hazards can be eliminated by re-

naming. True data dependences cannot be eliminated from a program.

19. How many of these computer architecture characteristics are visible in assembly language code: delayed branch instruction, 5-stage pipeline, L1 cache, and the use of data forwarding?
A 0 **B** 1 **C** 2 **D** 3 **E** All 4
Answer: B, delayed branch instruction is visible because its delay slot(s) must be filled, with useful instructions we hope, with NOPs otherwise.

20. Consider this C code snippet associated with the operation and control of an I/O device.

```
int * p = (int *) 0x20000000  // initialize pointer; assume int type size is 4 bytes
if (*p == 0) return -1;  // error condition
*(p + 1) = 1;
while (*(p + 3) != 0);
*(p + 2) = 1;
while (*(p + 3) != 0);
```

This code performs
A an infinite loop
B a store to command an I/O device action
C a load to command an I/O device action
D interrupt-driven I/O
E Two of the above
Answer: B. A is false because this is to control an I/O device and so the while loops are reading from the CSR address area of the device. C is false because the code lines just before the while loops are the ones controlling the device, and they both write a value to a memory address. This code is polling, via the while loops, so D is false. E is thus seen to be false.

21. The I/O device being controlled by the C code of the preceding question
A uses address 0x2000000C as a location to accept input
B is a printer
C uses address *(p + 1) as a location to store input
D likely performs at least two distinct actions
E None of the above is correct
Answer: D. Address 0x2000000C = *(p + 3) and is read by the code, so A describes the opposite of what occurs. We have no information that B is true. The code writes a 1 to location *(p + 1) where an I/O device would read and act upon that input (command), rather than storing it, ruling out C. Both location *(p + 1) and location *(p + 2) are written to by the code, strongly suggesting that there are two different commands accepted by the I/O device, likely corresponding to two distinct actions. E is ruled out by D.

22. An instruction has been fetched and then, before the instruction is executed, the processor is interrupted. This is
    A possible when polling is being used for I/O.
    B impossible, because interrupts are checked before an instruction is fetched.
    C possible when a processor is pipelined.
    D impossible when there is an instruction cache operating at the same speed as the processor.
    E None of the above
    Answer: C. A pipeline will fetch an instruction and then fetch the default next instruction before the first instruction executes. Interrupts will be checked between these two fetches, which may result in the processor being interrupted, all before the first instruction has yet to execute. Choice A is a contradiction because polling is the alternative to interrupt-driven I/O. B seems promising, but then there is C. D fails because memory hierarchy speed has nothing to do with the sequence of operations that will be executed for a program being interrupted.

23. The L1 cache of a 32-bit computer is direct-mapped, has 1024 blocks each holding 16 bytes, and includes a dirty bit. Which one of the following does this cache have the most of?
    A Tag bits
    B Valid bits
    C Dirty bits
    D XOR gates
    E Bytes of block memory
    Answer: A. There are 16-byte blocks, thus 4 offset bits; 1024 blocks, thus 10 index bits; thus, 32-4-10 = 18 tag bits per block. Direct mapped means 1 block per index. Valid and dirty bits come 1 per block. XOR gates are used to compare tag bits, 1 gate per 1 tag bit, of the block selected by the index bits, with CPU-provided address bits. This is enough to count up everything in all the bits and gates.
    Tag bits (total) = 18 bits/block * 1024 blocks = 18 Kbits
    Valid bits (total) = 1 bit/block * 1024 blocks = 1 Kbit
    Dirty bits (total) = 1 bit/block * 1024 blocks = 1 Kbit
    XOR gates (total) = 1 gate/tag-bit-of-selected-block &address-bit pair * 18 tag-bits-of-selected-block = 18 gates
    Bytes of block memory = 2^(# index field bits + # offset field bits) bytes = 2^(10+4) bytes = 2^14 bytes = 16 Kbytes
    So 18K versus 16K versus 1K versus 18. 18K is the maximum.

24. The stages of a pipeline have propagation delays of 20, 40, 40, 30, and 10 nanoseconds (ns), or 10^{-9} seconds, respectively. The stage registers each have 5 ns of propagation delay to record an input. Ideally, how much faster is this processor because of pipelining?
    A 40/5
    B 140/40
    C 115/40

D 10/5
E None of the above.
Answer: The maximum clock rate for the pipelined processor is 40 ns. There are 4 pipelining registers added to the non-pipelined version of this processor, so the total propagation delay in the non-pipelined circuit is 20-5+40-5+40-5+30-5+10 = 120 ns. Thus, the speedup from pipelining is 120ns/40ns = 3. So, E.

25. To incorporate vertical microcode in the implementation of the processor shown in Figure 6.9, we must add
A a 16-bit version of the ALU
B the option to compute the default_next_instruction_address as current_instruction_pointer + 2
C the ability to hold two 16-bit operands in a single register in the register unit
D an instruction memory and ability to fetch from it
E All of the above
Answer: D. Neither A nor B is appropriate, and C is not necessary or likely of much use.

26. Assume that a computer has a physical memory organized into 64-bit words. How many of the following byte addresses are aligned? Addresses: 0, 6, 16, 30, 120, and 256.
A 2 **B** 3 **C** 4 **D** 5 **E** 6
Answer: C. All that are multiples of 8 are aligned, which is 0, 16, 120, and 256, so 4 are aligned.

27. Physical main memory has 8 word-addressed modules and 8-way interleaving to improve performance. Each module can be accessed during one clock cycle and then requires 3 more clock cycles before it can be accessed again. That is, if clock cycle i = memory access, then clock cycle i+2 = rest, clock cycle i+3 = rest, clock cycle i+4 = rest, and clock cycle i+5 and later are ready if an access is made. The following word access patterns are used to test the performance of this memory:
Test pattern 1: Access word j, j+1, j+2, j+3, j+4, j+5, …
Test pattern 2: Access word j, j+2, j+4, j+6, j+8, j+10, …
Test pattern 3: Access word j, j+4, j+8, j+12, j+16, j+20, …
Test pattern 4: Access word j, j+5, j+10, j+15, j+20, j+25, …
How many of the four word address patterns do not stall?
A 4 **B** 3 **C** 2 **D** 1 **E** 0
Answer: Analyzing the four test patterns for the stride, we see that
Test pattern 1: has stride = 1, accesses all 8 modules, and accesses a given memory module after 8 clock cycles. No stall.
Test pattern 2: has stride = 2, accesses only 4 of the 8 modules, and accesses a given memory module after 4 clock cycles. No stall.
Test pattern 3: has stride = 4, accesses only 2 of the 8 modules (not good), and access a given memory module after just 2 clock cycles. Stalls 2 cycles.
Test pattern 4: has stride = 5, accesses all 8 memory modules because 5 and 8 are relatively prime, and thus accesses a given memory module after 8 clock cycles.

No stall cycles.
Only test pattern 3 accesses fewer than four of the modules, so only pattern 3 stalls, leaving three patterns that do not stall. Answer B.

28. The designer of a direct-mapped cache says that the cache has16-byte blocks and is constructed from 1-bit SRAM latches. If the designer next says that the cache is write-back and has 20-bit tags, is this enough information to determine the total number of 1-bit SRAM latches in the circuit for this cache?
    A Yes
    B No
    Answer: B. Without knowing the number of bits in an address, the size of the index field cannot be known. Without the index field size, the number of blocks is not knowable, so the number of SRAM latches used to build the cache blocks is not knowable.

29. Reducing the time to find and transfer a block in the L2 cache (faster latches and logic gates) up to the L1 cache improves
    A L1 hit time
    B L1 hit rate
    C L1 miss rate
    D L1 miss penalty
    E None of the above
    Answer: D. A quicker response from L2 reduces the penalty for missing in L1.

30. Which program structure is likely to have the highest cache hit rate?
    A a basic block
    B an if statement
    C a switch statement
    D a for loop
    E Cache hit rate is so poorly correlated to high-level language statement types that none of the above is a good candidate for highest cache hit rate.
    Answer: D. A basic block, if statement, and switch statement are all variations on straight line code. Without re-fetching any instructions, the opportunity for cache hits is somewhat lessened. A for loop gives the opportunity for increased program locality by virtue of re-fetching the instructions of the loop over some number of iterations.

31. Which one of the following does not belong with the others?
    A Direct-mapped
    B Instruction cache
    C Valid bit
    D Dirty bit
    E 4-word block
    Answer: D or B. D is justified for the viewpoint that because an instruction cache should not be writeable, there is no need for a dirty bit. Answer B is justified because “instruction cache” is a usage choice that is at a different level of

abstraction than the other four choices.

32. Assume that a page table entry occupies 32 bits, page size is 8 Kbytes, memory addresses are 32 bits, and memory is byte-addressed. How many megabytes of memory will a single-level page table occupy for this example computer?
    A 0.25 **B** 0.50 **C** 1.0 **D** 2.0 **E** 4.0
    Answer: D. Offset within page requires 13 bits of the 32-bit address, so page number occupies 19 bits for 0.5 Mega-pages. Each page entry occupies 4 bytes, so the table size is 0.5 Mega-entries * 4 bytes/entry = 2 Mbytes.

33. What is the purpose of a "Used?" bit in a virtual memory page table entry?
    A To indicate that the page is dirty
    B To support the policy for page replacement in DRAM
    C To indicate that the given page has been loaded into DRAM more than once
    D To indicate that the given page is in use
    E None of the above
    Answer: B. A used bit could guide the selection of a page to replace (presumably not one that is marked used).

34. For which of the following actions must a virtual address be translated into a physical address?
    A The CPU executes a store instruction
    B Responding to an L1 cache miss
    C Placing a page into a page frame in main memory (DRAM)
    D To read from a main memory location that has not been copied to cache
    E None of the above require a virtual to physical address translation
    Answer: D. This location will, by definition, miss in all levels of cache. Thus, the address will reach the Memory Management Unit, where it will be translated. For A, the store could be captured in a write-back cache, and no translation required. For B, the miss might be satisfied in the virtually-addressed L2 cache. For C, the addressing is from the page replacement algorithm, which must work within the physical addresses of DRAM to be able to refer to the chosen page frame.

35. If the virtual address is 0x00003003 and the page size is 8 Kbytes, what is the page number plus the offset, expressed in hexadecimal notation?
    A 0x00006 **B** 0x08004 **C** 0x01004 **D** 0x03003 **E** None are correct
    Answer: C. The offset field is for 8 Kbytes, so has a size of 13 bits. In hexadecimal notation: 0x00001 + 0x1003 = 0x01004.

36. A system call is more time consuming than a function call because
    A the processor must change mode from user to system
    B the processor must switch contexts from the application to the operating system
    C the processor must copy information from the application address space to the operating system address space
    D all of the above three reasons

E none of the above reasons
Answer: D.

37. How many of the computer types in the Flynn taxonomy execute N instructions at a time?
A 4 **B** 3 **C** 2 **D** 1 **E** 0
Answer: C. MISD, and MIMD can execute N instructions at a time. SISD and SIMD execute one instruction at a time.

38. Which instruction type requires the use of a processing element enable stack in the processing elements of an SIMD computer?
A Load
B Register-register
C Jump to subroutine
D Conditional branch
E None of the above
Answer: D.

39. Which Flynn taxonomy architectures are most similar in their execution of the program statement if (A) { B; } else { C; } ?
A SISD and SIMD
B SIMD and MISD and MIMD
C MIMD and SISD and SIMD
D MIMD and SISD
E All four architecture types execute if–else very much the same way.
Answer: D. Each processor in an MIMD or in an MISD computer behaves the same way as the single SISD processor when executing an if–else statement: they all skip the code not selected by the tested condition. SIMD must "linearize" the if–else statement and broadcast both the then and else parts of the statement to all processors. Thus, SIMD must not be paired with the other three types. Answer D does not include SIMD, and thus is the correct answer.

40. When a request passes across the main memory bus, all attached memory modules receive the request. A module only responds if the address in the request lies within the range that has been assigned by its hardware I/O socket to that memory module. This behavior of a memory module is analogous to that of a PE in an SIMD computer executing or ignoring an instruction from the Control Unit. The address on the main memory bus is analogous to what aspect of an SIMD computer?
A The instruction placed on the bus connecting the control unit to the PEs
B The address of the instruction that the control unit broadcasts to the PEs
C The value on the top of the processor enable stacks
D The load or store address for each PE if the control unit broadcasts a load or a store
E The address on the interconnection network linking the PE memory units for data transfer
Answer: A. PEs examine the broadcast instruction and if it is a control type they

execute it and if the instruction is a non-control type then the PE may ignore or execute the instruction based on the value of the top of its enable stack.

41. A computer has four CPU cores plus two GPU cores. This system likely has
    A symmetric parallelism
    B asymmetric parallelism
    C Neither answer A nor answer B are correct.
    D Both answer A and answer B are correct.
    Answer: D. The like cores (4 of CPU and 2 of GPU) show symmetric parallelism is present, if the cores are identical. The dissimilar cores show asymmetric parallelism exists in the machine.

42. Device driver software
    A uses buffering
    B makes it easier to write the software for applications that perform I/O
    C is typically divided into three parts: upper half, lower half, and shared variables
    D All of the above statements are true.
    E Some, but not all, of the above statements are false.
    Answer: E, because A is optional for a device driver, but B and C are true.

43. Buffered I/O
    A improves throughput by doing less work.
    B should flush the buffer often.
    C improves the performance of text editor applications.
    D is not possible with interrupt-driven I/O.
    E None of the above
    Answer: A. The work reduction referred to in A is making far fewer system calls. Because A is true, it is also true that B should be done rarely to obtain the most benefit from buffering. Text editor applications need to put each typed character up on the screen as soon as possible, so C is false. Buffering is fully compatible with interrupt-driven I/O, so answer D is false. Because A, not E.

44. A serial interface operates at a throughput of 100 million bits per second and requires 100 microseconds to configure (prepare) a packet of bits to be transmitted regardless of the size of the packet. The most common case for processor-to-processor messages in an MIMD computer is a series of short messages each conveying a few data items. What improvement would most improve MIMD computer performance if this interface is to be used for processor-to-processor communication?
    A Increase the bits per second throughput rate
    B Decrease the time to configure a packet of bits to be transmitted
    Answer: B. Shorter messages are given to be the most common case. The time taken for shorter messages of a few data items will be the configuration time. Reducing configuration time will, by Amdahl's Law, offer more improvement than increasing bits per second throughput rate.

45. If interrupts are disabled, this means

A I/O devices must revert to polling for their operation
B I/O data transfers can be lost
C a user application is running at this time
D there has been a page fault
E None of the above
Answer: B. Per one of our homework problems, leaving interrupts disabled for too long can "starve" an I/O device of support leading to data loss and worse. I/O devices designed for providing and responding to interrupts are not likely to be suitable for polling-based operation. Interrupts a never disabled during the running of that lowest of priority computations called a user application. While interrupts may be disabled at the time of a page fault this is not required, nor particularly likely.

46. A bus controller
A is not necessary if the assembly language programmer is careful
B provides an API for using the bus
C is only necessary for a device sending information on the bus
D is usually part of the bus and not part of the chips connected to the bus
E All of the above
Answer: B. For A, care is not the issue, simple electronic compatibility is the concern. For C, receivers need a controller as well. For D, see the figures in oru text and lecture slides for the hardware configuration. Typically, the bus is implemented as a simple set of wires, with all the circuit-based intelligence placed within the attached device.

47. Which software memory operation is easier for parallel computer hardware to support?
A reading
B writing
Answer: A. Reading does not require coordination. Writing may require locking to ensure atomicity.

48. Your manager asks you to parallelize the company software application to run on up to N processors. The application has a shared variable that will be updated by every processor from time to time. Executing the critical section code that updates this shared variable, including the lock and release instructions to provide mutual exclusion, uses 1 percent of the total time to run the application. The rest of the application is embarrassingly parallel, so execution time decreases in proportion to the number of processors available. The maximum overall speedup possible for this application from running it on N processors is
A equal to 1
B approximately 10
C no more than 100
D up to N
E None of the above
Answer: C. The 1% critical section cannot be parallelized, so 99% of this

application can be enhanced by the available N processors. An embarrassingly parallel application speeds up in proportion to the number of processors, so the speedup due to enhancement is N. Using Amdahl's Law, overall speedup is 1/(1 – 0.99 + 0.99/N) = 1/(0.01 + 0.99/N). As N approaches infinity, 0.99/N approaches zero, so overall speedup approaches 1/0.01 = 100 from below.

49. Which factor has the greatest effect on processor power consumption?
    A clock rate
    B supply voltage, Vdd
    C the fraction of the processor circuit that is actively switching logic levels
    Answer: B, because Vdd is a quadratic term in the average power equation on textbook page 398.

50. The timer coalescing technique for energy saving increases the probability that a processor can sleep long enough to save more energy than required to enter sleep mode and then recover to actively executing instructions.
    A True
    B False
    Answer: A, true, because the interval between coalesced timers is greater than between non-coalesced timers, so, when put to sleep a processor will tend to be able to stay asleep for a longer time.

51. SPEC benchmarks are
    A reproducible
    B similar to actual workloads
    C portable among computers
    D measure time
    E all of the above
    Answer: E.

52. The design of a new machine (computer) should be based on
    A Available technology
    B Affordable technology
    C Technology performance
    D Predicted technology trends
    E All of the above
    Answer: E