CS 250 Midterm Exam 01 SOLUTION
Purdue University
Fall 2016

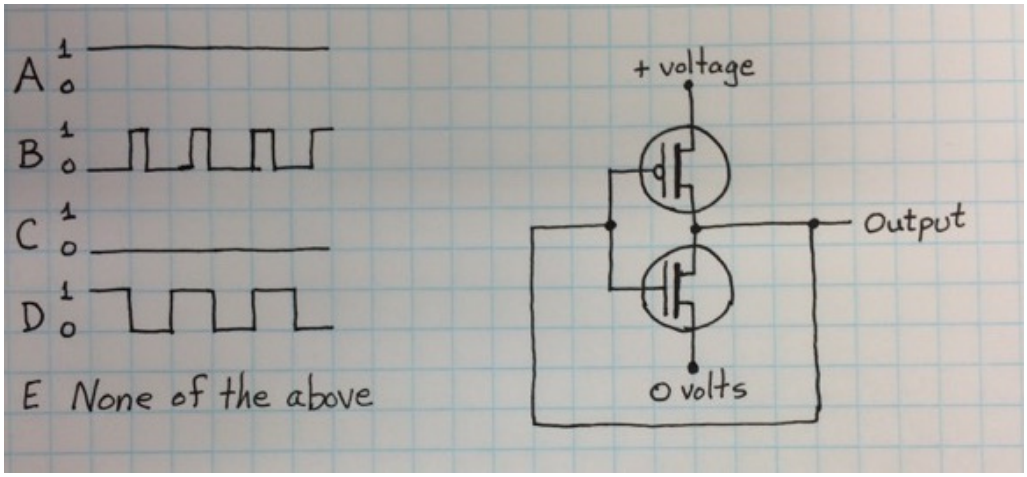
1. Technology change is a significant concern of computer designers and programmers.
   A True New technologies change the way we choose to design and program computers.
   B False

2. Abstraction is a technique for removing or omitting details.
   A True
   B False

3. The bit string 01001001 has no meaning.
   A True A bit string has no meaning until we define how we will interpret it.
   B False

4. Computer hardware is designed to have a failure probability much less than
   A 0.000000001 Failure rates less that 1 part in 10^9 are necessary for successful computation involving billions of steps.
   B 0.000001
   C 0.001
   D Zero Failure propability cannot be less than zero, no matter how we may wish so.
   E None of the above

5. At approximately one second after power is applied to this circuit, which waveform best represents what would be observed, using appropriate measuring instruments, for the signal labeled Output?



Answer: D This is the inverter circuit; with feedback it will oscillate. The high and low logic levels in the oscillating signal are set by the propagation delay through the circuit, which is very similar whether the transition is from high to low or low to high. Waveform D is the best choice. I could have drawn it better.

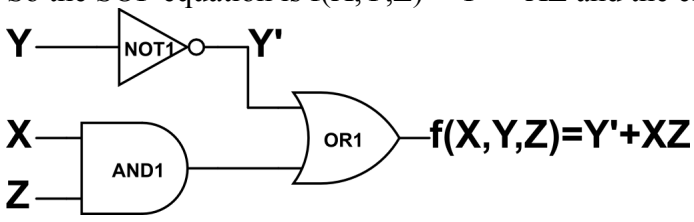
6. Consider this Karnaugh map for inputs X, Y, and Z.

f(X,Y,Z)	XY = 00	XY = 01	XY = 11	XY =10
Z = 0	1	0	0	1
Z = 1	1	0	1	1

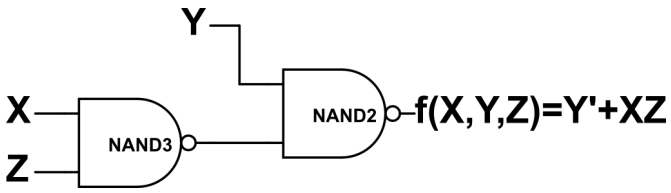
Assume that you have access only to X, Y, and Z, so if you want Z', your circuit must compute it. A minimal sum of products circuit to implement this truth table has

A Three two-input NAND gates
B **Two two-input NAND gates**
C One four-input NAND gate and an inverter
D Five two-input NAND gates
E None of the above is correct

Grouping 4 ones from the left and right columns yields the product term Y'. Grouping the final one with the one in the lower right corner yields the term XZ. So the SOP equation is f(X,Y,Z) = Y' + XZ and the circuit is



which, by DeMorgan's Law is equivalent to the circuit



7. Consider the following two Boolean functions of A and B named Function 1 and Function 2.

A	B	Function 1	Function 2
0	0	1	1
0	1	1	0
1	0	0	0
1	1	0	0

We want to compare the complexity of the minimal circuit necessary to implement each function. Only wire and CMOS transistors may be used to construct the circuit for each function. Any amount of wire is to be considered less complex than one transistor. Which of the following complexity rankings is correct?

A **Function 1 < Function 2** Function 1 is an inverter, which requires wire and 2 CMOS transistors (text Figure 2.3). Function 2 is a NOR gate, which requires wire and 4 CMOS transistors (Homework 01 Question 04 solution).
B Function 2 < Function 1
C Function 1 = Function 2

8. When software would use iteration, hardware uses
A An increase in supply voltage
B **Replication** Consider how multiple bit numbers can be added by stringing together copies of the full adder.
C Higher speed gates
D Exclusive-Or gates
E None of the above

9. To point to one of 20 locations requires
A A positive, 5-bit sign-magnitude pointer
B **A 5-bit-long string for pointing** A 4-bit string can provide only 16 pointer values: too few. A 5-bit string provides 2^5 which is sufficient. More than 5 bits is not required by virtue of being excessive.
C A 20-bit-long string for pointing
D A decoder with 32 or more outputs
E A decoder with 20 inputs

10. The truth table for a 4-bit adder made from full adders has how many rows?
A 4
B 16
C 256
D 2^{256}

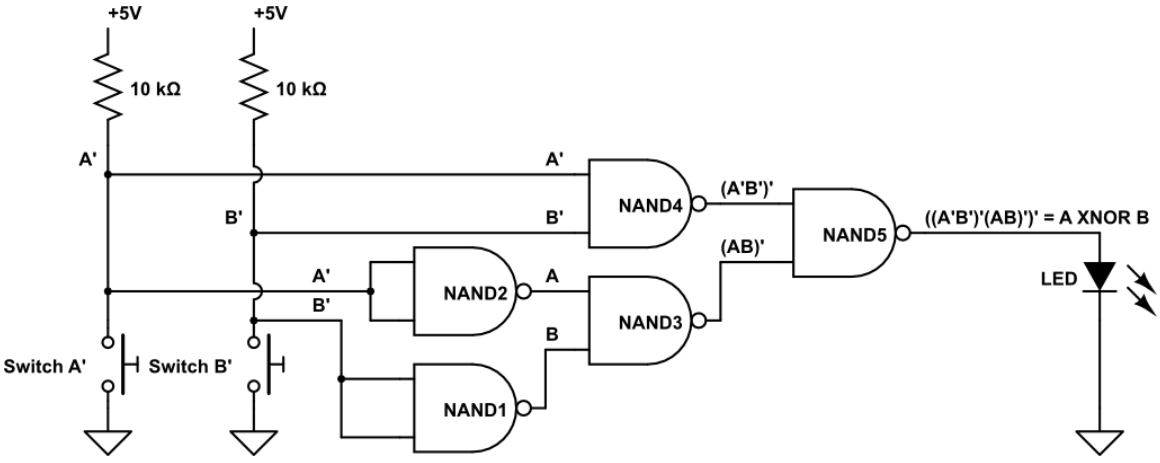
E **None of the above** The inputs to a 4-bit adder made from full adders are 4 bits of addend, 4 bits of augend, and 1 bit of carry in. The answer of 2^9 rows or 512.

11. Which adder circuit type operates the fastest assuming that all gate delays are equal and all wire lengths are equal.
    A 1's complement
    B **2's complement** 2's complement avoids the end around carry required of 1's complement
    C 1's and 2's complement are equally fast
    D 1's complement is faster than 2's complement for some (addend, augend) pairs
    E None of the above answers is correct.

12. Which of the following expressions and notations represents or corresponds to the most negative value possible for an 8-bit 2's complement number?
    A 11111111
    B **0x80** The most negative 8-bit 2's complement number has the form 1000 0000, with a space added for readability. It's value is -2^7 or -128.
    C $-(2^7 - 1)$ This is the most negative value possible with 8-bit 1's complement.
    D $-(2^8 - 1)$
    E None of the above answers is correct

13. The bit string 1001000000011101 is a negative packed BCD value.
    A **True** This string is 0x901D where the digits of the number are 901 and D represents the minus sign.
    B False

Consider the circuit below, which was constructed for Lab 01, when answering the two questions that follow.



14. The operation of this circuit will be unchanged if a 2-input NOR gate is substituted for NAND1 and no other change is made.
    A **True** A 2-input nor with its inputs tied together also functions as an inverter.

B False

15. The operation of this circuit will be unchanged if the 10 kΩ resistors are replaced with zero ohm resistors.
    A True
    B **False** If the 10 kΩ resistors are replaced with 0 Ω resistors, then the voltage divider circuit pairs two essentially zero ohm devices, the new resistors and the NO SPST push-button switches. The logic 0 function of these inputs will be compromised and there will be a zero ohm path from power to ground when either switch is pushed (closed), also not good due to excessive current that will from power to ground in this case.

16. Consider Figure 2.14 from the textbook.

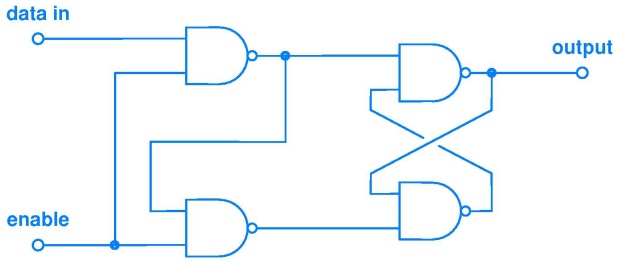


Figure 2.14 Illustration of four *nand* gates used to implement a one-bit latch.

Let t be the initial time this circuit is examined. Which statement is true?
A If at time t enable = 1 and data in = 0 and are held constant, then output(t) = 0 and output(t+1) = 0
B If at time t enable = 1 and data in = 0 and are held constant, then output(t) = X and output(t+1) = 1
C If at time t enable = 0 and data in = 1 and are held constant, then output(t) = X and output(t+1) = 1
D **None of the statements A, B, and C are true** Statement A would be true if is said that output(t) = X. Statements B gets the value of output(t+1) wrong. Statement C, where enable = 0 should have output(t+1) = output(t), i.e., no change.

17. For 8-bit sign-magnitude and 1's complement representations of the decimal value -3, in how many bit positions do these two representations differ?
    A 1
    B 3
    C 5
    D **7** Sign-magnitude for -3 is 1000 0011 with a space added for readability. For 1's complement -3 is the bitwise inverse of 0000 0011 or 1111 1100. These representations differ in all but the sign bit, so they differ in 7 bit positions.
    E None of the above

18. A digital logic circuit with a single input and a single output behaves as follows at five points in time.

Time	1 2 3 4 5 …
Input	0 0 1 0 1 …
Output	0 0 1 1 0 …

This logic circuit must contain

A A counter

B An OR gate

C **A latch** The output of this circuit is not the same for each identical input, therefore this is not a combinatorial circuit that is computing the results in a truth table. Rather, this must be a sequential circuit that can behave differently depending on its accumulated history of operation. The only sequential circuit choices among the answers are the latch and a 5-bit register. The behavior shown is output = input until input =1 then output = input'. A single latch can remember this much history, so can a 5-bit register, but then, a 5-bit register is built from latches. Answer C is certain.

D An adder

E A 5-bit register

19. A function in a program produces a result when called. Hardware, when receiving power, produces an output signal at all times no matter how many gate delays signals must propagate through on the longest signal path.

A **True** The output signals of hardware start generating output logic values the moment that power is given. These outputs may well not reflect the current inputs, but that is for the circuit designer and the programmers to allow for.

B False

20. What fraction of the possible input values yield Sum = 0 and Carry out = 1 for a full adder?

A 1/8

B 2/4

C **3/8** The ways to produce the specified outputs are (addend, augend, carry in) of (1,1,0), (1,0,1), and (0,1,1). These are three of eight possible input combinations of three input bits.

D 4/16

E 5/8

21. Unlike for analog circuits, there is no noise present on the wires in digital circuits.

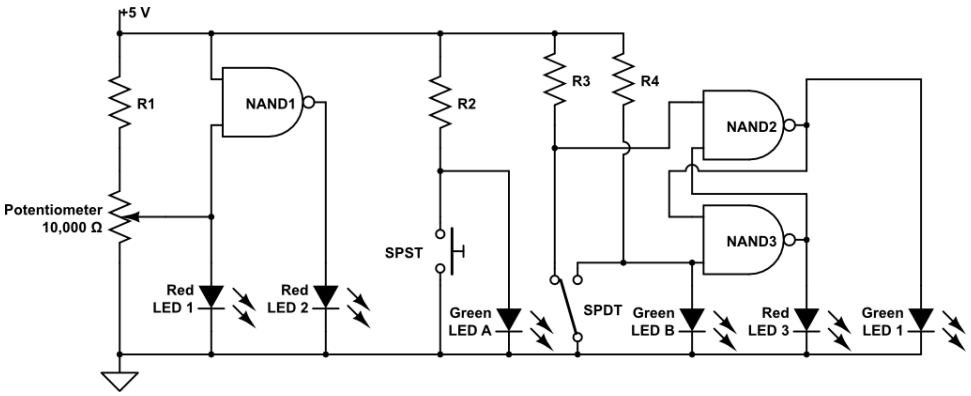
A True

B **False** Noise is always present in electrical circuits. It is the gap between the acceptable high band signal voltages and the low band signal voltages that provides the strong immunity to noise possessed by digital circuits. If noise becomes strong enough it can will overwhelm the gap designed into digital circuits and cause the voltage on a wire to transition, erroneously, from the intended logic band to the other logic level voltage band.

22. Mechanical computers are always analog systems.
    A True
    B **False** Marchant and Curta calculators (lecture slides 27 and 49) are examples of digital base 10 mechanical computers.

23. 2^4 bytes is 4 times as much as 20 (base 16) bits.
    A **True** 2^4 bytes = 2^4 x 2^3 bits = 2^7 bits. 20 base 16 = $2x16^1+0x16^0 = 32 = 2^5$. The ratio of 2^7 to 2^5 is $2^2 = 4$.
    B False

24. In this circuit, Green LED B is used to monitor a signal that is equally as digital in its behavior as the signal monitored by Red LED 3.



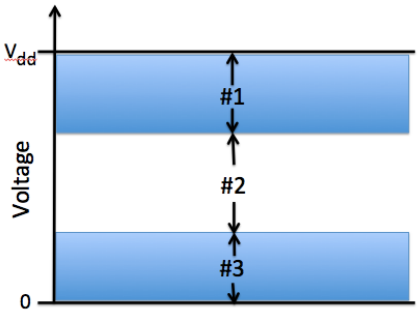
    A **True** Green LED B monitors the voltage divider input generated by R4 and the SPDT switch. This input is bouncy because of the SPDT switch, but it generates quality low and high voltage signals just as digital as the low and high voltage levels generated by the output of NAND3, monitored by Red LED 3.
    B False

25. Which of the following is one of DeMorgan's Laws?
    A (X')' = X
    B **(AB)' = A' + B'**
    C (A'B') = A' + B'
    D (A + B)' = A' + B'
    E None of the above is one of DeMorgan's Laws

26. Memory locations are pointed to by hardware. Designing a computer with four times more memory than specified in the original design requires
    A Using one more address bit
    B **Using two more address bits** Each additional address bit doubles the number of locations that can be pointed to.
    C Using four more address bits
    D Using four times the number of address bits
    E Waiting 3 years if memory density is increasing by 60% per year

27. What lab kit component is the key to automating the operation of sequential circuits?
    A The 7400 chip
    B The 74138 chip
    C The 74163 chip
    D **The 555 chip** This chip electronically generates a clock signal so that we do not have to manually generate clock signals for our sequential circuits.
    E The key is a lab kit component not listed above.

28. Consider the following diagram showing three voltage bands labeled #1, #2, and #3.



    Which band, or which combination of bands, guides us in designing digital computer circuits where the logic gate input signal voltage levels need not be perfect yet gate operation will be digital, not analog?
    A #1
    B #1 and #2
    C #2
    D #2 and #3
    E **None of the above answers is correct** The correct answer is bands #1 and #3.

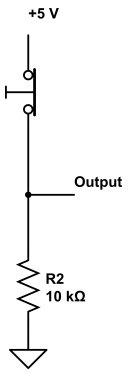
29. Consider the following truth table.

A	B	f(A,B)
0	0	
0	1	
1	0	
1	1	

    The missing truth table entries, in order from top to bottom, are
    A 0 0 1 0 if f(A,B) = (A + B) modulo 2 [A+Bmod 2 entries would be 0110]
    B 0 1 1 0 if f(A,B) = A XNOR B [A XNOR B entries would be 1001]
    C **1 0 0 0 if f(A,B) corresponds to a universal logic gate** Because 1000 corresponds to A NOR B and NOR is a universal gate.
    D 0 0 0 1 if f(A,B) corresponds to a universal logic gate [0001 is AND which is not universal]
    E X 1 0 X if f(A,B) = A' [for A' the table would be 1100]

30. The binary string 1010, when interpreted as a 2's complement number represents the decimal number value
    A 10
    B -2
    C -5
    D **-6**
    E None of the above

31. Consider this circuit to generate a digital input.



    A **This input circuit is an active low design**
    B This input circuit is fine for use with digital logic circuits of every type [This input bounces, so it is inappropriate as an input to an edge-triggered digital logic circuit.]
    C We cannot say whether this input circuit is active high or not until information about whether the switch is being pushed is given to us [See lecture slides on high-active, low-active]
    D This circuit will work only when we exchange the positions of the switch and the resistor in the circuit, that is, put the switch where the resistor is shown and put the resistor where the switch is shown [This circuit works fine as is. A related variant of this circuit can be built as described.]
    E This design would be improved if R2 had the value 470 ohms [470 ohms will make for a poorer voltage divider. Do the math to determine the quality of the low level and high level voltage outputs in comparison to the two voltage levels produced when he resistor is 10,000 ohms.]

32. How many sign bits might possibly be found in a number representation using a binary string of length 2n bits?
    A Zero
    B 1
    C n
    D **All of the above** A could be unsigned format, B any of sign-magnitude, 1's complement, and 2's complement, and C could be signed-digit format.
    E Both A and B

33. The reason we prefer to build digital logic circuits to operate in base 2 rather than base 10 given a fixed maximum power supply voltage is
    A Cost
    B Speed
    C Increased resistance to noise-induced logic errors
    D **Any of the above** Each of these characteristics is true for base 2 in relation to base 10 and each is a desirable trait.
    E None of the above