1. Please separate this **COVER SHEET** from the rest of the exam document.
2. Diagrams and information that may be useful for this exam **are shown on both sides of this sheet.**

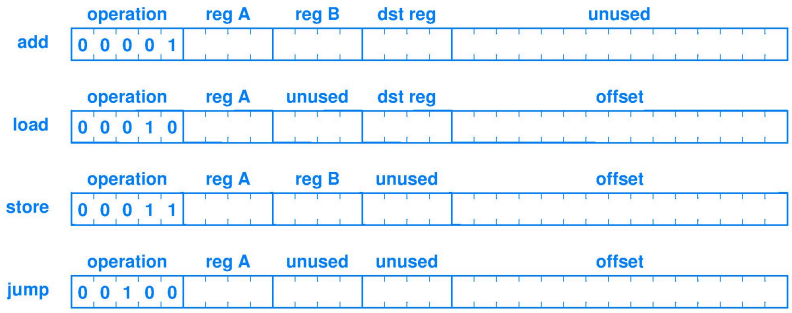

Figure 6.2 The binary representation for each of the four instructions listed in Figure 6.1. Each instruction is thirty-two bits long.

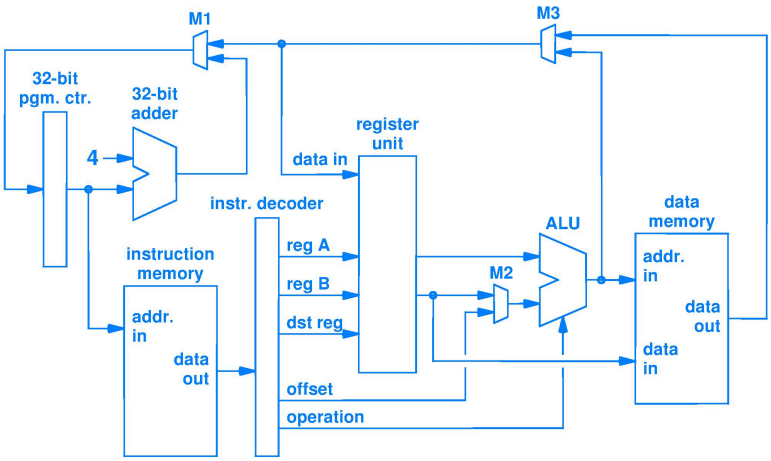

Figure 6.9 Illustration of data paths including data memory.

Table 1. RISC instruction set data.

Frequency	**Instruction type**
45%	Add, sub, multiply, divide, compare, load immediate, shift left, shift right, and, or, other register-register
35%	Load, store
17%	Conditional branch
3%	Jump, call, return

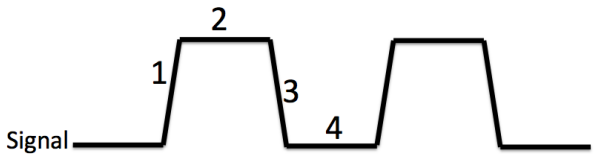

Figure 1.A: Waveform

[See other side of this cover sheet for more reference information.]

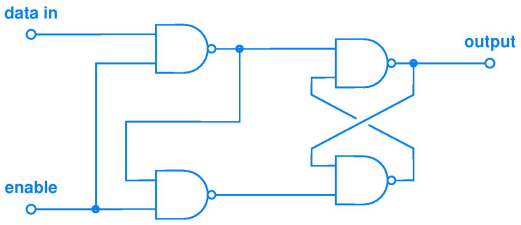

Figure 2.14 Illustration of four *nand* gates used to implement a one-bit latch.

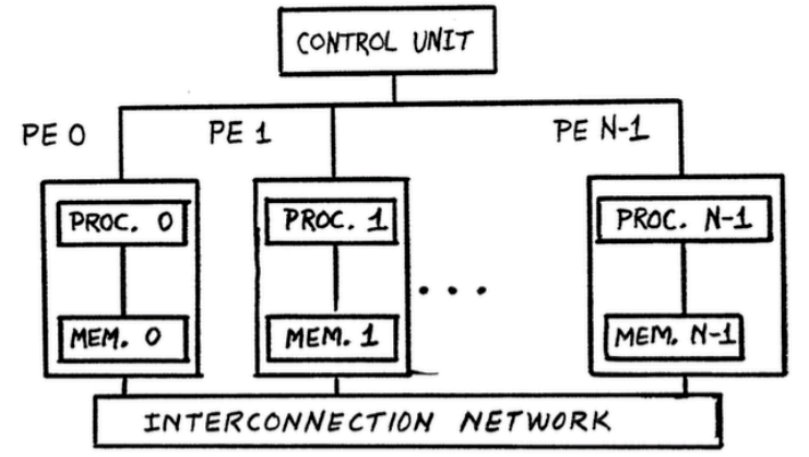

Figure 1.B SIMD computer diagram.

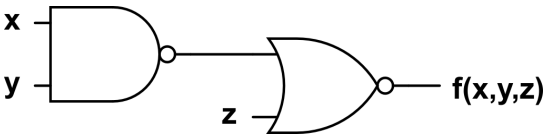

Figure 1.C Logic circuit.

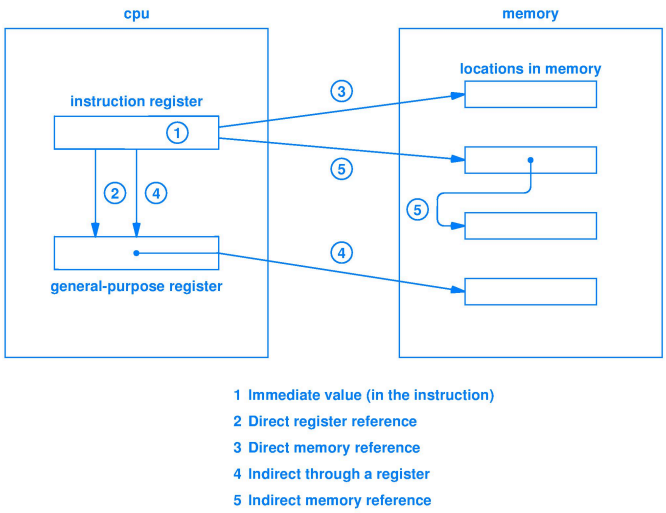

Figure 7.6 Illustration of the hardware units accessed when fetching an operand in various addressing modes. Indirect references take longer than direct references.

Prof. George Adams
Final Exam
CS 250 Fall 2016
Purdue University

Pre-exam instructions.

1. STORE your name, section number [0001 for MWF lecture; 0002 for TR lecture], and ID on your bubble sheet.

2. The preceding tear-off cover sheet is to be your only source of reference information. This exam is closed book, closed notes, and no calculators or devices with state.

3. **Whenever an exam question refers by name to a Figure or Table, you will find that figure or table on the tear-off sheet.**

4. The exam is printed on both sides of the sheets of paper.

5. I and the TAs will not answer questions during the exam, so do not ask. Instead, carefully re-read the question and proceed as best you can.

6. Do not open the exam document until given permission to begin.

This is version A of the exam document.

1. **Fill in bubble A in the TEST FORM space on the bubble sheet.**
2. Check that your exam document contains
    a. 14 numbered pages, including the two pages of the tear-off sheet.
    b. 59 multiple choice questions to bubble in.
3. Hand in your bubble sheet when you complete the exam.

Write your answers to the following questions on your bubble sheet.

1. I have bubbled in my first and last name, section number, and student ID, and exam version.
   A True
   B False

2. I will neither give nor receive aid on this exam. [Please abide by this policy.]
   A True
   B False

The following multiple choice questions are worth 3 points each, except for question 59.

3. Which of the following is an abstraction?
   A Ground
   B 470 Ω
   C A MOSFET
   D Logical 1
   E None of the above

4. Consider the circuit of Figure 1.C on the exam cover sheet. If the input logic values are x=Don't Care, y=0, and z=1, then the output f(x,y,z) logic value is
   A 0
   B 1
   C Don't care
   D Either 0 or 1 depending on the chosen value of input x
   E Can not be determined from the given information

5. Pointing to one of 7 locations, each holding a single ASCII character, requires
   A a 7-bit string
   B a byte string
   C a multiplexer with 7 inputs
   D a multiplexer with 8 outputs
   E none of the above answers is correct

6. How many distinct Boolean functions are there that have three inputs?
   A 3
   B 2^3
   C 3^2
   D 2^8
   E 2^{32}

7. Data hazards can occur within a single machine language instruction.
   A True
   B False

8. How many two-input NAND gates are necessary to build a two-input OR gate with active high inputs and active high output?
   A one
   B two
   C three
   D four
   E five

9. The binary string 10110100, when interpreted as a 1's complement number, has the base ten value
   A 180
   B -52
   C -75
   D -196
   E None of the above

10. In Figure 1.A, which numbered segment(s) of the waveform may be used to control the Test-Fetch-Execute cycle of the processor circuit?
   A 1, 2, 3, and 4
   B 2 and 4
   C 1 and 3
   D 4
   E Only one of the numbered segments may be used

11. What lab kit component can be used to produce exactly two very different resistance values for a circuit?
   A The potentiometer
   B 2-input NAND gate
   C The 555 timer
   D The SPST switch
   E None of the above

12. 2^{15} bytes is 128 times as much as
   A 512 bytes
   B 2^{-9} Mbits
   C 2^{-21} GB
   D a 1 KB page
   E None of the above

13. A computer has 32-bit addresses, 32-bit words, and byte-addressed memory. A word starting at address 0x01ff044b is aligned.
   A True
   B False

14. Consider Figure 2.14 from the textbook, available to you on the exam cover sheet. Let t be the initial time this circuit is examined. Which statement is true?
    A If at time t enable = 1 and data in = 0 and are held constant, then output(t) = X and output(t+1) = 0
    B If at time t enable = 1 and data in = 0 and are held constant, then output(t) = X and output(t+1) = 1
    C If at time t enable = 0 and data in = 1 and are held constant, then output(t) = X and output(t+1) = 1
    D None of the statements A, B, and C are true

15. The constant 0xcefa1db0 is stored in a little endian byte-addressed memory. Reading this constant one byte at a time from lowest address to highest address will yield what sequence of hexadecimal digits?
    A 0xcefa1db0
    B 0x0bd1afec
    C 0xecafd10b
    D 0x1db0cefa
    E None of the above

16. Which field in an IEEE Floating Point number determines the range of representable values?
    A Sign
    B Biased exponent
    C Hidden bit
    D Magnitude
    E Unbiased exponent

17. In text Figure 6.9 multiplexers M1 and M3 are set so that *data memory data out* is connected to *32-bit pgm. ctr.* Which instruction of text Figure 6.2 is being executed?
    A add
    B load
    C store
    D jump
    E Setting multiplexers M1 and M3 in this way does not correspond to executing any instruction in Figure 6.2

18. Referring to the addressing modes depicted in Figure 7.6, the number of assembly language instructions shown in Figure 6.2 that contain exactly one instance each of addressing modes 1 and 4 and two instances of mode 2, is
    A 0
    B 1
    C 2
    D 3
    E 4

19. Pipelining does not reduce the execution time of an instruction.
    A True
    B False

20. The decimal value –2 written as a two's complement, 4-bit binary number is
    A 0010
    B 1010
    C 1101
    D 1011
    E None of the above

21. A register operand field in a machine language instruction is
    A a pointer
    B a value
    C a hexadecimal digit
    D a two's complement bit string
    E None of the above

22. Instruction set design determines
    A What specific logic circuits will be used to implement a processor
    B How processor hardware is partitioned into units with specialized capabilities
    C What instructions the processor will be built to execute
    D What clock rate can be used for the processor
    E Whether the processor will directly access the memory hierarchy

23. What register is the input to the IF stage of a 32-bit processor pipeline circuit?
    A PC
    B IF/ID
    C Instruction memory
    D Address 0x00000000
    E There is no such register

24. The register file is used in two stages of the 5-stage pipelined version of Figure 6.9.
    A True
    B False

25. A dirty bit in L1 data cache is set when
    A accessing a given cache block for the second time.
    B the processor executes a store operation.
    C every time a new block is brought into the L1 data cache.
    D it is time to enforce Rule 1 of the memory hierarchy.
    E None of the above.

26. One way to increase the hit ratio for a cache is to speed up the tag matching circuitry.
    A True
    B False

27. The designer of a direct-mapped cache would make the following choice for the cache replacement policy.
    A LRU
    B Random
    C First-in/First-out
    D Any one of A, B, or C may be chosen because this is a design situation
    E None of the above

28. What type or types of hazard can be eliminated by loop unrolling alone?
    A Structural hazard
    B Control hazard
    C Data hazard
    D Both B and C
    E None of the above

29. Which term of the CPU Time equation most closely relates to the way a processor checks for interrupt-driven I/O?
    A Instructions/program
    B Average clocks per instruction
    C Clock cycle time
    D Fraction enhanced
    E Overall speedup

30. Convenience, efficiency, and simplicity are all reasons for a computer to
    A have a 32-bit adder
    B have L1, L2, and L3 cache
    C use a single size for data words and memory addresses
    D use polling
    E have ALU instructions that access memory

31. The most important logic gate parameter for the prevention of error is the
    A width of the voltage band representing logic 1
    B width of the voltage band representing logic 0
    C power supply voltage
    D gap between the highest logic 1 voltage and the lowest logic 0 voltage
    E gap between the lowest logic 1 voltage and the highest logic 0 voltage

32. Multiple virtual memory spaces may exist at the same time in a computer.
    A True
    B False

33. Buffer flushing
    A allows buffering to be used with most any application
    B is very much like Rule 1 of the memory hierarchy
    C is similar to hitting on a store access to a dirty cache block
    D all of the above
    E none of the above

34. An L1 cache with a hit time of 2 nanoseconds is now added to a computer that originally had no cache and sent all memory accesses directly to main memory DRAM that has an access time of 60 nanoseconds. You wish to compute the overall speedup for performing memory accesses using Amdahl's Law. What additional information do you need to know?
    A No additional information is needed
    B The size of the L1 cache
    C The miss rate of the L1 cache
    D The number of blocks in the L1 cache
    E None of the above is correct

35. A RISC computer having a 1 GHz clock rate executes a program by performing 1.0×10^9 instructions having a measured CPI of 2.0 with the mix shown in Table 1. What is the number of memory accesses performed during the execution of this program?
    A Cannot be determined from the given information
    B 1.97×10^9
    C 1.35×10^9
    D 0.35×10^9
    E None of the above

36. Which has higher priority, I/O devices or application programs?
    A I/O devices
    B Application programs
    C I/O devices have higher priority only if the hardware supports priority interrupts
    D The relative priority of I/O devices and application programs is not fixed

37. Computer #1 generates a message and its hash and transmits both via a noisy channel to Computer #2. Computer #2 hashes the received message and this hash matches the hash received from Computer #1. From this we can prove that
    A the message was received without error.
    B both the message and the hash were received without error.
    C its quite likely that either the message or the hash were received with one or more errors.
    D None of the above answers is correct

38. Which one of the following computer characteristics is part of the computer's architecture from the viewpoint of an assembly language programmer?
    A 5-stage pipeline
    B 3-address instructions
    C L1 cache
    D branch prediction
    E out-of-order instruction execution

39. Which of the following might be expected to serve as the CSR for an I/O device?
    A Memory addresses 0x00000000 through 0x00FFFFFF
    B Memory addresses 0x80000000 through 0xF0000000
    C Memory addresses 0x20000000 through 0x2000000F
    D Memory addresses corresponding to certain holes in physical memory
    E A CSR is a register, so we would not expect the above to serve as a CSR

40. When does a processor check for interrupt-driven I/O?
    A Before executing every instruction
    B After executing every instruction
    C After fetching every instruction, but before executing that instruction
    D When an interrupt is received
    E None of the above

41. Programs often contain control structures of the form
        if (logical test) {then statements; else statements;}
    The function of the instruction PUSH* issued by the control unit of an SIMD computer is to
    A update the control unit enable stack
    B control execution of the "else" statements by the PEs
    C record the result of the logical test by each PE
    D enable the PEs to execute either the "then" or the "else" statements, as appropriate
    E to provide logical balance with the control unit instruction POP*

42. What instruction type is present in an SISD computer instruction set but is missing from the instruction set of an SIMD computer?
    A Load
    B Register-register
    C Conditional branch
    D Jump to subroutine
    E None of the above

43. An application program can count the number of times it is interrupted during the course of its execution if the computer uses interrupt-driven I/O.
    A True
    B False

44. An MIMD computer with N PEs is to run an application written in C that has a shared integer variable and a shared pointer variable that are infrequently updated. Examination of the application source code will reveal
    A the use of at least one *if* statement
    B the use of at least one *for* statement
    C the use of at least one *lock* statement
    D a programming error because shared pointer variables are not allowed with MIMD computation
    E None of the above

45. PC architectures commonly control their slower buses with a special-purpose chip called the
    A Northbridge
    B Southbridge
    C Bridge
    D Memory Management Unit
    E None of the above

46. Your manager asks you, a brand new employee, to optimize a subroutine in a software product to achieve an overall speedup for the product of 2. Measurements show that the product spends 40% of its execution time in this subroutine. You would best showcase your competence as a computing professional by
    A accepting the assignment
    B accepting the assignment and requesting to team-program with a senior programmer in your group who could serve as a mentor
    C asking for a week to study the code base to determine if your skill is sufficient
    D declining the assignment
    E telling your manager that the product is not worthy of further development

47. Which one of the following representation schemes provides the ability for a receiver to detect some, but not all, errors when numbers are encoded in this format and their bits are transmitted over a noisy channel?
    A unsigned integer
    B sign magnitude
    C 1's complement
    D 2's complement
    E binary coded decimal

48. (Select the one *best* answer.) Removing dependences from code
    A is not possible.
    B requires re-naming.
    C requires scheduling.
    D is always possible.
    E More than one of the answers above is correct

49. A program requests to read information from an I/O device and two devices respond. The type of bus event that has occurred is
    A an unassigned address error
    B an instance of parallel I/O
    C an address conflict
    D an example of the fetch-store paradigm for I/O
    E none of the above

50. Assume that a page table entry occupies 32 bits, page size is 1 Kbyte, memory addresses are 32 bits, and memory is byte-addressed. How many megabytes of memory will a single-level page table occupy for this example computer?
    A 2
    B 4
    C 8
    D 16
    E 32

51. What is the purpose of a "Used?" bit in a virtual memory page table entry?
    A To indicate that the page is dirty
    B To support the policy for page placement into DRAM
    C To indicate that the given page has been loaded into DRAM more than once
    D To indicate that the given page is in use
    E None of the above

52. Which factor or factors of the CP Time equation:
    CPU Time=(Instructions/Program)x(Clock cycles/Instruction)x(Seconds/Clock cycle)
    is/are a function of either (1) instruction set architecture or (2) compiler technology?
    A Instructions/Program and Clock cycles/Instruction
    B Clock cycles/Instruction and Seconds/Clock cycle
    C Seconds/Clock cycle and Instructions/Program
    D Seconds/Clock cycle
    E Clock cycles/Instruction

53. Which statement of the rules of operation of the memory hierarchy is false?
    A The lowest level in the memory hierarchy is the ultimate repository for all long-term information.
    B A level above is provided a copy of information from the level below when the level above cannot satisfy a processor request.
    C When the processor reads information at the top level, that change must eventually propagate down the levels.
    D None of the above

54. Sleeping a processor whenever possible saves energy.
    A True
    B False

55. Search engine response time delays of as little as 0.5 seconds have been shown to reduce the advertising revenue per user by
    A about 10%
    B about 1%
    C 0% because users do not pay for advertising
    D None of the above

56. How many of the computer types in the Flynn classification system fetch N instructions at a time?
    A 0
    B 1
    C 2
    D 3
    E 4

57. An SIMD computer executes the following code with line numbers 1, 2, 3, and 4.

```
1:  if ( X <= Y )
2:        X = X + Y;
3:  else
4:        X = X – Y;
```

    The last time that the Control Unit will broadcast an instruction to update the contents of the processor enable stacks corresponds to
    A completing the execution of line 1
    B entering line 2
    C completing line 3
    D entering line 4
    E completing line 4

58. A system call is more time consuming than a subroutine call because
    A the processor must change mode from user to system
    B the processor must switch contexts from the application to the operating system
    C the processor must copy information from the application address space to the operating system address space
    D all of the above three reasons
    E none of the above four reasons

59. [2 points] The meaning of a bit string is
    A known by the hardware.
    B known by the compiler.
    C known by the assembler.
    D ours to define.
    E none of the above.