CS 250 Practice Midterm Exam 02 and HW07
2017 Fall
Purdue University

Due 9:00 pm Tuesday, Oct. 24, 2017
No late uploads accepted this time. Upload early; don't let Blackboard byte you.

Upload to Blackboard as PDF.
Uploads with an answer for each question will receive 15 points.

To indicate your answer for multiple choice questions, make the font for your selected answer have a green color.

0. This practice midterm is not for CS 25000.
   A True
   B False

For fill in the blank type questions, just fill in the blank space with your answer in green.

1. The register file is used in two stages of the 5-stage pipelined version of Figure 6.9.
   A True
   B False

2. Pipelining is a form of hardware parallelism.
   A True
   B False

3. Which one of the following instructions is the most likely to cause a structural hazard in the EX stage of a pipeline?
   A load
   B branch
   C comparison of sign-magnitude format integers
   D floating point divide
   E BCD addition

4. Of the pairs of different computer architectures below, which pair is most similar with respect to accessing data memory?
   A 0-address architecture & Load/Store architecture
   B 0-address architecture & 1-address architecture
   C Accumulator machine & 1-address architecture
   D Load/Store architecture & Reg-Reg architecture
   E Stack architecture & Reg-Memory architecture

5. A microcode program in which there is an instruction to continue the operation of a given hardware unit for an additional micro-instruction cycle because that hardware

unit needs more than one cycle to complete its task is which type of microcode program?

A Vertical microcode
B Horizontal microcode
C Both answers A and B
D Insufficient information has been given to answer the question
E All of the above answers are incorrect

6. What happens to instruction(s) in a pipeline that were fetched earlier than an instruction that is stalled?

A Those instruction(s) stall, also.
B Those instruction(s) do not stall.
C Those instruction(s) do not stall if they have no dependence with the stalled instruction.
D Those instruction(s) stall if they have a true data dependence with the stalled instruction.
E Those instruction(s) are replaced with NOP instruction(s).

7. Which one of the following instructions causes a control hazard in a pipelined processor?

A load R1, R2, 16
B add R1, R1, R3
C store R1, R2, 32
D subi R3, R3, 8
E bne R2, R3, target

8. The instruction AND R6, R6, R1 ;R6 ← R6 and R1 contains an anti-dependence data hazard on register R6.

A True
B False

9. The most informative description of the contents of a register operand field in a machine language instruction is which one of the following?

A Pointer
B Value
C Hexadecimal number
D Bit string
E Register

10. Assume a pipeline with stages IF, ID, EX, MEM, and WB and no forwarding hardware. Which instructions in the following code sequence must be prevented from accessing an operand before it is available?

```
ADD R3,R4,R5      ; R3 = R4 + R5
SUB R6,R3,R7      ; R6 = R3 – R7
AND R8,R9,R3      ; R8 = R9 and R3
```

```
XOR R10,R3,R11       ; R10 = R3 xor R11
```

A All four instructions
B SUB, AND, XOR
C AND, XOR
D XOR
E None of the above answers is correct

The following questions make use of Figures 6.2 and 6.9 shown here.

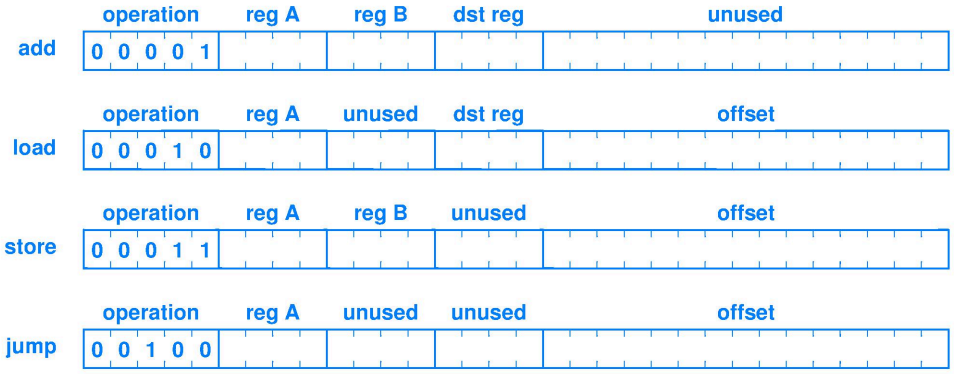

Figure 6.2 The binary representation for each of the four instructions listed in Figure 6.1. Each instruction is thirty-two bits long.

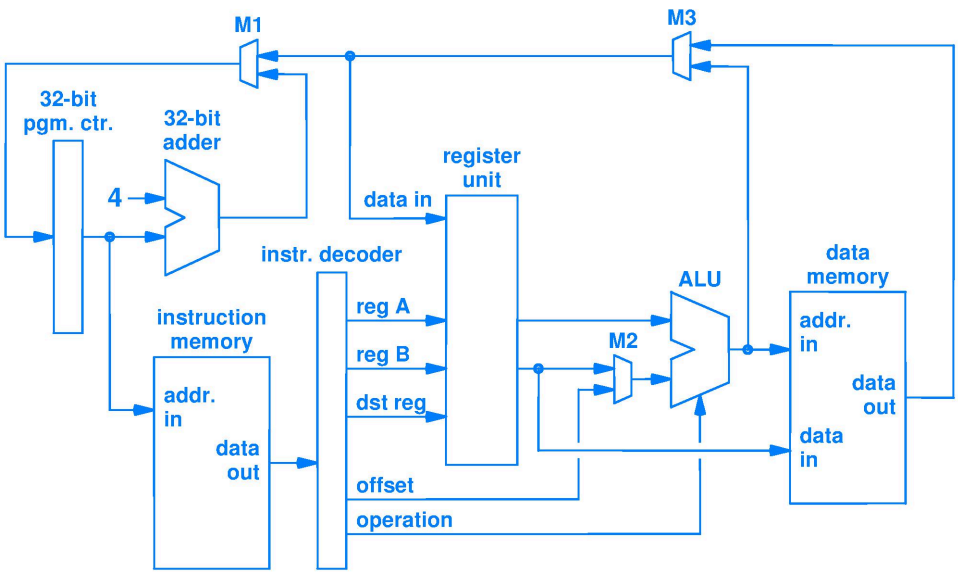

Figure 6.9 Illustration of data paths including data memory.

11. Which part(s) of Figure 6.9 is/are incompatible with variable length instructions?
    - **A** 32-bit pgm ctr.
    - **B** 32-bit adder with constant value 4 operand
    - **C** instruction memory
    - **D** ALU
    - **E** All of the above are incompatible with variable length instructions.

12. Which one of the following instructions has M1 make a different selection than the other three instructions?
    - **A** ADD
    - **B** LOAD
    - **C** STORE
    - **D** JUMP
    - **E** None of the above

13. How many data paths in Figure 6.9 have widths other than 4 and 32?
    - **A** 0
    - **B** 1
    - **C** 2
    - **D** 3
    - **E** More than 3

14. The register unit is involved in only one stage of the 5-stage pipelined version of Figure 6.9.
    - **A** True

B False

15. How many clock cycles does it take to execute the following code snippet on the 5-stage pipelined version of Figure 6.9? Assume that the pipelined circuit detects any hazards and stalls to preserve program semantic correctness. Assume that the pipelined circuit is not capable of forwarding, but that the register file is capable of writing a register early in a given clock cycle and then reading that same register later in the same clock cycle.

```
add    r6, r7, r8
add    r5, r6, r7
```

A 6 cycles
B 7 cycles
C 8 cycles
D 9 cycles
E more than 9 cycles

16. How many labels are necessary to implement an if-then-else statement in assembly language?
A 0
B 1
C 2
D 3
E Labels are not necessary

17. An assembler is two-pass because
A programs may contain if statements.
B using two passes prevents errors in filling opcode fields.
C assembly language labels correspond to unknown offset amounts.
D the need to fill in unused instruction format fields.
E none of the above answers is correct.

18. A technology for quickly prototyping a new processor circuit design is
A vertical microcode
B horizontal microcode
C field-programmable gate array
D programmable read-only memory
E none of the above

19. Pipelining a processor
A increases the execution time of an instruction
B increases the number of instructions completed per unit time
C increases clock frequency
D increases stall cycles
E all of the above

20. Pipeline registers store

A instruction opcodes
B instruction operands
C control signals
D pointers
E all of the above

21. There is a true data dependence between the following two instructions.

```
load    r7, (64)r4      ; r7 ← Memory[64 + r4]
store   r6, (128)r5     ; Memory[128 + r5] ← r6
```

A True
B False
C Insufficient information to determine if a true data dependence exists

22. Which of the following is most improved by the effects of Moore's Law?
A Structural hazards
B Control hazards
C True data hazards
D Anti-dependence data hazards
E Output dependence data hazards

23. What type or types of hazard can, in some cases, be eliminated by scheduling?
A Structural hazard
B Control hazard
C Data hazard
D Both B and C
E None of the above

24. Choose the best answer from the four possibilities.
A The delay slot(s) of a delayed branch machine language instruction can be filled with certainty by NOP instructions.
B The delay slot(s) of a delayed branch machine language instruction can be filled with certainty by instructions from anywhere in the program before the branch.
C Both the A and the B statements are correct.
D Neither the A nor the B statement is correct

25. Which of these machine language instructions is memory location dependent?
A an ADD instruction used within a function rather than in main( )
B a branch instruction
C a jump instruction
D a subroutine call instruction
E a return instruction

26. A 64-bit RISC computer has byte-addressed memory. At what address should we expect to find the default next instruction? PC+8

27. Branch prediction has a positive ____payoff____ when correct, and likely a negative one when incorrect.

28. Two assembly language instructions are defined as follows.

```
jump offset(register)   ; PC ← offset + contents of register
brr regA, regB, offset  ; if contents of regA = contents of regB, then
                        ;     PC ← PC + offset else  PC ← PC + 4
```

Which instruction, jump or brr, is easier to use when writing program loops and why?
brr because target = PC + offset

29. How many levels of protection does a CPU that runs applications need and what code runs at each level?
It needs 4
Read instruction from memory; store data in register inside CPU; ALU does arithmetic operations; then communicating with other resources if needed

30. Consider this code.

```
for (i=1000; i>=1; i=i-1) {
        x[i] = x[i+1] + s;
}
```

Can this loop be unrolled 4 times and, after performing or not performing the loop unrolling, how many basic blocks will the code have?

A Cannot be unrolled 4 times; will have 1 basic block
B Cannot be unrolled 4 times; will have 1000 basic blocks
C Can be unrolled 4 times; will have 1 basic block
D Can be unrolled 4 times; will have 4 basic blocks
E Can be unrolled 4 times; will have 250 basic blocks

31. A computer using a given enhanced execution mode runs two times faster than when it does not use enhanced mode. The enhanced mode can be used during half of the execution time of a particular computational workload. What speedup is achieved by using the enhanced execution mode to process the given workload?

A 2
B Insufficient information is given to answer the question
C 1.5
D 0.5
E None of the above answers are correct

32. Match an item from the left column with most closely matching item in the right column. If there is no reasonable match in the right column, write "no match"

Left column	Place number of the matching item from the right column in this column on the row that it matches,	Right column

	if any. Right column items may be used more than once or not at all.	
Integer arithmetic instructions	2	1. Protection modes
Processor control instructions	5	2. General purpose computation
Logical/Boolean instructions	3	3. Structured programming support
Floating point instructions	2	4. Binary string manipulation
Branch type instructions	1	5. Subroutine calls

33. Branch instructions always cause a pipeline stall.
    A True
    B False