Fateme Shokouhinia

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Website, Google Scholar, LinkedIn

EDUCATION

SIMON FRASER UNIVERSITY (SFU)
M.Sc. in Computer Science
Sep 2021 - Aug 2024 | Burnaby , BC, Canada

AMIRKABIR UNIVERSITY OF TECHNOLOGY (AUT)
M.Sc. in Computer Engineering
Sep 2019 - July 2021 | Tehran , Iran

SHARIF UNIVERSITY OF TECHNOLOGY (SUT)
B.Sc. in Computer Engineering
Sep 2014 - Feb 2019 | Tehran, Iran

SKILLS

Programming
Experienced:
• C, C++, Python, VHDL and Verilog
Familiar:
• Matlab, Golang, HTML/CSS
System Simulation Tools:
• Gem5, ZSim, Ramulator-PIM, DAMOV
Others
• Scripting, Git
• Unix/Linux/Windows

COURSEWORK

- Basic/Advanced Computer Architecture
- Several System Design Courses and Labs
- Basic/Advanced Object-Oriented Programming
- Operating Systems
- Basic/Advanced Computer Networks

AWARDS

• 7 **Graduate Fellowship** Awards from SFU (2021 - 2024)
• Ranked 1st in my master's class at AUT, with a GPA of 19.49/20 (2019)

PUBLICATIONS

- Elham Cheshmikhani, Fateme Shokouhinia and Hamed Farbeh, 2024, "A Low-Cost Fault-Tolerant Racetrack Cache Based on Data Compression," in IEEE TCAS II: Express Briefs, DOI.
- Meisam Abdollahi, Mohammad Baharloo, Fateme Shokouhinia, and Masoumeh Ebrahimi, 2021, "RAP-NoC: Reliability Assessment of Photonic Network-on-Chips, A simulator". In Proceedings of ACM NANOCOM 21, DOI.

RESEARCH EXPERIENCE

RESEARCH ASSISTANT | Supervisor: Alaa Alameldeen | Sep 2021, present
- Reliability and Performance Improvement in Processing-In-Memory (PIM) Applications.
- Our performance-aware design for an ECC protected PIM system achieved an average of 79% performance improvement (currently preparing for submission in top-venue conferences).

RESEARCH ASSISTANT | Supervisor: Hamed Farbeh, Amirkabir University of Technology, Tehran, Iran | Sep 2019 - July 2021
- Reliability Improvement in Domain-Wall based Cache Memories using Data compression.
- Our design (Using Gem5 simulator and SPEC CPU 2006 benchmark suite) enhanced the mean-time-to-failure of the cache by an average of 11.3x with less than 1% hardware and performance overhead.
- This work was published in IEEE TCAS II: Express Briefs: Link.

STUDENT RESEARCHER Institute for Research in Fundamental Sciences, Tehran, Iran | Feb 2019 - July 2019
- Implemented an analytical simulator to evaluate the reliability of different 2D optical network-on-chip architectures and data traffic.
- Used Python as the main programming language. The simulator can be found on my Github.
- Our work was published in Proceedings of ACM NANOCOM '21: Link.

PROJECTS

- Implemented a tournament branch predictor (TAGE vs Multiperspective Perceptron) using Gem5 for the advanced computer architecture course at SFU.
- Enabled temperature reading using Arduino-Uno chip for hardware lab at SUT.
- Designed a Mini-MIPS Processor using Verilog for computer architecture course at SUT.
- Designed a compiler for a simple programming language using llvm for compiler design course at SUT.