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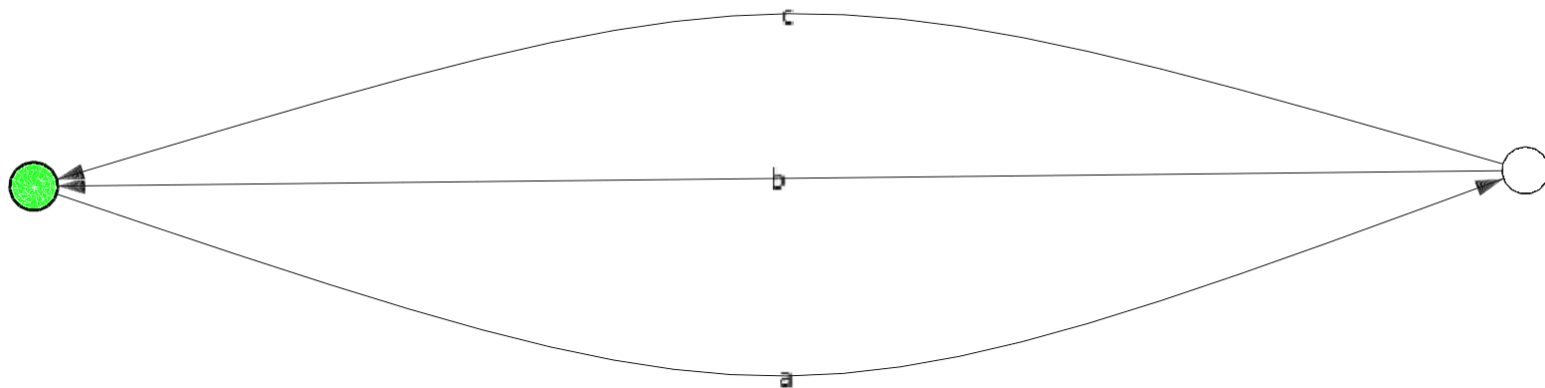
FMCS – Homework 2

Exercise 1:

Code for process P:

```
1 act
2   a,b,c;
3
4 proc
5   P = a.P1;
6   P1 = b.P + c.P;
7
8 init P;
```

The LTS graph for process P: the green dot is the P state, and by performing a action it goes to P1 state, the white dot. From the state P1, it can perform either b or c actions to go back to P state.

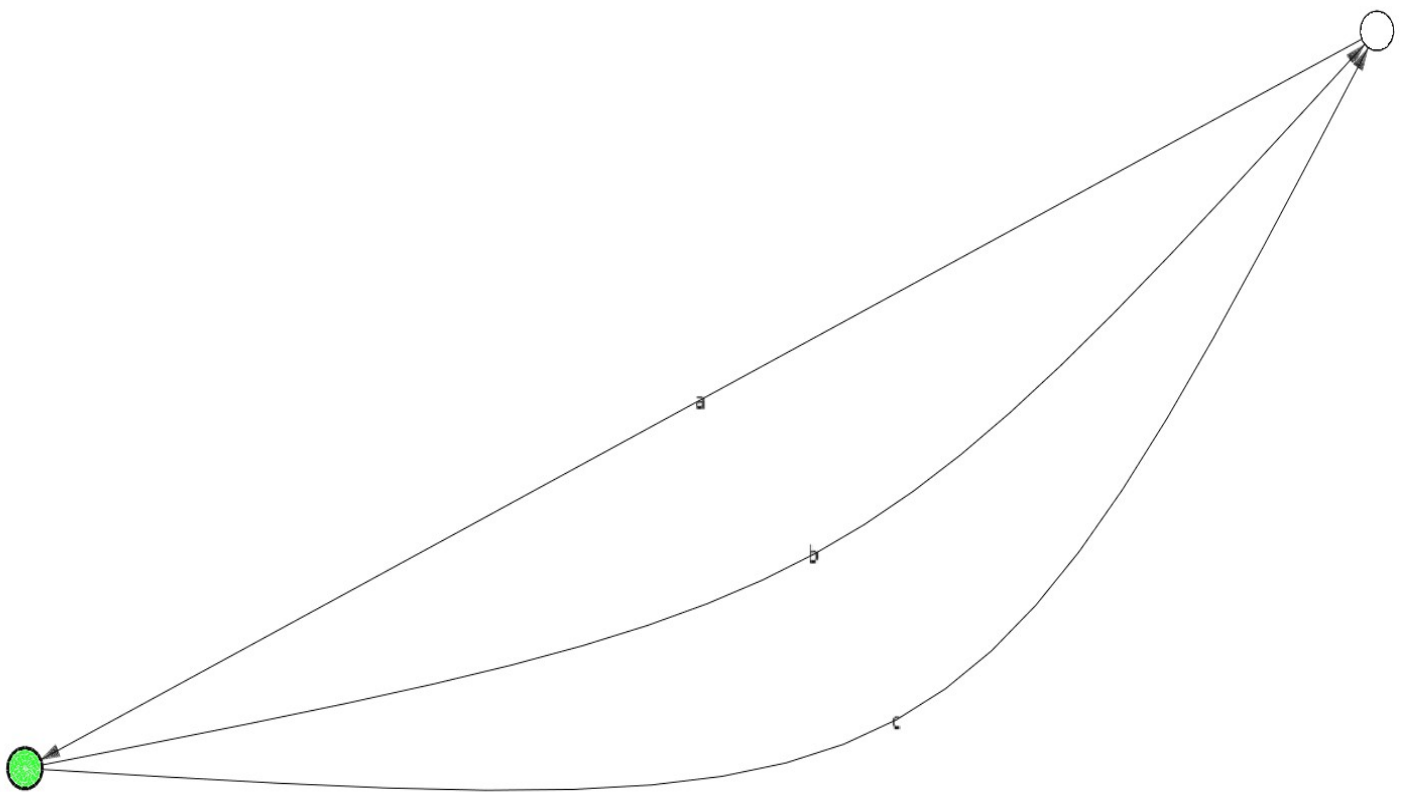


Code for process Q:

```
1 act
2   a, b, c;
3 proc
4   Q = a.Q1;
5   Q1 = b.Q2 + c.Q;
6   Q2 = a.Q3;
7   Q3 = b.Q + c.Q2;
8
9 init Q;
```

[20:40:41 verbose] type checking process specification...
[20:40:41 info] Specification is a valid mCRL2 specification
[20:42:23 info] Parsing and type checking specification
[20:42:23 verbose] type checking process specification...
[20:42:23 info] Specification is a valid mCRL2 specification

The LTS graph for process Q:



The LTS comparison between P and Q:

ltscompare

Run Abort

Working directory: C:/Users/stefa_000/Documents/FMCS-mCRL2
Input file: Ex1Q.lts

Input file #2: C:/Users/stefa_000/Documents/FMCS-mCRL2/Ex1P.lts

☐ **counter-example:** generate counter example traces if the input lts's are not equivalent

equivalence: use equivalence NAME (not allowed in combination with -p/--preorder):

- ☐ none identity equivalence
- ☒ bisim strong bisimilarity
- ☐ branching-bisim branching bisimilarity
- ☐ dpbranching-bisim divergence preserving branching bisimilarity
- ☐ weak-bisim weak bisimilarity
- ☐ dpweak-bisim divergence preserving weak bisimilarity
- ☐ sim strong simulation equivalence
- ☐ trace strong trace equivalence
- ☐ weak-trace weak trace equivalence

☐ **in1:** use FORMAT as the format for INFILE1 (or stdin)

☐ **in2:** use FORMAT as the format for INFILE2

preorder: use preorder NAME (not allowed in combination with -e/--equivalence):

- ☒ unknown unknown preorder
- ☐ sim strong simulation preorder
- ☐ trace strong trace preorder
- ☐ weak-trace weak trace preorder

☐ **tau:** consider actions with a name in the comma separated list ACTNAMES to be internal (tau) actions in addition to those defined as such by the input

ltscompare -h

Ex1P.mcr12 [Running] Ex1Q.mcr12 [Running] Ex1Q.mcr12 [Ready] Ex1P.mcr12 [Ready] Ex1P.lps [Ready] Ex1Q.lps [Ready] Ex1P.lts [Running] Ex1Q.lts [Running] Ex1Q.lts [Ready]

Run Abort **Ready**

Autodesk Application M...
BlueJ_Projects
BlueJProjects
Bluetooth Exchange Fol...
CodeBlocks_Projects
Cursuri
Custom Office Templates
Direct Connect
FMCS-mCRL2
Ex1P.lps
Ex1P.lts
Ex1P.mcr12
Ex1Q.lps
Ex1Q.lts
Ex1Q.mcr12
Ex2.lps
Ex2.lts
Ex2.mcr12
test1.lps
test1.lts
test1.mcr12
vending_machine.lps
vending_machine.lts
vending_machine.mcr12
VM_data_types.lps
VM_data_types.lts
VM_data_types.mcr12

[20:57:15 verbose] Detected mCRL2 extension.
[20:57:15 verbose] Detected mCRL2 extension.
[20:57:15 verbose] Starting to load file Ex1Q.lts
[20:57:15 verbose] Starting to load file C:/Users/stefa_000/Documents/FMCS-mCRL2/Ex1P.lts
[20:57:15 verbose] comparing LTSs using bisim...
[20:57:15 verbose] Bisimulation partitioner created for 6 states and 6 transitions
[20:57:15 info] LTSs are strongly bisimilar

As expected, processes P and Q are strongly bisimilar.

Exercise 2:

Code:

```
EX2 x
1 %define actions
2 act
3   send, send', sendSync;
4   ack, ack', ackSync;
5   error, error', errorSync;
6   trans, trans', transSync;
7   acc, del';
8 %define processes Send, Rec and Med, which will run in parallel
9 proc
10  Send = acc.Sending;
11  Sending = send'.Wait;
12  Wait = ack.Send + error.Sending;
13
14  Rec = trans.Del;
15  Del = del'.Ack;
16  Ack = ack'.Rec;
17
18  Med = send.Med';
19  Med' = tau.Err + trans'.Med;
20  Err = error'.Med;
21
22 init
23  hide( [sendSync, errorSync, transSync, ackSync],
24        allow( [acc, del', sendSync, errorSync, transSync, ackSync],
25              comm( [send|send' -> sendSync, ack|ack' -> ackSync, error|error' -> errorSync, trans|trans' -> transSync],
26                    (Send || Med || Rec)
27                )
28            )
29  );
```

In the *act* section, I declared actions: *send*, *ack*, *error* and *trans*. The actions *send'*, *ack'*, *error'* *trans'* can be seen as the co-action of the above mentioned 4 actions, but here are defined as proper actions, because mCRL2 doesn't have co-actions like CCS. Finally, for each pair action – co-action, I declared a channel for synchronization, namely: *sendSync*, *errorSync*, *transSync* and *ackSync*. Concretely, when actions *send* and *send'* happen, their synchronization occurs on *sendSync* channel, and the same for the other 3. Giving the fact that all those 4 actions (*sendSync*, *errorSync*, *ackSync* and *transSync*) are synchronizations, they can be seen as *tau* actions (internal actions).

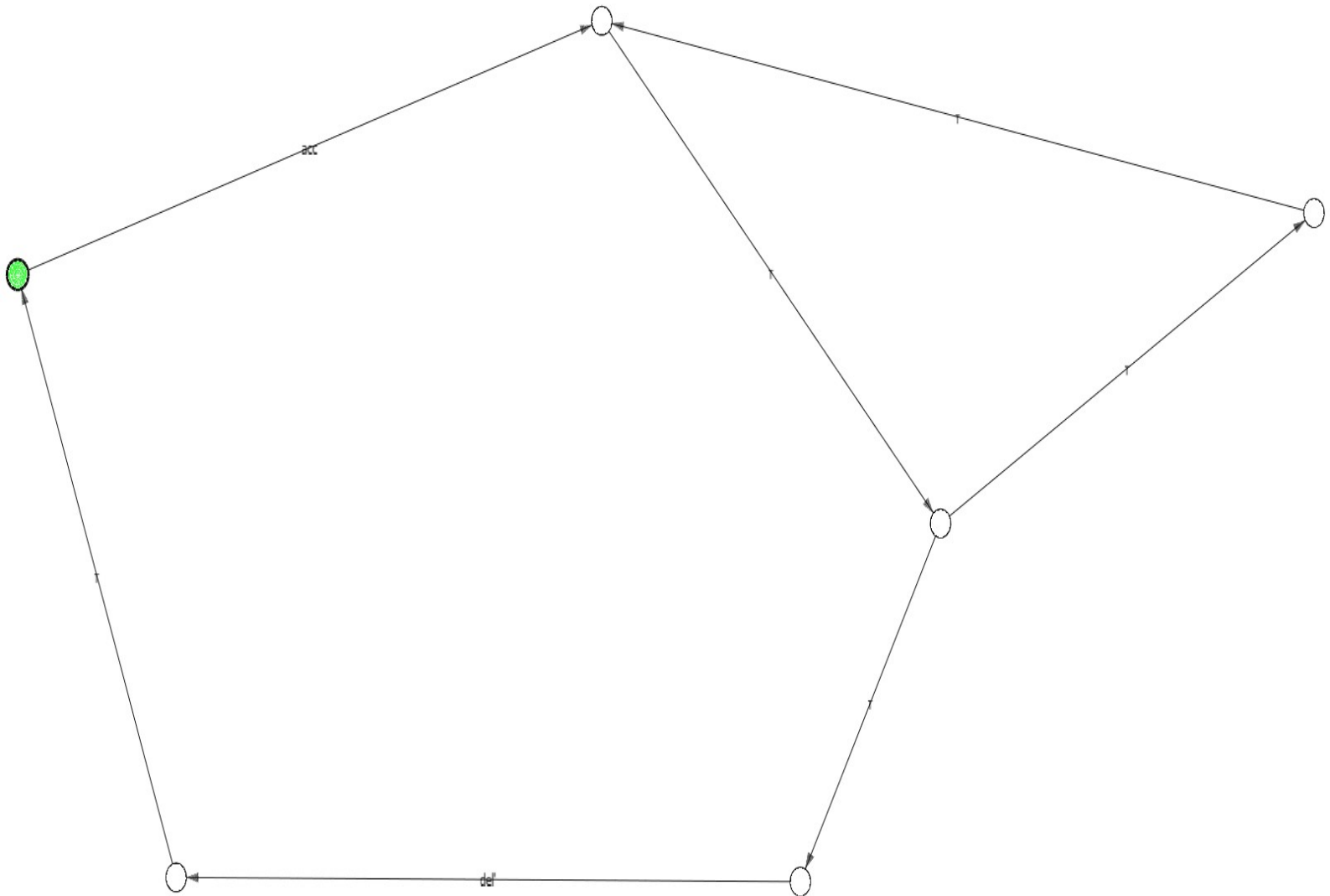
Also, there are defined *acc* and *del'* actions which can be seen as external actions.

In the *proc* section, I defined the processes as they are given in tutorial. The processes *Med*, *Rec* and *Send* will compute in parallel.

In the *init* section, I put the synchronization actions under the *hide* token, as they are restricted actions. Under the *allow* token, I wrote all those 4 synchronization actions and the external ones, namely *del'* and *acc*, as I want to let the communication to occur on those 6 channels. In the end, under the *comm* token, I specified that I want to let the communication between *send* and *send'* to occur on the *sendSync*

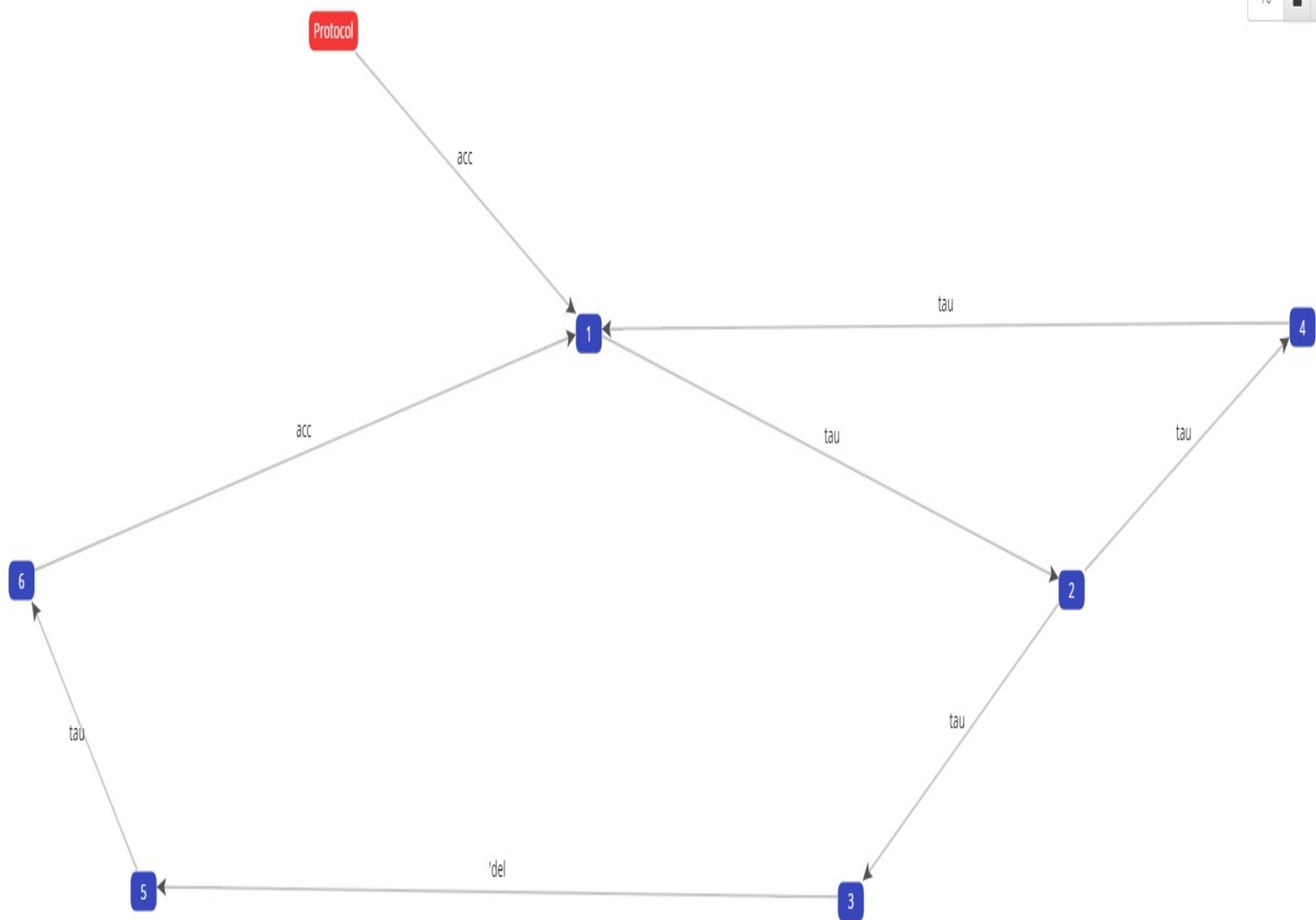
channel, and the same for the other 3 synchronizations. Then, I specified that the processes *Med*, *Rec* and *Send* are running in parallel.

The LTS graph generated with mCRL2:



There are 5 *tau* actions, one is that one *tau* might be executed when there is an error in the medium, as specified in the code, and the other 4 stand for *sendSync*, *errorSync*, *ackSync* and *transSync*. Also, there can be seen *acc* and *del'* external actions.

The LTS graph generated with CAAL (used as verification):



Exercise 3:

→ Version 1:

The code:

```
Ek3V1
1 act
2 %VM can receive five, ten, fifteen and can send chocolate, energyBar and water
3   takeFive, takeTen, takeFifteen, giveChocolate, giveEnergyBar, giveWater;
4 %User sends five and receives chocolate;
5   giveFive, takeChocolate;
6 %Sync channels
7   coinSync, chocolateSync;
8
9 proc
10  User = giveFive.takeChocolate.User;
11  VM = takeFive.giveChocolate.VM + takeTen.giveEnergyBar.VM + takeFifteen.giveWater.VM;
12
13 init
14   allow( {coinSync, chocolateSync},
15     comm( {takeFive|giveFive -> coinSync, giveChocolate|takeChocolate -> chocolateSync},
16       VM || User
17     )
18   );
19
```

```
[12:17:59 verbose] type checking process specification...
[12:17:59 info] Specification is a valid mCRL2 specification
```

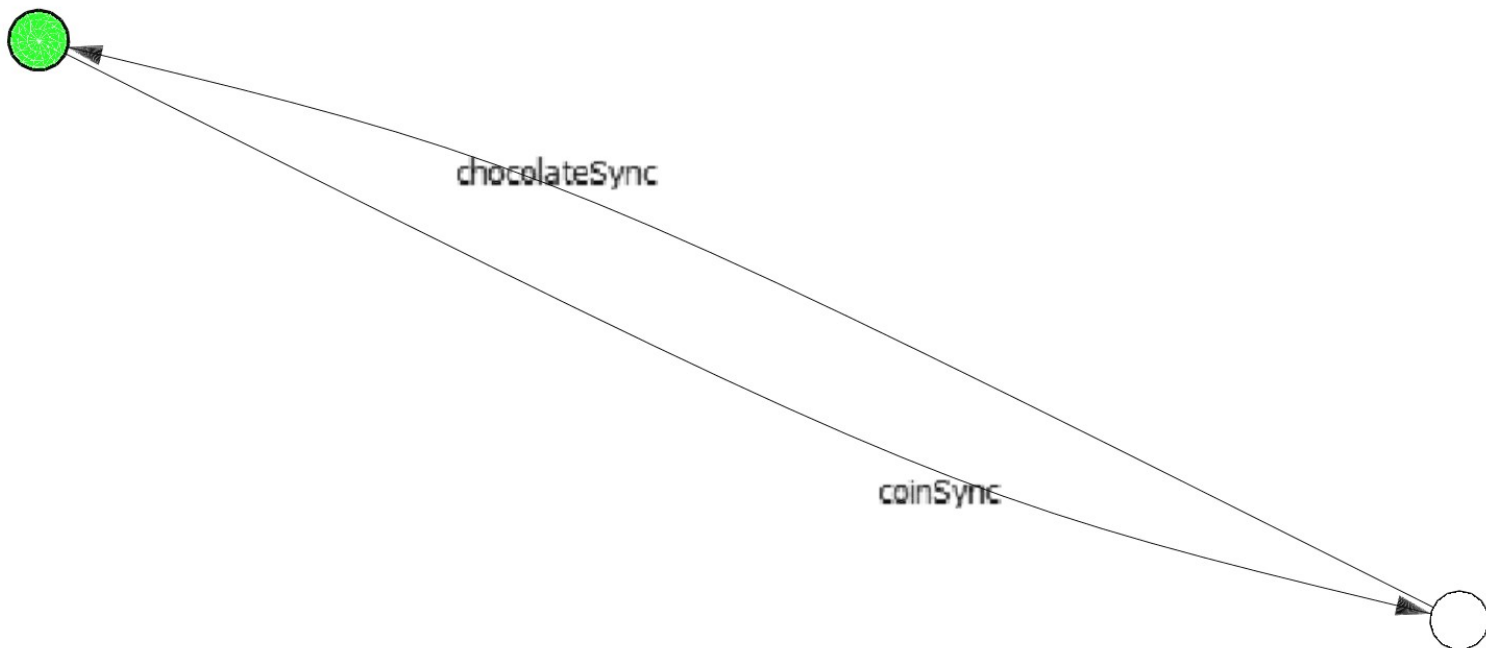
The User process does the following actions: sends a 5\$ coin (modeled by *giveFive* action) , receives a chocolate (modeled by *takeChocolate* action) and then continue to do the same (acts as User).

The VM (vending machine process) can receive a 5\$ coin (*takeFive*), then sends a chocolate (*giveChocolate*) and then acts like itself, or it can receive a 10\$ coin (*takeTen*), sends an energy bar (*giveEnergyBar*) and then act like itself, or it can receive a 15\$ coin (*takeFifteen*), sends a bottle of water (*giveWater*) and then acts like VM.

The *takeFive* and *giveFive* actions are complementary and they synchronize on channel *coinSync*. Also, *giveChocolate* and *takeChocolate* are complementary and they synchronize on channel *chocolateSync*. Those are specified under the *comm* token. Moreover, those synchronization actions are the only ones allowed, as the targeted process, namely User|| VM, exchanges information only on those 2 channels. This is specified under the *allow* token and can be seen in the graph below.

The graph:

File View Tools Help



→ Version 2:

The code:

```
Ex3V3
1 act
2 %VM can accept five, ten, fifteen on 'acc' channel, then gives an item and acts like VM
3 %User can insert 5 or 10 or 15 on 'ins' channel and, depending on the inserted coin, he takes chocolate, energyBar or water
4   ins, acc: Nat;
5   takeChocolate, giveItem, giveChocolate, giveEnergyBar, giveWater;
6 %Sync channels
7   coinSync: Nat;
8   chocolateSync;
9
10 proc
11   User(n:Nat) = (n == 5) -> ins(n).takeChocolate.User(n);
12
13   VM = sum n:Nat.( (n == 5) -> acc(n).giveChocolate.VM
14                   <> (n == 10) -> acc(n).giveEnergyBar.VM
15                   <> (n == 15) -> acc(n).giveWater.VM
16                   );
17
18 init
19   allow( {coinSync, chocolateSync},
20         comm( {ins|acc -> coinSync, takeChocolate|giveChocolate -> chocolateSync},
21              VM || User(5)
22            )
23         );
24
```

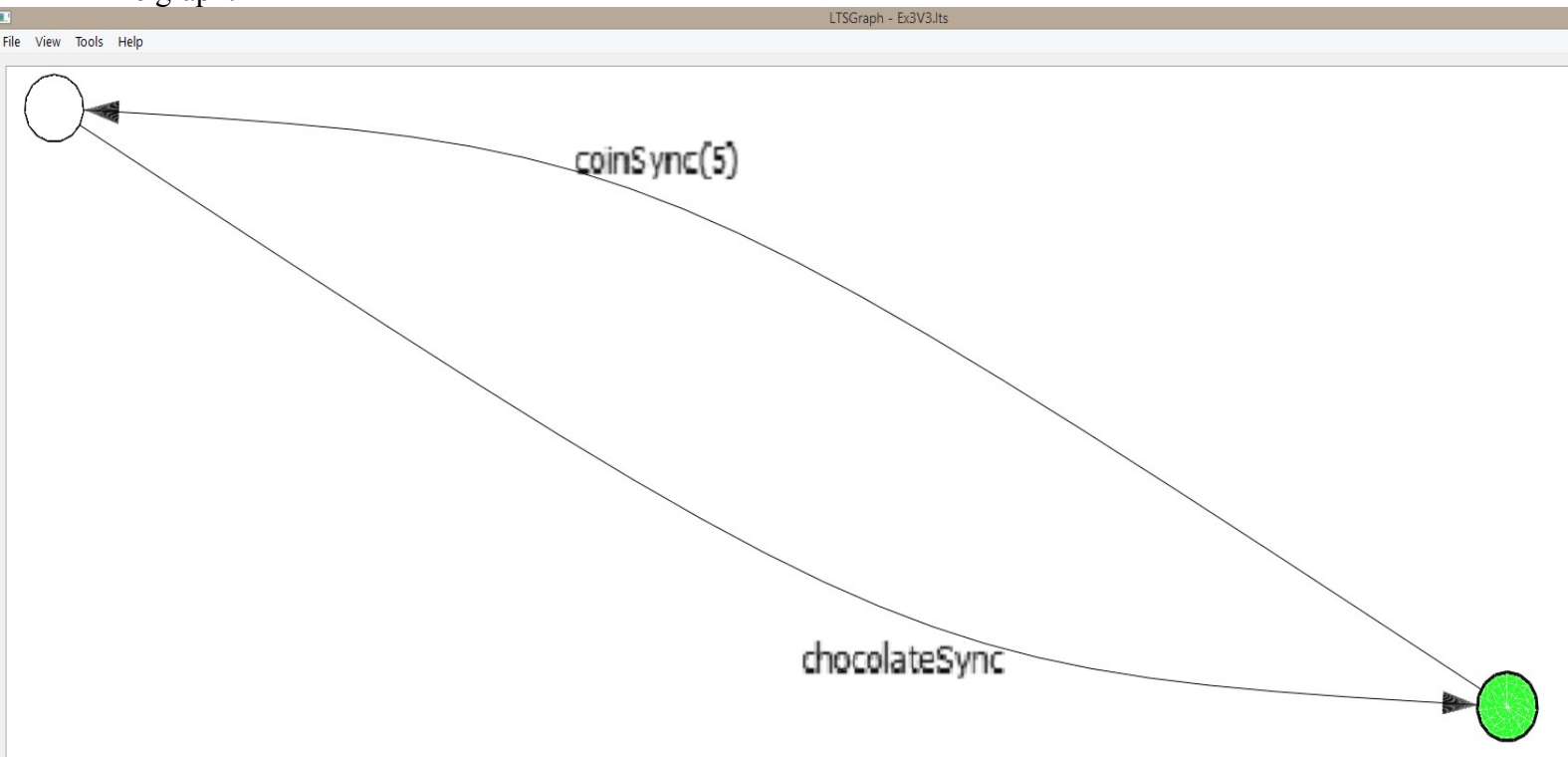
```
[12:52:48 verbose] type checking process specification...
[12:52:48 info] Specification is a valid mCRL2 specification
```

This code version is based on value passing. So, the User process is defined with a natural parameter, called n , he does action $ins(n)$ only if the condition $n==5$ is satisfied. This condition means that the User inserts a 5\$ coin. Then, he receives a chocolate ($takeChocolate$) and continue to do the same thing, behaving as $User(n)$.

The VM process is modeled as a choice between the 3 cases described in the task for this exercise. It uses the sum token to specify that and uses the natural n to specify that it can receive natural numbers on $acc(n)$ channel, which means coin receiving. Before accepting the coin, the VM verifies the coins type, then accepts it and then gives an item according to the inserted coin. In the end, it behaves like itself.

The $ins(n)$ and $acc(n)$ actions are complementary and they synchronize on $coinSync$ channel, also defined as natural. Likewise, $giveChocolate$ and $takeChocolate$ are complementary and they synchronize on channel $chocolateSync$. Those are specified under the $comm$ token. Moreover, those synchronization actions are the only ones allowed, as the targeted process, namely $User(5) \parallel VM$, exchanges information only on those 2 channels.. This is specified under the $allow$ token and can be seen in the graph below. In comparison to version 1, it is specified under the $init$ section which type of coin is inserted by using $User(5)$ call

The graph:



The LTS compare:

Ex3V1.mcr12 [Running] Ex3V3.mcr12 [Running] Ex3V1.mcr12 [Ready] Ex3V1.lps [Ready] Ex3V3.mcr12 [Ready] Ex3V3.lps [Ready] Ex3V3.lts [Running] ltscompare

Run Abort

Working directory: C:/Users/stefa_000/Documents/FMCS-mCRL2
 Input file: Ex3V3.lts
 Input file #2: C:/Users/stefa_000/Documents/FMCS-mCRL2/Ex3V1.lts

☐ **counter-example:** generate counter example traces if the input lts's are not equivalent

equivalence: use equivalence NAME (not allowed in combination with -p/--preorder):

- ☐ none identity equivalence
- ☐ bisim strong bisimilarity
- ☐ branching-bisim branching bisimilarity
- ☐ dpbranching-bisim divergence preserving branching bisimilarity
- ☒ weak-bisim weak bisimilarity
- ☐ dpweak-bisim divergence preserving weak bisimilarity
- ☐ sim strong simulation equivalence
- ☐ trace strong trace equivalence
- ☐ weak-trace weak trace equivalence

☐ **in1:** use FORMAT as the format for INFILE1 (or stdin)

*

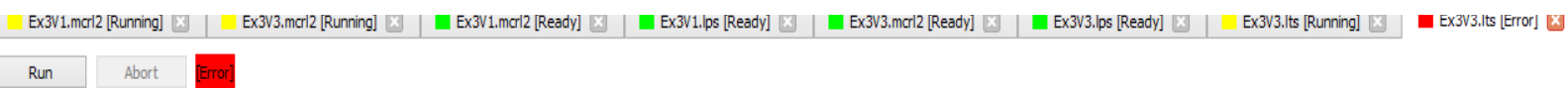
☐ **in2:** use FORMAT as the format for INFILE2

*

preorder: use preorder NAME (not allowed in combination with -e/--equivalence):

- ☒ unknown unknown preorder
- ☐ sim strong simulation preorder
- ☐ trace strong trace preorder
- ☐ weak-trace weak trace preorder

☐ **tau:** consider actions with a name in the comma separated list ACTNAMES to be internal (tau) actions in addition to those defined as such by the input

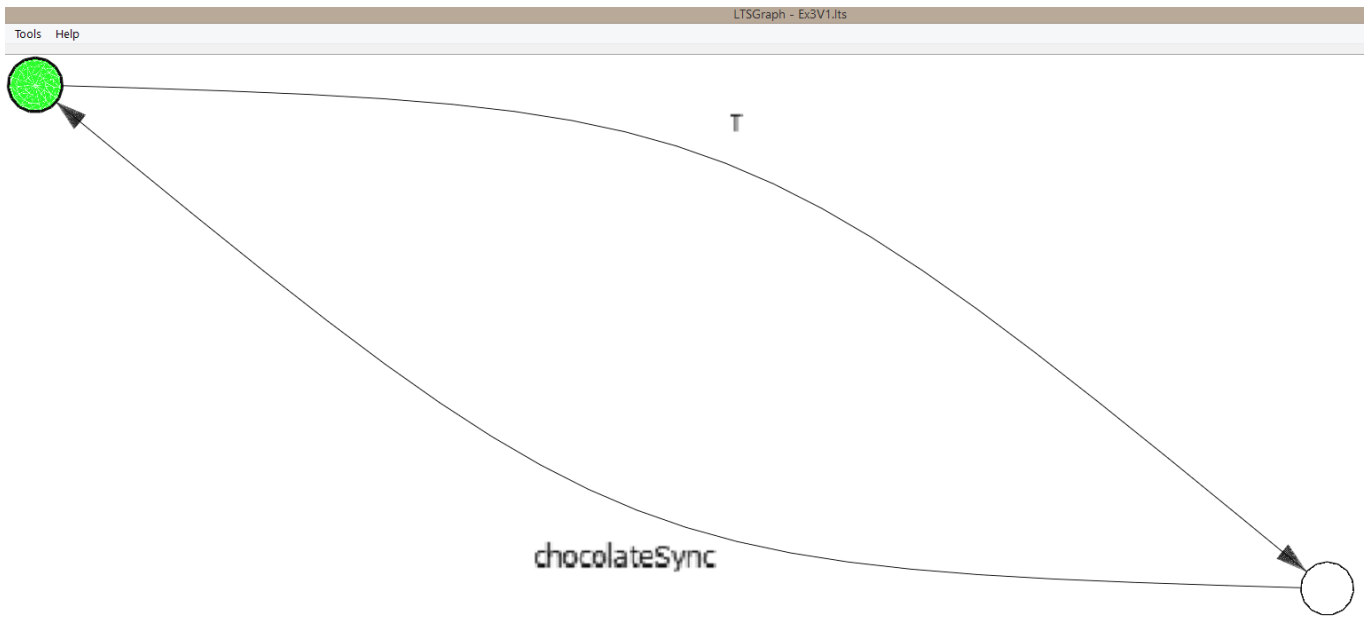


```
[13:25:38 verbose] Detected mCRL2 extension.
[13:25:38 verbose] Detected mCRL2 extension.
[13:25:38 verbose] Starting to load file Ex3V3.lts
[13:25:38 verbose] Starting to load file C:/Users/stefa_000/Documents/FMCS-mCRL2/Ex3V1.lts
[13:25:38 verbose] comparing LTSs using weak-bisim...
[13:25:38 verbose] Branching bisimulation partitioner created for 2 states and 2 transitions
[13:25:38 verbose] Bisimulation partitioner created for 2 states and 4 transitions
[13:25:38 verbose] Branching bisimulation partitioner created for 2 states and 2 transitions
[13:25:38 verbose] Bisimulation partitioner created for 1 states and 2 transitions
[13:25:38 verbose] Bisimulation partitioner created for 3 states and 3 transitions
[13:25:38 info] LTSs are not weak bisimilar
```

The 2 systems are not weakly bisimilar as the actions *coinSync* and *coinSync(5)* don't match, because they are different type of actions. This can be observed, also, in the LTS graphs. But, if in both cases the actions for sending and receiving a coin are restricted, concretely putting *coinSync* and *coinSync(5)* under the *hide* token, they will be weakly bisimilar, as the coin send-receive synchronization will be an internal action (tau), as it is presented below.

The code and the graph for version 1:

```
Ex3V1 x
1 act
2 %VM can receive five, ten, fifteen and can send chocolate, energyBar and water
3   takeFive, takeTen, takeFifteen, giveChocolate, giveEnergyBar, giveWater;
4 %User sends five and receives chocolate;
5   giveFive, takeChocolate;
6 %Sync channels
7   coinSync, chocolateSync;
8
9 proc
10   User = giveFive.takeChocolate.User;
11   VM = takeFive.giveChocolate.VM + takeTen.giveEnergyBar.VM + takeFifteen.giveWater.VM;
12
13 init
14   hide( {coinSync},
15         allow( {coinSync, chocolateSync},
16               comm( {takeFive|giveFive -> coinSync, giveChocolate|takeChocolate -> chocolateSync},
17                     VM || User
18                   )
19               )
20   );
```

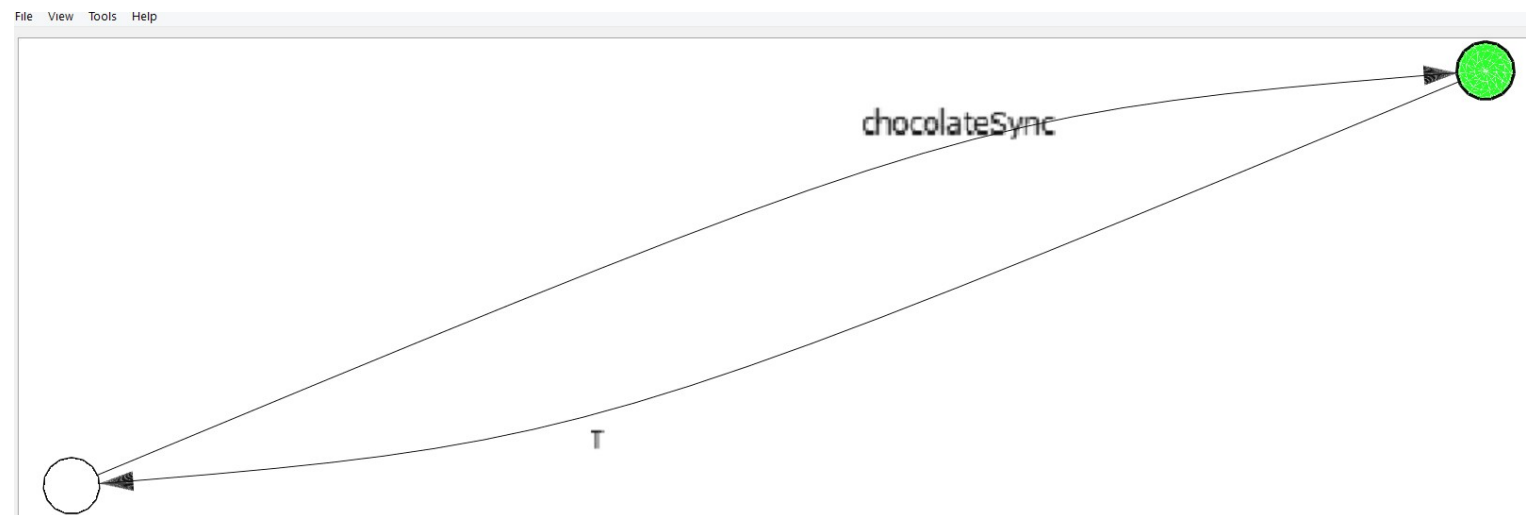


The code and the graph for version 2:

```

1 act
2 %VM can accept five, ten, fifteen on 'acc' channel, then gives an item and acts like VM
3 %User can insert 5 or 10 or 15 on 'ins' channel and, depending on the inserted coin, he takes chocolate, energyBar or water
4   ins, acc: Nat;
5   takeChocolate, giveItem, giveChocolate, giveEnergyBar, giveWater;
6 %Sync channels
7   coinSync: Nat;
8   chocolateSync;
9
10 proc
11   User(n:Nat) = (n == 5) -> ins(n).takeChocolate.User(n);
12
13   VM = sum n:Nat. ( (n == 5) -> acc(n).giveChocolate.VM
14                   <> (n == 10) -> acc(n).giveEnergyBar.VM
15                   <> (n == 15) -> acc(n).giveWater.VM
16                   );
17
18 init
19   hide( {coinSync},
20     allow( {coinSync, chocolateSync},
21       comm( {ins|acc -> coinSync, takeChocolate|giveChocolate -> chocolateSync},
22         VM || User(5)
23       )
24     )
25   );
26

```



The LTS compare:

Working directory: C:/Users/stefa_000/Documents/FMCS-mCRL2
 Input file: Ex3V3.lts
 Input file #2: C:/Users/stefa_000/Documents/FMCS-mCRL2/Ex3V1.lts

☐ **counter-example:** generate counter example traces if the input lts's are not equivalent
equivalence: use equivalence NAME (not allowed in combination with -p/--preorder):

- ☐ none identity equivalence
- ☐ bisim strong bisimilarity
- ☐ branching-bisim branching bisimilarity
- ☐ dpbranching-bisim divergence preserving branching bisimilarity
- ☒ weak-bisim weak bisimilarity
- ☐ dpweak-bisim divergence preserving weak bisimilarity
- ☐ sim strong simulation equivalence
- ☐ trace strong trace equivalence
- ☐ weak-trace weak trace equivalence

☐ **in1:** use FORMAT as the format for INFILE1 (or stdin)

☐ **in2:** use FORMAT as the format for INFILE2

preorder: use preorder NAME (not allowed in combination with -e/--equivalence):

- ☒ unknown unknown preorder
- ☐ sim strong simulation preorder
- ☐ trace strong trace preorder
- ☐ weak-trace weak trace preorder

☐ **tau:** consider actions with a name in the comma separated list ACTNAMES to be internal (tau) actions in addition to those defined as such by the input

Ex3V1.mcr12 [Running] Ex3V3.mcr12 [Running] Ex3V1.mcr12 [Ready] Ex3V1.lps [Ready] Ex3V1.lts [Running] Ex3V3.mcr12 [Ready] Ex3V3.lps [Ready] Ex3V3.lts [Running] Ex3V3.lts [Ready]

Run Abort [Ready]

```
[13:40:57 verbose] Detected mCRL2 extension.
[13:40:57 verbose] Detected mCRL2 extension.
[13:40:57 verbose] Starting to load file Ex3V3.lts
[13:40:57 verbose] Starting to load file C:/Users/stefa_000/Documents/FMCS-mCRL2/Ex3V1.lts
[13:40:57 verbose] comparing LTSs using weak-bisim...
[13:40:57 verbose] Branching bisimulation partitioner created for 2 states and 2 transitions
[13:40:57 verbose] Bisimulation partitioner created for 1 states and 2 transitions
[13:40:57 verbose] Branching bisimulation partitioner created for 2 states and 2 transitions
[13:40:57 verbose] Bisimulation partitioner created for 1 states and 2 transitions
[13:40:57 verbose] Bisimulation partitioner created for 2 states and 2 transitions
[13:40:57 info] LTSs are weak bisimilar
```

Exercise 4:

The code:

```
Ex4
1 %define actions
2 act
3   send, send', sendSync:Nat;
4   ack, ack', ackSync;
5   error, error', errorSync;
6   trans, trans', transSync:Nat;
7   acc:Nat;
8   del':Nat;
9
10 %define processes Send, Rec and Med, which will run in parallel
11 proc
12 %For a list received as a parameter for process Send, take the first element as long as list is not empty and try to send it.
13 %Thus, there will be send one at a time, in order.
14   Send(phoneBook:List(Nat)) = (#phoneBook > 0 )-> acc(head(phoneBook)).Sending(phoneBook);
15 %Send the first element and wait for a signal. Each phone number is an element of the phoneBook and is considered a natural m
16   Sending(phoneBook:List(Nat)) = send'(head(phoneBook)).Wait(phoneBook);
17 %If it is an error, retry to send it, else continue with the remaining list
18   Wait(phoneBook:List(Nat)) = ack.Send(tail(phoneBook)) + error.Sending(phoneBook);
19
20 %Receiver gets the phone number, deletes request for that phone nr and sends feedback
21   Rec(n:Nat) = trans(n).Del(n);
22   Del(n:Nat) = del'(n).Ack(n);
23   Ack(n:Nat) = ack'.Rec(n);
24
25 %Medium receives a natural number = phone number and tries to send it.
26   Med = sum n:Nat.(( n <= 9999999 )-> send(n).Med'(n));
27 %If there is an internal error try to handle it, else transmit the number to the receiver.
28   Med'(n:Nat)= tau.Err + trans'(n).Med;
29 %Send an error signal to the sender.
30   Err = error'.Med;
31
32 init
33   hide( {sendSync, errorSync, transSync, ackSync},
34     allow( {acc, del', sendSync, errorSync, transSync, ackSync},
35       comm( {send|send' -> sendSync, ack|ack' -> ackSync, error|error' -> errorSync, trans|trans' -> transSync},
36         Send([3453345, 2334123, 6564322, 4342312, 5432543, 5432555]) || Med ||
37         Rec(3453345) || Rec(2334123) || Rec(6564322) || Rec(4342312) || Rec(5432543) || Rec(5432555)
38       )
39     )
40   );
```

[13:07:06 verbose] type checking process specification...
[13:07:06 info] Specification is a valid mCRL2 specification

The *Send* process receives a list of phone numbers, it check if the list is empty and sends the first number, which is the head of the list, to the *Med* process. Then, it continues its behavior with the remaining elements in the list, namely the tail of the list. This process stops when the list is empty.

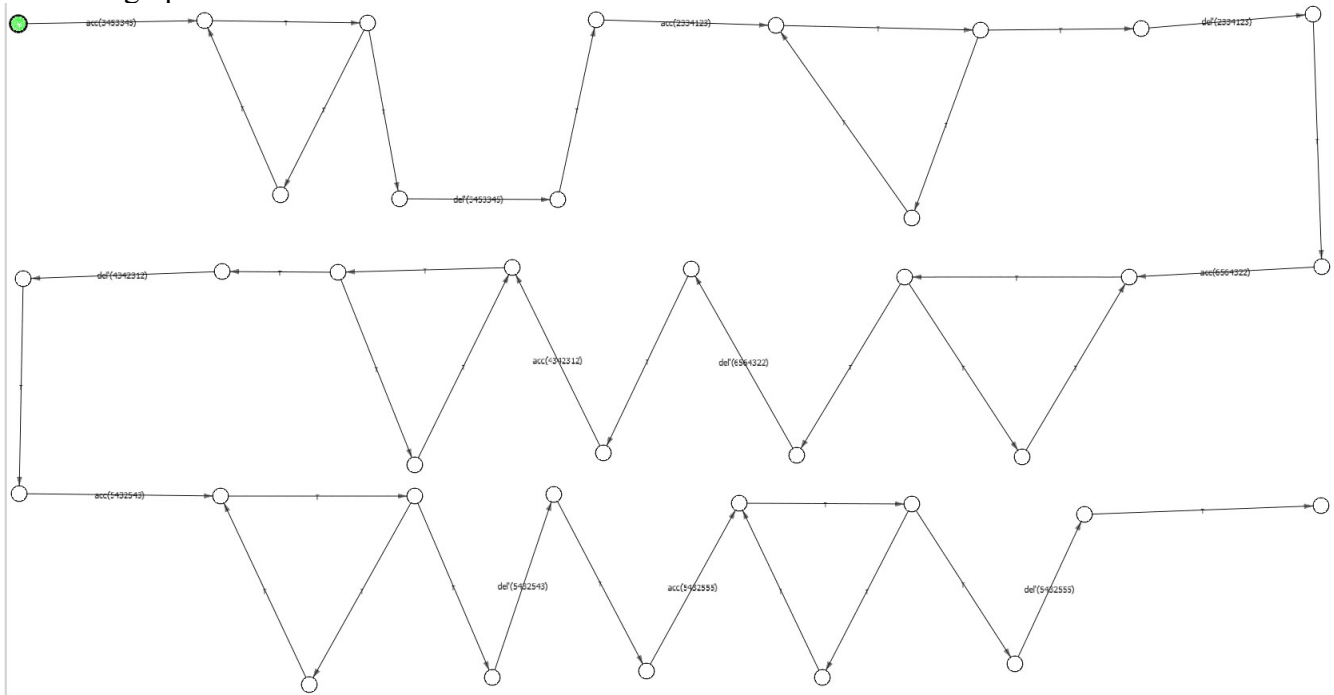
The *Med* process has the possibility of receiving natural numbers no bigger than 9 999 999, which is the largest number of 7 digits. The lower threshold is not verified as I want to let the possibility for transmit a phone number like this: 0 000 010 for example. Once received such a number, if an internal error occurs, it gets back to the state when waits for a number. Otherwise, it sends the number to the receiver, namely *Rec* process.

The *Rec* process receives a number from the *Med*, it deletes the request for that number and sends an acknowledge signal to the sender. It gets as a parameter a natural number which represents the phone number.

For each phone number, there is one *Rec* process running in parallel, as it implements the behavior of

unpredictable data transmission. This means that, despite the sender transmits packets in order, they might not arrive in the same order at the receiver.

The LTS graph:



The LTS graph is pretty similar to the graph from exercise 2, just it repeats 6 times, one time for each number. Also, the last tau action doesn't get back to the initial state, it goes to another state where it is performed *acc* action for the next number in the list. Each sequence executes 5 tau's one *acc* and one *del'* for the respective number.