IPACC IRAM Package Alpha Release 106_x_19

General

This IRAM package includes the following main features: Coarse Classification (CC), Independent-Mode (IM), Host-Commands (HC), IPv4/6 Fragmentation (IPF), IPv4/6 Reassembly (IPR), IPsec and Header Manipulation (HM).

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Version Number	Compiler version	Loader file name (.h .bin)
P2041 rev 1.0 P2041 rev 1.1 P2041 rev 2.0 (Available starting with version 106.1.0)	106_1_19	—	p2041_r1.0.h fsl_fman_ucode_p2041_r1.0_106_1_19.bin p2041_r1.1.h fsl_fman_ucode_p2041_r1.1_106_1_19.bin p2041_r2.0.h fsl_fman_ucode_p2041_r2.0_106_1_19.bin

Table 1. Package Availability by Device

P3041 rev 1.0 P3041 rev 1.1 P3041 rev 2.0 (Available starting with version 106.5)	106_1_19	—	p3041_r1.0.h fsl_fman_ucode_p3041_r1.0_106_1_19.bin p3041_r1.1.h fsl_fman_ucode_p3041_r1.1_106_1_19.bin p3041_r2.0.h fsl_fman_ucode_p3041_r2.0_106_1_19.bin
P4080 rev 2.0 P4080 rev 3.0 (Available starting with version 106.6)	106_2_19	—	p4080_r2.0.h fsl_fman_ucode_p4080_r2.0_106_2_19.bin p4080_r3.0.h fsl_fman_ucode_p4080_r3.0_106_2_19.bin
P5020 rev 1.0 P5020 rev 2.0 (Available starting with version 106.6)	106_1_19	—	p5020_r1.0.h fsl_fman_ucode_p5020_r1.0_106_1_19.bin p5020_r2.0.h fsl_fman_ucode_p5020_r2.0_106_1_19.bin
P5040 rev 1.0 P5040 rev 2.0 P5040 rev 2.1 (Available starting with version 106.6)	106_1_19	—	p5040_r1.0.h fsl_fman_ucode_p5040_r1.0_106_1_19.bin p5040_r2.0.h fsl_fman_ucode_p5040_r2.0_106_1_19.bin p5040_r2.1.h fsl_fman_ucode_p5040_r2.1_106_1_19.bin
B4860 rev 2.0 B4860 rev 2.2	106_4_19	—	b4860_r2.0.h fsl_fman_ucode_b4860_r2.0_106_4_19.bin b4860_r2.2.h fsl_fman_ucode_b4860_r2.2_106_4_19.bin
T4240 rev 1.0 T4240 rev 2.0	106_4_19	—	t4240_r1.0.h fsl_fman_ucode_t4240_r1.0_106_4_19.bin t4240_r2.0.h fsl_fman_ucode_t4240_r2.0_106_4_19.bin

Table 1. Package Availability by Device

T2080 rev 1.0 T2080 rev 1.1	106_4_19	—	t2080_r1.0.h fsl_fman_ucode_t2080_r1.0_106_4_19.bin t2080_r1.1.h fsl_fman_ucode_t2080_r1.1_106_4_19.bin
T1040 rev 1.0 T1040 rev 1.1	106_4_19	—	t1040_r1.0.h fsl_fman_ucode_t1040_r1.0_106_4_19.bin t1040_r1.1.h fsl_fman_ucode_t1040_r1.1_106_4_19.bin
T1024 rev 1.0	106_4_19	—	t1024_r1.0.h fsl_fman_ucode_t1024_r1.0_106_4_19.bin
LS1043 rev 1.0	106_4_19	—	ls1043_r1.0.h fsl_fman_ucode_ls1043_r1.0_106_4_19.bin

Table 2. Package Availability by Device

Device	Version Number	Compiler version	Loader file name (.h .bin)
P2041 rev 1.0 P2041 rev 1.1 P2041 rev 2.0 (Available starting with version 106.1.0)	106_1_18	—	p2041_r1.0.h fsl_fman_ucode_p2041_r1.0_106_1_18.bin p2041_r1.1.h fsl_fman_ucode_p2041_r1.1_106_1_18.bin p2041_r2.0.h fsl_fman_ucode_p2041_r2.0_106_1_18.bin
P3041 rev 1.0 P3041 rev 1.1 P3041 rev 2.0 (Available starting with version 106.5)	106_1_18	—	p3041_r1.0.h fsl_fman_ucode_p3041_r1.0_106_1_18.bin p3041_r1.1.h fsl_fman_ucode_p3041_r1.1_106_1_18.bin p3041_r2.0.h fsl_fman_ucode_p3041_r2.0_106_1_18.bin

Table 2. Package Availability by Device

P4080 rev 2.0 P4080 rev 3.0 (Available starting with version 106.6)	106_2_18	—	p4080_r2.0.h fsl_fman_ucode_p4080_r2.0_106_2_18.bin p4080_r3.0.h fsl_fman_ucode_p4080_r3.0_106_2_18.bin
P5020 rev 1.0 P5020 rev 2.0 (Available starting with version 106.6)	106_1_18	—	p5020_r1.0.h fsl_fman_ucode_p5020_r1.0_106_1_18.bin p5020_r2.0.h fsl_fman_ucode_p5020_r2.0_106_1_18.bin
P5040 rev 1.0 P5040 rev 2.0 P5040 rev 2.1 (Available starting with version 106.6)	106_1_18	—	p5040_r1.0.h fsl_fman_ucode_p5040_r1.0_106_1_18.bin p5040_r2.0.h fsl_fman_ucode_p5040_r2.0_106_1_18.bin p5040_r2.1.h fsl_fman_ucode_p5040_r2.1_106_1_18.bin
B4860 rev 2.0 B4860 rev 2.2	106_4_18	—	b4860_r2.0.h fsl_fman_ucode_b4860_r2.0_106_4_18.bin b4860_r2.2.h fsl_fman_ucode_b4860_r2.2_106_4_18.bin
T4240 rev 1.0 T4240 rev 2.0	106_4_18	—	t4240_r1.0.h fsl_fman_ucode_t4240_r1.0_106_4_18.bin t4240_r2.0.h fsl_fman_ucode_t4240_r2.0_106_4_18.bin
T2080 rev 1.0 T2080 rev 1.1	106_4_18	—	t2080_r1.0.h fsl_fman_ucode_t2080_r1.0_106_4_18.bin t2080_r1.1.h fsl_fman_ucode_t2080_r1.1_106_4_18.bin
T1040 rev 1.0 T1040 rev 1.1	106_4_18	—	t1040_r1.0.h fsl_fman_ucode_t1040_r1.0_106_4_18.bin t1040_r1.1.h fsl_fman_ucode_t1040_r1.1_106_4_18.bin

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Table 2. Package Availability by Device

T1024 rev 1.0	106_4_18	—	t1024_r1.0.h fsl_fman_ucode_t1024_r1.0_106_4_18.bin
LS1043 rev 1.0	106_4_18	—	ls1043_r1.0.h fsl_fman_ucode_ls1043_r1.0_106_4_18.bin

Revision History

Table 3. Revision History for Alpha Release 106.x.19

Release Date: Feb 18, 2016	
New Features	1. Changed internal IP header replace HMTD.The type of service (TOS)/traffic class field in the IPv4/IPv6 header which is inserted, determines wether this field will be duplicated from the original IPv4/IPv6 header or not. If the value in this inserted field equals “0xff” (this value is considered as invalid TOS/traffic class value), then it will be duplicated from the original frame otherwise it will remain as it was in the inserted header. 2. User can modify IPF MTU on the fly by changing MTU field in IPF Manip TD.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes/CCB	None.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 4. Revision History for Alpha Release 106.x.18

Release Date: Nov 26, 2015	
New Features	1. Fixed ERR IPR18: IPR timeout with mode enqueue may result with port stuck. Although this errata is fixed it is recommanded not using this mode of to-fqid<>0 (maybe only for debug purposes as described in the spec) and only use to-fqid=0 mode. 2. Fixed ERR IPR19: IPR timeout disable host command should flush all timeout entries. 3. Added feature which is complementary to the MBMS (Multimedia Broadcast Multicast Services) CRC error detection feature in SEC descriptor (opcode=13 in Pre/Post BMI Fetch NIAs section).
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes/CCB	None.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 5. Revision History for Alpha Release 106.x.17

Release Date: Sep 21 2015	
New Features	1. Anti-Replay window software support. 2. Implement work-around for ERR008975: FMan btcam support of 0 entries lookup (table_size = 0). 3. Added dynamic table update host-command when aging is enabled (host command opcode=0x13).
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes/CCB	None.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 6. Revision History for Alpha Release 106.x.16

Release Date: Aug18 2015	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.

Release Date: Aug18 2015	
Spec Un-Supported Features	None.
Bug Fixes/CCB	Fixed IPR17: IPR issue when last fragment is less than 60 bytes ethernet and fragment size is odd. When last IPv4 fragment is less than 60 bytes ethernet, and ip total length is odd, parser after reassembly completes reports L4 checksum error even if checksum is correct.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 7. Revision History for Alpha Release 106.x.15

Release Date: Jan 14, 2014	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes/CCB	Fixed Errata HM2 (FManV3): HM on OP when input frame is SG and VSPE=1 may result with frame data corruption.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 8. Revision History for Alpha Release 106.x.14

Release Date: Jan 14, 2014	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.

Release Date: Jan 14, 2014	
Spec Un-Supported Features	None.
Bug Fixes/CCB	This release addresses the following CCB (Change Control Board): IP short frames with L2 padding should not be encrypted with the padding. Added in IPsec Manipulation Table Descriptor before encryption mechanism to remove the padding. For more information about these changes refer to the FMan Controller spec.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 9. Revision History for Alpha Release 106.x.13

Release Date: Dec 23, 2013	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.

Release Date: Dec 23, 2013	
Bug Fixes/CCB	This release addresses the following CCB (Change Control Board): 1.) FMan V2 and FMan V3:In case frame came from RMan and it is sRIO type 9 then the FD is of SG format and most likely it is with only one entry; in order to increase performance/latency (especially if frame is directed to the SEC) the firmware converts this one entry SG format frame into single buffer format. 2.) FMan V2 only: In case frame came from SEC decryption on FMan V2 device the firmware removes the ESP trailer and updates the FD[Length] accordingly. In addition firmware adjusts the SEC S/G output frame to be compatible to FMan S/G format (valid only for FMan V2 devices after SEC decryption). For FMan V3 devices SEC HW supports ESP trailer removal and enabling storage profile also solves the FMan S/G compatible issues. For more information about these changes refer to the FMan Controller spec.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 10. Revision History for Alpha Release 106.x.12

Release Date: Nov 5, 2013	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.

Release Date: Nov 5, 2013	
Bug Fixes/CCB	This release fixes the FMan/RMan inter operability issues. A new CCB was opened for this issue with No. ENGR00285816. The following inter operability issues are tackled: – Clearing FCSI bit in the FD status (this bit has affect on the parser). – Adjust Scatter/Gather FD offset to the correct value as used for the first SG entry. – Check for RMan errors. User should set the proper OPCODE into the FQ (which is where the RMan packet enters) Context-A[A1] field in-order to support this mode. For more information refer to FMan-Controller chapter specification.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 11. Revision History for Alpha Release 106.x.11 (FMan V2)

Release Date: Aug25, 2013	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes	Relevant only to FMan V2: • Fixed IPR16- IPR malformed behaviour when there is discard on successfully reassembled frame.

Release Date: Aug25, 2013	
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 12. Revision History for Alpha Release 106.x.10

Release Date: May 30, 2013	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes	All versions: • Fixed IPR15- IPR code may return a NULL buffer to the BM pool and create deadlock. Relevant only to FMan V3 (B4860/T4240/T2080): • Fixed IPR14- Completed IPR frame corruption on V3 in case OOO fragments and VSPE=1 and forward to error queue.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 13. Revision History for Alpha Release 106.x.9

Release Date: May 6, 2013	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes	• Added check in IP Manipulation that frame is indeed IP before checking the MTU for fragmentation. In case it is not IP the fragmentation process is skipped. • IPR in FManV2 may very rarely call IPR TO with both opening and closing flags set which may result with un-expected behaviour. FMan V3 (B4860/T4240): • Fix the following HW erratas regarding discard/error frames on V3: OP with VSPE=0 does not support discard and port with VSPE=1 can have multiple VSP to the same error queue. The following defines should be set in the FMD: 'FM_OP_NO_VSP_NO_RELEASE_ERRATA_FMAN_A006675' and 'FM_ERROR_VSP_NO_MATCH_SW006 '. • IPR13 - IPR errors may result with buffer leak in case of discard decision. This can happen on both Rx or offline ports regardless of the VSP mode. • IPACC12 - If IPACC offloading is not enabled in the driver and there is parser header error in the custom classifier check- it results with un-expected behavior.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the external buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – Frame replication limitations related to IP fragmentation/reassembly were added to the spec. – On the port where IPF is enabled there will be no Storage Profile support.

Table 14. Revision History for Alpha Release 106.x.8

Release Date: April 4, 2013	
New Features	• Added another OPCODE in the context A for clearing RPD bit. • IPR TO frames: discard partially reassembled frames in FMan level by setting TO FQID=0.
New Features for B4860/T4240	• Added TotalNCSPCounter.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	None.
Bug Fixes	• IPR11 - L4 checksum validation does not work for reassembled frames in which the last fragment contains non zero Ethernet padding. • HM1 - Internal IP Header Replace HMCD (InsL3Mode =1) can be executed only if L2 is existing. • Change in IPR TO for very rare condition of disabling the last IPR port and at the same time there is HW external request that ignite the TO. • Fix an issue for Non FMan (IPsec) error - when going to BMIPreTOEnq need to set only Non FMan error bit so the BMI will not check non relevant SEC error status for the decision to discard/enqueue to error queue. The SEC error status is then restored in the NIA PostBMIPreTOEnq. FMan V3 (B4860/T4240): • IPR12 - When BMIDiscardFrame NIA is called and it is a fragment on FMan V3 then the fragment is subject to reassembly. • enhanced IPF performance by enable fragment interleaving.
Known Issues	• None. •
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the extrernal buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – On the port where IPF is enabled there will be no Storage Profile support.

Table 15. Revision History for Alpha Release 106.x.7

Release Date: Jan 17, 2013	
New Features	None.
New Features for B4860/T4240	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	1. ESPTrRem_EN mode in IPsec Manipulation TD. 2. Virtual Storage Profile Host Command.
Bug Fixes	• Fixed IPACC9 - Potential risc endless loop when reading SB_FMBM_xIBLF. FMan V3 (B4860/T4240): • Fixed IPACC10 - IP fragment header is overwritten if forwarded to another OP and VSP is disabled on this port. • Fixed IPACC11 - For IPsec error frame the FD status DCL4C/DTC bit should not be cleared. • Fixed several issues related to HM on IP fragments.
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the extrernal buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – On the port where IPF is enabled there will be no Storage Profile support.

Table 16. Revision History for Alpha Release 106.x.6

Release Date: Nov 22, 2012	
New Features	None.
New Features for B4860/T4240	None.

Release Date: Nov 22, 2012	
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	• Basic Header Manipulation. 1. Only the following HM commands are supported. – Header Removal Command Descriptor (opcode=0x01) – Local Header Insert Command Descriptor (opcode=0x02) – VLAN Priority Update Command Descriptor (opcode=0x0B) – L4 checksum calculation Command Descriptor (opcode=0x14) – Local IPv4 Update Command Descriptor (Only IP ID, IPSrc and IPDst are fields supported). (opcode=0x0C) – Local UDP/TCP Update Command Descriptor. (opcode=0x0E) – Local Header Replace Command Descriptor. (opcode=0x05) – Protocol Specific Header Removal Command Descriptor Descriptions (Only RmMode == 0000 and 0001). (opcode=0x08) – Local IPv6 Update Command Descriptor (Only IPSrc and IPDst fields are supported). (opcode=0x10) 2. The "Parse After Header Manipulation" feature is not supported. 3. ESPTrRem_EN mode in IPsec Manipulation TD. 4. Virtual Storage Profile Host Command.
Bug Fixes	• IPv6 is now supported for both IPR and IPF (removed restriction). Firmware use internally Shim2 and ShimR - Shim1 is free for the user. • Fix an issue in which IPR TO igniter goes to wrong NIA instead to the IPRTO_TimeoutTask NIA in some rare cases when: RFD[Valid]=0 or when no SG entries were built by the IPR (IPR7). • IPR bug FIX: need to dma write the first fragment header to external memory within the SW semaphore region to assure that closing thread will read updated opening fragment from external memory. This is the root cause why after IP reassembly when we go to second parser we actually returned to IPR process again and reported received fragment with SG counter error (IPR8). • When reading the TSR for TO expired decision the MTSPR that triggers the TSR sampling should be inside the lockTable limits - this may result with false TO event (IPR9). • Avoid possible dead lock when we do st.sm and immediately after it ld.sm and a SW semaphore inside the ld/st.sm limits (IPR10). FMan V3 (B4860/T4240): • it is not possible to enable more than one timeout function and it is not possible to disable timeout function (IPR6). • IPR can cause tnum starvation in very low rates due to abnormal synchronization done internally by the uCode. • Fix L4 checksum validation on OP for V3 for IPsec flow. • When ECN propagation drop appears on incoming fragment then this fragment will not enter the IP reassembly process. • Remove uCode WA for the BMI HW bug that releases the wrong internal buffer. This uCode WA is only necessary for B4 rev1 silicon.

Release Date: Nov 22, 2012	
Known Issues	• None.
Restrictions	• MPLS frame headers are not supported. • See Table 19. • Additional FManV3 restrictions: – L4 checksum offloading (validation or update) requires not to overwrite the parser results on the OP dequeue VSP. If VSP is not enabled and L4 checksum offloading is needed then parser results can not be reflected in the extrernal buffer (for example if IPF is enabled). – After SEC decryption on SEC5 (FManV3) need to enable AOFL mode (see AOFL description in SEC 5.3) if L4 checksum validation is required. – Checksum update for FManV3 done by HW on TX port is not possible when frame is FW from OP to TX port since uCode clears DTC bit in the FD. Therefore user need to use HM to update L4 checksum in this case. User also need to use this HM command when need to update L4 checksum on the frame before encryption or when we do fragmentation. In case CPU wants to push directly to TX port a frame then it can use the TX HW feature in order to update the L4 checksum (in the same method as done for FManV2). – On the port where IPF is enabled there will be no Storage Profile support.

Table 17. Revision History for Alpha Release 106.x.5

Release Date: Sep 23, 2012	
New Features	• IPR on V3 • HM New commands: – Local Header Replace Command Descriptor. – Protocol Specific Header Removal Command Descriptor Descriptions (Only RmMode == 0000 and 0001)
New Features for B4860/T4240 (Partialy verified on simulator only)	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	• Basic Header Manipulation. 1. Only the following HM commands are supported. – Header Removal Command Descriptor (opcode=0x01) – Local Header Insert Command Descriptor (opcode=0x02) – VLAN Priority Update Command Descriptor (opcode=0x0B) – L4 checksum calculation Command Descriptor (opcode=0x14) – Local IPv4 Update Command Descriptor (Only IP ID, IPSrc and IPDst are fields supported). (opcode=0x0C) – Local UDP/TCP Update Command Descriptor. (opcode=0x0E) – Local Header Replace Command Descriptor. (opcode=0x05) – Protocol Specific Header Removal Command Descriptor Descriptions (Only RmMode == 0000 and 0001). (opcode=0x08) 2. The "Parse After Header Manipulation" feature is not supported.

Release Date: Sep 23, 2012	
Bug Fixes	• RFD dma was rejected more than 16 time may result with non returned RFD Index resource (IPR5 errata). • IP reassembly and IP fragmentation consume two shim offset fields in parser results array (IPACC8 errata). FMan V3 (B4860/T4240): • IPv4 options counter may stuck the system when it gets illegal frames (IPF3 errata). • IPF implementation may result with un expected behaviour of the BMI (IPF4 errata).
Known Issues	•
Restrictions	• IPv6 and MPLS frame headers are not supported. • See Table 19.

Table 18. Revision History for Alpha Release 106.x.4

Release Date: Aug 23, 2012	
New Features	• HM New commands: – Local IPv4 Update Command Descriptor (Only IP ID, IPSrc and IPDst are fields supported). – Local UDP/TCP Update Command Descriptor.
New Features for B4860/T4240 (Partialy verified on simulator only)	None.
New Features (Not in spec)	• See Table 19.
Spec Un-Supported Features	• Basic Header Manipulation. 1. Only the following HM commands are supported. – Header Removal Command Descriptor (opcode=0x01) – Local Header Insert Command Descriptor (opcode=0x02) – VLAN Priority Update Command Descriptor (opcode=0x0B) – L4 checksum calculation Command Descriptor (opcode=0x14) – Local IPv4 Update Command Descriptor (Only IP ID, IPSrc and IPDst are fields supported). (opcode=0x0C) – Local UDP/TCP Update Command Descriptor. (opcode=0x0E) 2. The "Parse After Header Manipulation" feature is not supported. • IPR for FMan V3. • Conditional statistics on V3. • Custome Classifier operational code: – IPv4 and IPv6 TOS shared handling.
Bug Fixes	• IPR ECN propagation feature may result with deadlock (IPR4 errata). • IPF and HM may fail due to malformed FOF after 6 different types of CC OperationCodes (IPACC7). FMan V3 (B4860/T4240): • Avoid overwriting Parser-Results by the meta-data both by uCode (which does not initialoize it anymore) and user. This was an issue for V3 OP after decryption - since we could not do L4 checksum validation since the running-sum was overwritten by the meta-data (or ucode initialization). • Frame corruption caused by the TX Port's checksum update on FManV3: For B4860Rev1, there is a uCode workaround that always clears the Do TCP Checksum (DTC) bit. This effectively removes the TX Port's checksum offload feature when flow starts on the OP. • On B4860Rev1 there is a BMI HW bug that releases the wrong internal buffer. uCode WA is implemented in this release. This workaround requires the following from the driver: – RX FIFOs of all ETH ports must be enlarged by 4K each. – The BMI should be configured to discard frames that encounter MAC errors (Frame Physical Error = FPE). – On Rx and offline ports driver must use “Pre-BMIPreToEnq” (Post-BMIPreToEnq is optional for this WA) and “PopToNextStep” RISC NIAs as illustrated in the AN. • TCP checksum calculation feature should tribute 0xFFFF as any other checksum value.

Table 18. Revision History for Alpha Release 106.x.4

Release Date: Aug 23, 2012	
Known Issues	• RFD dma was rejected more than 16 time may result with non returned RFD Index resource (IPR5 errata). • IP reassembly and IP fragmentation consume two shim offset fields in parser results array (IPACC8 errata). FMan V3 (B4860/T4240): • IPv4 options counter may stuck the system when it gets illegal frames (IPF3 errata). • IPF implementation may result with un expected behaviour of the BMI (IPF4 errata).
Restrictions	• See Table 19.

Table 19. Revision History for Alpha Release 106.x.3

Release Date: July 15, 2012	
New Features	• IPsec DPOVRD VarIPLen/NextHdr new implementation. • IPR ECN propagation. • IPF after SEC with SG support. • New statistics AD + MIB support per flow (STD). • HM New commands: – Header Removal Command Descriptor . – Local Header Insert Command Descriptor. – VLAN Priority Update Command Descriptor.
New Features for B4860/T4240 (Partialy verified on simulator only)	• HM New commands: – L4 checksum calculation. • IPF on FMan V3. • Policer after IPF. • Frame Replicator. • IPF IPv4 options counter.

Table 19. Revision History for Alpha Release 106.x.3

Release Date: July 15, 2012	
New Features (Not in spec)	10G MAC ECC error work around (FMAN11 Errata - valid only for P2041, P3041, P4080, P5020, P5040): The loopback should be ignited after the 10GMAC and the common part of the BMI was initialized. To ignite the loop back user need to enable Lynx and then write 0x40000000 to 0xc3074 (FMFP_ EXTC[INV1] bit). On external request completion this bit is cleared (FMFP_ EXTC[INV1] bit). More detailed user flow: 1. Enable the 10G MAC and set promiscuous mode. 2. Enable workaround and wait for it to end: 2.1 Write 0x80000000 to FM_BASE_ADDR + 0xc400c (IRAM Ready) . 2.2 Wait (wait 5 ms). 2.3 Write 0x40000000 to FM_BASE_ADDR + 0xc3074 (FMFP_EXTC). 2.4 Wait till FMFP_EXTC[INV1] bit is cleared. 3. Disable the 10G MAC and clear promiscuous mode. The following are the requirements for the DMA Semaphore SW implementation on P4080: (Note that possible number of entries are: 8, 16, 24 and 32) • Allocate 128 bytes plus (72 Bytes* #Number of Entries) in the MURAM, aligned to 64 Bytes, in the following way: a. All but first 4 bytes with '0' values. b. First 4 bytes by the following rules: – 0xff000000 for 8 entries. – 0xffff0000 for 16 entries. – 0xffffff00 for 24 entries. – 0xffffffff for 32 entries. • FMDMEBCR contains <address> of memory block. • Bits 16-18 in FMDMMR (CEN) contains: – 000 for 8 entries. – 001 for 16 entries. – 010 for 24 entries. – 011 for 32 entries.
Spec Un-Supported Features	• Basic Header Manipulation. 1. Only four HM commands are supported. – Header Removal Command Descriptor (opcode=0x01) – Local Header Insert Command Descriptor (opcode=0x02) – VLAN Priority Update Command Descriptor (opcode=0x0B) – L4 checksum calculation Command Descriptor (opcode=0x14) 2. The "Parse After Header Manipulation" feature is not supported. 3. IPR for FMan V3.
Bug Fixes	• IPACC3 - IP fragmentation after SEC encryption supports only single buffer format. • IPACC6 - Propagate ECN/DSCP feature may cause data corruption on subsequent TX port. • IPF2 - Setting the FD[Status][RPD] bit on a frame that is forwarded to an Offline Port which enables IP Fragmentation may cause data corruption on the subsequent TX port.

Table 19. Revision History for Alpha Release 106.x.3

Release Date: July 15, 2012	
Known Issues	• IPF and HM may get malformed FOF after the following CC OperationCodes: Shim1, Shim2, IPPidOffset, Generic_1_Off_OffParserResult_GMASK, Generic_3_Off, Generic_4_Off_GMASK. This issue is relevant only if the IPF/HM occurs after the above CC operational codes w/o any HW engine between. FMan V3 (B4860/T4240): • Current driver always use 64 bytes meta-data transfer size. This means that Parser-Results is always overwritten. This is an issue for V3 OP after decryption - since we will not be able to do L4 checksum validation since the running-sum was overwritten by the meta-data. • Frame corruption caused by the TX Port's checksum update on FManV3: For B4860Rev1, there is a uCode workaround that always clears the Do TCP Checksum (DTC) bit. This effectively removes the TX Port's checksum offload feature. • On B4860Rev1 there is a BMI HW bug that releases the wrong internal buffer. uCode WA is not implemented i this release. • TCP checksum calculation feature should tribute 0xFFFF as any other checksum value.
Restrictions	• IP Reassembly and IP Fragmentation can not run on the same port in FManV2. • IP Fragmentation does not support re-writing the fragments to a new storage profile. (This means that OMB must be set as follows: EBD=0, EBAD=1.) • IPR and IPF can run on the same port on FManV3 in accordance with restriction #2 above. • IP Fragmentation runs only on OP (not RX or TX) • HM can be performed before IP Fragmentation, but must not be performed after IP Fragmentation. e.

Table 20. Revision History for Alpha Release 106.x.2

Release Date: May 6, 2012	
New Features	• The UDP/TCP checksum field can now be validated for re-assembled frames. • The DSCP/ECN fields can each be independently propagated from the inner/outer IP Header to the outer/inner IP Header during IPsec Encapsulation/De-capsulation. See the IPsec Manipulation Table Descriptor in the RM. • Frames with varying IP Header lengths belonging to the same Security Assocation are now supported. See the IPsec Manipulation Table Descriptor in the RM.
New Features (Not in spec)	10G MAC ECC error work around (FMAN11 Errata): The loopback should be ignited after the 10GMAC and the common part of the BMI was initialized. To ignite the loop back user need to enable Lynx and then write 0x40000000 to 0xc3074 (FMFP_ EXTC[INV1] bit). On external request completion this bit is cleared (FMFP_ EXTC[INV1] bit). More detailed user flow: 1. Enable the 10G MAC and set promiscuous mode. 2. Enable workaround and wait for it to end: 2.1 Write 0x80000000 to FM_BASE_ADDR + 0xc400c (IRAM Ready) . 2.2 Wait (wait 5 ms). 2.3 Write 0x40000000 to FM_BASE_ADDR + 0xc3074 (FMFP_EXTC). 2.4 Wait till FMFP_EXTC[INV1] bit is cleared. 3. Disable the 10G MAC and clear promiscuous mode. The following are the requirements for the DMA Semaphore SW implementation on P4080: (Note that possible number of entries are: 8, 16, 24 and 32) • Allocate 128 bytes plus (72 Bytes* #Number of Entries) in the MURAM, aligned to 64 Bytes, in the following way: a. All but first 4 bytes with '0' values. b. First 4 bytes by the following rules: – 0xff000000 for 8 entries. – 0xffff0000 for 16 entries. – 0xffffff00 for 24 entries. – 0xffffffff for 32 entries. • FMDMEBCR contains <address> of memory block. • Bits 16-18 in FMDMMR (CEN) contains: – 000 for 8 entries. – 001 for 16 entries. – 010 for 24 entries. – 011 for 32 entries.

Table 20. Revision History for Alpha Release 106.x.2

Release Date: May 6, 2012	
Spec Un-Supported Features	• Basic Header Manipulation. 1. Only two HM commands are supported. – Header Removal Command Descriptor (opcode=0x01) – Local Header Insert Command Descriptor (opcode=0x02) 2. The HM commands are not supported with S/G operation mode. 3. The "Parse After Header Manipulation" feature is not supported. The following features are not supported: • Reassembly of fragments does not lose indications of congestion. • An interrupt is raised if an IPv4 frame with IPv4 Options is encountered and the COPIED flag on one of the options is cleared. • Statistics Table Descriptor (STD).
Bug Fixes	• Variable IP Length feature caused unpredictable behavior when run in combination with IP Reassembly. • Frames with a Parser Error potentially caused Coarse Classification functions (such as IP Fragmentation) to behave unpredictabely. The fix forwards these frames directly to BMI Prepare To Enqueue. • Frame corruption occurred on SEC SG output frames with metadata. • IPSecManip[ECN_EN] and IPSecManip[CDSCP_EN] modes resulted in a corrupted TOS field when used together with IP Reassembly. • IP in IP can result in an unexpected behaviour if IPR/IPF are enabled. • When propagating metadata through the SEC, the initiailzed parser result contents may be corrupted.
Known Issues	• None
Restrictions	• IP Fragmentation of Scatter Gather frames generated by the SEC is not supported. • IP Reassembly and IP Fragmentation can not run on the same port in FManV2. • IP Fragmentation does not support re-writing the fragments to a new storage profile. (This means that OMB must be set as follows: EBD=0, EBAD=1.) • IPR and IPF can run on the same port on FManV3 in accordance with restriction #2 above. • IP Fragmentation runs only on OP (not RX or TX) • HM can be performed before IP Fragmentation, but must not be performed after IP Fragmentation. e.

Table 21. Revision History for Engineering Release 106.x.1

Release Date: Apr 19, 2012	
New Features (Not in spec)	None.
Spec Un-Supported Features	• Basic Header Manipulation. 1. Only two HM commands are supported. – Header Removal Command Descriptor (opcode=0x01) – Local Header Insert Command Descriptor (opcode=0x02) 2. The HM commands are not supported with S/G operation mode. 3. The "Parse After Header Manipulation" feature is not supported. • Reassembly of fragments does not lose indications of congestion. • An interrupt is raised if an IPv4 frame with IPv4 Options is encountered and the COPIED flag on one of the options is cleared. • Statistics Table Descriptor (STD).
Bug Fixes	• Introduced the new SW flow-ID method. • IPR L4 checksum validation was added.
Known Issues	• SEC output frame of format SG is not supported. • There are some potential erroneous frames/fragments that may reach the IP reassembly or IP fragmentation processes and will not be related as such (meaning processing will continue as usual). For example for IP fragmentation parser error can continue its IP fragmnetation processing, and other possible errors as frame physical error set by the HW can continues their normal IP reassembly or IP fragmentation processes. • IP in IP can result un expected behaviour in case IPR/IPF.

Table 22. Revision History for Engineering Release 106.x.0

Release Date: Feb28, 2012	
New Features (Not in spec)	None. **Note:** This package uses internal buffers required by the IP reassembly process from a special IP reassemly pool instead from the BMI port resources. In addition the LIODN used for the S/G buffer built by the IPR process is taken from the FD of the fragment instead from the IP reassembly table descriptor. This is the last IP reassembly release that supports the “old” SW flow-ID method.
Spec Un-Supported Features	None. This release still does not introduces the new SW flow-ID method.

Table 22. Revision History for Engineering Release 106.x.0

Release Date: Feb28, 2012	
Bug Fixes	1. IP reassemblly now uses the LIODN from the processed fragment FD and not from IPR TD when accessing the SG list which the IPR builds. 2. IP reassembly now uses its own internal buffer pool instead of using the HW port resources. The reasons for this change are: a) There is an HW bug that can cause SKY BLUE dead lock for FMan V2 devices (except SC1023). b) BMI internal calculations assumes that the internal FIFO resources should not be shared with the RISC. 3. Fix several IP reassembly time-out issues: a) Fix of potential bug: added verification of sky-blue write for parking and unparking TNUMs. b) Performance optimization: using sw flag to minimize the duration between ld.sm and st.sm c) When last timeout function is disabled, the resources (TNUM and page) of the timeout igniter are released.
Known Issues	There are some potential errornes frames/fragments that may reach the IP reassembly or IP fragmentation processes and will not be related as such (meaning processing will continue as usual). For example for IP fragmentation parser error can continue its IP fragmnetation processing, and other possible errors as frame physical error set by the HW can continues their normal IP reassembly or IP fragmentation processes. These issues will be solved by next IPR releases when introducing the new flow-ID method. 1. Frames or IP fragments on a Pre-SEC OP port that bypass the SEC will encounter a SEC error in the post-SEC OP port. 2. IP fragments on a Pre-SEC OP port that bypass the SEC will encounter a UDP Length Error. 3. Setting FD[RFD] bit for frames on Pre-SEC OP that goes to SEC will cause SEC Error. 4. IP fragmentation after SEC encryption supports only single buffer format.

Table 23. Revision History for Engineering Release 106.8

Release Date: Dec 12, 2011	
New Features (Not in spec)	User-configurable Buffer Pool ID for buffer allocation performed by the IP Fragmentation function.
Spec Un-Supported Features	None.

Table 23. Revision History for Engineering Release 106.8

Release Date: Dec 12, 2011	
Bug Fixes	None.
Known Issues	1. Frames or IP fragments on a Pre-SEC OP port that bypass the SEC will encounter a SEC error in the post-SEC OP port. 2. IP fragments on a Pre-SEC OP port that bypass the SEC will encounter a UDP Length Error. 3. Setting FD[RFD] bit for frames on Pre-SEC OP that goes to SEC will cause SEC Error. 4. IP fragmentation after SEC encryption supports only single buffer format. 5. IP reassemblly shall use the LIODN from the processed fragment FD and not from IPR TD when accessing the SG list which the IPR builds.

Table 24. Revision History for Engineering Release 106.7

Release Date: Nov 7, 2011	
New Features (Not in spec)	None.
Spec Un-Supported Features	None.
Bug Fixes	1. Inbound Rule Validation according to SW FlowID (written into ContextA[A0] or in ContextB 9 lsb for devices not supporting this field) is fixed. 2. Forwarding re-assembled frames directly to the post-SEC port is fixed.
Known Issues	1. Frames on a Pre-SEC OP port that bypass the SEC will encounter a SEC error in the post-SEC OP port. 2. IP fragmentation after SEC encryption supports only single buffer format.

Table 25. Revision History for Engineering Release 106.6

Release Date: Oct 03, 2011	
New Features (Not in spec)	None.
Spec Un-Supported Features	None.

Table 25. Revision History for Engineering Release 106.6

Release Date: Oct 03, 2011	
Bug Fixes	
Known Issues	1. Inbound Rule Validation according to SW FlowID (written into ContextA[A0] or in ContextB 9 lsb for devices not supporting this field) is not supported. 2. In the IPR/IPsec code we have two scenarios where we deliberately set/clear bits in FD[status] that may have affect on sequential ports. For example: FD[Status][DCL4C] bit that IPR set as a workaround for not able to validate UDP/TCP checksum - if the IPR frame would be forwarded to the OP which is also used as SEC output (this is as DTI UC works) - we will get SEC error. For IPsec OP we also set this bit to indicate the parser that L4 checksum validation is not supported. 3. IP fragmentation after SEC encryption supports only single buffer format.

Table 26. Revision History for Engineering Release 106.5

Release Date: June 15, 2011	
New Features (Not in spec)	None.
Spec Un-Supported Features	IPv6 Fragmentation and IPv6 Reassembly. IPv4 IPF and IPv4 IPR do not support error flows nor IPv4 options in this initial release.
Bug Fixes	
Known Issues	

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