

CFG-LED Latches

The diagram illustrates the logic for the CFG-LED Latches, showing three stages of logic (log1, log2, log3) and their corresponding LED outputs.

Stage 1 (Left):

- U1A:** SN74LVC00APWE4 (Inverter), VCC to +2V5, GND to GND.
- U1B:** SN74LVC00APWE4 (Inverter), VCC to +2V5, GND to GND.
- U1C:** SN74LVC00APWE4 (NAND gate), VCC to +2V5, GND to GND.
- Inputs:** CFG_Failed (4), Rst (2).
- Outputs:** 2Y (6), 1Y (3).
- LED:** RED LED (D13) connected to GND through a 200R resistor (R8).

Stage 2 (Middle):

- U2:** 74AUP1G04 (Inverter), VCC to +2V5, GND to GND.
- U1D:** SN74LVC00APWE4 (NAND gate), VCC to +2V5, GND to GND.
- Inputs:** CFG_Done (2), Rst (13).
- Outputs:** 3Y (8), 4Y (11).
- LED:** GREEN LED (D14) connected to GND through a 200R resistor (R9).

Stage 3 (Right):

- U1E:** SN74LVC00APWE4 (Inverter), VCC to +2V5, GND to GND.
- U1F:** SN74LVC00APWE4 (NAND gate), VCC to +2V5, GND to GND.
- Inputs:** CFG_Done (2), Rst (13).
- Outputs:** 3Y (8), 4Y (11).
- LED:** BLUE LED (D15) connected to GND through a 200R resistor (R10).

CFG-LED Latches

The diagram illustrates the logic for the CFG-LED Latches, showing three stages of circuitry.

Stage 1 (Left): This stage uses two 74LVC00APWE4 inverters (U1A and U1B) and a 74LVC00APWE4 NAND gate (U1C). The inputs are `CFG_Failed` (pin 4 of U1C) and `Rst` (pin 2 of U1B). The output of U1C (pin 6) is connected to a red LED (D13) through a 200R resistor (R8), labeled **FAILED**. The output of U1B (pin 3) is connected to the input of U1C (pin 5). The circuit is powered by +2V5.

Stage 2 (Middle): This stage uses a 74AUP1G04 inverter (U2) and a 74LVC00APWE4 NAND gate (U1D). The input is `CFG_Done` (pin 2 of U2). The output of U2 (pin 4) is connected to the input of U1D (pin 9). The output of U1D (pin 8) is connected to a green LED (D14) through a 200R resistor (R9), labeled **DONE**. The circuit is powered by +2V5.

Stage 3 (Right): This stage shows two 74LVC00APWE4 inverters (U1A and U1B) connected to a +2V5 supply. The output of U1A (pin 7) is connected to the input of U1B (pin 12). The output of U1B (pin 11) is connected to the input of U1A (pin 14).

IO Configuration

Header Interface

{User_Clks}D {User_Clks}

The diagram illustrates the IO Configuration. On the left, a green box labeled 'Header Interface' contains the text '{User_Clks}D {User_Clks}'. A blue line connects this box to a list of pins on the right. The pins are numbered 1 through 10 and are connected to a common bus labeled '{SerDes}'. The pins are: 1 TX0_P, 2 TX0_N, 3 RX0_P, 4 RX0_N, 5 CLK_N, 6 CLK_P, 7 TX1_P, 8 TX1_N, 9 RX1_P, and 10 RX1_N.

Pin	Signal
1	TX0_P
2	TX0_N
3	RX0_P
4	RX0_N
5	CLK_N
6	CLK_P
7	TX1_P
8	TX1_N
9	RX1_P
10	RX1_N

Resistor values if not specified = 200R
Color if not specified = green

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Pin	Signal
1	TX0_P
2	TX0_N
3	RX0_P
4	RX0_N
5	CLK_N
6	CLK_P
7	TX1_P
8	TX1_N
9	RX1_P
10	RX1_N

Resistor values if not specified = 200R
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IO Configuration

Header Interface

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Pin	Signal
1	TX0_P
2	TX0_N
3	RX0_P
4	RX0_N
5	CLK_N
6	CLK_P
7	TX1_P
8	TX1_N
9	RX1_P
10	RX1_N

Resistor values if not specified = 200R
Color if not specified = green

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Size: A4	Date: 2024-12-20	Rev: 0.1
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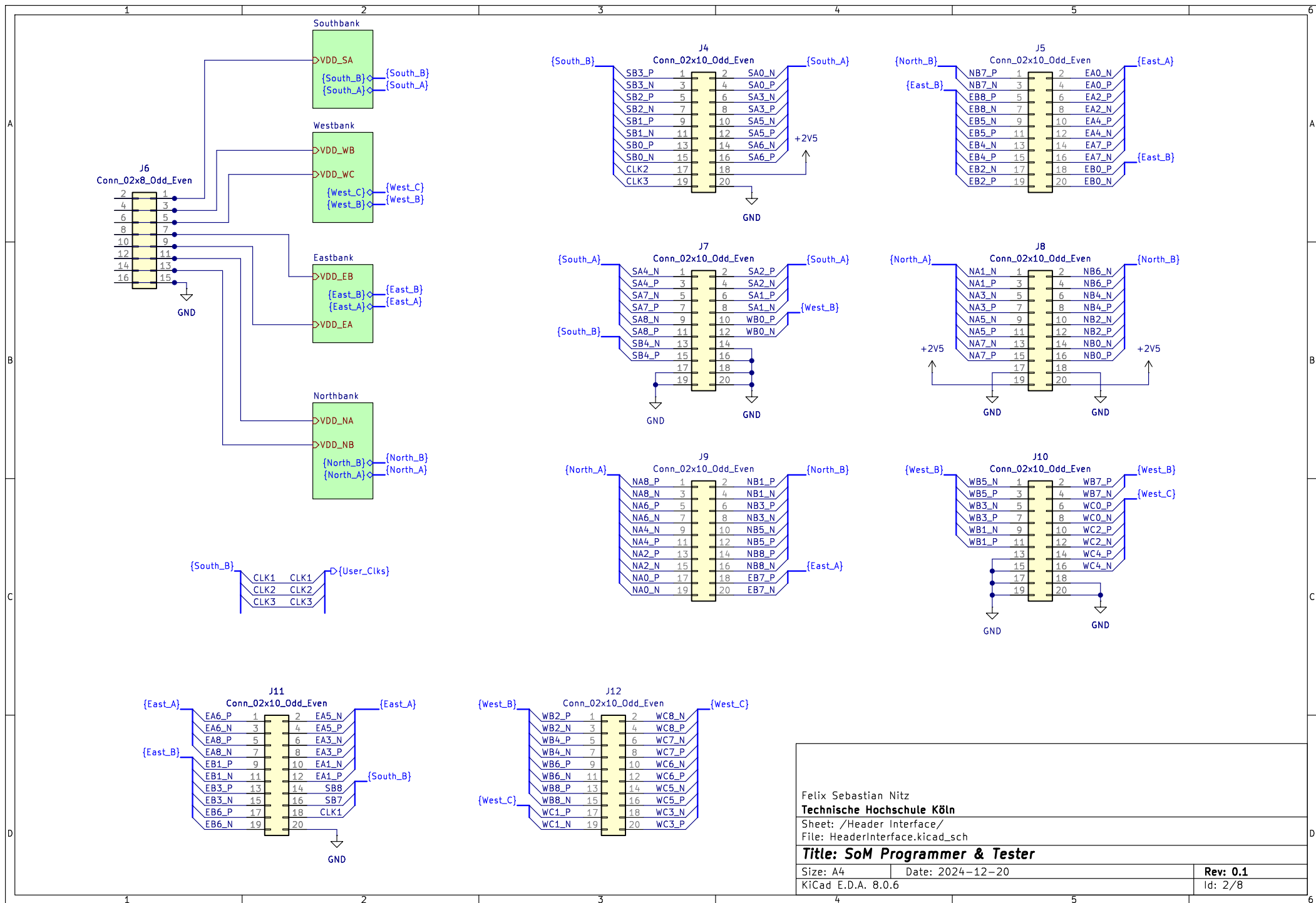
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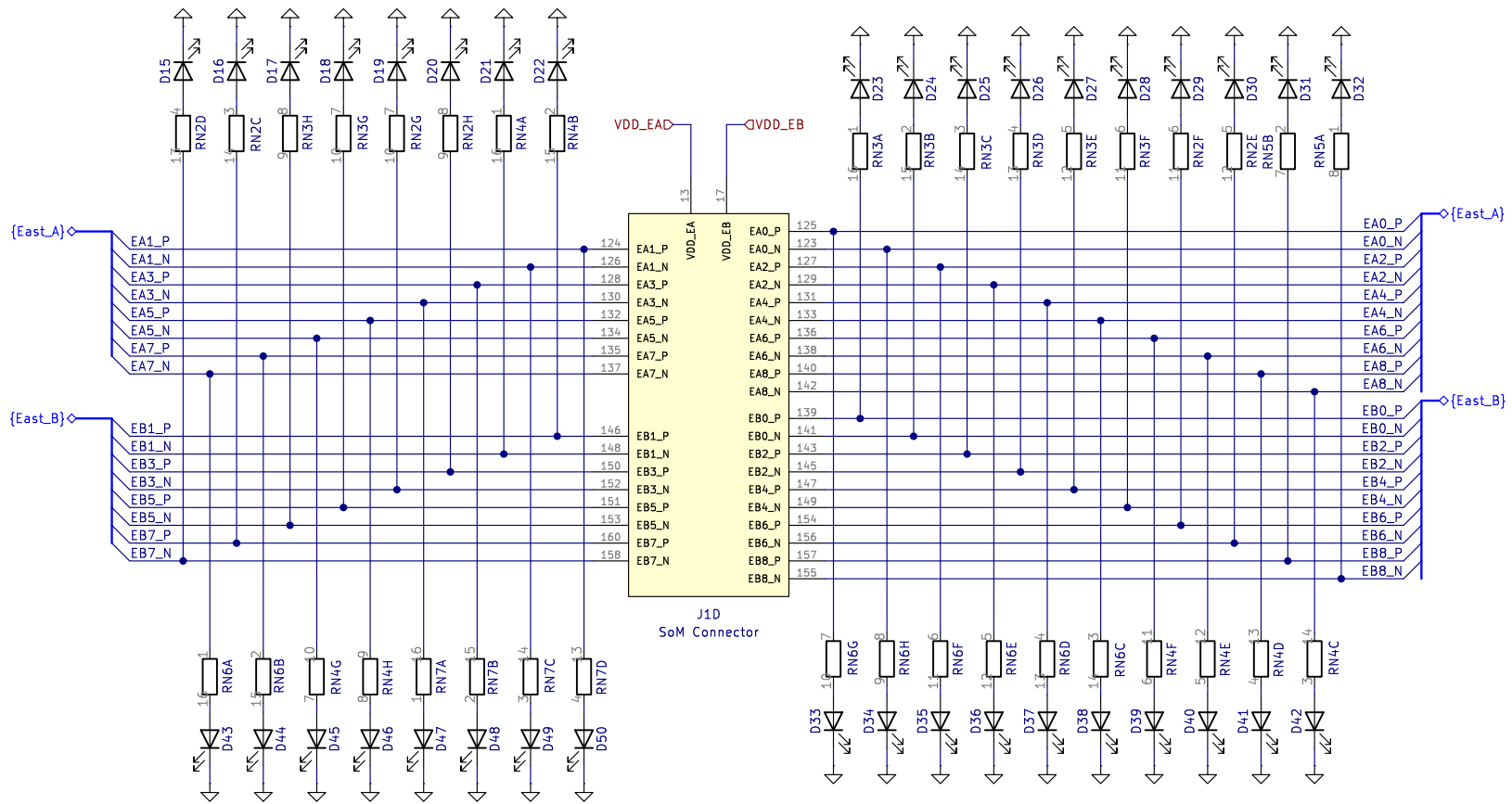
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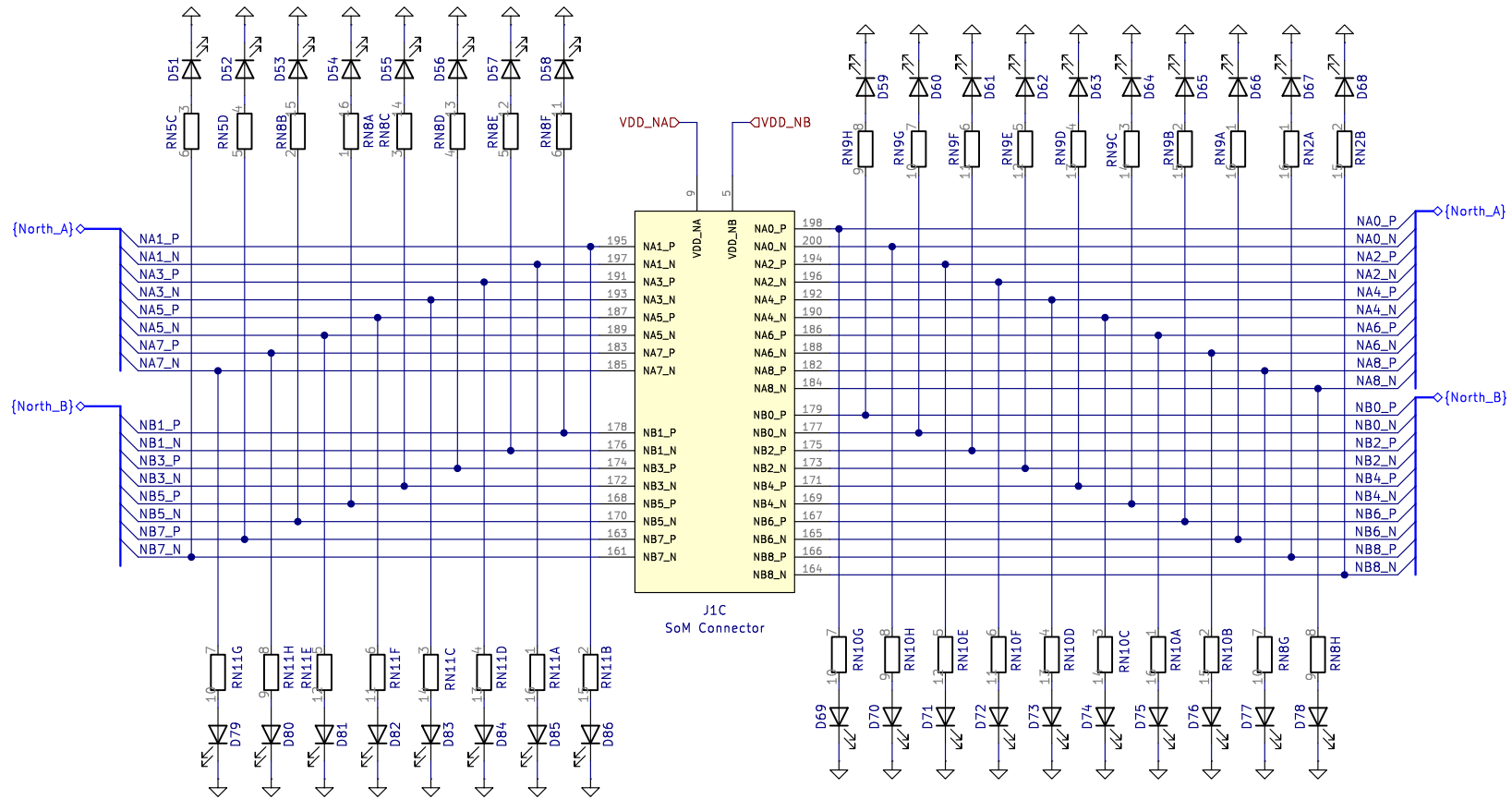
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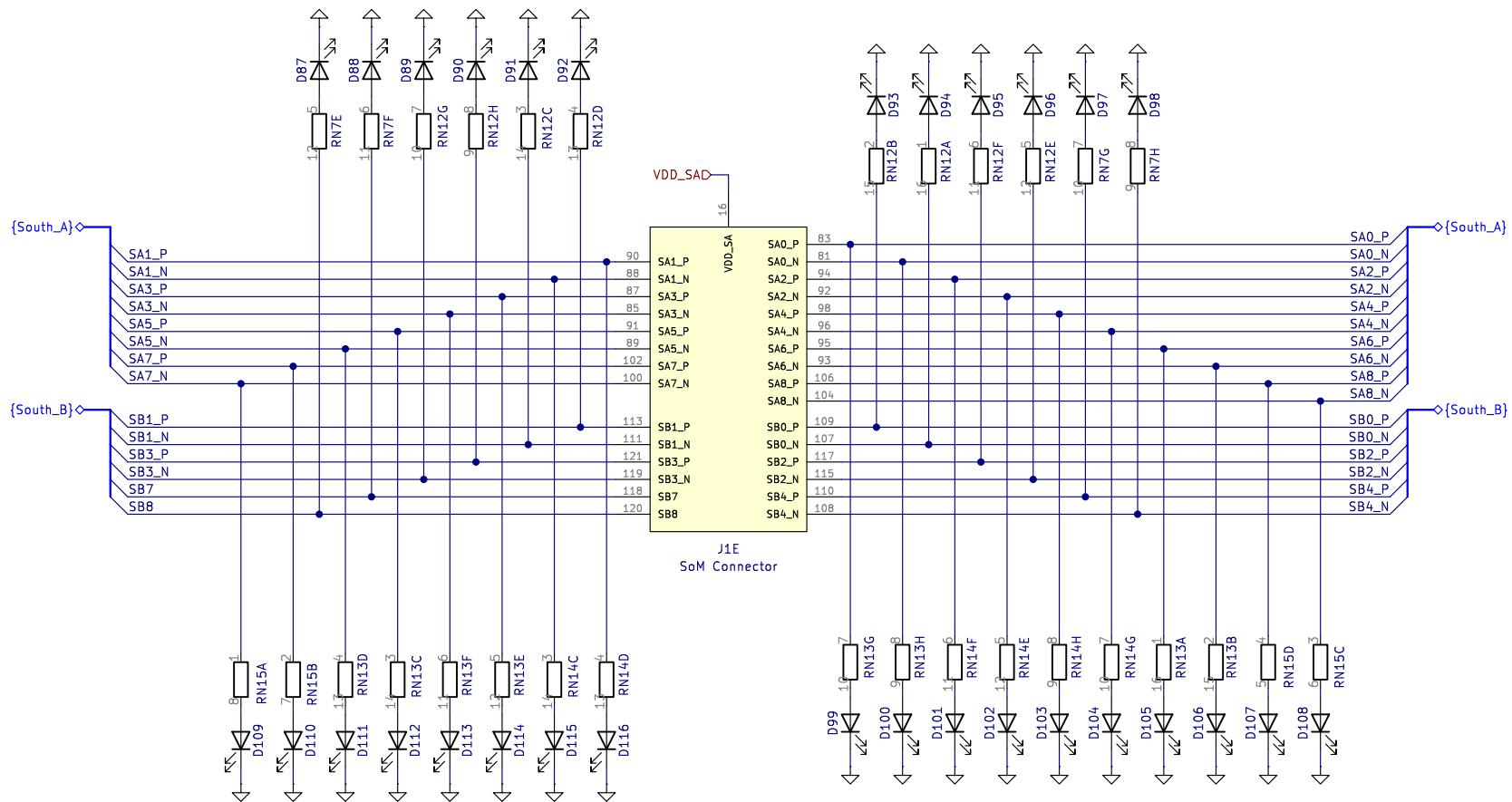




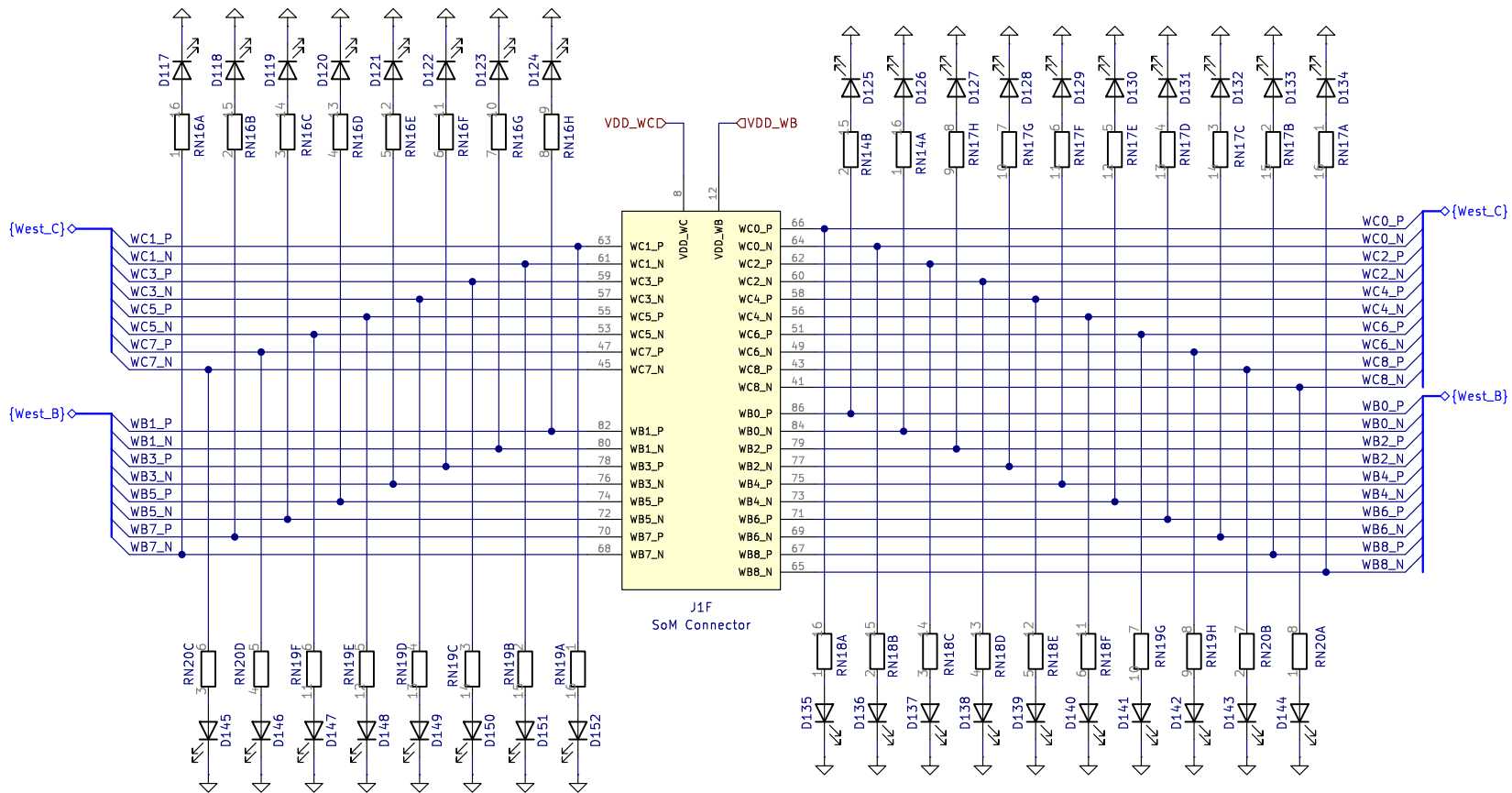
Resistor network values if not specified = 200R
Color if not specified = green



Resistor network values if not specified = 200R
Color if not specified = green

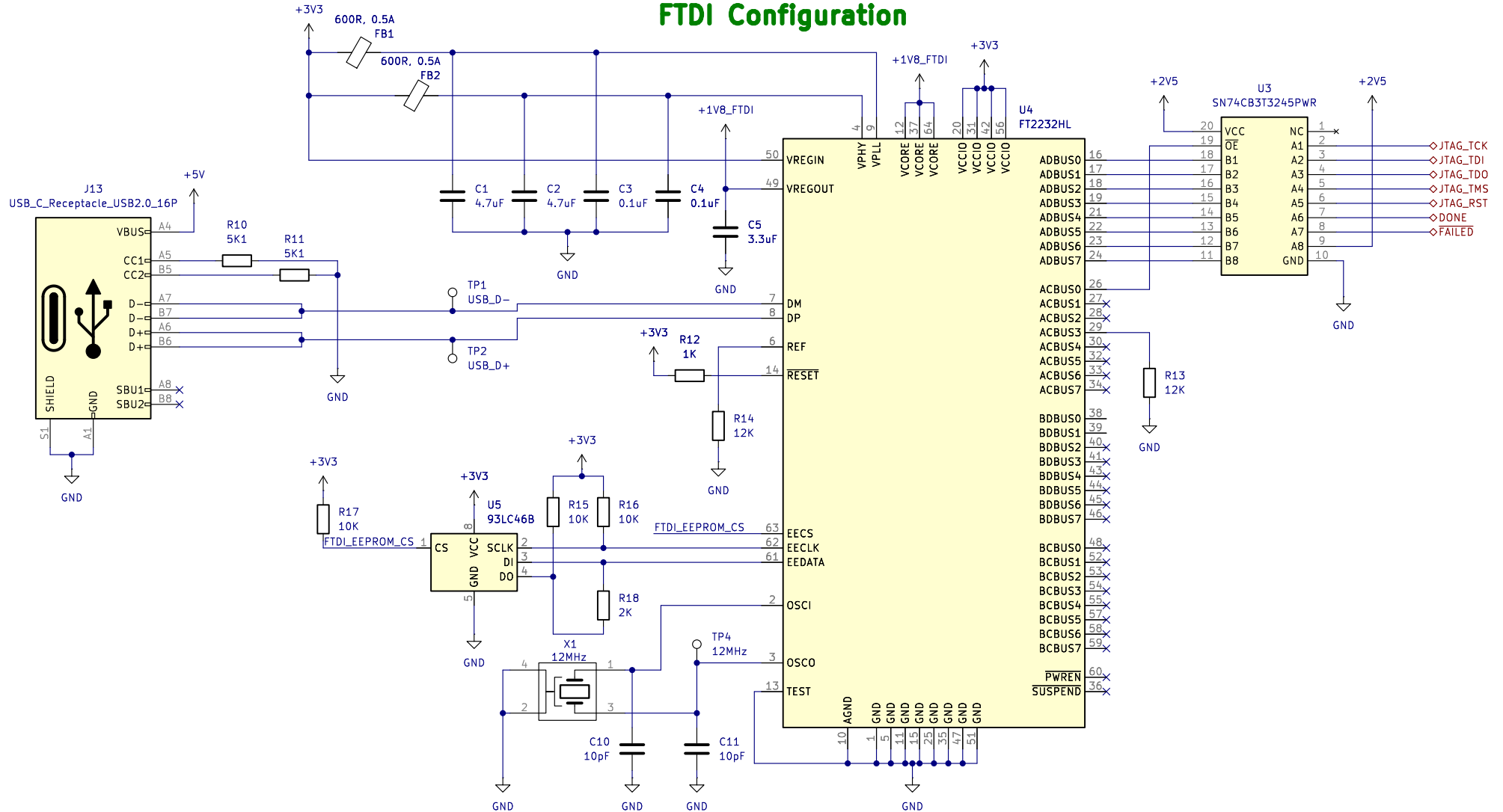


Resistor network values if not specified = 200R
Color if not specified = green

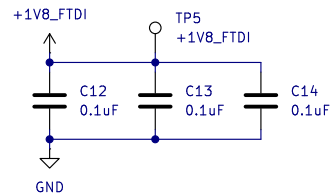
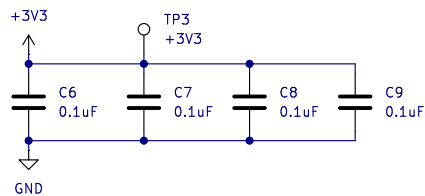


Resistor network values if not specified = 200R
Color if not specified = green

FTDI Configuration



Fitering



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Technische Hochschule KÖln

Sheet: /FTDI/
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Title: SoM Programmer & Tester

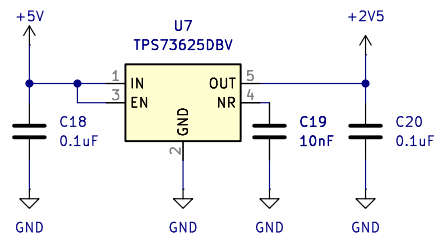
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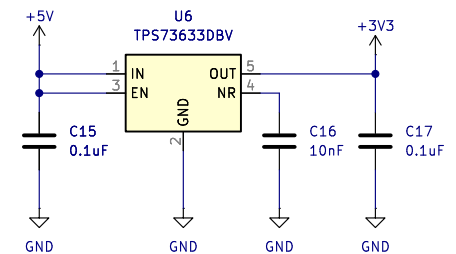
Rev: 0.1

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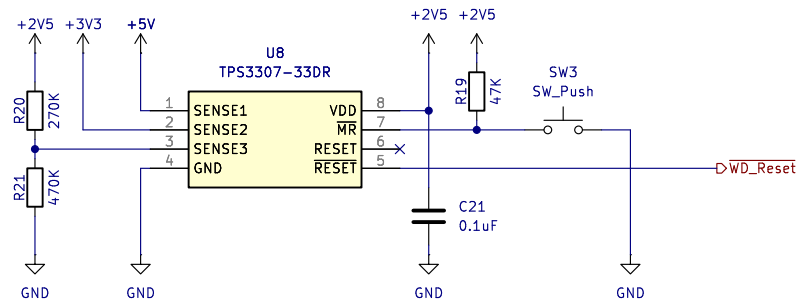
2.5V Regulator



3.3V Regulator



Supervisory Circuit with manual reset



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