MARK 5 MEMO #034.1

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To: List

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Subject: Mark 5A Output FPGA Parameters

The table below shows the control bits for the Mark 5A I/O board's output FPGA. The interface consists of eight registers of sixteen bits each. Only those bits within boxes in the table below are functional.

ADDR	TYPE	BITS 15 — 12	11 — 8	7 — 4	3 — 0
0	Read / Write		Ch B Select	Ch A Select	
1	Read / Write	F I A+ A_{P1} A_{P2} V SF			CODE
2	Read / Write				C Q
3	Read Only				S
4	Read Only	Number of Sync's			
5	Read Only			DIM Rev #	
6	Read / Write	Fill Detection Pattern (MSB's)			
7	Read / Write	Fill Detection Pattern (LSB's)			

Table 1
Output FPGA Control

The single letter symbols in the table are defined as follows:

        F => Enable Fill Detection
        I => Internal (Clock generator to be used)
        A+ => 5A+ version of DOM expects input files to be Mark 5B format

AP1 => track mapping option 1
AP2 => track mapping option 2 (AP1 =1 and AP2 =1 is not allowed.)
V => VLBA Mode (Must be set to "1" if A+ is "1".)
SF => Suspend Flag
C => Clear (Initialize)
Q => Seek Sync
S => Sync Found

The four "CODE" bits are defined as follows:

0100 Straight through Mark 5P Compatibility mode

0000 32 Track mode

0001 64 Track mode (multiplexed 64:32)

0010 16 Track mode (de-multiplexed 16:32)

0011 8 Track mode (de-multiplexed 8:32)

1xxx Test Vector receiver mode (not implemented as of this date)

All unspecified codes are reserved.

The normal sequence for configuring the output FPGA is as follows:

Set Q to "0".
Set F, I, A+, AP1, AP2, V, and CODE to the desired values.
Set C to "1".
Set C to "0".
Set Q to "1".

This will start the process whereby the output FPGA will attempt to find sync in the specified mode. The mode will be either bypass or playback depending on the FPDP signal DIR* which is controlled by the CONDUANT "StreamStore board. (DIR* = "0" implies that the operation is playback.) It is assumed that the "StreamStore board will present a stable value for DIR* before Q is set to "1".

The output FPGA has no view of the clock frequency except that it uses the clock for many internal operations. It is necessary that the clock be stable and well defined before the output FPGA parameters are set. If the clock frequency is changed, the parameter set up should be repeated after the new clock rate has become stable.

A successful discovery of sync will be indicated by the value of S becoming "1".

During operation, the six bit values "CH A Select" and "CH B Select" may be changed at any time. These values determine which of the 64 output streams are sent to the two channels of the Mark 4 decoder. These streams are selected without regard for the timing on the channels, so it is possible that the decoder will report a short error transient when the change is made.

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