## Description

The µPD8085A-2, µPD8085AH, and µPD8085AH-2 8-bit, single-chip microprocessors are 100 percent software compatible with the industry standard 8080A. They have the ability of increasing system performance of the 8080A by operating at a higher speed. Using the µPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count. The H (HMOS) versions have lower power consumptions than the non-H versions.

## Features

☐ Single power supply, +5 V, ±10%
☐ Internal clock generation and system control
☐ Internal serial in/out port
☐ Fully TTL-compatible
☐ Internal four-level interrupt structure
☐ Multiplexed address/data bus for increased system performance
☐ Complete family of components for design flexibility
☐ Software compatible with industry standard 8080A
☐ Higher throughput
  — µPD8085A-2 — 5 MHz
  — µPD8085AH — 3 MHz
  — µPD8085AH-2 — 5 MHz

## Ordering Information

| Part Number | Package Type | Max Frequency of Operation |
|---|---|---|
| µPD8085AC-2 | 40-pin plastic DIP | 5 MHz |
| µPD8085AHC | 40-pin plastic DIP | 3 MHz |
| µPD8085AHC-2 | 40-pin plastic DIP | 5 MHz |

## Pin Configuration
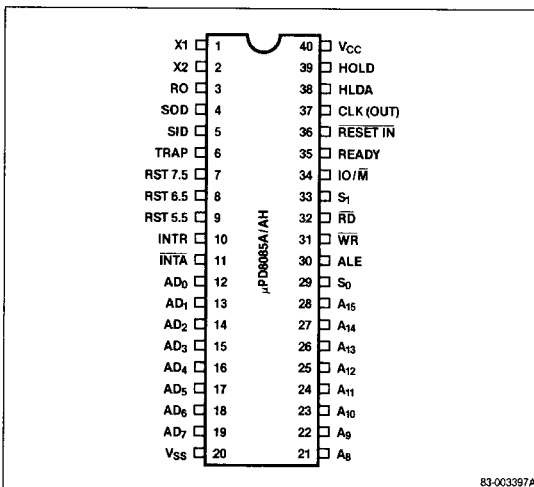


## Pin Identification

| No. | Symbol | Function |
|---|---|---|
| 1, 2 | X1, X2 | Crystal in |
| 3 | RO | Reset out |
| 4 | SOD | Serial out data |
| 5 | SID | Serial in data |
| 6 | TRAP | Trap interrupt input |
| 7 | RST 7.5 | Restart interrupts |
| 8 | RST 6.5 | Restart interrupts |
| 9 | RST 5.5 | Restart interrupts |
| 10 | INTR | Interrupt request in |
| 11 | $\overline{INTA}$ | Interrupt acknowledge |
| 12–19 | $AD_0$–$AD_7$ | Low address / data bus |
| 20 | $V_{SS}$ | Ground |
| 21–28 | $A_8$–$A_{15}$ | High address bus |
| 29, 33 | $S_0$, $S_1$ | Status outputs |
| 30 | ALE | Address latch enable out |
| 31, 32 | $\overline{WR}$, $\overline{RD}$ | Write / read strobes out |
| 34 | $IO/\overline{M}$ | I/O or memory indicator |
| 35 | READY | Ready input |
| 36 | $\overline{RESET\ IN}$ | Reset input |
| 37 | CLK | Clock out |
| 38, 39 | HLDA, HOLD | Hold acknowledge out and hold input request |
| 40 | $V_{CC}$ | +5 V supply |

## Pin Functions

### Crystal In

Crystal, RC, or external clock input.

### Reset Out

Acknowledges that the processor is being reset to be used as a system reset.

### Serial Out Data

1-bit data out by the SIM instruction.

### Serial In Data

1-bit data into ACC bit 7 by the RIM instruction.

### Trap Interrupt Input

Highest priority nonmaskable restart interrupt.

### Restart Interrupts

Priority restart interrupt inputs, of which 7.5 is the highest and 5.5 the lowest priority.

### Interrupt Request In

A general interrupt input which stops the PC from incrementing, generates $\overline{INTA}$, and samples the data bus for a restart or call instruction.

### Interrupt Acknowledge

An output which indicates that the processor has responded to INTR.

### Low Address / Data Bus

Multiplexed low address and data bus.

### Ground

Ground Reference.

### High Address Bus

Nonmultiplexed high 8 bits of the address bus.

### Status Outputs

Outputs which indicate data bus status: Halt, Write, Read, Fetch.

### Address Latch Enable Out

A signal which indicates that the lower 8 bits of address are valid on the AD lines.

### Write / Read Strobes Out

Signals out which are used as write and read strobes for memory and I/O devices.

### I/O or Memory Indicator

A signal out which indicates whether $\overline{RD}$ or $\overline{WR}$ strobes are for I/O or memory devices.

### Ready Input

An input which is used to increase the data and address bus access times (can be used for slow memory).

### Reset Input

An input which is used to start the processor activity at address 0, resetting IE and HLDA flip-flops.

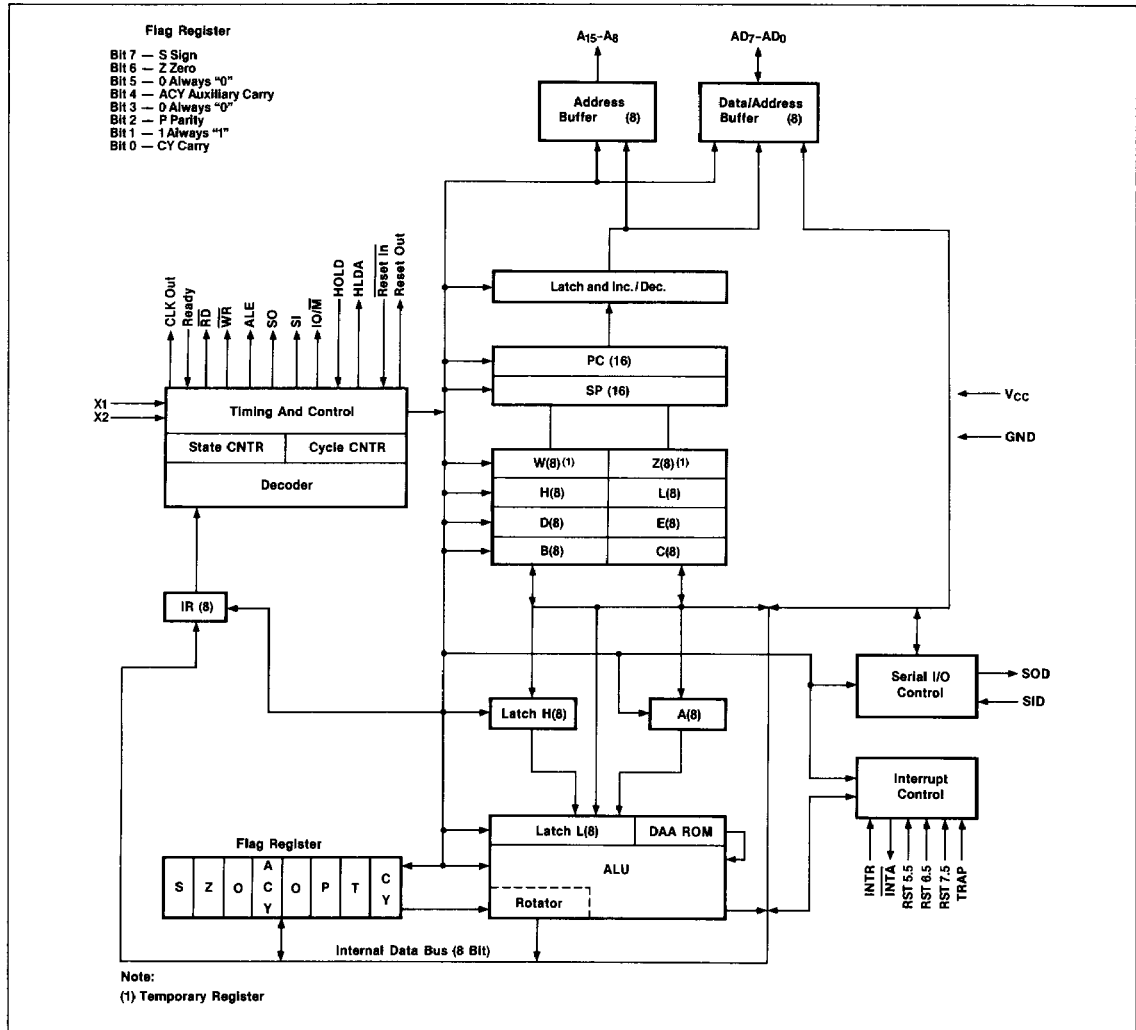### Clock Out

System clock output.

### Hold Acknowledge Out and Hold Input Request

Used to request and indicate that the processor should relinquish the bus for DMA activity. When hold is acknowledged, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, address and data buses are all three-stated.

### +5 V Supply

Power supply input.

## Block Diagram



Flag Register

Bit 7 — S Sign
Bit 6 — Z Zero
Bit 5 — 0 Always "0"
Bit 4 — ACY Auxiliary Carry
Bit 3 — 0 Always "0"
Bit 2 — P Parity
Bit 1 — 1 Always "1"
Bit 0 — CY Carry

Note:
(1) Temporary Register

## Absolute Maximum Ratings

μPD8085A-2: $T_A = 25°C$; $V_{CC} = +5 V \pm 5\%$

| | |
|---|---|
| Power supply voltage, $V_{DD}$ | $-0.5$ V to $+7$ V |
| Input voltage, $V_I$ | $-0.5$ V to $+7$ V |
| Output voltage, $V_O$ | $-0.5$ V to $+7$ V |
| Operating temperature, $T_{OPT}$ | 0°C to $+70$°C |
| Storage temperature, $T_{STG}$ | $-65$°C to $+150$°C |
| Power dissipation, $P_D$ | 1.5 W |

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

μPD8085AH, μPD8085AH-2: $T_A = 0°C$ to $+70$°C, $V_{CC} = +5 V \pm 10\%$, $V_{SS} = GND$

μPD8085A-2: $T_A = 0°C$ to $+70$°C, $V_{CC} = +5 V \pm 5\%$, $V_{SS} = GND$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input voltage low | $V_{IL}$ | $V_{SS} - 0.5$ | | $V_{SS} + 0.8$ | V | |
| Input voltage high | $V_{IH}$ | 2.0 | | $V_{CC} + 0.5$ | V | |
| Output voltage low | $V_{OL}$ | | | $+0.45$ | V | $I_{OL} = 2.0$ mA, $I_{OH} = -400 \mu A$, (Notes 1 & 2) |
| Output voltage high | $V_{OH}$ | 2.4 | | | V | $I_{OH} = -400 \mu A$, $I_{OL} = 2$ mA, (Notes 1 & 2) |
| Input leakage current | $I_{LI}$ | | | $\pm 10(1)$ | $\mu A$ | $0 V \leqslant V_{IN} \leqslant V_{CC}$ |
| Output leakage current | $I_{LO}$ | | | $\pm 10(1)$ | $\mu A$ | $0.45 V \leqslant V_{OUT} \leqslant V_{CC}$ |
| Input level low, reset | $V_{ILR}$ | $-0.5$ | | $+0.8$ | V | |
| Input level high, reset | $V_{IHR}$ | 2.4 | | $V_{CC} + 0.5$ | V | |
| Hysteresis, reset | $V_{HY}$ | 0.25 | | | V | |
| X1, X2 input voltage high | $V_{IHX}$ | 4.0 | | $V_{CC} + 0.5$ | V | |
| Power supply current ($V_{CC}$) μPD8085A-2 | $I_{CC}(AV)$ | | | 170 | mA | $t_{CY}$ min |
| μPD8085AH, μPD8085AH-2 | | | | 135 | mA | $t_{CY}$ min, (Note 3) |

**Note:**

(1) Minus ( $-$ ) designates current flow out of the device.

(2) On all outputs.

(3) Maximum unit test.

## AC Characteristics

µPD8085A-2: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 5\%$
µPD8085AH, µPD8085AH-2: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

| Parameter | Symbol | Limits | | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | µPD8085AH | | µPD8085AH-2, µPD8085A-2 | | | |
| | | Min | Max | Min | Max | | |
| CLK cycle period | $t_{CYC}$ | 320 | 2000 | 200 | 2000 | ns | |
| CLK low time | $t_1$ | 80 | | 40 | | ns | |
| CLK high time | $t_2$ | 120 | | 70 | | ns | |
| CLK rise time | $t_r$ | | 30 | | 30 | ns | |
| CLK fall time | $t_f$ | | 30 | | 30 | ns | |
| X1 rising to CLK rising | $t_{XKR}$ | 30 | 120 | 30 | 100 | ns | |
| X1 rising to CLK falling | $t_{XKF}$ | 30 | 150 | 30 | 110 | ns | |
| $A_8$–$A_{15}$ valid to leading edge of CONTROL | $t_{AC}$ | 270 | | 115 | | ns | (Note 1) |
| $A_0$–$A_7$ valid to leading edge of CONTROL | $t_{ACL}$ | 240 | | 115 | | ns | |
| $A_0$–$A_{15}$ valid to data input | $t_{AD}$ | | 575 | | 350 | ns | |
| Address float after leading edge of $\overline{RD}$ ($\overline{INTA}$) | $t_{AFR}$ | | 0 | | 0 | ns | |
| $A_8$–$A_{15}$ valid before trailing edge of ALE | $t_{AL}$ | 115 | | 50 | | ns | (Note 1) |
| $A_0$–$A_7$ valid before trailing edge of ALE | $t_{ALL}$ | 90 | | 50 | | ns | |
| READY valid from address valid | $t_{ARY}$ | | 220 | | 100 | ns | |
| $A_8$–$A_{15}$ valid after CONTROL | $t_{CA}$ | 120 | | 60 | | ns | |
| Width of control low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) | $t_{CC}$ | 400 | | 230 | | ns | |
| Trailing edge of CONTROL to leading edge of ALE | $t_{CL}$ | 50 | | 25 | | ns | |
| Data valid to trailing edge of $\overline{WR}$ | $t_{DW}$ | 420 | | 230 | | ns | |
| HLDA to bus enable | $t_{HABE}$ | | 210 | | 150 | ns | |
| Bus float after HLDA | $t_{HABF}$ | | 210 | | 150 | ns | |
| HLDA valid to trailing edge of CLK | $t_{HACK}$ | 110 | | 40 | | ns | |
| HOLD hold time | $t_{HDH}$ | 0 | | 0 | | ns | |
| HOLD setup time to trailing edge of CLK | $t_{HDS}$ | 170 | | 120 | | ns | |
| INTR hold time | $t_{INH}$ | 0 | | 0 | | ns | |
| INTR, RST, TRAP setup time to trailing edge of CLK | $t_{INS}$ | 160 | | 150 | | ns | |
| Address hold time after ALE | $t_{LA}$ | 100 | | 50 | | ns | |
| Trailing edge of ALE to leading edge of CONTROL | $t_{LC}$ | 130 | | 60 | | ns | |
| ALE low time during CLK high | $t_{LCK}$ | 100 | | 50 | | ns | |
| ALE to valid data input during read | $t_{LDR}$ | | 460 | | 270 | ns | |
| ALE to valid data during write | $t_{LDW}$ | | 200 | | 120 | ns | |
| ALE pulse width | $t_{LL}$ | 140 | | 80 | | ns | |
| ALE to READY stable | $t_{LRY}$ | | 110 | | 30 | ns | |

**4**

## AC Characteristics (cont)

μPD8085A-2: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$
μPD8085AH, μPD8085AH-2: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

| Parameter | Symbol | Limits | | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | μPD8085AH | | μPD8085AH-2, μPD8085A-2 | | | |
| | | Min | Max | Min | Max | | |
| Trailing edge of $\overline{RD}$ to re-enabling of address | $t_{RAE}$ | 150 | | 90 | | ns | |
| $\overline{RD}$ (or $\overline{INTA}$) to valid data | $t_{RD}$ | | 300 | | 150 | ns | |
| Trailing edge of CONTROL to leading edge of next CONTROL | $t_{RV}$ | 400 | | 220 | | ns | |
| Data hold time after $\overline{RD}$ ($\overline{INTA}$) | $t_{RDH}$ | 0 | | 0 | | ns | (Note 7) |
| READY hold time | $t_{RYH}$ | 0 | | 0 | | ns | |
| READY setup time to leading edge of CLK | $t_{RYS}$ | 110 | | 100 | | ns | |
| Leading edge data valid after trailing edge of $\overline{WR}$ | $t_{WD}$ | 100 | | 60 | | ns | |
| Leading edge of $\overline{WR}$ to data valid | $t_{WDL}$ | | 40 | | 20 | ns | |

**Note:**

(1) $A_8$–$A_{15}$ address specs apply to IO/$\overline{M}$. $S_0$ and $S_1$ except $A_8$–$A_{15}$ are undefined during $T_4$–$T_6$ of OF cycle whereas IO/$\overline{M}$, $S_0$ and $S_1$ are stable.

(2) Test conditions: $t_{CYC} = 320$ ns (8085AH)/200 ns (8085A-2) $C_L = 150$ pF

(3) For all output timing except where $C_L = 150$ pF use the following correction factors:
25 pF, $C_L = 150$ pF: $-0.10$ ns/pF
150 pF, $C_L = 300$ pF: $+0.3$ ns/pF

(4) Output timings are measured with purely capacitive load.

(5) All timings are measured as the following:
Output voltage: $V_L = 0.8$ V, $V_H = 2.0$ V
Input voltage: 1.5 V; $t_r$, $t_f = 20$ ns

(6) To calculate timing specifications at other values of $t_{CYC}$ use Bus Timing Specifications.

(7) Data hold time is guaranteed under all loading conditions.

## Bus Timing Specifications

### $t_{CYC}$ as a Dependent

| Symbol | Timing Formula | | Min/Max |
|---|---|---|---|
| | μPD8085AH | μPD8085A-2, μPD8085AH-2 | |
| $t_{AL}$ | $(1/2) t_{CY} - 45$ | $(1/2) t_{CY} - 50$ | Min |
| $t_{LA}$ | $(1/2) t_{CY} - 60$ | $(1/2) t_{CY} - 50$ | Min |
| $t_{LL}$ | $(1/2) t_{CY} - 20$ | $(1/2) t_{CY} - 20$ | Min |
| $t_{LCK}$ | $(1/2) t_{CY} - 60$ | $(1/2) t_{CY} - 50$ | Min |
| $t_{LC}$ | $(1/2) t_{CY} - 30$ | $(1/2) t_{CY} - 40$ | Min |
| $t_{AD}$ | $(5/2+N) t_{CY} - 225$ | $(5/2+N) t_{CY} - 150$ | Max |
| $t_{RD}$ | $(3/2+N) t_{CY} - 180$ | $(3/2+N) t_{CY} - 150$ | Max |
| $t_{RAE}$ | $(1/2) t_{CY} - 10$ | $(1/2) t_{CY} - 10$ | Min |
| $t_{CA}$ | $(1/2) t_{CY} - 40$ | $(1/2) t_{CY} - 40$ | Min |
| $t_{DW}$ | $(3/2+N) t_{CY} - 60$ | $(3/2+N) t_{CY} - 70$ | Min |
| $t_{WD}$ | $(1/2) t_{CY} - 60$ | $(1/2) t_{CY} - 40$ | Min |

| Symbol | Timing Formula | | Min/Max |
|---|---|---|---|
| | μPD8085AH | μPD8085A-2, μPD8085AH-2 | |
| $t_{CC}$ | $(3/2+N) t_{CY} - 80$ | $(3/2+N) t_{CY} - 70$ | Min |
| $t_{CL}$ | $(1/2) t_{CY} - 110$ | $(1/2) t_{CY} - 75$ | Min |
| $t_{ARY}$ | $(3/2) t_{CY} - 260$ | $(3/2) t_{CY} - 200$ | Max |
| $t_{HACK}$ | $(1/2) t_{CY} - 50$ | $(1/2) t_{CY} - 60$ | Min |
| $t_{HABF}$ | $(1/2) t_{CY} + 50$ | $(1/2) t_{CY} - 50$ | Max |
| $t_{HABE}$ | $(1/2) t_{CY} + 50$ | $(1/2) t_{CY} - 50$ | Max |
| $t_{AC}$ | $(2/2) t_{CY} - 50$ | $(2/2) t_{CY} - 85$ | Min |
| $t_1$ | $(1/2) t_{CY} - 80$ | $(1/2) t_{CY} - 60$ | Min |
| $t_2$ | $(1/2) t_{CY} - 40$ | $(1/2) t_{CY} - 30$ | Min |
| $t_{RV}$ | $(3/2) t_{CY} - 80$ | $(3/2) t_{CY} - 80$ | Min |
| $t_{LDR}$ | $(4/2+N) t_{CY} - 180$ | $(4/2+N) t_{CY} - 130$ | Max |

**Note:**
(1) N = Number of WAIT state.

## Timing Waveforms
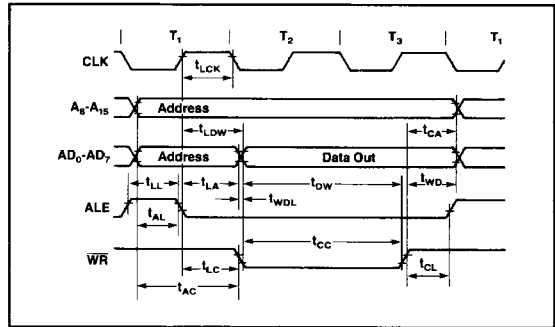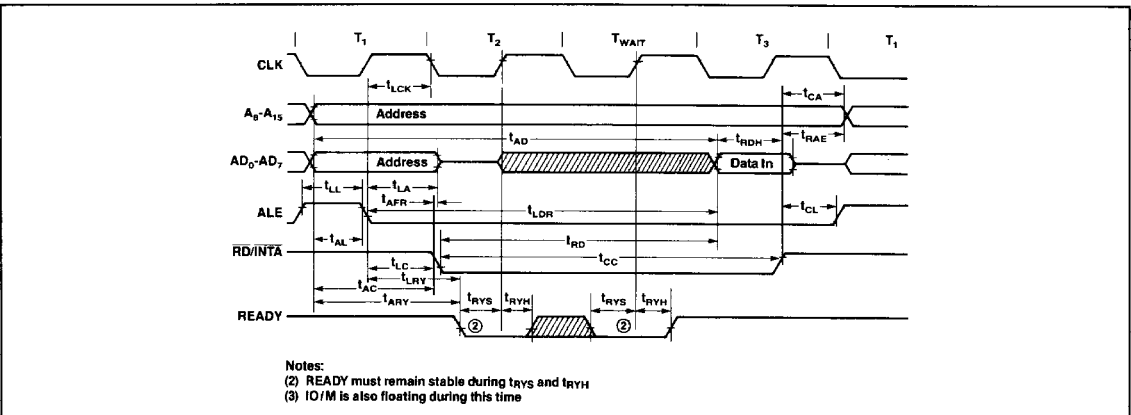
### Clock Timing Waveform
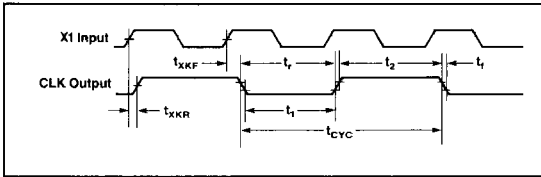


### Hold Timing
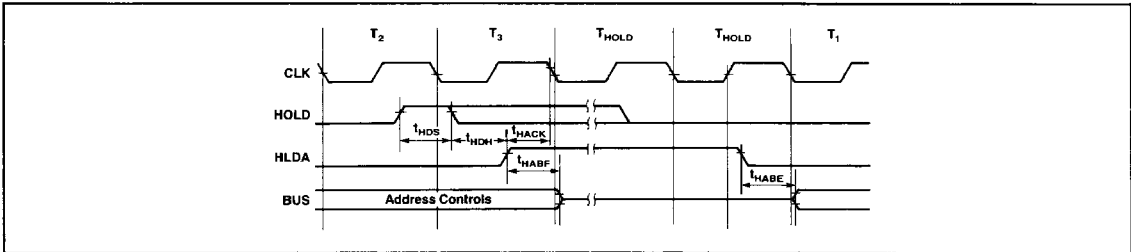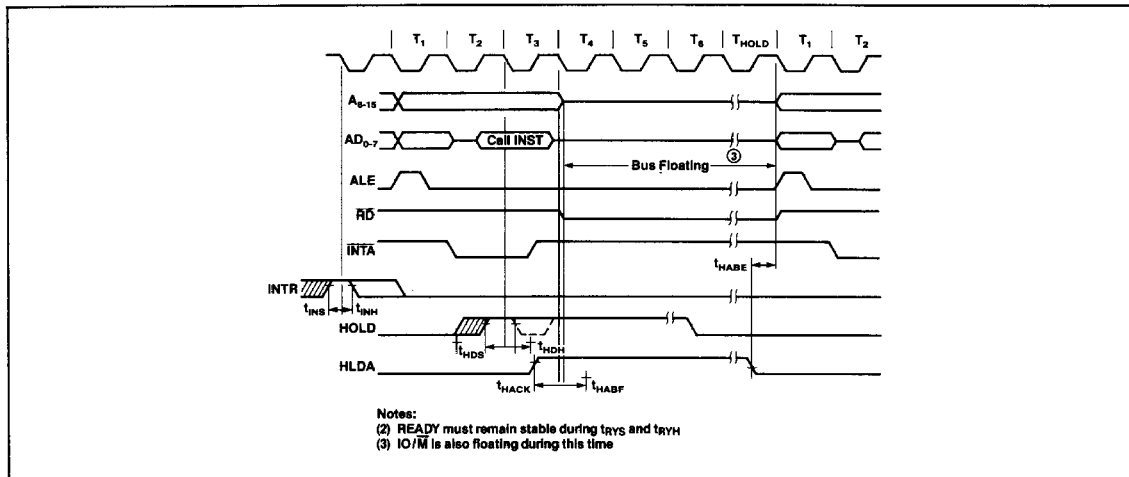


### 8085AH Bus Timing Read Operation
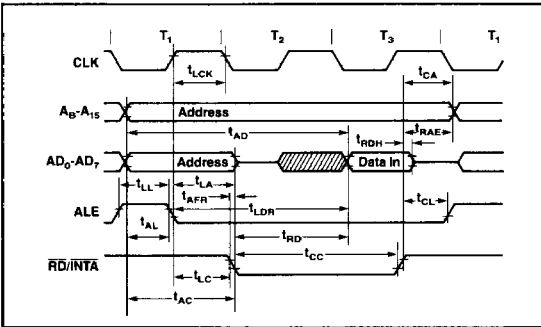


### Write Operation



### Read Operation with Wait Cycle (same Ready Timing Applies to Write Operation)



Notes:
(2) READY must remain stable during $t_{RYS}$ and $t_{RYH}$
(3) IO/M is also floating during this time

## Timing Waveforms (cont)

*Interrupt and Hold Timing*



Notes:
(2) READY must remain stable during tRYS and tRYH
(3) IO/M is also floating during this time

## Functional Description

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL-compatible.

The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the hold acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data buses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On-chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

**Processor State Transition Diagram**

T_RESET ← RESET

RESET

T₁   Halt

HALT

T₂   (READY + BI) (1)   T_WAIT   READY

READY + BI (1)

Hold = 1   Yes

No

Set HLDA FF

HOLD   T_HALT   HOLD / VALIDINT

VALIDINT

Set HLDA FF   Reset HALT FF

T₃   M₁   T₄   CK = 6 (2)   Hold = 1   Yes

Set HLDA FF

CK = 4 (2)   No   Set INTA FF Reset INTE FF

T₆   T₅

HLDA FF = Set   Yes

No

T_HOLD   Hold

Last Machine Cycle of Instruction   No

HOLD

Yes   Reset HLDA FF

VALIDINT = 1   No

Yes   HALT = 1   Yes

Set INTA FF Reset INTE FF   No
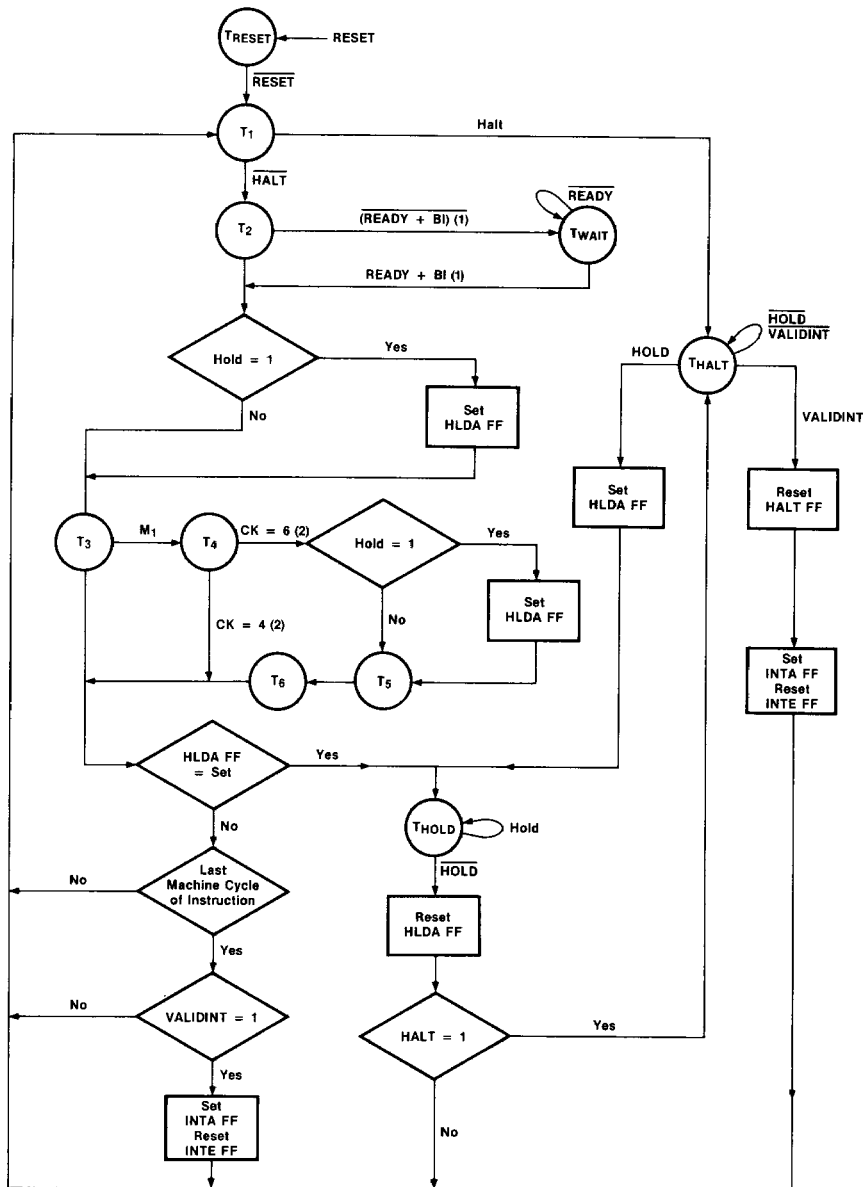
Notes:
1. BI indicates that the bus is idle during this machine cycle.
2. CK indicates the number of clock cycles in this machine cycle.

83-003840C

**4**

## Clock Inputs

As stated, the timing for the μPD8085A may be generated in one of two ways: crystal, or external clock. Recommendations for these methods are shown below. Note the input frequency must be twice the internal operating frequency.

## Status Outputs

The status outputs are valid during ALE time and have the following meaning:

|  | $S_1$ | $S_0$ |
|---|---|---|
| Halt | 0 | 0 |
| Write | 0 | 1 |
| Read | 1 | 0 |
| Fetch | 1 | 1 |

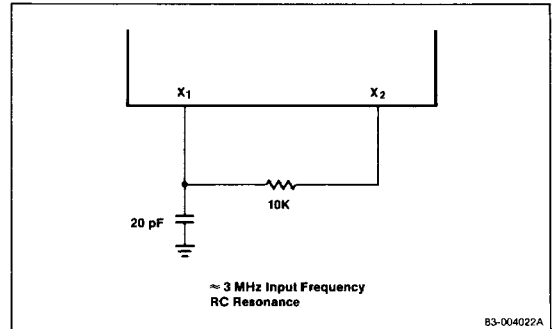These pins may be decoded to portray the processor's data bus status.

## Interrupts

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5, and 7.5, and TRAP, a non-maskable restart.

| Priority | Interrupt | Restart Address |
|---|---|---|
| Highest | TRAP | $24_{16}$ |
| | RST 7.5 | $3C_{16}$ |
| | RST 6.5 | $34_{16}$ |
| | RST 5.5 | $2C_{16}$ |
| Lowest | INTR | |

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising-edge. TRAP, the highest priority interrupt, is non-maskable and is set on the rising-edge or positive level. It must make a low-to-high transition and remain high to be seen, but it will not be generated again until it makes another low-to-high transition.

*RC*



≈ 3 MHz Input Frequency
RC Resonance

83-004022A

*Crystal*



1–6 MHz Input Frequency
Parallel Resonant Crystal

For 1–6 MHz Input Frequency,
$C_1 = C_2 = 10$ pF max.

For 6–10 MHz Input Frequency,
$C_1 = C_2 = 5$ pF max.

83-003832A

*External*



1–6 MHz 25–50% DC
$X_2$ not used

1–6 MHz > 50% DC

83-003834A
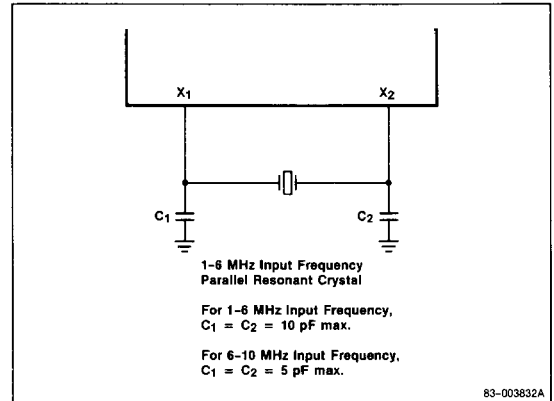
## Serial I/O

Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:
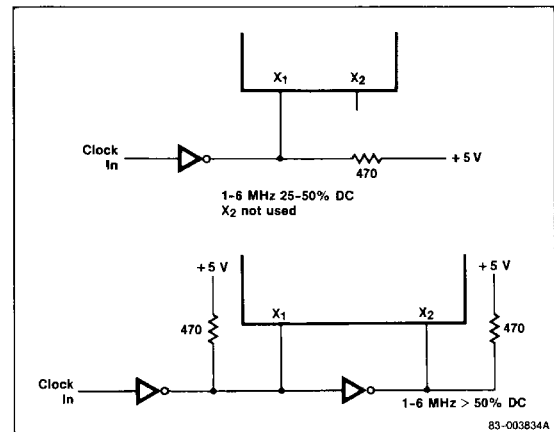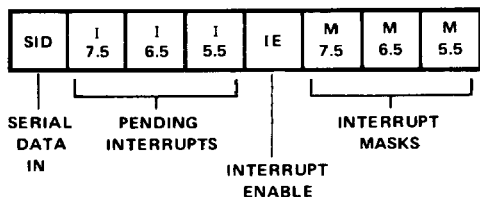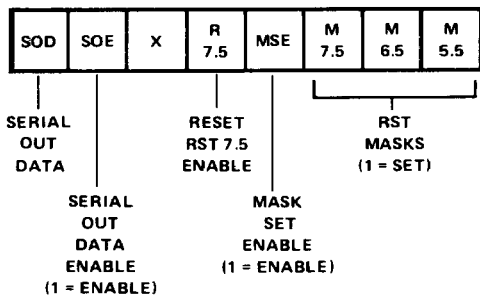
| SID | I 7.5 | I 6.5 | I 5.5 | IE | M 7.5 | M 6.5 | M 5.5 |
|-----|-------|-------|-------|-----|-------|-------|-------|

SERIAL DATA IN — PENDING INTERRUPTS — INTERRUPT ENABLE — INTERRUPT MASKS

**Note:**
(1) After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:

| SOD | SOE | X | R 7.5 | MSE | M 7.5 | M 6.5 | M 5.5 |
|-----|-----|---|-------|-----|-------|-------|-------|

SERIAL OUT DATA — SERIAL OUT DATA ENABLE (1 = ENABLE) — RESET RST 7.5 ENABLE — MASK SET ENABLE (1 = ENABLE) — RST MASKS (1 = SET)

## Instruction Set

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (sign, zero, parity and carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table)

The sign flag is set (high) if bit 7 of the result is a "1"; otherwise it is reset (low). The zero flag is set if the result is "0"; otherwise it is reset. The parity flag is set if the modulo 2 sum of the bits of the result is "0" (even parity); otherwise (odd parity) it is reset. The carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the µPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The auxiliary carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the µPD8085A. The ability to increment and decrement memory, the six general registers, and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the µPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

The special instruction group completes the µPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

## Data and Instruction Formats

Data in the µPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|-------|-------|-------|-------|-------|-------|-------|-------|

MSB — DATA WORD — LSB

4
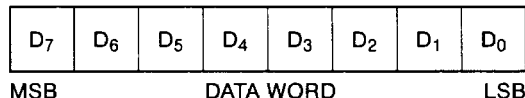
Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

One Byte Instructions
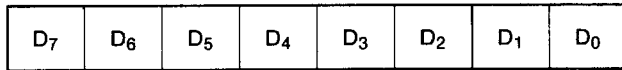
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | OP CODE |
|---|---|---|---|---|---|---|---|---|

**Typical Instructions**

Register to register, memory referance, arithmetic or logical, rotate, return, push, pop, enable, or diable interrupt instructions

Two Byte Instructions
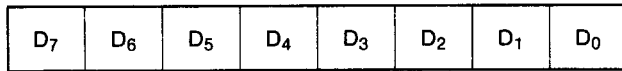
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | OP CODE |
|---|---|---|---|---|---|---|---|---|

Immediate mode or I/O instructions
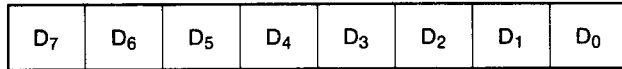
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | OPERAND |
|---|---|---|---|---|---|---|---|---|

Three Byte Instructions
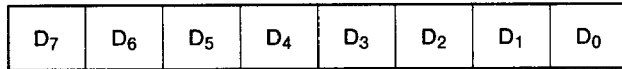
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | OP CODE |
|---|---|---|---|---|---|---|---|---|

Jump, call or direct load and store instructions
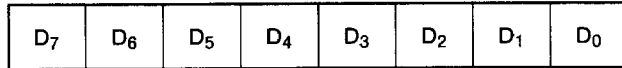
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | LOW ADDRESS OR OPERAND 1 |
|---|---|---|---|---|---|---|---|---|

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | HIGH ADDRESS OR OPERAND 2 |
|---|---|---|---|---|---|---|---|---|
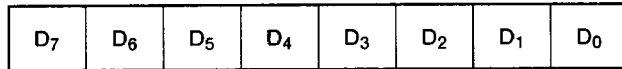
## Instruction Cycle Times

One to five machine cycles ($M_1$–$M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times (T1–T5).

Machine cycles and clock states used for each type of instruction are shown below.

| Instruction Type | Machine Cycles Executed Min/Max | Clock Status Min/Max |
|---|---|---|
| ALU R | 1 | 4 |
| CMC | 1 | 4 |
| CMA | 1 | 4 |
| DAA | 1 | 4 |
| DCR R | 1 | 4 |
| DI | 1 | 4 |
| EI | 1 | 4 |
| INR R | 1 | 4 |
| MOV R, R | 1 | 4 |
| NOP | 1 | 4 |
| ROTATE | 1 | 4 |
| RIM | 1 | 4 |
| SIM | 1 | 4 |
| STC | 1 | 4 |
| XCHG | 1 | 4 |
| HLT | 1 | 5 |
| DCX | 1 | 6 |
| INX | 1 | 6 |
| PCHL | 1 | 6 |

| Instruction Type | Machine Cycles Executed Min/Max | Clock Status Min/Max |
|---|---|---|
| RET COND. | 1/3 | 6/12 |
| SPHL | 1 | 6 |
| ALU I | 2 | 7 |
| ALU M | 2 | 7 |
| JNC | 2/3 | 7/10 |
| LDAX | 2 | 7 |
| MVI | 2 | 7 |
| MOV M, R | 2 | 7 |
| MOV R, M | 2 | 7 |
| STAX | 2 | 7 |
| CALL COND. | 2/5 | 9/18 |
| DAD | 3 | 10 |
| DCR M | 3 | 10 |
| IN | 3 | 10 |
| INR M | 3 | 10 |
| JMP | 3 | 10 |
| LOAD PAIR | 3 | 10 |
| MVI M | 3 | 10 |
| OUT | 3 | 10 |
| POP | 3 | 10 |
| RET | 3 | 10 |
| PUSH | 3 | 12 |
| RST | 3 | 12 |
| LDA | 4 | 13 |
| STA | 4 | 13 |
| LHLD | 5 | 16 |
| SHLD | 5 | 16 |
| XTHL | 5 | 16 |
| CALL | 5 | 18 |

**4**

# Instruction Set

| Mnemonic(1) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Cycles(3) | Sign | Zero | Parity | Carry |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Move** | | | | | | | | | | | | | | |
| MOV d, s | Move register to register | 0 | 1 | d | d | d | s | s | s | 4 | | | | |
| MOV M, s | Move register to memory | 0 | 1 | 1 | 1 | 0 | s | s | s | 7 | | | | |
| MOV d, M | Move memory to register | 0 | 1 | d | d | d | 1 | 1 | 0 | 7 | | | | |
| MVI d, D8 | Move immediate to register | 0 | 0 | d | d | d | 1 | 1 | 0 | 7 | | | | |
| MVI M, D8 | Move immediate to memory | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 10 | | | | |
| **Increment / Decrement** | | | | | | | | | | | | | | |
| INR d | Increment register | 0 | 0 | d | d | d | 1 | 0 | 0 | 4 | • | • | • | |
| DCR d | Decrement register | 0 | 0 | d | d | d | 1 | 0 | 1 | 4 | • | • | • | |
| INR M | Increment memory | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 10 | • | • | • | |
| DCR M | Decrement memory | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 10 | • | • | • | |
| **ALU – Register to Accumulator** | | | | | | | | | | | | | | |
| ADD s | Add register to A | 1 | 0 | 0 | 0 | 0 | s | s | s | 4 | • | • | • | • |
| ADC s | Add register to A with carry | 1 | 0 | 0 | 0 | 1 | s | s | s | 4 | • | • | • | • |
| SUB s | Subtract register from A | 1 | 0 | 0 | 1 | 0 | s | s | s | 4 | • | • | • | • |
| SUBB s | Subtract register from A with borrow | 1 | 0 | 0 | 1 | 1 | s | s | s | 4 | • | • | • | • |
| ANA s | AND register with A | 1 | 0 | 1 | 0 | 0 | s | s | s | 4 | • | • | • | 0 |
| XRA s | Exclusive OR register with A | 1 | 0 | 1 | 0 | 1 | s | s | s | 4 | • | • | • | 0 |
| ORA s | OR register with A | 1 | 0 | 1 | 1 | 0 | s | s | s | 4 | • | • | • | 0 |
| CMP s | Compare register with A | 1 | 0 | 1 | 1 | 1 | s | s | s | 4 | • | • | • | • |
| **ALU – Memory to Accumulator** | | | | | | | | | | | | | | |
| ADD M | Add memory to A | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 7 | • | • | • | • |
| ADC M | Add memory to A with carry | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 7 | • | • | • | • |
| SUB M | Subtract memory from A | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 7 | • | • | • | • |
| SBB M | Subtract memory from A with borrow | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 7 | • | • | • | • |
| ANA M | AND memory with A | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 7 | • | • | • | 0 |
| XRA M | Exclusive OR memory with A | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 7 | • | • | • | 0 |
| ORA M | OR memory with A | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 7 | • | • | • | 0 |
| CMP M | Compare memory with A | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 7 | • | • | • | • |
| **ALU – Immediate to Accumulator** | | | | | | | | | | | | | | |
| ADI D8 | Add immediate to A | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 7 | • | • | • | • |
| ACI D8 | Add immediate to A with carry | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 7 | • | • | • | • |

## Instruction Set (cont)

| Mnemonic(1) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Cycles(3) | Sign | Zero | Parity | Carry |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **ALU – Immediate to Accumulator (cont)** | | | | | | | | | | | | | | |
| SUI D8 | Subtract immediate from A | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 7 | • | • | • | • |
| SBI D8 | Subtract immediate from A with borrow | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 7 | • | • | • | • |
| ANI D8 | AND immediate with A | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 7 | • | • | • | 0 |
| XRI D8 | Exclusive OR immediate with A | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 7 | • | • | • | 0 |
| ORI D8 | OR immediate with A | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 7 | • | • | • | 0 |
| CPI D8 | Compare immediate with A | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7 | • | • | • | • |
| **ALU – Rotate** | | | | | | | | | | | | | | |
| RLC | Rotate A left, MSB to carry (8-bit) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 4 | | | | • |
| RRC | Rotate A right, LSB to carry (8-bit) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 4 | | | | • |
| RAL | Rotate A left through carry (9-bit) | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 4 | | | | • |
| RAR | Rotate A right through carry (9-bit) | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 4 | | | | • |
| **Jump** | | | | | | | | | | | | | | |
| JMP ADDR | Jump unconditional | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 10 | | | | |
| JNZ ADDR | Jump on not zero | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 7/10 | | | | |
| JZ ADDR | Jump on zero | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 7/10 | | | | |
| JNC ADDR | Jump on no carry | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 7/10 | | | | |
| JC ADDR | Jump on carry | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 7/10 | | | | |
| JPO ADDR | Jump on parity odd | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 7/10 | | | | |
| JPE ADDR | Jump on parity even | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 7/10 | | | | |
| JP ADDR | Jump on positive | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 7/10 | | | | |
| JM ADDR | Jump on minus | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7/10 | | | | |
| **Call** | | | | | | | | | | | | | | |
| CALL ADDR | Call unconditional | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 18 | | | | |
| CNZ ADDR | Call on not zero | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 9/18 | | | | |
| CZ ADDR | Call on zero | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 9/18 | | | | |
| CNC ADDR | Call on no carry | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 9/18 | | | | |
| CC ADDR | Call on carry | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 9/18 | | | | |
| CPO ADDR | Call on parity odd | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 9/18 | | | | |
| CPE ADDR | Call on parity even | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 9/18 | | | | |
| CP ADDR | Call on positive | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 9/18 | | | | |
| CM ADDR | Call on minus | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 9/18 | | | | |

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# Instruction Set (cont)

| Mnemonic(1) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Cycles(3) | Sign | Zero | Parity | Carry |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Call (cont)** | | | | | | | | | | | | | | |
| **Return** | | | | | | | | | | | | | | |
| RET | Return | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 10 | | | | |
| RNZ | Return on not zero | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 6/12 | | | | |
| RZ | Return on zero | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 6/12 | | | | |
| RNC | Return on no carry | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 6/12 | | | | |
| RC | Return on carry | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 6/12 | | | | |
| RPO | Return on parity odd | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 6/12 | | | | |
| RPE | Return on parity even | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 6/12 | | | | |
| RP | Return on positive | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 6/12 | | | | |
| RM | Return on minus | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6/12 | | | | |
| **Load Register Pair** | | | | | | | | | | | | | | |
| LXI B, D16 | Load immediate register pair BC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10 | | | | |
| LXI D, D16 | Load immediate register pair DE | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 10 | | | | |
| LXI H, D16 | Load immediate register pair HL | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 10 | | | | |
| LXI SP, D16 | Load immediate stack pointer | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 10 | | | | |
| **Push** | | | | | | | | | | | | | | |
| PUSH B | Push register pair BC on stack | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 12 | | | | |
| PUSH D | Push register pair DE on stack | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 12 | | | | |
| PUSH H | Push register pair HL on stack | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 12 | | | | |
| PUSH PSW | Push A and flags on stack | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 12 | | | | |
| **Pop** | | | | | | | | | | | | | | |
| POP B | Pop register pair BC off stack | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 10 | | | | |
| POP D | Pop register pair DE off stack | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 10 | | | | |
| POP H | Pop register pair HL off stack | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 10 | | | | |
| POP PSW | Pop A and flags off stack | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 10 | ● | ● | ● | ● |
| **Double Add** | | | | | | | | | | | | | | |
| DAD R | Add BC to HL | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 10 | | | | ● |
| DAD D | Add DE to HL | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 10 | | | | ● |
| DAD H | Add HI to HL | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 10 | | | | ● |
| DAD SP | Add stack pointer to HL | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 10 | | | | ● |

## Instruction Set (cont)

| Mnemonic(1) | Description | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Cycles(3) | Sign | Zero | Parity | Carry |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Increment Register Pair** | | | | | | | | | | | | | | |
| INX B | Increment BC | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 6 | | | | |
| INX D | Increment DE | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 6 | | | | |
| INX H | Increment HL | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 6 | | | | |
| INX SP | Increment stack pointer | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 6 | | | | |
| **Decrement Register Pair** | | | | | | | | | | | | | | |
| DCX B | Decrement BC | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 6 | | | | |
| DCX D | Decrement DE | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 6 | | | | |
| DCX H | Decrement HL | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 6 | | | | |
| DCX SP | Decrement stack pointer | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 6 | | | | |
| **Register Indirect** | | | | | | | | | | | | | | |
| STAX B | Store A at ADDR in BC | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 7 | | | | |
| STAX D | Store A at ADDR in DE | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 7 | | | | |
| LDAX B | Load A at ADDR in BC | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7 | | | | |
| LDAX D | Load A at ADDR in DE | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 7 | | | | |
| **Direct** | | | | | | | | | | | | | | |
| STA ADDR | Store A direct | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 13 | | | | |
| LDA ADDR | Load A direct | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 13 | | | | |
| SHLD ADDR | Store HL direct | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 16 | | | | |
| LHLD ADDR | Load HL direct | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 16 | | | | |
| **Move Register Pair** | | | | | | | | | | | | | | |
| XCHG | Exchange DE and HL register pairs | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 4 | | | | |
| XTHL | Exchange top of stack and HL | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 16 | | | | |
| SPHL | HL to stack pointer | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 6 | | | | |
| PCHL | HL to program counter | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 6 | | | | |
| **Input / Output** | | | | | | | | | | | | | | |
| IN A | Input | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 10 | | | | |
| OUT A | Output | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 10 | | | | |
| EI | Enable interrupts | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 4 | | | | |
| DI | Disable interrupts | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 4 | | | | |
| RIM | Read interrupt mask | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 4 | | | | |
| SIM | Set interrupt mask | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 4 | | | | |
| RST A | Restart | 1 | 1 | A | A | A | 1 | 1 | 1 | 12 | | | | |

(Note: column group header **Operation Code(2)** spans D7–D0; **Flags(4)** spans Sign, Zero, Parity, Carry.)

**4**

## Instruction Set (cont)

| Mnemonic(1) | Description | Operation Code(2) | | | | | | | | Cycles(3) | Flags(4) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Sign | Zero | Parity | Carry |
| **Miscellaneous** | | | | | | | | | | | | | | |
| CMA | Complement A | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 4 | | | | |
| STC | Set carry | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 4 | | | | |
| CMC | Complement carry | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 4 | | | | 1/Cy |
| DAA | Decimal adjust A | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 4 | ● | ● | ● | ● |
| NOP | No operation | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | | | | |
| HLT | Halt | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 5 | | | | |

**Note:**

(1) Operand symbols used

   A = 8-bit address or expression

   s = source register

   d = destination register

   PSW = Processor status word

   SP = Stack pointer

   D8 = 8-bit data quantity, expression, or constant, always $B_2$ of instruction

   D16 = 16-bit data quantity, expression, or constant, always $B_3B_2$ of instruction

   ADDR = 16-bit memory address expression

(2) ddd or sss = 000-B, 001-C, 010-D, 011-E, 100-H, 101-L, 110-Memory, 111-A

(3) Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags.

(4) ● = flag affected

   = flag not affected

   0 = flag reset

   1 = flag set

## µPD8085A Family Minimum System Configuration

A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3 40-pin packs. This system is shown below with its address, data, control buses and I/O ports.

*Three Pack Computer System*



**4**