IM6402/IM6403
Universal Asynchronous Receiver Transmitter (UART)

INTERSIL

GENERAL DESCRIPTION

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 8.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

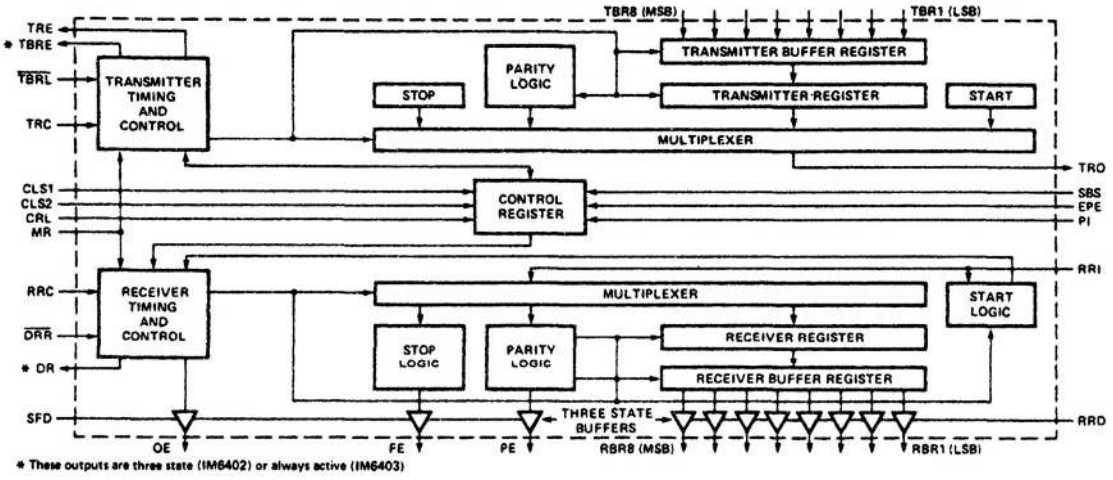
The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 4.

FEATURES

- **Low Power — Less Than 10mW Typ. at 2MHz**
- **Operation Up to 4MHz Clock (IM6402A)**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible With Industry Standard UART's (IM6402)**
- **On-Chip Oscillator With External Crystal (IM6403)**
- **Operating Voltage —**
  IM6402-1/03-1: 5V
  IM6402A/03A: 4–11V
  IM6402/03: 5V

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-IPL	IM6402/03AIPL	IM6402/03IPL
CERAMIC PKG	IM6402-1/03-1IJL	IM6402/03AIJL	IM6402/03IJL
MILITARY TEMP.	IM6402-1/03-1MJL	IM6402/03AMJL	—
MILITARY TEMP. WITH /Hi-Rel processing	IM6402-1/03-1MJL/HR	IM6402/03AMJL/HR	—



0374-1

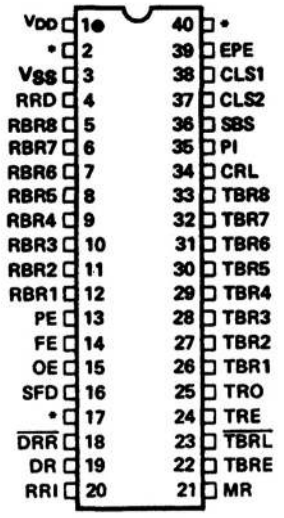
Figure 1: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (IM6402/03)

Operating Temperature
IM6402/03 (I) ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to 150°C
Supply Voltage ($V_{DD}-V_{SS}$) ..... +8.0V
Voltage On Any Input or Output Pin ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0374-2

*See Table 1

Figure 2: Pin Configuration

TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT TTL CLOCK	IM6402 w/EXT CMOS CLOCK
2	N/C	Divide Control	Divide Control	Divide Control
17	RRC	XTAL	External Clock Input	No Connection
19	Tri-State	Always Active	Always Active	Always Active
22	Tri-State	Always Active	Always Active	Always Active
40	TRC	XTAL	V_{SS}	External Clock Input

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0V \pm 10\%$ $V_{SS}=0V$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IH}	Input Voltage High		$V_{DD}-2.0$			V
V_{IL}	Input Voltage Low				0.8	V
I_{IL}	Input Leakage [1]	$V_{SS} \le V_{IN} \le V_{DD}$	−5.0		5.0	μA
V_{OH}	Output Voltage High	$I_{OH}=-0.2mA$	2.4			V
V_{OL}	Output Voltage Low	$I_{OL}=1.6mA$			0.45	V
I_{OLK}	Output Leakage	$V_{SS} \le V_{OUT} \le V_{DD}$	−5.0		5.0	μA
I_{STBY}	Power Supply Current Standby	$V_{IN}=V_{SS}$ or V_{DD}		1.0	800	μA
I_{DD}	Power Supply Current IM6402	$f_c=500kHz$			1.2	mA
I_{DD}	Power Supply Current IM6403	$f_{crystal}=2.46MHz$			3.7	mA
C_{IN}	Input Capacitance [1] [3]	$T_A=25°C$		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	$T_A=25°C$		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
2. $V_{DD}=5V$, $T_A=25°C$.
3. These parameters are guaranteed but not 100% tested.

NOTE: All typical values have been characterized but are not tested.

IM6402/IM6403

INTERSIL

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ±10% V_{SS} = 0V, C_L = 50pF, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 4,5,6)	D.C.		1.0	MHz
$f_{crystal}$	Crystal Frequency IM6403				2.46	MHz
t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
t_{mr}	Pulse Width MR		600	200		ns
t_{ds}	Input Data Setup Time		75	20		ns
t_{dh}	Input Data Hold Time		90	40		ns
t_{en}	Output Enable Time			80	190	ns

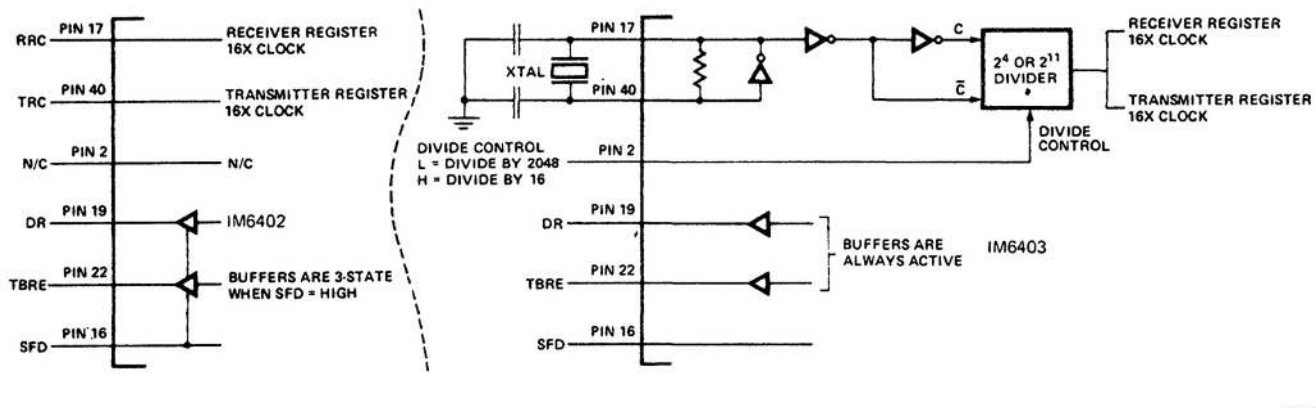


Figure 3: Functional Difference Between IM6402 and IM6403 UART (IM6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three Inputs (RRC, TRC, pin 2) as shown in Figure 3. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 12). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

NOTE: All typical values have been characterized but are not tested.

(IM6402AI/AM, IM6403AI/AM) ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) ..... +12.0V
Voltage On Any Input or Output Pin ..... ($V_{SS}-0.3V$) to ($V_{DD}+0.3V$)

Operating Temperature Range
IM6402AI/03AI ..... −40°C to +85°C
IM6402AM/03AM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=4.0V$ to 11.0V $V_{SS}=0V$, $T_A=$ Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IH}	Input Voltage High		70% V_{DD}			V
V_{IL}	Input Voltage Low				10% V_{DD}	V
I_{IL}	Input Leakage [1] [3]	$V_{SS} \le V_{IN} \le V_{DD}$	−1.0		1.0	μA
V_{OH}	Output Voltage High	$I_{OH}=0mA$		$V_{DD}-0.01$		V
V_{OL}	Output Voltage Low	$I_{OL}=0mA$		$V_{SS}+0.01$		V
I_{OLK}	Output Leakage	$V_{SS} \le V_{OUT} \le V_{DD}$	−1.0		1.0	μA
I_{CC}	Power Supply Current Standby	$V_{IN}=V_{SS}$ or V_{DD}		5.0	500	μA
I_{CC}	Power Supply Current IM6402A	$f_{crystal}=4MHz$			9.0	mA
I_{CC}	Power Supply Current IM6403A	$f_{crystal}=3.58MHz$			13.0	mA
C_{IN}	Input Capacitance [1] [3]	$T_A=25°C$		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	$T_A=25°C$		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
2. $V_{DD}=5V$, $T_A=25°C$.
3. These parameters are guaranteed but not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=10.0V \pm 5\%$ $V_{SS}=0V$, $C_L=50pF$, $T_A=$ Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
f_c	Clock Frequency IM6402A	See Timing Diagrams (Figures 4,5,6)	D.C.		4.0	MHz
$f_{crystal}$	Crystal Frequency IM6403A				6.0	MHz
t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
t_{mr}	Pulse Width MR		400	200		ns
t_{ds}	Input Data Setup Time		40	0		ns
t_{dh}	Input Data Hold Time		30	30		ns
t_{en}	Output Enable Time			40	70	ns

NOTE: All typical values have been characterized but are not tested.

IM6402/IM6403

INTERSIL

(IM6402-1I/1M, IM6403-1I/1M)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) ..... +8.0V
Voltage On Any Input or Output Pin ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)

Operating Temperature Range
IM6402-1I/03-1I ..... −40°C to +85°C
IM6402-1M/03-1M ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0\pm10\%$ $V_{SS}=0V$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IH}	Input Voltage High		$V_{DD}-2.0$			V
V_{IL}	Input Voltage Low				0.8	V
I_{IL}	Input Leakage [1] [3]	$V_{SS}\le V_{IN}\le V_{DD}$	−1.0		1.0	μA
V_{OH}	Output Voltage High	$I_{OH}=-0.2mA$	2.4			V
V_{OL}	Output Voltage Low	$I_{OL}=2.0mA$			0.45	V
I_{OLK}	Output Leakage	$V_{SS}\le V_{OUT}\le V_{DD}$	−1.0		1.0	μA
I_{CC}	Power Supply Current Standby	$V_{IN}=V_{SS}$ or V_{DD}		1.0	100	μA
I_{CC}	Power Supply Current IM6402 Dynamic	$f_c=2MHz$			1.9	mA
I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}=3.58MHz$			5.5	mA
C_{IN}	Input Capacitance [1] [3]	$T_A=25°C$		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	$T_A=25°C$		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
2. $V_{DD}=5V$, $T_A=25°C$.
3. These parameters are guaranteed but not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0V\pm10\%$ $V_{SS}=0V$, $C_L=50pF$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
f_c	Clock Frequency IM6402-1	See Timing Diagrams (Figures 4,5,6)	D.C.		2.0	MHz
$f_{crystal}$	Crystal Frequency IM6403-1				3.58	MHz
t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
t_{mr}	Pulse Width MR		400	200		ns
t_{ds}	Input Data Setup Time		50	20		ns
t_{dh}	Input Data Hold Time		60	40		ns
t_{en}	Output Enable Time			80	160	ns

NOTE: All typical values have been characterized but are not tested.

TIMING DIAGRAMS

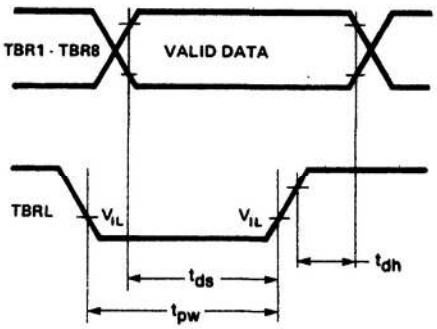


Figure 4: Data Input Cycle

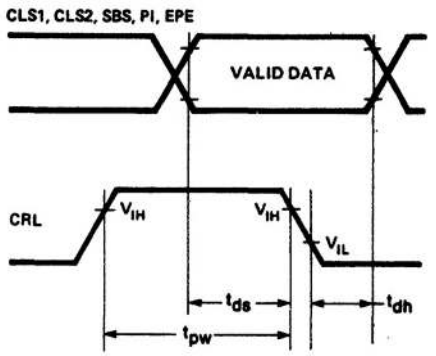


Figure 5: Control Register Load Cycle

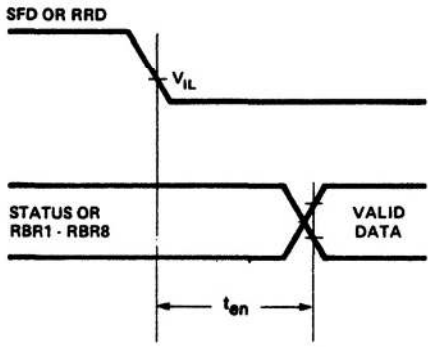


Figure 6: Status Flag Enable Time or Data Output Enable Time

Table 1: IM6402/3 Pin Description

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	V_{SS}	Negative Supply
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$; active low).

NOTE: All typical values have been characterized but are not tested.

Table 1: IM6402/3 Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR*, TBRE* to a high impedance state. See Block Diagram and Figure 6. * IM6402 only.
17	IM6402-RRC IM6403-XTAL	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 4.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

Table 1: IM6402/3 Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 5.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits)(CLS1 high CLS2 low 6-bits)(CLS1 low CLS2 high 7-bits)(CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

NOTE: All typical values have been characterized but are not tested.

Table 2: Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

x = Don't Care

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal.

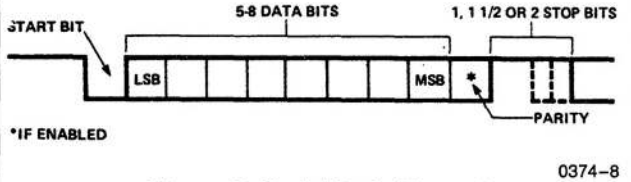


Figure 7: Serial Data Format

Transmitter timing is shown in Figure 8. Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{\text{TBRL}}$oad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{\text{TBRL}}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. The rising edge of $\overline{\text{TBRL}}$ clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high.

Output data is clocked by TRClock, which is 16 times the data rate. A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Data is automatically transferred to the transmitter register and transmission of that character begins.

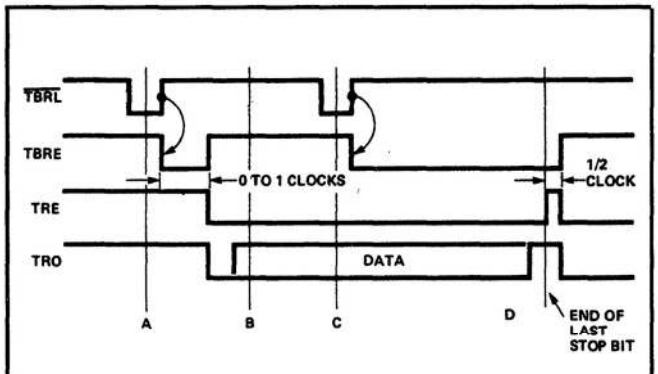


Figure 8: Transmitter Timing (Not to Scale)

NOTE: All typical values have been characterized but are not tested.

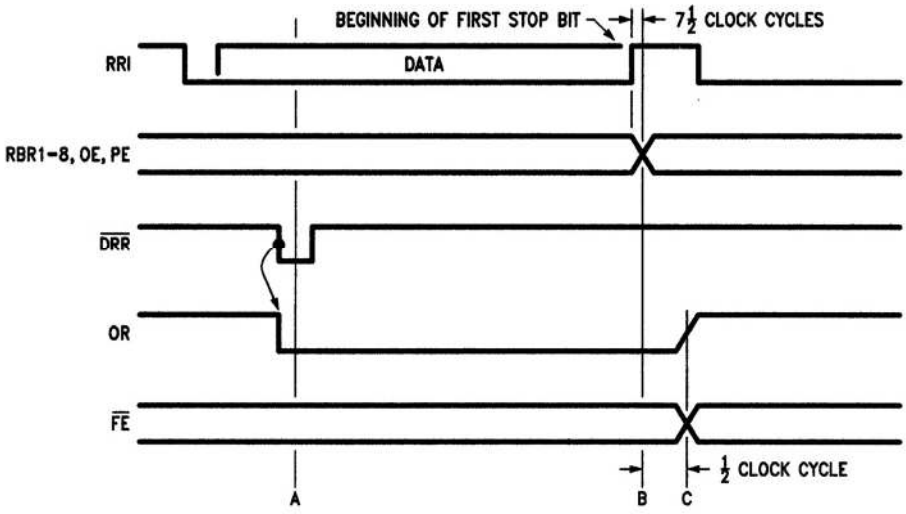


Figure 9: Receiver Timing (Not to Scale)

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 9.

A low level on $\overline{DRR}$eset clears the DReady line. During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. ½ clock cycle later, DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

START BIT DETECTION

The receiver uses a 16X clock for timing. (See Figure 10.) The start bit (A) could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±½ clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

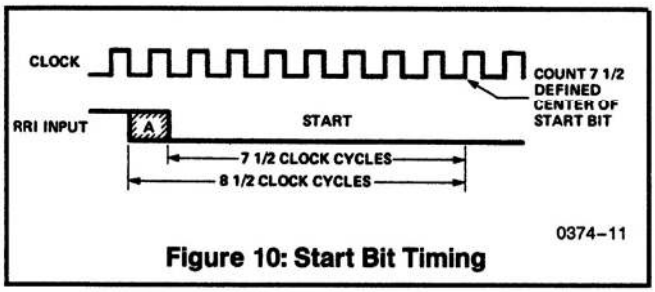


Figure 10: Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 11 shows how the IM6402 can be interfaced to an IM80C48 microcomputer system.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs *should be tied to either V_{DD} or V_{SS}.*

The baud rate at which the transmitter and receiver will operate is determined by the IM4702 Baud Rate Generator.

To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM80C48 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not re-trigger RESET. A long reset pulse after power-up (~20ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a $\overline{DRR}$ is performed.

NOTE: All typical values have been characterized but are not tested.

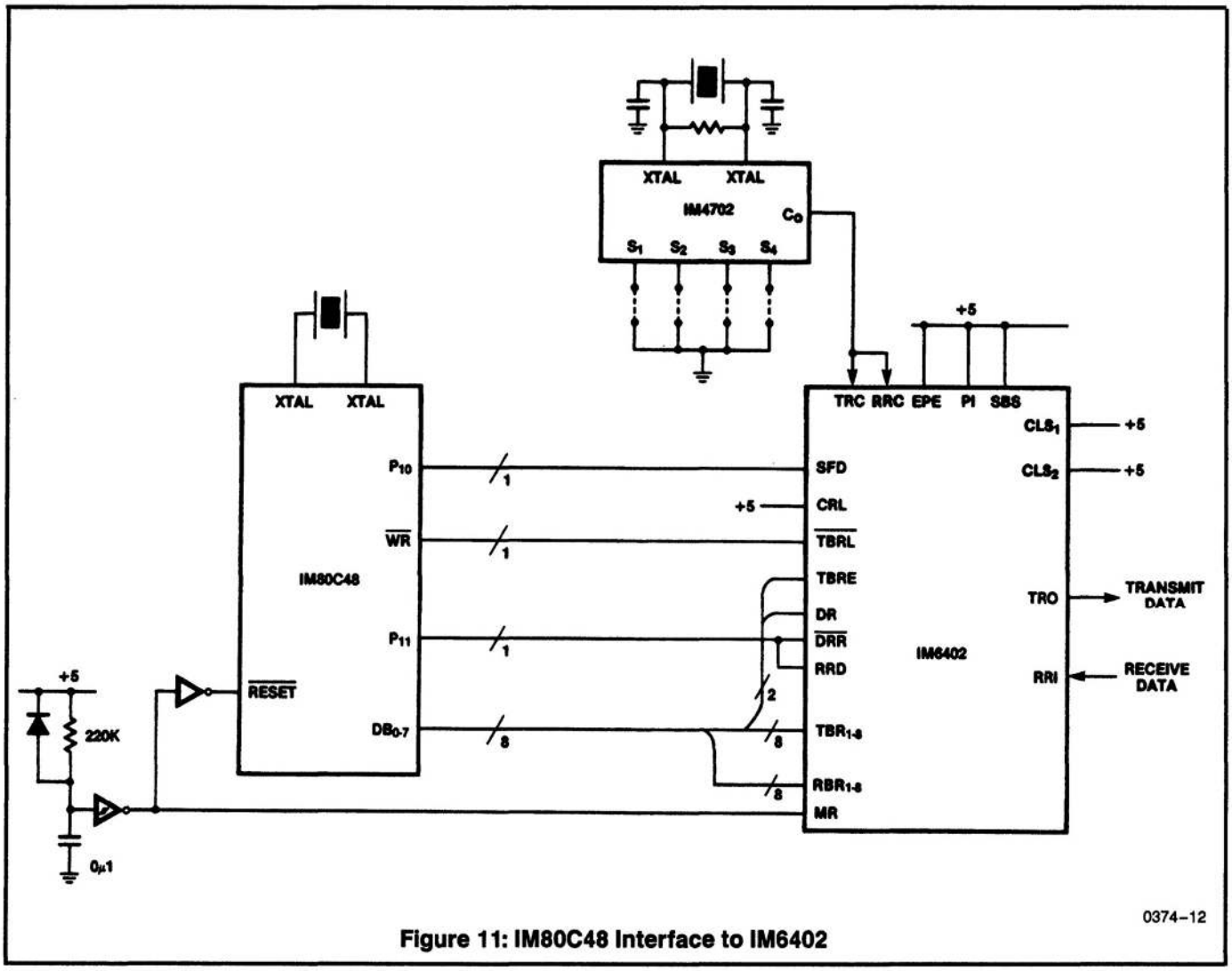


Figure 11: IM80C48 Interface to IM6402

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NOTE: All typical values have been characterized but are not tested.