2011

Application of an Intelligent Tuning Algorithm for Three-Level NPC Rectifier for Shipboard Power Distribution

Yusi Liu

THE FLORIDA STATE UNIVERSITY

COLLEGE OF ENGINEERING

APPLICATION OF AN INTELLIGENT TUNING ALGORITHM FOR THREE-LEVEL NPC RECTIFIER FOR SHIPBOARD POWER DISTRIBUTION

By

YUSI LIU

A Thesis submitted to the
Electrical and Computer Engineering Department
in partial fulfillment of the
requirement for the degree of
Master of Science

Degree Awarded:
Summer Semester, 2011

The members of the committee approve the thesis of Yusi Liu defended on June 8th, 2011.

_____
Chris S. Edrington
Professor Directing Thesis

_____
Simon Y. Foo
Committee Member

_____
Mark H. Weatherspoon
Committee Member

Approved:

_____
Simon Y. Foo, Chair, Electrical and Computer Engineering Department

_____
John Collier, Dean, College of Engineering

The Graduate School has verified and approved the above-named committee members.

ACKNOWLEDGEMENTS

First, I would like to thank my research and academic supervisor Chris S. Edrington PhD for his continuous and careful supervision, advice, and guidance from the first day I involved in the Non-Linear Dynamic Load Project. At beginning I was even very good at MATLAB, but through Dr. Edrington's comprehensive knowledge and patient direction, I completed the three-level NPC rectifier hardware test bed and its advanced controller research. Without his provisions, which include computer, power equipment, software licences, office and lab space, funding, this work could not be achieved. What's more, he taught me how to think, analyze and learn independently, how to illustrate and present my ideas and work in front of other researchers, such as giving me the opportunity to participate in scientific conference. I obtained the experience how to cooperate with other engineers as well. He made me a more professional and mature engineer.

I want to specially thank Saritha Balathandayuthapani PhD and Amin Hasanzadeh PhD for their self-giving help in details of my research even when it's after work hours. Their patience and experience of power electronics ensured my research could go ahead step by step. Sincere thanks go to Jesse Leonard, who works with me most in the lab, helping me improve my lab ability a lot. Thanks to other students from the EC&I group: Troy Bevis, Michael Sattler, Fletcher Fleming, Stroupe Nick, Brian Hacker, Dionne Soto, Furkan Akar, Ryster Shawn, Shawn Henry PhD, who make an excellent team, but also my lifelong friends. Zhan Wang, Yan Zhou, Xiaohu Liu, who are Chinese researchers in CAPS, thank you share your for academic experience and daily life with me when I'm studying and living at FSU.

Last but not least, thank you to my parents and my girlfriend Ziqing Zhai, who are supporting and loving me from more than a thousand miles away in China. Without your care and patience, my American dream can never happen. Everyone who contributed that was not specifically named I thank you too. During my course of work at Florida State University (2009-2011), I'm supported by Office of Naval Research (ONR) Grant Number N00014-09-1-1097.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converter
ADC	Digital-to-Analog Converter
BNC	British naval connector
CHIL	Controller-Hardware-in-the-Loop
CSR	Current Source Rectifier
DC	Direct Current
DSP	Digital Signal Processor
dSPACE	Digital Signal Processing and Control Engineering
EMI	Electromagnetic Interference
FOC	Field Oriented Control
FPGA	Field Programmable Gate Array
HIL	Hardware in the Loop
HUT	Hardware under test
I/O	Input/Output
IGBT	Insulated-Gate Bipolar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MVDC	Medium-Voltage Direct Current
NPC	Neutral Point Clamped
PCB	Print Circuit Board
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
RPC	Rapid Prototyping Controller
RTDS	Real Time Digital Simulator
SISO	Single Input Single Output

SPTT	Single Pole Triple Throw
SPWM	Sine Wave Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
VSR	Voltage Source Rectifier

ABSTRACT

The demand for high-voltage and high-power power electronics devices, especially for the next generation electrical ship system, has increased rapidly these years. The three-phase three-level neutral point clamped (NPC) rectifier attracts more and more engineers' attention due to it has many advantages: sinusoidal input current which contains low harmonics, unity power factor, bidirectional power flow, low voltage and switching loss for each switch and so on. It could potentially provide DC power to medium voltage DC distribution system on ships. A NPC rectifier system is introduced in this thesis and the hardware test bed for validating is built successfully.

Base on the topology of NPC rectifier, the PWM math model in ABC stationary frame is set up first. In order to obtain constant control variables as in DC motor control, the NPC rectifier PWM math model in DQ0 reference frame is built. And then for design the control loop, the NPC rectifier average models are developed in both ABC stationary frame and DQ0 reference frame.

Three-level SVM is used for achieving sinusoidal input current, lower current THD and lower switching loss. Neutral point voltage balance problem is an inherent problem of three-level PWM rectifier. Without neutral point voltage control, the harmonic components of input current will greatly increase, and the DC-link capacitors and the switching devices may probably be destroyed. The influences of every switching state on neutral-point are analyzed and the small-vector is actively utilized to solve the neutral point balance problem.

When to design the PI controller gains, the classic Nichols and Ziegler rules and the NPC system responses to this tuning algorithm are showed firstly. Further optimization for the system PI controller gains, which base on Particle Swarm Optimization (PSO), is used and the system responses are compared to the classic Nichols and Ziegler rules'. Hardware data validate the improvement of PSO contributes to the NPC system.

A NPC rectifier real-time Controller-hardware-in-the-loop (CHIL) test is completed before the real hardware experiment since it could de-risk the controller for hardware experiment. The real-time simulation is compared to the hardware experiment, the CHIL methodology is approved.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Electricity is an enabling form of energy. It's making possible many technologies that would not be possible otherwise, i.e., robotics, information system, laser, etc. It also enables more efficient use of raw source of energy such as oil. The power electronics converters are at the heart of increasing and numerous uses of electricity because they can convert electricity to DC and different frequencies, pulses, and variation of radiation. This thesis focused on one of very useful power electronics converter topologies: three-level three-phase rectifier, which changes power from AC to DC.

Future marine electrical systems will be profoundly different from today's systems due to the power electronics that are making tremendous impacts on virtually every marine system including propulsion, power distribution, auxiliary, and radar. Figure 1-1 shows the IEEE Std 1709-2010, which describes the recommended practice for 1 kV to 35 kV medium-voltage DC power systems on ships. It's clear that the rectifier plays one of the most important roles in this MVDC power system. The advanced three-level three-phase NPC rectifier topology potentially meets ships systems' requirements because of its lower harmonics, four-quadrant operation so that the power factor is controlled as commanded. If the harmonic current which back fed to the generator could be reduced, it could reduce the generator harmonic load torque and corresponding acoustic noise, which is especially benefit to the future navy ship and submarine. With the high power factor, ships may have smaller-sized power cables and less power loss during the distribution. It requires a much smaller-sized filter and may replace certain transformer functions which could reduce the room required by the power system on ships.

PWM is a useful and powerful technology, but its advantages are not without sacrifice. Its high switching frequency results in higher switching losses which limits the power electronics device application. The three-level rectifier has more switches than the conventional two-level rectifier, so the losses and voltage stress on each switch are

comparably smaller. Therefore, this topology has higher switching frequency and voltage limitation.

As the developed power electronics devices are becoming more complicated and sophisticated, optimized and advanced controller designs are needed. Although classic Nichols and Ziegler algorithm, which is based on the linear transfer function response, could tune the PI controller parameters for non-linear power electronics system very well, there still exist further optimization algorithms which may control the system better. Modeled after the flocking behavior of birds, Particle Swarm Optimization (PSO) gives engineers a new method to determine the PI controller parameters based on a more accurate non-linear math model. This Optimization algorithm may help power electronics engineers improve their controller design and obtain better system performance.

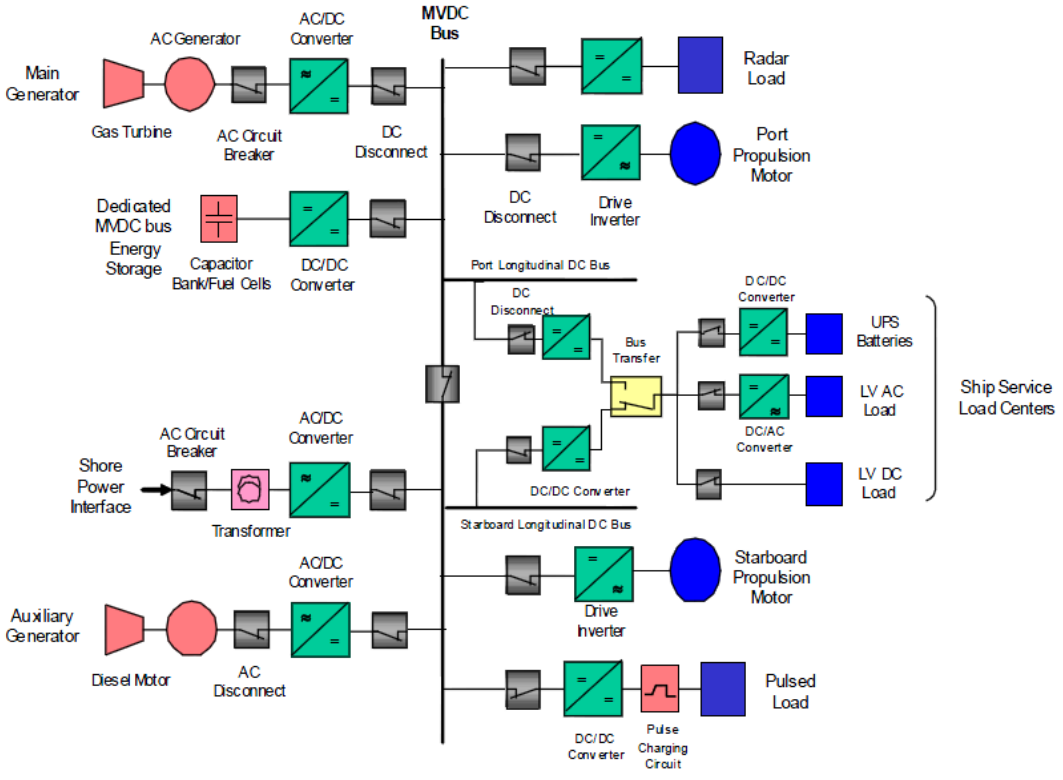


Figure 1- 1 IEEE recommended practice for 1 kV to 35 kV medium-voltage DC power systems on ships

When engineers finish the complex system design and succeed in testing the system in the non-real-time simulation such as in MATLAB, they are not guaranteed that there's no problem in the hardware test due to the face that non-real-time simulation could not

reflect all possible physical characteristics of the power electronic devices. Controller-hardware-in-the-loop (CHIL) allows engineers to test the system controller in real-time simulation environment which can de-risk the hardware failure due to the design bug in the controller.

1.2 Literary Review

The first very high power electronic devices were mercury arc valves rectifier used for converting AC into DC invented by Peter Cooper Hewitt in 1902 and further developed by researchers throughout the 1920s and 1930s [1]. Until about 1975, high-voltage solid-state devices, silicon diode and thyristor, etc, had made mercury-arc rectifiers greatly obsolete. When the diode rectifier and thyristor rectifier became more and more popular, engineers found that they cause many serious problems [2]:

- They inject a lot of harmonics to the grid
- Low power factor which increases the loss and the size of devices
- They need large smoothing reactors and filter capacitors to obtain constant DC output. Reactors and capacitors cost additional loss.
- Thyristor rectifier dynamic response is slow.

In [3], different common passive filter topologies are compared. The harmonic currents generated by diode and thyristor rectifiers cause various power quality problems when flowing through the utility system. The distribution bus voltage is distorted by the distorted currents flowing though line source inductance. The harmonics may create problems on sensitive loads which operate on the same bus, also causing errors in meter reading, protective relay malfunction. The harmonics reduce the energy utilizing rate by causing additional loading and losses in generators, transmission, and distribution line, transformer, and circuit breaker. The service life of cable and other system components becomes shorter due to the harmonic currents. Harmonics also cause EMI (electromagnetic interference) which create communication line interference and malfunctions to sensitive signal electronic circuits [2]. IEEE 519-1992 restricts the THD which allowed injecting to the utility grid [3].

Pulse Width Modulation (PWM) technique is initially implemented for the inverter to reduce the large current distortion caused by the six-step inverter in which there are

only six switching per cycle of fundamental frequency. In the 1970s, engineers succeeded introducing the PWM technique into rectifier. Due to the lack of market demand and lagging development of switching devices, this technique didn't attract early attention. In the1990s, with the help of heavy power switching (such as IGTB) and the harmonic problems becoming more and more serious, the PWM rectifier became a very popular topic in both power electronics research and industry [2][4]. The reactive power causes extra loss in transmission line and reduces the utilization ratio of devices. Compared to the diode rectifier's low power factor, the PWM rectifier could achieve nearly unity power factor which increase the power utilization ratio and reduces the devices' sizes.

There are two types of PWM rectifier: voltage source rectifier (VSR) and current source rectifier (CSR). VSR is a boost type rectifier which uses capacitors on the output DC side to store energy. Its DC side voltage is higher than the peak value of the input AC voltage. The CSR is a buck type rectifier which uses inductances on the output DC side to store energy. Its DC side voltage is lower than the peak value of the input AC voltage. Currently, the VSR accounts for the majority of rectifiers, especially in the media and small power rating area [4]. In this thesis, the three-phase three-level NPC rectifier is VSR.

Figure 1-2 shows the common circuit topology of a three-phase fully-controlled VSR. Except for the input AC reactors, this topology is similar to that of the three-phase inverter. Since this rectifier obtains many desirable features such as sinusoidal line currents with low THD, controllable power factor (could achieve unity power factor), a nearly constant DC output voltage without excessively large capacitors, fast and accurate dynamic response, and bidirectional power delivery capability. But when the output DC voltage or semiconductor device switching frequency increases, it's possible that the switches could fail due to the stress. In [4], damage of power system components, such as motors, has been reported by industry due to the converters' high voltage change rate (dV/dt), as a result of the common-mode voltage across the motor windings. The damage may be exacerbated by the high frequency switching. Can we reduce the voltage and switching stress on switches?

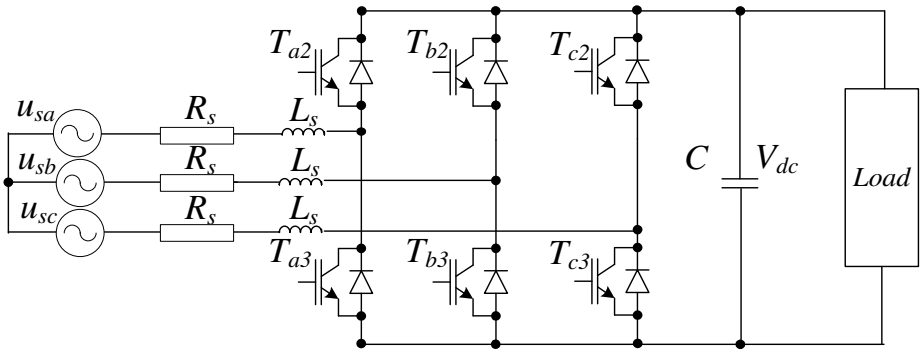


Figure 1- 2 Two-level PWM rectifier main circuit

Yes, introduced by Nabae in 1981 [6], compared to conventional two-level converters, multi-level converters have attracted more and more attention from power electronics engineers since their advantages [2][7][8]:

- Produce multi- level input voltage and then reduce the line-current THD;
- Decrease voltage stress across semiconductor devices;
- Decrease switching loss on each semiconductor devices;

Three-level three-phase rectifier topology is showed in figure 1-3 [9][10]. If the total output DC voltage $V_{dc}'=V_{dc1}+V_{dc2}$ in figure 1-3 is equal to output DC voltage V_{dc} in figure 1-2, and the voltage across two capacitors $V_{dc1}=V_{dc2}$, then $V_{dc1}=V_{dc2}=V_{dc}/2$. Each switch only connects to at most one capacitor C_d with the control algorithm which will discussed later, so the voltage across each switch is $V_{dc}/2$. With a proper modulation strategy, there are four switches in each phase; they could share the switching task. So the thermal problem which limits higher switching frequency could be solved in certain range and the system switching frequency may go higher. Therefore, applying three-level technology, the voltage stress on switches is reduced, the harmonic distortion of AC input current is diminished and the power rating of the system as a whole is increased.

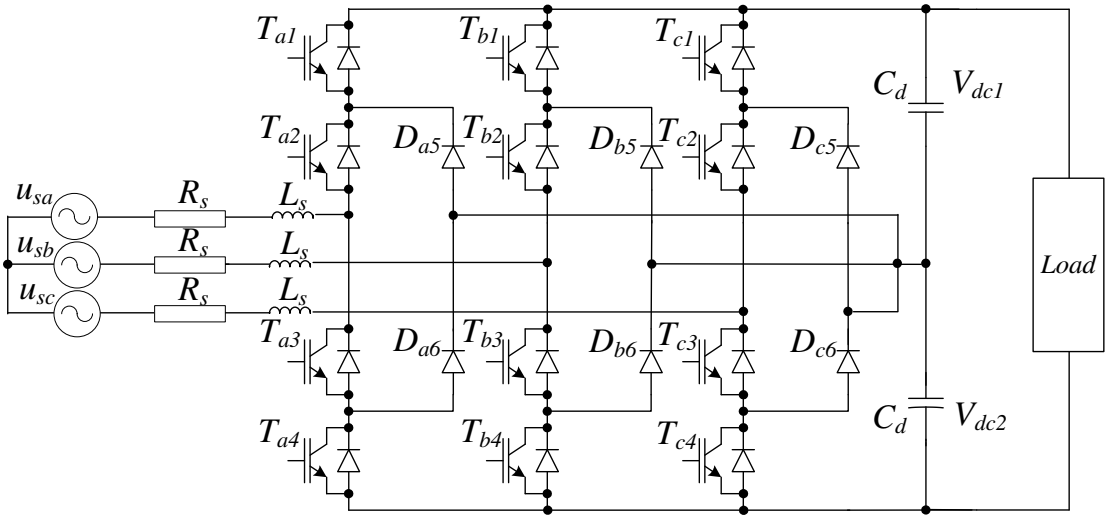


Figure 1- 3 Three-level PWM rectifier main circuit

As the saying goes, “No pain no gain”. Engineers could not obtain so much advantage from this three-level topology without extra paying. Firstly, there are more switches which increase the cost, along with a more complicated control strategy than the two-level rectifier. Most importantly is the neutral point voltage balancing problem [11], which is an inherent problem of this topology and has been widely recognized in literature, must be solved; otherwise if V_{dc1} and V_{dc2} are not equal, high voltage may stress on switches and distort the PWM pulse voltage. Finally, large harmonic distortion current even the entire three level converters would be at risk. Space vector modulation [2][12] with Bang-bang neutral point control technique [13], which is comparably easy to apply in DSP, could control the V_{dc1} and V_{dc2} to be balanced and the system dynamic response satisfied.

When designing the controller of this three level rectifier, establishing a precise and comprehensive math model is an effective methodology [9]. MATLAB software is good tool to simulate the circuit, but it’s still difficult to analyze the whole system. The average math model is helpful in designing the controller of a power electronics system [13]. Double closed-loop, which includes outer speed or torque loop and inner current loop, is a prevalent methodology in modern motor speed control [2]. It could simply be apply in a rectifier controller in which there are outer voltage loops and inner current loops. The direct current control, where phase currents are fed back to the controller, has an outstanding transient dynamic response so the system can respond to the varying inputs

and command references with ease. Additionally, this control technique makes it convenient for designers to limit current within a safe range to avoid harming the equipment.

There are several PI controllers in the three-level rectifier system, so how to tune the PI controller gains is a question needs to be solved. The classic Nichols and Ziegler method needs linearization of the system into a single input single output transfer function, and then tunes the PI gains based on the dynamic response performance of the transfer function [14]. There are many information been omitted and the non-linear characters of the three-level rectifier is lost. Base on flocking behavior of birds, Particle Swarm Optimization (PSO) [15] is potential method to further optimize the PI controller gains [16]. It retains the system non-linear characters and multiple inputs and outputs information. The system response to this new tuning method will be discussed in this thesis.

As the three-level rectifier system and its control are complex, it's reasonable for engineers to conduct a controller-hardware-in-the-loop (CHIL) test prior to the real hardware test [17]. This real-time simulation test could evaluate, de-risk and debug the hardware controller algorithm of the three-level rectifier. It gives an almost seamless transition to the hardware, so the methodology could potentially save research hours and hardware investment since the risk of destroying the device is decreased after the CHIL test.

CHAPTER 2

NPC RECTIFIER MODELING

Modeling of the Neutral Point Clamped (NPC) rectifier is fundamental and essential to the research work of NPC rectifier. At the beginning of this chapter, the Pulse Width Modulation (PWM) math model of the NPC converter is showed in both ABC stationary frame and DQ0 reference frame. Since the PWM switch based model is difficult to use for analyzing the system performance for control design, the average model of the NPC converter is built after the PWM model.

2.1 NPC Rectifier Math Model

There are two types of rectifiers: voltage source rectifier (VSR) and current source rectifier (CSR) [5]. The NPC rectifier discussed in this thesis is a VSR since the DC side connected to capacitors and performs low impedance as a voltage source and the DC side voltage level is higher than the AC side line-to-neutral peak value. The main circuit of NPC rectifier is showed in Figure 2-1.

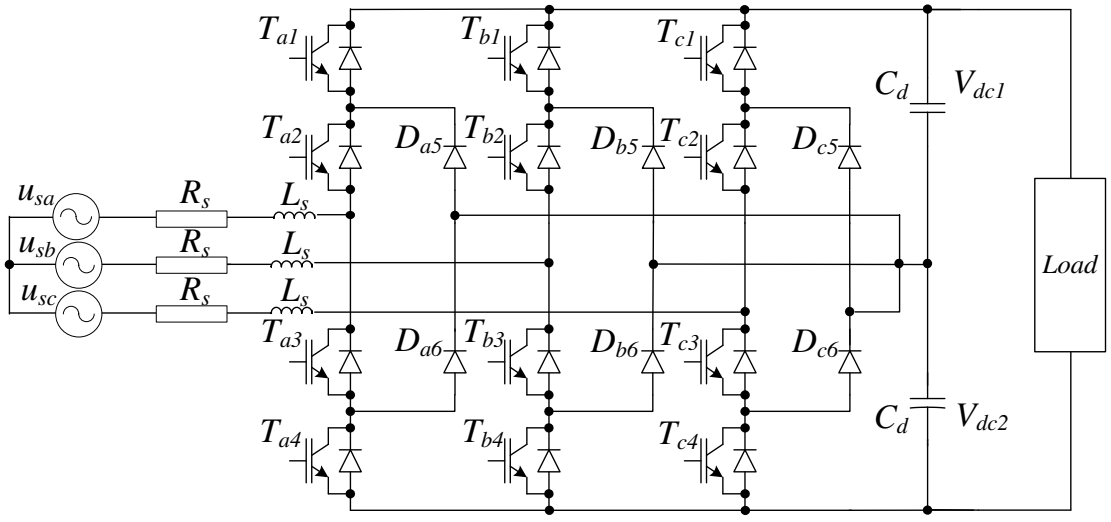


Figure 2- 1: Three-phase three-level NPC rectifier main circuit

Parameters in Figure 2-1 are explained as following:

- u_{sa}, u_{sb}, u_{sc} : AC input voltage from grid or generator.

- R_s: line resistance.
- L_s: the inductance of the reactor.
- T_{ax}, T_{bx}, T_{cx}: switches in converters, in this thesis, they are IGBTs with anti-parallel diodes.
- $D_{ax,}$ $D_{bx,}$ D_{cx}: clamped diodes.
- C_d: the DC capacitor. The capacitor value of the upper level and the lower level are equal.

We define the phase A switch function S_a as follow:

$$S_a = \begin{cases} 2, T_{a1} \text{ and } T_{a2} \text{ turned on, } T_{a3} \text{ and } T_{a4} \text{ turned off;} \\ 1, T_{a2} \text{ and } T_{a3} \text{ turned on, } T_{a1} \text{ and } T_{a4} \text{ turned off;} \\ 0, T_{a3} \text{ and } T_{a4} \text{ turned on, } T_{a1} \text{ and } T_{a2} \text{ turned off.} \end{cases} \quad (2\text{-}1)$$

Regardless whether phase A current flows into the NPC rectifier or out from it, when $S_a = 2$, the phase A current flows to or from the upper level of DC side. Similarly, when $S_a = 1$, the phase A current flows to or from the neutral point of DC side. When $S_a = 0$, the phase A current flows to or from the lower level of DC side. S_b and S_c are defined in identical way. Then the switches and clamped diodes in each phase in figure 2-1 could simplified to a single pole triple throw (SPTT) switch, the equivalent circuit is illustrated in figure 2-2. For example, when $S_a = 2$, the blade of the phase A SPTT connects to the point 2 in figure 2-2.

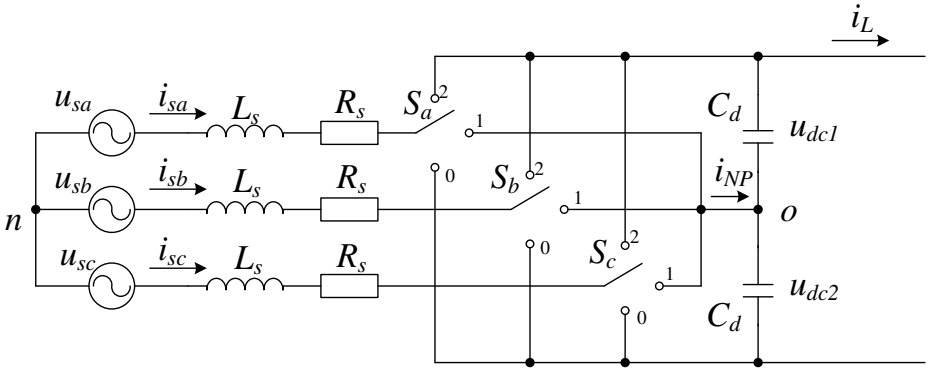


Figure 2- 2: Three level NPC rectifier equivalent circuit

In order to make future math derivations easier, further definition of switch state is explained as follow: when $S_a = 2$, it means $S_{a1}= 1$, $S_{a2}= 0$, $S_{a3}= 0$; when $S_a = 1$, it means

S_{a1}= 0, S_{a2}= 0, S_{a3}= 1; when S_a = 0, it means S_{a1}= 0, S_{a2}= 1, S_{a3}= 0. Phase B and phase C switch can be defined in the same method.

2.2 NPC Rectifier PWM Math Model in ABC Stationary Frame

The input of the NPC rectifier is a three-phase non-neutral line AC. We assume the three phase voltage is balance. u_{no} is voltage between grid neutral point and NPC rectifier neutral point at DC side in figure 2-1. u_{sa}, u_{sb}, u_{sc} are three-phase input AC voltage and i_{sa}, i_{sb}, i_{sc} are three-phase input AC currents.

$$\begin{cases} u_{sa} + u_{sa} + u_{sa} = 0 \\ i_{sa} + i_{sb} + i_{sc} = 0 \end{cases} \tag{2-2}$$

The instantaneous values of the AC voltages are

$$\begin{cases} u_{sa} = V_{sm} \cdot \cos(\omega t) \\ u_{sb} = V_{sm} \cdot \cos(\omega t - \dfrac{2\pi}{3}) \\ u_{sc} = V_{sm} \cdot \cos(\omega t + \dfrac{2\pi}{3}) \end{cases} \tag{2-3}$$

V_{sm} is the peak value of phase to neutral voltage and ω is grid angle frequency.

Base on the Kirchhoff's Voltage Law (KVL), Kirchhoff's Current Law (KCL) and the character of inductor and capacitor, the PWM math model of NPC rectifier is [18]

$$\begin{cases} u_{sa} = L_s \cdot \dfrac{di_{sa}}{dt} + R_s \cdot i_{sa} + S_{a1} \cdot V_{dc1} - S_{a2} \cdot V_{dc2} + u_{no} \\ u_{sb} = L_s \cdot \dfrac{di_b}{dt} + R_s \cdot i_{sb} + S_{b1} \cdot V_{dc1} - S_{b2} \cdot V_{dc2} + u_{no} \\ u_{sc} = L_s \cdot \dfrac{di_c}{dt} + R_s \cdot i_{sc} + S_{c1} \cdot V_{dc1} - S_{c2} \cdot V_{dc2} + u_{no} \end{cases} \tag{2-4}$$

$$\begin{cases} C_d \dfrac{dV_{dc1}}{dt} = S_{a1} \cdot i_{sa} + S_{b1} \cdot i_{sb} + S_{c1} \cdot i_{sc} - i_L \\ C_d \dfrac{dV_{dc2}}{dt} = -S_{a2} \cdot i_{sa} - S_{b2} \cdot i_{sb} - S_{c2} \cdot i_{sc} - i_L \end{cases} \tag{2-5}$$

From equation (2-2) and (2-4) we could calculate:

$$u_{no} = -\frac{1}{3}(S_{a1} + S_{b1} + S_{c1})V_{dc1} + \frac{1}{3}(S_{a2} + S_{b2} + S_{c2})V_{dc2} \tag{2-6}$$

2.3 NPC Rectifier PWM Math Model in DQ0 Reference Frame

In previous section 2.1.1, Variables (voltages, current) associated with stationary frame are time-varying. It causes problems to feedback control of the system. R. H. Park, in 1920s, firstly proposed the reference frame theory of electrical machine analysis to solve this time-varying variables problem [12]. Currently, this reference frame theory is well-know to electrical engineers as Park's transformation which showed in (2-7), in which, $\omega=\frac{d\theta}{dt}$ is electrical angle frequency in rad/s as unit, and θ is electrical angle in rad as unit.

$$T_{abc\to dq0}=\frac{2}{3}\begin{bmatrix}\cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3})\\ \sin\theta & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3})\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix} \tag{2-7}$$

Variables (voltages, currents, or flux linkages in motor) in ABC stationary frame are considered as f_{as}, f_{bs}, f_{cs}, and variables in DQ0 reference frame are considered as f_{ds}, f_{qs}, f_{0s} as

$$\begin{cases}(f_{dq0s})^T=\begin{bmatrix}f_{ds} & f_{qs} & f_{0s}\end{bmatrix}\\ (f_{abcs})^T=\begin{bmatrix}f_{as} & f_{bs} & f_{cs}\end{bmatrix}\end{cases} \tag{2-8}$$

We have the relationship:

$$f_{dq0s}=T_{abc\to dq0}f_{abcs} \tag{2-9}$$

The inverse of the matrix $T_{abc\to dq0}$ is knew as inverse Park's transformation $T_{dq0\to abc}$

$$f_{abcs}=T_{dq0\to abc}f_{dq0s} \tag{2-10}$$

$$T_{dq0\to abc}=T_{abc\to dq0}^{-1}=\begin{bmatrix}\cos\theta & \sin\theta & 1\\ \cos(\theta-\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) & 1\\ \cos(\theta+\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) & 1\end{bmatrix} \tag{2-11}$$

Combining the above Equation (2-4), (2-5), (2-6) with the Park's and inverse Park's transformation (2-7), (2-11), the math model of three phase NPC rectifier in DQ0 reference frame could be derived as input d axis (active power) and q axis (reactive power) currents:

$$\begin{cases} L\dfrac{di_{ds}}{dt} = -R_s i_{ds} + \omega L i_{sq} - V_{dc1} S_{d1} + V_{dc2} S_{d2} + u_{sd} \\ L\dfrac{di_{qs}}{dt} = -R_s i_{qs} - \omega L i_{sd} - V_{dc1} S_{q1} + V_{dc2} S_{q2} + u_{sq} \end{cases} \tag{2-12}$$

and two DC capacitor voltages

$$\begin{cases} C_d \dfrac{dV_{dc1}}{dt} = \dfrac{3S_{d1}}{2} i_{sd} + \dfrac{3S_{q1}}{2} i_{sq} - i_L \\ C_d \dfrac{dV_{dc2}}{dt} = -\dfrac{3S_{d2}}{2} i_{sd} - \dfrac{3S_{q2}}{2} i_{sq} - i_L \end{cases} \tag{2-13}$$

$$\text{in which } \begin{cases} [S_{d1} \quad S_{q1}]^T = T_{dq0\to abc}[S_{a1} \quad S_{b1} \quad S_{c1}] \\ [S_{d2} \quad S_{q2}]^T = T_{dq0\to abc}[S_{a2} \quad S_{b2} \quad S_{c2}] \end{cases} \tag{2-14}$$

From (2-12) and (2-13) we could conclude the three phase NPC rectifier math model block in DQ0 reference frame in figure 2-3

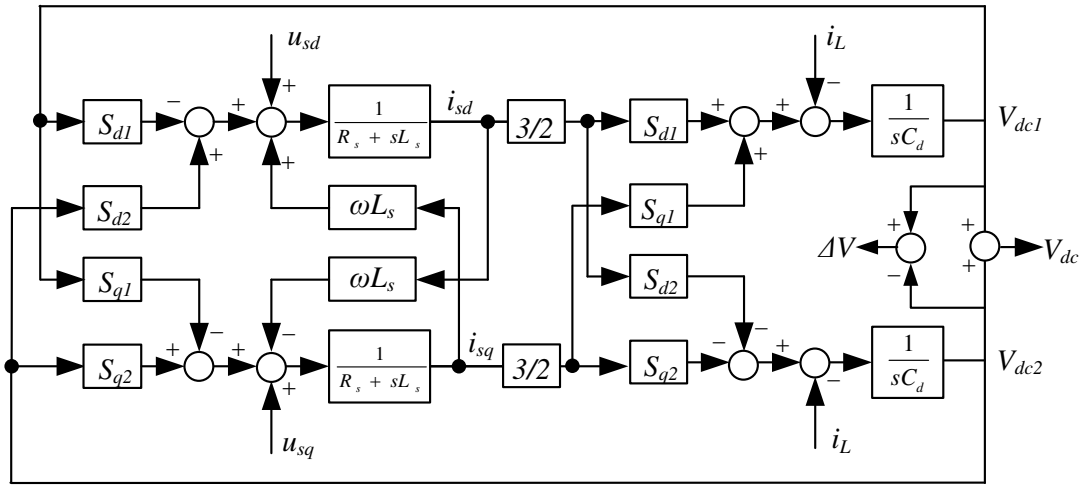


Figure 2- 3: Three level NPC rectifier math model in reference frame

2.4 NPC Rectifier Average Math Model.

In section 2.2, the switching states (S_a, S_b, S_c) are instantaneous discrete values (2, 1, 0) at different time. Although the PWM model is a precise model and the MATLAB could simulate the circuit performance very well, it takes a long time to calculate the solution since the precise model requires a small step size, especially when the PWM switching frequency in high. Because the non-linear characteristics and the long time

calculation, it is extremely difficult for engineers analyze and design the system control. To solve this problem, the NPC rectifier average model is discussed in this section.

The principle of PWM requires a rectangular pulse wave whose pulse width is modulated resulting in the variation of the average value of the low frequency waveform (for example, grid's 60 Hz). In the average model, only the low frequency modulation component is kept and the high frequency switching component is omitted. If the switching frequency is high enough (more than several kilo Hz for power electronics devices), the system performance of average model is almost like the high frequency PWM model, except there is no high frequency ripple and its related non-linear behavior. 2-15 illustrates the average switching state for NPC rectifier:

$$\begin{cases} \overline{S_{a1}} = d_{a1} \\ \overline{S_{a2}} = d_{a2} \\ \overline{S_{a3}} = d_{a3} \end{cases} \quad \begin{cases} \overline{S_{b1}} = d_{b1} \\ \overline{S_{b2}} = d_{b2} \\ \overline{S_{b3}} = d_{b3} \end{cases} \quad \begin{cases} \overline{S_{c1}} = d_{c1} \\ \overline{S_{c2}} = d_{c2} \\ \overline{S_{c3}} = d_{c3} \end{cases} \tag{2-15}$$

In (2-15): d_{a1}, d_{a3}, d_{a3} are duty cycle of S_{a1}, S_{a2}, S_{a3} respectively, $d_{a1}+d_{a3}+d_{a3}=1$. Phase B and C duty cycle are defined in the same way.

Combining the (2-15) into (2-4) and (2-5), we derive the NPC rectifier average model as follow:

$$\begin{cases} u_{sa} = L_s \cdot \dfrac{di_{sa}}{dt} + R_s \cdot i_{sa} + \overline{S_{a1}} \cdot V_{dc1} - \overline{S_{a2}} \cdot V_{dc1} + u_{no} \\ u_{sb} = L_s \cdot \dfrac{di_b}{dt} + R_s \cdot i_{sb} + \overline{S_{b1}} \cdot V_{dc1} - \overline{S_{b2}} \cdot V_{dc1} + u_{no} \\ u_{sc} = L_s \cdot \dfrac{di_c}{dt} + R_s \cdot i_{sc} + \overline{S_{c1}} \cdot V_{dc1} - \overline{S_{c2}} \cdot V_{dc1} + u_{no} \end{cases} \tag{2-16}$$

$$\begin{cases} C_d \dfrac{dV_{dc1}}{dt} = \overline{S_{a1}} \cdot i_{sa} + \overline{S_{b1}} \cdot i_{sb} + \overline{S_{c1}} \cdot i_{sc} - i_L \\ C_d \dfrac{dV_{dc2}}{dt} = -\overline{S_{a2}} \cdot i_{sa} - \overline{S_{b2}} \cdot i_{sb} - \overline{S_{c2}} \cdot i_{sc} - i_L \end{cases} \tag{2-17}$$

(2-16) and (2-17) are NPC rectifier average math model in ABC stationary frame. From (2-12) and (2-13), we could further derive the NPC rectifier average math model in DQ0 reference frame as follow:

$$\begin{cases} L\dfrac{di_{ds}}{dt} = -R_s i_{ds} + \omega L i_{sq} - V_{dc1}\overline{S_{d1}} + V_{dc2}\overline{S_{d2}} + u_{sd} \\ L\dfrac{di_{qs}}{dt} = -R_s i_{qs} - \omega L i_{sd} - V_{dc1}\overline{S_{q_1}} + V_{dc2}\overline{S_{q2}} + u_{sq} \end{cases} \tag{2-18}$$

$$\begin{cases} C_d \dfrac{dV_{dc1}}{dt} = \dfrac{3\overline{S_{d1}}}{2} i_{sd} + \dfrac{3\overline{S_{q1}}}{2} i_{sq} - i_L \\ C_d \dfrac{dV_{dc1}}{dt} = -\dfrac{3\overline{S_{d2}}}{2} i_{sd} - \dfrac{3\overline{S_{q2}}}{2} i_{sq} - i_L \end{cases} \tag{2-19}$$

in which $\begin{cases} [\overline{S_{d1}} \quad \overline{S_{q1}}]^T = T_{dq0\to abc}[\overline{S_{a1}} \quad \overline{S_{b1}} \quad \overline{S_{c1}}] \\ [\overline{S_{d2}} \quad \overline{S_{q2}}]^T = T_{dq0\to abc}[\overline{S_{a2}} \quad \overline{S_{b2}} \quad \overline{S_{c2}}] \end{cases}$

In chapter 4, the average model in (2-18) and (2-19) are showed to be essential to the system control design.

CHAPTER 3

THREE-LEVEL SVM STRATEGY IN NPC RECTIFIER

Originally used in the AC machine drive system, pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches [2]. There are several different PWM techniques [12], such as Sine Wave Pulse Width Modulation (SPWM), hysteresis band current control PWM, space-vector PWM (SVM), etc. The space-vector PWM is chosen for the three-level NPC rectifier for this thesis since it is an advanced, computation-intensive PWM and is possibly the best among all PWM techniques for variable-frequency power electronic application. Its merits simply listed as follow: it is particularly designed to work with voltage command in reference DQ0 frame; it increases available DC voltage by 15% which can be obtained by SPWM; its total harmonic distortion (THD), usually, is less than other strategies under the same condition; last but most important, in the three-level NPC converter, it could control the neutral point current to guarantee the voltages across two capacitors are balanced, which is difficult for other PWM strategies.

3.1 Three-level NPC Space Vector Pulse Width Modulation Strategy

The topology of three phase converter is showed in figure 3.1. In the figure, the DC link capacitors C_1 and C_2, which are in series, split the DC voltage U_d to create the neutral point O. P and Q are the positive and negative terminal of the DC source. The voltages across capacitor C_1 and C_2 are equal to $U_d/2$. The neutral point O is connected to all three phases AC though two clamped diodes as showed in figure 3.1.

Now let's take phase A as an example to illustrate the three-level NPC SVM strategy. Phase A includes the following components: 4 power switches (IGBTs) T_1, T_2, T_3, T_4, 4 anti-parallel diodes D_1, D_2, D_3, D_4 for current flow continuously, 2 clamped diodes D_5, D_6 for current flowing to neutral point and preventing short circuit of capacitors. N is the neutral point of the load.

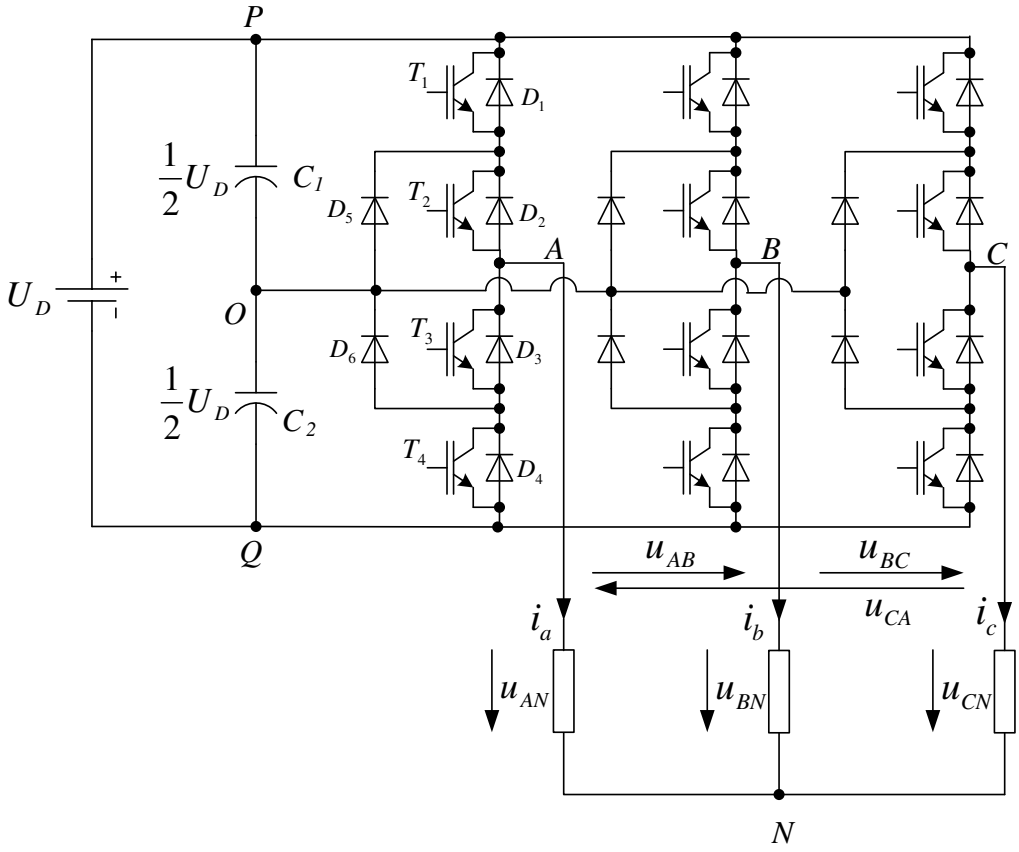


Figure 3- 1 Three-level converter topology

Similar to three-phase two-level SVM, there are switching states in three-level SVM which are S_a, S_b, S_c for each phase bridge respectively. Compared to only 2 switching states (0 and 1) in two-level SVM for each phase, there are three states which are 2, 1 and 0 in three-level SVM. Details about the states are explained as follow:

Let's still take phase A as an example. If T_1 and T_2 are turned off, T_3 and T_4 are turned on. The voltage between point A and O is $V_{AO} = -\frac{1}{2}U_D$. Under this condition, T_4 or D_4 is conducting, while the D_6 prevents C_2 from being short circuited. If the i_a is positive, the current flows from Q to A through D_3 and D_4; on the other hand, if the i_a is negative, the current flows from Q to A through T_3 and T_4. Therefore, regardless of whether i_a is positive or negative, phase A is connected to Q. This state is defined as S_a=0.

If T_1 and T_2 are turned on, T_3 and T_4 are turned off, this state is defined as S_a=2. Under this condition, $V_{AO} = \frac{1}{2}U_D$.

Another state is defined as S_a=1 which means T_2 and T_3 are turned on, while T_1 and T_4 are turned off. Under this condition, if the i_a is positive, the current flows from O to A though D_5 and T_2; on the other hand, if the i_a is negative, the current flows from O to A though T_3 and D_6. Therefore, no matter i_a is positive or negative, phase A is connected to O. The Voltage between point A and O is V_{AO}=0.

We could obtain phase B and C switching states in the same method.

Therefore, there are three different states 2, 1, 0 for each phase in the three-level SVM. So it has in total 3^3=27 switching states compared to 2^3=8 switching states in two-level SVM. The 27 states of three-level SVM make 19 various voltage vectors which are shown in figure 3-2. There are four kinds of voltage vectors [19]: zero vector V_0(000, 111, 222), small vector V_1 to V_6 (100, 211, 110, etc), middle vector V_7 to V_{12} (210, 120, 021, etc), and large vector V_{13} to V_{18} (200, 220, 020, etc). The zero vector has three redundant states (000, 111, 222). The small vector has two redundant states (for example, V_1 has 211 and 110)

The entire vector space [20] in figure 3-2 is divided into 24 triangle sections (D1 to D24) by dash-line. There are 6 areas (I to VI) divided by bold lines. Each area includes 4 triangle sections.

The essence of the SVM is to compound the command voltage vector V^* using the nearest three vectors in which triangle section the V* locates. After V_d^* and V_q^* are calculated by the control loop, the magnitude and position of V^*, which are $|V^*|$ and θ, can be obtained by complex method. Let $V^* = |V^*| \angle \theta$, so $V^* = V_d^* + j*V_q^*$, and θ= angle (V^*).

The definition of modulation index is

$$m = \frac{|V^*|}{\frac{2}{3}U_D} = \frac{3|V^*|}{2U_D} \tag{3-1}$$

$\frac{2}{3}U_D$ is the magnitude of large vector in figure (3-2).

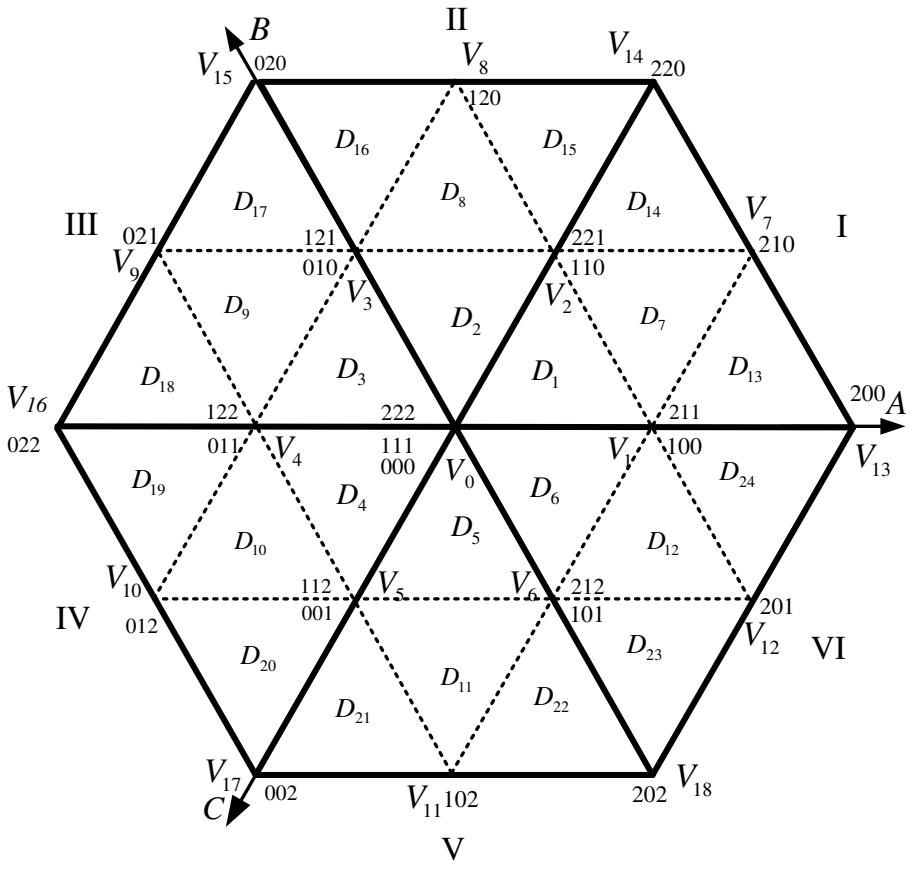


Figure 3- 2 Three level SVM voltage vectors

The command voltage V* is rotating in the stationary α-β frame [2] in figure 3-2. It is made up by three voltage vector V_x, V_y, V_z, which are from the section V* locates at the moment. The operation time of V_x, V_y, V_z are T_x, T_y, T_z respectively. The switching cycle time $T_s = T_x + T_y + T_z$. The unit of T_s is second, for example, if T_s=0.5e-3 (s), it means the switching frequency of the NPC rectifier is $1/T_s$ = 2 kHz. We have this further definition

$$X = \frac{T_x}{T_s}, \quad Y = \frac{T_y}{T_s}, \quad Z = \frac{T_z}{T_s} \tag{3-2}$$

Let's take Area I ($0 < \theta < \pi/3$) as example to discuss the details of how to calculate T_x, T_y and T_z. Firstly, we need solve which triangle section the V^* locates. So the boundary of each section needs to be marked in modulation index m shown in figure 3-3.

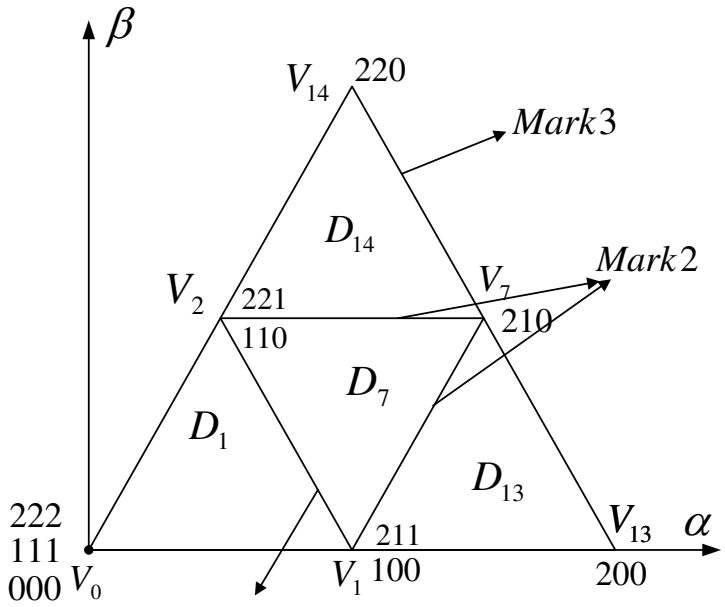


Figure 3- 3 Mark of sections when Command V* in area I

$$Mark1 = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta + \sin\theta} \tag{3-3}$$

$$Mark2 = \begin{cases} \dfrac{\sqrt{3}/2}{\sqrt{3}\cos\theta - \sin\theta}, \theta \le \dfrac{\pi}{6} \\ \dfrac{\sqrt{3}/4}{\sin\theta}, \dfrac{\pi}{6} < \theta \le \dfrac{\pi}{3} \end{cases} \tag{3-4}$$

$$Mark3 = \frac{\sqrt{3}}{\sqrt{3}\cos\theta + \sin\theta} \tag{3-5}$$

Then we have the following four conditions depending on which section V^* locates (D_1, D_7, D_{13} or D_{14})

(a) When the modulation index m < Mark1, the V^* locates in section D_1. V^* is made by V_1, V_2 and V_0 which showed in figure 3-4. So V_1, V_2, V_0 represent V_x, V_y, V_z in equation (3-2). From equation we know that X+Y+Z=1. Base on the orthogonal decomposition of m, X, Y and Z in figure 3-4, the following equation is obtained:

$$\begin{cases} \frac{1}{2}X + \frac{1}{2}\cos\left(\frac{\pi}{3}\right)\cdot Y = m\cdot\cos(\theta) \\ \frac{1}{2}\sin\left(\frac{\pi}{3}\right)\cdot Y = m\cdot\sin(\theta) \\ X + Y + Z = 1 \end{cases} \tag{3.6}$$

in which θ is the angle of command voltage V^*.

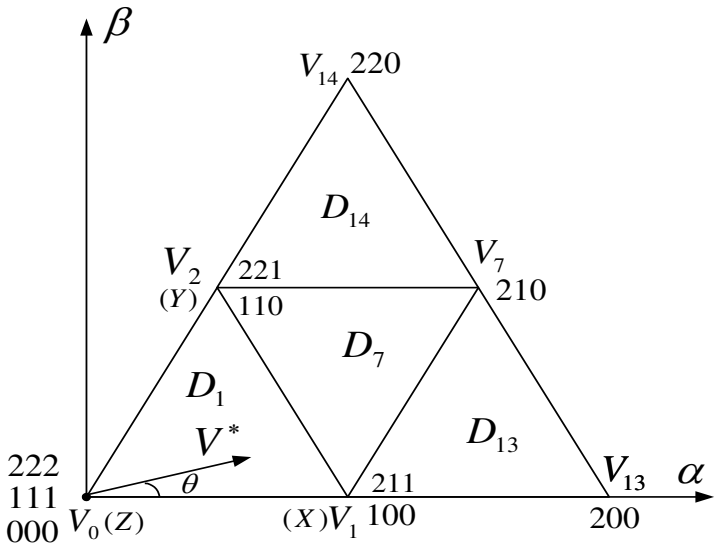


Figure 3- 4: Command voltage V^* in section D_1

From equation (3-6), we could obtain the solution:

$$\begin{cases} X = 2m\cdot\left[\cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}}\right] \\ Y = m\cdot\frac{4\sin(\theta)}{\sqrt{3}} \\ Z = 1 - 2m\cdot\left[\cos(\theta) + \frac{\sin(\theta)}{\sqrt{3}}\right] \end{cases} \tag{3-7}$$

Combine the equation (3-2) and (3-7) we could derive the operation time T_x, T_y, T_z for V_x, V_y, V_z in D_1 as follow:

$$\begin{cases} T_x = \left(2m\cdot\left[\cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \\ T_y = \left(m\cdot\frac{4\sin(\theta)}{\sqrt{3}}\right)\cdot T_s \\ T_z = \left(1 - 2m\cdot\left[\cos(\theta) + \frac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \end{cases} \tag{3-8}$$

(b) When the modulation index: Mark1 < m < Mark2, the V^* locates in section D_7. V^* is made by V_1, V_2 and V_7 which showed in figure 3-5. So V_1, V_2, V_7 represent V_x, V_y, V_z in equation (3-2). Similar to equation (3-6), the following equation is obtained:

$$\begin{cases} \frac{1}{2}X + \frac{1}{2}\cos\left(\frac{\pi}{3}\right)\cdot Y + \cos\left(\frac{\pi}{6}\right)\cdot\cos\left(\frac{\pi}{6}\right)\cdot Z = m\cdot\cos(\theta) \\ \frac{1}{2}\sin\left(\frac{\pi}{3}\right)\cdot Y + \cos\left(\frac{\pi}{6}\right)\cdot\sin\left(\frac{\pi}{6}\right)\cdot Z = m\cdot\sin(\theta) \\ X + Y + Z = 1 \end{cases} \tag{3-9}$$

Combine the equation (3-2) and (3-9) we could derive the operation time T_x, T_y, T_z for V_x, V_y, V_z in D_7 as follow:

$$\begin{cases} T_x = \left(1 - m\cdot\frac{4\sin(\theta)}{\sqrt{3}}\right)\cdot T_s \\ T_y = \left(1 - 2m\cdot\left[\cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \\ T_z = \left(-1 + 2m\cdot\left[\cos(\theta) + \frac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \end{cases} \tag{3-10}$$

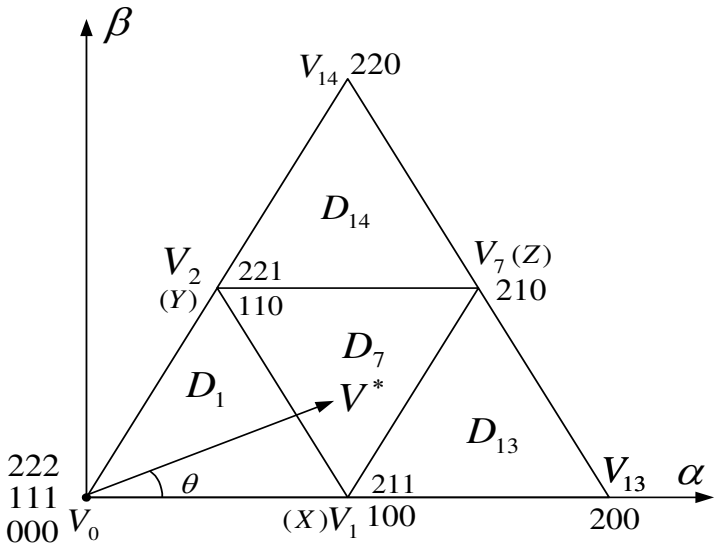


Figure 3- 5 Command voltage V^* in section D_7

(c) When the modulation index: Mark2 < m < Mark3 and the angle $\theta < \pi/6$, the V^* locates in section D_{13}. V^* is made by V_{13}, V_7 and V_1 which showed in figure 3-6. So V_{13}, V_7, V_1 represent V_x, V_y, V_z in equation (3-2). Similar to equation (3-6), the following equation is obtained:

$$\begin{cases} X+\cos\left(\dfrac{\pi}{6}\right)\cdot\cos\left(\dfrac{\pi}{6}\right)\cdot Y+\dfrac{1}{2}Z=m\cdot\cos(\theta) \\ \cos\left(\dfrac{\pi}{6}\right)\cdot\sin\left(\dfrac{\pi}{6}\right)\cdot Y=m\cdot\sin(\theta) \\ X+Y+Z=1 \end{cases} \tag{3-11}$$

Combine the equation (3-2) and (3-11) we could derive the operation time T_x, T_y, T_z for V_x, V_y, V_z in D_{13} as follow:

$$\begin{cases} T_x=\left(-1+2m\cdot\left[\cos(\theta)-\dfrac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \\ T_y=\left(m\cdot\dfrac{4\sin(\theta)}{\sqrt{3}}\right)\cdot T_s \\ T_z=\left(2-2m\cdot\left[\cos(\theta)+\dfrac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \end{cases} \tag{3-12}$$

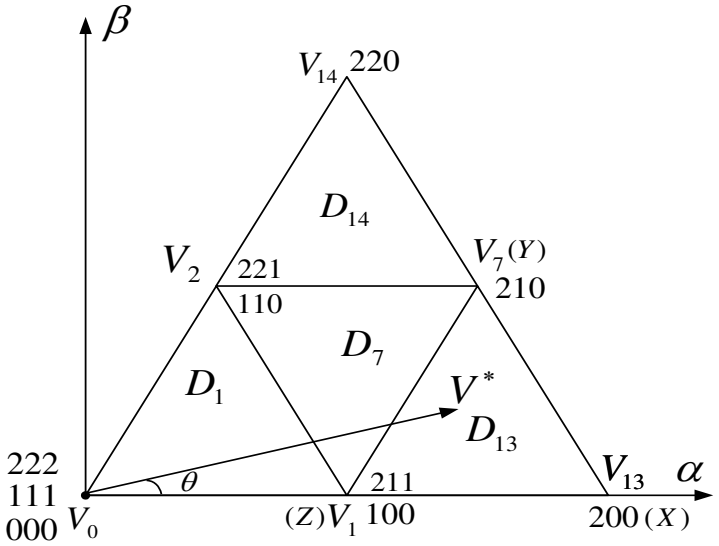


Figure 3- 6 Command voltage V^* in section D_{13}

(d) When the modulation index: Mark2 < m < Mark3 and the angle: $\pi/6 < \theta < \pi/3$, the V^* locates in section D_{14}. V^* is made by V_7, V_{14} and V_2 which showed in figure 3-7. So V_7, V_{14}, V_2 represent V_x, V_y, V_z in equation (3.2). Similar to equation (3.6), the following equation is obtained:

$$\begin{cases} \frac{\sqrt{3}}{2}\cos\left(\frac{\pi}{6}\right)\cdot X+\cos\left(\frac{\pi}{3}\right)\cdot Y+\frac{1}{2}\cos\left(\frac{\pi}{3}\right)\cdot Z=m\cdot\cos(\theta) \\ \frac{\sqrt{3}}{2}\sin\left(\frac{\pi}{6}\right)\cdot X+\sin\left(\frac{\pi}{3}\right)\cdot Y+\frac{1}{2}\sin\left(\frac{\pi}{3}\right)\cdot Z=m\cdot\sin(\theta) \\ X+Y+Z=1 \end{cases} \tag{3-13}$$

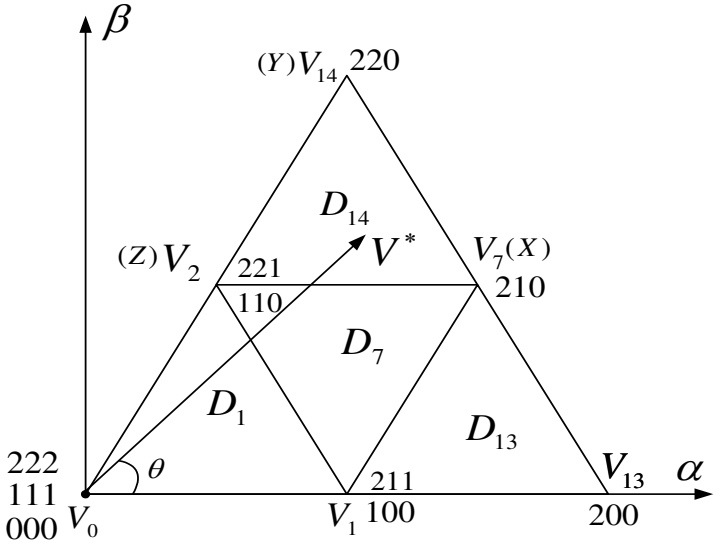


Figure 3- 7 Command voltage V^* in section D_{14}

Combine the equation (3.2) and (3.11) we could derive the operation time T_x, T_y, T_z for V_x, V_y, V_z as follow:

$$\begin{cases} T_x=\left(2m\cdot\left[\cos(\theta)-\frac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \\ T_y=\left(-1+m\cdot\frac{4\sin(\theta)}{\sqrt{3}}\right)\cdot T_s \\ T_z=\left(2-2m\cdot\left[\cos(\theta)+\frac{\sin(\theta)}{\sqrt{3}}\right]\right)\cdot T_s \end{cases} \tag{3-14}$$

So far, SVM strategy of all sections, which are in area I, has been completed. Switching period calculations for other five areas (II to VI) is quite similar. When command voltage V^* is in area II to VI, we need replace the angle θ in the area I to θ-π/3, θ-2π/3, θ-π, θ-4π/3, θ-5π/3 which are in areas II, III, IV,V, VI, respectively.

If the modulation index m is bigger than the outer boundary of figure 3-2, it is given the term over-modulation [12]. In this case, the command voltage magnitude $|V^*|$ can not

be achieved. Restriction and limitation on $|V^*|$ should been given before switching period calculation of SVM.

The sequence of switching states V_x, V_y, V_z in one switching cycle is important because it affects the THD and switching loss during the SVM [5]. Nowadays, in order to reduce the THD and switching loss, it is popular to (1) make the switching cycle symmetric; (2) to begin and end the cycle with the same switching state; (3) there is only one state change at a time. The switching states of S_a, S_b and S_c waveforms are illustrated in figure 3-8.

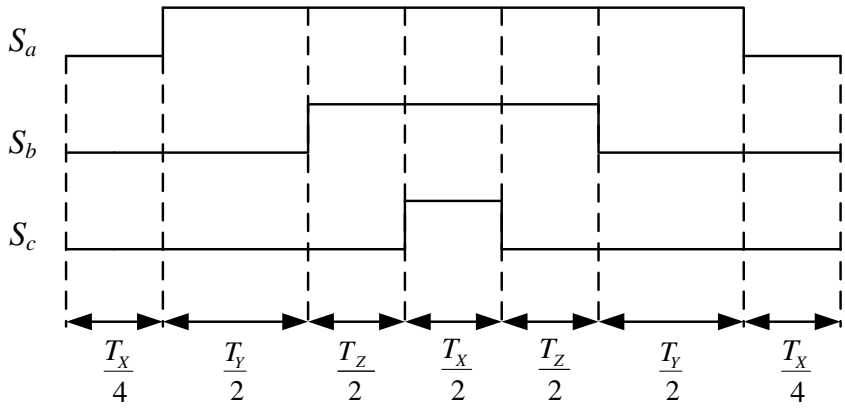


Figure 3- 8 Sequence of switching states

3.2 Bang-Bang Neutral Point Voltage Control

The three-level NPC converter attracts more and more attention from power electronic engineers due to its lower THD, and lower voltage pressure on each switch compared to the two-level converter. But the voltage V_{dc1} and V_{dc2} across the two capacitors C_d in figure 3-9 are not always equal [11][20]. If they are not equal, the voltages which connect to the ideally SPTT switches are not $+U_d/2$, 0, $+U_d/2$ anymore, in this case, the NPC loses its advantage or even causes certain accident.

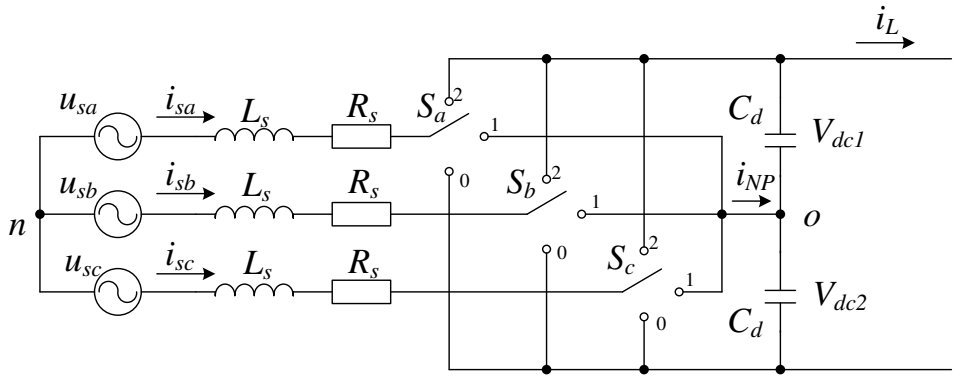


Figure 3- 9 Neutral point voltage control in three-level NPC converter

The voltage difference between V_{dc1} and V_{dc2} is defined as $\Delta V = V_{dc1} - V_{dc2}$. From figure 3-9, the ΔV is affected by neutral point current i_{NP} and the capacitor value C_d.

$$\Delta V = \frac{i_{NP}}{2C_d} \tag{3-15}$$

Since the capacitor value C_d is constant when the system operates. The only way to control ΔV in (3-15) is to control the neutral point current i_{NP}. As showed in figure 3-9, if i_{NP} is positive, ΔV will increase; analogously, if i_{NP} is negative, ΔV will decrease. After further analyze, we find that different switching states cause different direction of i_{NP}. Take state (211) as an example, when S_a connects to point P, both S_b and S_c connect to neutral point O. Therefore, the neutral point current $i_{NP} = i_{sb} + i_{sc}$. We have $i_{sa} + i_{sb} + i_{sc} = 0$. Then $i_{NP} = -i_{sa}$ when switching state is (211). For other switching states, the i_{NP} values and voltage types are showed in the following table.

From Table 3-1 we find:

(a) Zero vector and large vector don't affect the neutral point current i_{NP}.

(b) For each voltage vector V_1 to V_6, there are two redundant small vectors correspond to it. For example, S_4 and S_{10} correspond to V_1. Additionally, the sign of i_{NP} produced by the two redundant small vectors is opposite to each other. S_4 matches for i_{sa}, but S_{10} matches for $-i_{sa}$. Therefore, redundant small vector characteristics allow us to control ΔV by choosing sign of i_{NP}.

(c) Middle vectors affect the neutral point current i_{NP}, but there is no redundant vector, so we couldn't actively choose the sign of i_{NP} by middle vectors.

Table 3- 1 Each switching state affects neutral point current i_{NP}

Switching State	S_a S_b S_c	Voltage vector	i_{NP}	Vector type
S_1	000	V_0	0	Zero vector
S_2	111	V_0	0	Zero vector
S_3	222	V_0	0	Zero vector
S_4	100	V_1	i_{sa}	Small vector
S_5	110	V_2	$-i_{sc}$	Small vector
S_6	010	V_3	i_{sb}	Small vector
S_7	011	V_4	$-i_{sa}$	Small vector
S_8	001	V_5	i_{sc}	Small vector
S_9	101	V_6	$-i_{sb}$	Small vector
S_{10}	211	V_1	$-i_{sa}$	Small vector
S_{11}	221	V_2	i_{sc}	Small vector
S_{12}	121	V_3	$-i_{sb}$	Small vector
S_{13}	122	V_4	i_{sa}	Small vector
S_{14}	112	V_5	$-i_{sc}$	Small vector
S_{15}	212	V_6	i_{sb}	Small vector
S_{16}	210	V_7	i_{sb}	Middle vector
S_{17}	120	V_8	i_{sa}	Middle vector
S_{18}	021	V_9	i_{sc}	Middle vector
S_{19}	012	V_{10}	i_{sb}	Middle vector
S_{20}	102	V_{11}	i_{sa}	Middle vector
S_{21}	201	V_{12}	i_{sc}	Middle vector
S_{22}	200	V_{13}	0	Large vector
S_{23}	220	V_{14}	0	Large vector
S_{24}	020	V_{15}	0	Large vector
S_{25}	022	V_{16}	0	Large vector
S_{26}	002	V_{17}	0	Large vector
S_{27}	202	V_{18}	0	Large vector

In conclusion, in order to ensure V_{dc1} and V_{dc2} to be equal, we could choose the corresponding small vector to control the neutral point current $i_{NP.}$

After analyzing the reason of the unbalanced ΔV (i_{NP}) and how different state vectors affect i_{NP}, the bang-bang neutral point voltage control is discussed here: This is a relatively easy, but robust and also most prevalent strategy recently. It only requires the sign (positive or negative) of ΔV and the signs of input AC currents, instead of precise

values of ΔV, input AC currents. The ΔV could be control within a small ripple area around zero.

When coding the SVM for NPC converter to control the neutral point voltage, through choosing or abandoning certain small vector in the switching cycle, controlling of i_{NP}'s direction can be achieved. Section D_7 in area I is took as an example, which is showed in figure 3-10, to illustrate the details of this strategy. In this section, the command voltage space vector V^* is made by small vector V_1, V_2 and middle vector V_7. Since there is no redundant vector for middle vector (only S_{17}), we can not choose the sign of i_{NP} by middle vector. But for the small vectors V_1 and V_2, redundant vectors are available, S_4 (100) and S_{10} (211) for V_1, and S_5 (110) and S_{11} (221) for V_2. From table 3-1 we know the i_{NP} corresponds to S_4 is i_{sa}; i_{NP} corresponds to S_{10} is $-i_{sa}$. If the direction of i_{sa} is known, we could choose S_4 and abandon S_{10} to increase ΔV, or choose S_{10} and abandon S_4 to decrease ΔV.

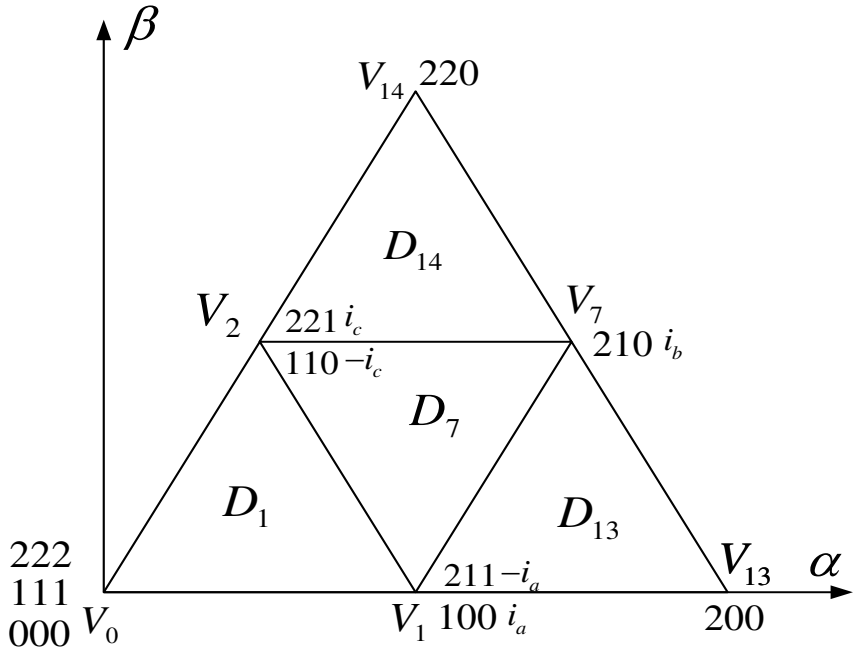


Figure 3- 10 Choosing small vector in bang-bang control for D_7

By considering the symmetric vector sequence method mentioned in figure 3-8 to prevent more than one switch changing at the same time, we could achieve a basic switching state sequence for D_7 as follows: $S_{11}(221)\rightarrow S_{10}(211)\rightarrow S_{16}(210)\rightarrow$

$S_5(110)\rightarrow S_4(100)\rightarrow S_4(100)\rightarrow S_5(110)\rightarrow S_{16}(210)\rightarrow S_{10}(211)\rightarrow S_{11}(221)$. In this sequence, all the vectors in this section are included. For convenience and reduction of the switching losses when section changes take place (for example from D_7 to D_{14} we don't want more than one IGBT switches), only $S_{11}(221)$ and $S_4(100)$ are considered to be retained or abandoned. Then we analyze the different scenarios as follow:

(1) When error $\Delta V \geq 0$, there are four different scenarios:

a) When $i_{sc} \geq 0$, $i_{sa} \geq 0$. $S_{11}(221)$ corresponds i_{sc}, $S_4(100)$ corresponds $i_{sa,}$ both states could inject positive current i_{NP} to neutral point to the reduce the ΔV. Therefore, both S_{11} and S_4 should not be abandoned. The SVM sequence remains $S_{11}(221)\rightarrow S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_4(100)\rightarrow S_4(100)\rightarrow S_5(110)\rightarrow S_{16}(210)\rightarrow S_{10}(211)\rightarrow S_{11}(221)$.

For reader's convenience, the SVM sequence is plotted in figure 3-11.

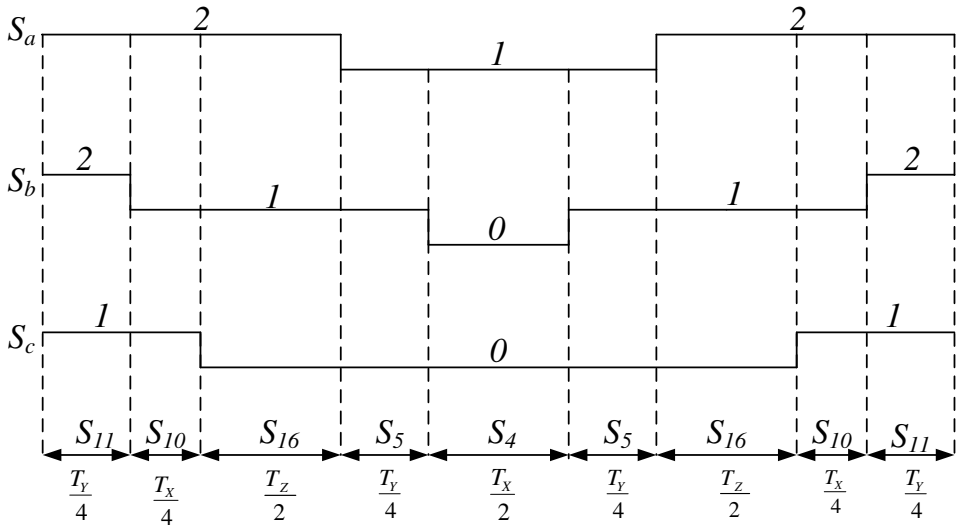


Figure 3- 11 SVM strategy in D_7 when $\Delta V \geq 0$, $i_{sc} \geq 0$, $i_{sa} \geq 0$

b) When $i_{sc} \geq 0$, $i_{sa} < 0$. $S_{11}(221)$ corresponds i_{sc}, which could inject positive current i_{NP} to neutral point to reduce the ΔV. Therefore, S_{11} should not be abandoned. $S_4(100)$ corresponds $i_{sa,}$ which injects negative current i_{NP} to neutral point to further increase the error ΔV. Therefore, S_4 should be abandoned. The SVM sequence in this scenario is: $S_{11}(221)\rightarrow S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_5(110)\rightarrow S_{16}(210)\rightarrow S_{10}(211)\rightarrow S_{11}(221)$.

c) When $i_{sc} < 0$, $i_{sa} \geq 0$. $S_{11}(221)$ corresponds $i_{sc,}$ which injects negative current i_{NP} to neutral point which further increases the ΔV. Therefore, S_{11} should be abandoned.

$S_4(100)$ corresponds $i_{sa,}$ which injects positive current i_{NP} to neutral point to reduce the error ΔV. Therefore, S_4 should not be abandoned. The SVM sequence in this scenario is:

$S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_4(100)\rightarrow S_4(100)\rightarrow S_5(110)\rightarrow S_{16}(210)\rightarrow S_{10}(211)$

d) When $i_{sc} < 0$, $i_{sa} < 0$. S_{11} (221) corresponds i_{sc}, S_4 (100) corresponds $i_{sa,}$ both states inject negative current i_{NP} to neutral point which further increase the error ΔV. Therefore, both S_{11} and S_4 should be abandoned. The SVM sequence in this scenario is: $S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_5(110)\rightarrow S_{16}(210) \rightarrow S_{10}(211)$.

(2) Similarly, when error $\Delta V< 0$, there are four different scenarios as well. We only show the result as follow:

a) When $i_{sc} \geq 0$, $i_{sa} \geq 0$. The SVM sequence is:
$S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_5(110)\rightarrow S_{16}(210) \rightarrow S_{10}(211)$. We find this is identical to when $\Delta V \geq 0$ the scenario (d).

b) When $i_{sc} < 0$, $i_{sa} \geq 0$. The SVM sequence is:
$S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_4(100)\rightarrow S_4(100)\rightarrow S_5(110)\rightarrow S_{16}(210)\rightarrow S_{10}(211)$. We find this is identical to when $\Delta V \geq 0$ the scenario (c).

c) When $i_{sc} \geq 0$, $i_{sa} < 0$. The SVM sequence is:
$S_{11}(221)\rightarrow S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_4(100)\rightarrow S_4(100)\rightarrow S_5(110)$
$\rightarrow S_{16}(210)\rightarrow S_{10}(211)\rightarrow S_{11}(221)$. We find this is identical to when $\Delta V \geq 0$ the scenario (b).

d) When $i_{sc} \geq 0$, $i_{sa} \geq 0$. The SVM sequence is:
$S_{11}(221)\rightarrow S_{10}(211)\rightarrow S_{16}(210)\rightarrow S_5(110)\rightarrow S_4(100)\rightarrow S_4(100)\rightarrow S_5(110)\rightarrow S_{16}(210)$
$\rightarrow S_{10}(211)\rightarrow S_{11}(221)$. We find this is identical to when $\Delta V \geq 0$ the scenario (a).

The SVM sequences for other sections could be obtained in a similar fashion. Appendix A shows the details about the three-level SVM sequence in all sections with bang-bang neutral point voltage control.

CHAPTER 4

NPC RECTIFIER CONTROL

Nowadays, it's popular for PWM rectifier using double close loop control which includes inner current loops and an outer voltage loop since it has many advantages: physical meaning is clear (for example, active current and reactive current in inner current loop); control structure is relatively simple; good dynamic respond to the command, etc. Inner current loop is helpful to protect power electronics devices because it could limit the current magnitude within a safe range.

As showed in figure 2-3, the active current i_{sd} and reactive current i_{sq} in the NPC rectifier model of DQ0 reference frame is heavily coupled. Similar decouple methodology of AC machine drive [2] control to decouple the inner current loops of NPC rectifier is used here to control the i_{sd} and i_{sq} separately [21].

In the control loop of the NPC rectifier, there are three Proportional–integral (PI) controller. A PI controller is very commonly used feedback controller because there is no steady state error. The system with PI controller responds fast to commands if the controller gains tunings are appropriately set[14]. P and I value can be interpreted in terms of present error and accumulation of past error, respectively.

There are a couple of methods to tune the PI controller. Firstly, in this chapter, based on the transfer function, the conventional Nicholson Ziegler method of tuning a PI controller is presented.

Compared to the conventional Nicholson Ziegler method, a new method of tuning the PI controller by Particle Swarm Optimization (PSO) is illustrated in a subsequent chapter.

4.1 Double Close Loop Control for NPC Rectifier

The double closed-loop control design in DQ0 reference frame is based on the equations (2-18) to (2-19). The target is to control active current i_{ds} and reactive current i_{qs} separately just like direct current (DC) motor or field oriented control (FOC) of an induction motor. As showed in (2-12), i_{ds} and i_{qs} are coupled with other components,

without decoupling, the stress in the PI controller is tremendous and the system dynamic responds is far from engineers' satisfaction. The grid voltage are supposed to remain constant, the most effective way to control the NPC rectifier output voltage and unity power factor is to control the currents i_{ds} and i_{qs}.

Though current PI controller, the active and reactive command voltages [5], which are in reference DQ0 frame, V_d^* and V_q^* are calculated separately with decouple components in (4-1) and figure 4-1.

$$\begin{cases} V_d^* = -(k_{dp} + \dfrac{k_{di}}{s})(i_d^* - i_{sd}) + \omega L i_{sq} + u_{sd} \\ V_q^* = -(k_{qp} + \dfrac{k_{qi}}{s})(i_q^* - i_{sq}) - \omega L i_{sd} + u_{sq} \end{cases} \tag{4-1}$$

k_{dp}, k_{di}, k_{qp}, k_{qi} are proportional gain and integral gain in active current control loop, and proportional gain and integral gain in reactive current control loop, respectively.

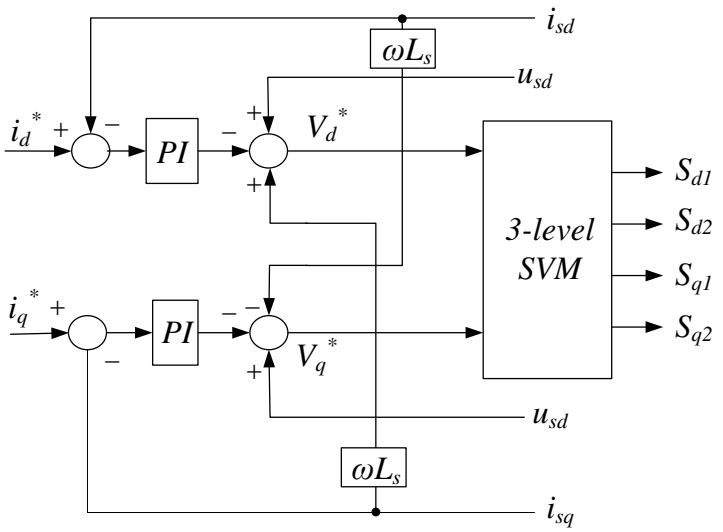
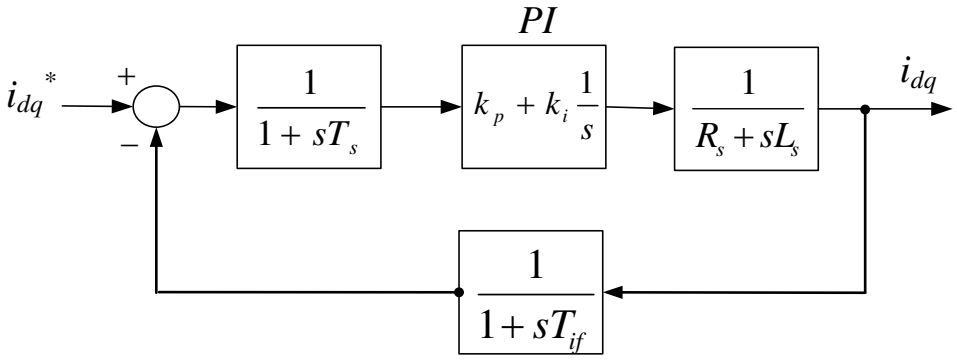


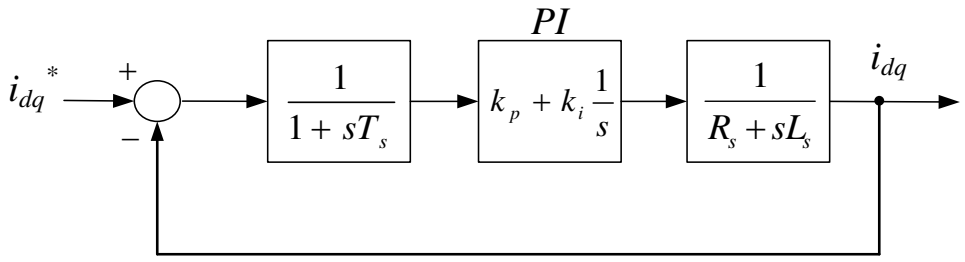
Figure4- 1 Coupled inner current control loop

4.2 Tuning NPC Rectifier PI controller by Nichols and Ziegler rules

In order to obtain PI gains by MATLAB, it requires the system SISO (single input single output) transfer function. The simplified inner current control transfer function block diagram could be obtained as figure 4-2 (a) from a combination of control loop of figure 4-1 and math model of the NPC rectifier circuit which showed in figure 2-3.



(a)



(b)

Figure4- 2 Inner current control loop

T_s is PWM switching period. $\frac{1}{1+sT_s}$ is the delay of sampling and DSP calculation. T_{if} is the sensor sampling time. Combining the two delays $\frac{1}{1+sT_s}$ and $\frac{1}{1+sT_{if}}$ into one, a further simplified transfer function block of current control is showed in figure 4-2 (b), where $T_e = T_{if} + T_s$.

The process of selecting the controller parameters to meet given performance specifications is known as controller tuning. Since 1942, developed by John G. Ziegler and Nathaniel B. Nichols, the Nichols and Ziegler rules for tuning PID controllers are popular among engineers. These methods are performed by setting the integral gain and derivative gain to zero. The proportional gain, k_p is then increased (from zero) until it reaches the ultimate gain K_u, at which point the output of the control loop oscillates with a constant amplitude. K_u and the oscillation period T_u are used to set the P, I, and D gains depending on the type of controller used.

In the MATLAB toolboxes, SISO design tool could be used for obtaining the PI gain value in figure 4-2 by the Nichols and Ziegler rules. Given the system parameters

shown in table 4-1, based on Nichols and Ziegler rules, the tuning results of PI gain in current loop are: k_p=8.4, k_i=442. With the help of SISO design tool, the step response of inner current loop with PI controller is showed in figure 4-3.

Table 4- 1 NPC rectifier system parameters

Line resistance R_s	0.3 Ω
Line inductance L_s	5 mH
Switching period T_s	0.5e-3 s
DC capacitor C_d	5 mF
Resistor load R_L	100 Ω
Grid AC line to neutral peak voltage V_{as}	30 V
Grid AC frequency	60 Hz

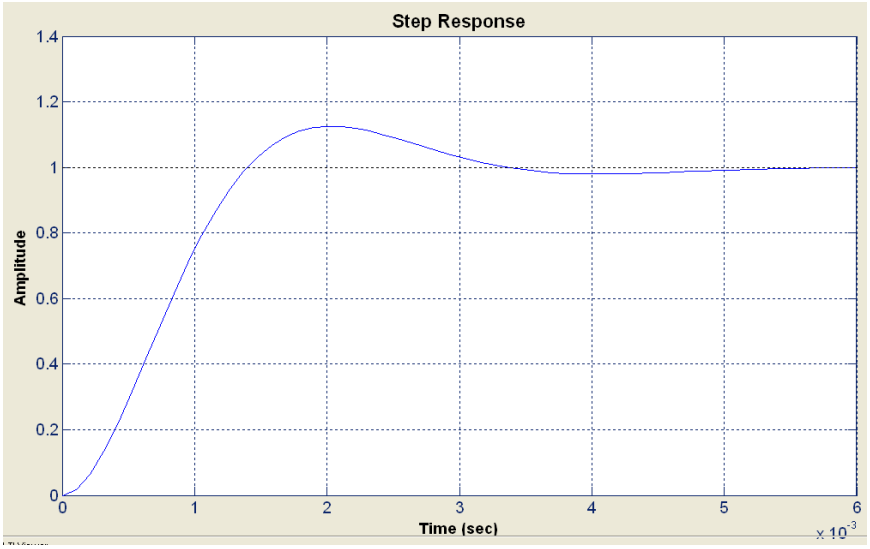


Figure4- 3 Step response of inner current loop with PI compensator

Nichols and Ziegler rules are used for tuning the NPC rectifier outer voltage control loop PI gain as well. In order to achieve the SISO transfer function of NPC rectifier voltage control loop, we have further simplifications as following: (1) The relationship between i_{sq} and output DC voltage is showed in equation (2-3). Since in steady state, the reactive current i_{sq} suppose to remain as command i_q^*=0, the affect of i_q in voltage control loop is omitted. (2) Because the inner current loop response is much faster than the outer voltage loop, so the active current loop is simplified to a small delay $C(s)=\frac{1}{1+0.005s}$ in voltage transfer function block. (3) The load in the system is a constant resistive load R_L=100 Ω for design convenience. (4) S_{d1} and S_{d2} values are constant which come from

steady state. Therefore, from combination of control loop of figure 4-1 and math model of NPC rectifier circuit which showed in figure 2-3, the transfer function block diagram of outer voltage loop could be obtained as figure 4-4.

The capacitor value C_d is 5 mF from table 4-1. By using the same Nichols and Ziegler tuning algorithm of current control loop, the MATLAB SISO design tool produces the PI gains in voltage control loop: k_p=1, k_i=9.1. Readers could check the step response of the voltage control loop with SISO design tool as figure 4-3.

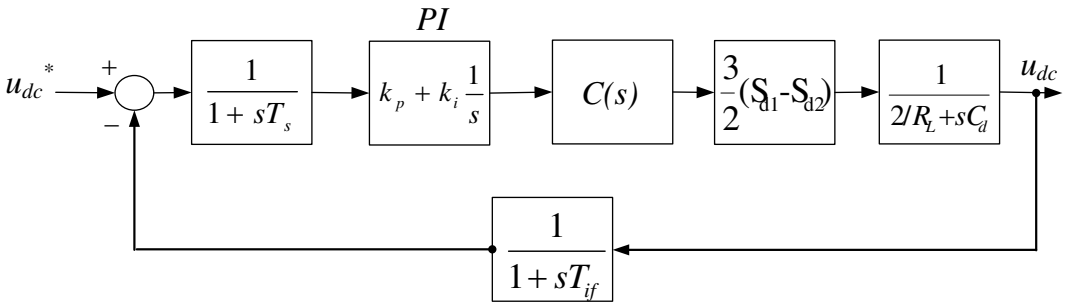


Figure4- 4 Outer voltage control loop

4.3 Tuning NPC Rectifier PI controller by PSO

As showed in the previous section, tuning PI controllers by Nichols and Ziegler rules, many aspects of NPC rectifier are omitted and the system is simplified to a transfer function block. Although the performance of the NPC rectifier system with the PI controller which tuned by Nichols and Ziegler rules is good, it could be improved by other more advanced tuning algorithm. In this subsection, Particle Swarm Optimization (PSO) is showed to further optimize PI controller parameters in NPC rectifier and the process is explained in detail.

4.3.1 Introduction of PSO

Particle Swarm Optimization (PSO) is an optimization technique which is modeled after the flocking behavior of birds or swarming locusts to stochastically approach the local optimum of a function [16]. Proposed in 1995, this technique has found application in several areas, which include power electronics [22], due mainly to its ease of implementation and its resistance to local optimal traps. Since its introduction, the

original PSO has undergone modifications aimed at obtaining a good balance between exploitation and exploration of the solution space so that the algorithm is able to avoid local optimal locations while approaching the global best location faster.

Particle Swarm Optimization (PSO) proceeds by randomly choosing a set of solutions called particles. Each particle is ranked by a suitably chosen cost function, which is an indication of its suitability as the optimal solution of the optimization problem. The cost function depends on the problem at hand. In the case of filter application and function approximation applications, the cost function is the squared deviation from an expected value. If the application at hand is function optimization, then cost function is the function value at the particle location and the local optima is the optimal function value within the range of allowable particle locations. In the original PSO algorithm, the global best particle position is adjusted based only on its initial velocity. Modifications to this algorithm employ an inertia factor to enable the global best particle to explore other locations of the solution space. Other modifications have been employed to increase the depth of penetration of particles into the solution space. Classical unconstrained optimization methods depend on a type of gradient descent implementation. These techniques are inherently limited to finding only local optimal solutions very fast. PSO by its nature can be adapted to avoid local optimal solution; if the algorithm is allowed to run for a long time, it is possible to obtain a good approximation to the global best location. Each particle is then adjusted by (4-2).

$$\begin{aligned} V_i(k+1) &= W(k)V_i(k) + c_1 \times rand(0,1)(gbest(k)) + c_2 \times rand(0,1)(pbest_i(k)) \\ X_i(k+1) &= X_i(k) + V_i(k+1) \end{aligned} \tag{4-2}$$

In (4-2), $V_i(k)$ is described as the velocity of particle i at time k, $X_i(k)$ is particle i location at time k, $W(k)$ is the inertia weight of the system at time k, *gbest* is the global best particle location, $pbest_i$ is the personal best location of the particle under consideration and rand(0,1) are randomly generated numbers that could come from a normal distribution or uniform distribution. The inertia weight, W, is implemented as (4-3)

$$W(k+1) = \left(\frac{2}{1 + \exp\left(\alpha \times \frac{i}{ITER} \right)} \right) \times W(k) \tag{4-3}$$

The initial values of W and α are set by a trial and error process. The weight is implemented to enable the particles to initially have large velocities to explore the solution space and to slow down and converged around the global best solution when the limit of the number of iterations is approached. c_1 and c_2 are the learning factors and can be adjusted to enable particles approach the global best solution with greater accuracy.

4.3.2 Tuning PI controller parameters using PSO

Nowadays, PSO is powerful tool for tuning PI controller parameters in power electronics system [23][24]. The process of tuning PI controller parameters for the NPC rectifier is showed in this sub-section. For readers better understanding what PSO could do. Let's begin from a very simple function in (4-4) as an example. Assume that the task is to find the maxim value of (4-4) in the range $x_1, x_2 \in [-10,10]$. At the beginning, PSO sets particles to randomly positions (X_1, X_2) in the range which showed in figure 4-5 just like a group of birds are randomly searching food in an area. The function values f(x_1, x_2) from every particle are recorded. Each particle is given two updated 'best' values in every iteration. One 'best' value is known as pbest which is the maximum value it has achieved so far. Another 'best' value which is tracked by the particle swarm optimizer is the maximum value, obtained so far by any particle in the population. This maximum value is a global best, 'gbest'. After finding the two best values, the particle updates its velocity and positions base on (4-2). With enough iteration, the best position (0.0015, 1) is fund and the maximum value of (4-6) is 2.0001.

$$f(x_1, x_2) = \frac{x_1 \cos(x_1)}{20} + 2e^{-x_1^2-(x_2-1)^2} + 0.01 x_1 x_2 \tag{4-4}$$

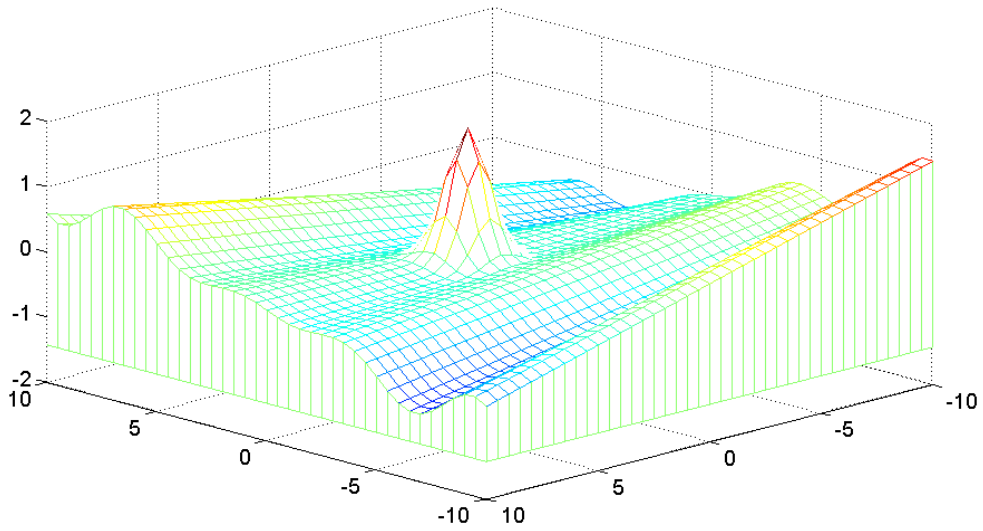


Figure4- 5 Three-dimension plot of (4-6)

In the NPC rectifier system, our target is to optimize the system respond to the command in terms of fast response and small overshoot. Therefore, the best values of NPC system is the minimum values of settling-time and overshoot which could be analyzed by MATLAB 'stepinfo' command. Similar methodology could be used as what had been done in function (4-6), but the math model of the NPC rectifier system is much more complicated than (4-6) which only has two parameters x_1 and x_2. There are 3 PI (outer voltage loop, inner active current loop, and inner reactive current loops) controllers in the NPC rectifier system control loop. There are one P gain and one I gain in each PI controller. In total, there are 6 control parameters needed to be optimized by PSO. The NPC rectifier math model (right side) and its control (left side) are showed in figure 4-6. In the PSO tuning process, the PSO code is built in MATLAB mdl file and sets particles with 6 parameters into the system. In every iteration, when the NPC rectifier system responds to the command output DC voltage, settling-time in units of seconds and the overshoot in units of percentage are stored for every particle. Similar to the optimization process in (4-4), the minimum value of the sum of settling-time and overshoot for each particle achieved so far is the 'pbest' value of the individual particle; the minimum value of the sum of settling-time and overshoot for any particle is 'gbest' value of the whole population. After one cycle, the particle's velocity updates using (4-2). Finally, the best value can converge to the optimized value and the related PI controller gains are obtained. The weight for settling-time and overshoot could be adjusted by designer's requiring. For

example, if overshoot is considered to be more important than settling-time, one could set overshoot take 80% of the total weight, so there is only 20% weight left for settling-time.

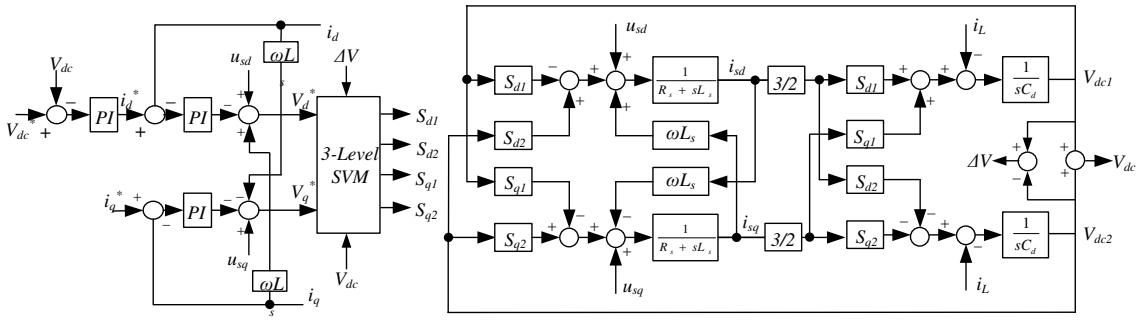


Figure4- 6 Math model of NPC rectifier and its control

The PSO code is written in MATLAB m-file which is show in Appendix B. With the system parameter in table 4-1, and the optimization function (4-5), the optimized PI controller gains are shown in table 4-2 and the data of the NPC rectifier performance is shown in subsection 6.3.

$$f(PI) = T_{set} + V_{ost}/10 \tag{4-5}$$

In (4-5) T_{set} is the settling-time of the NPC rectifier response to command, unit in second. V_{ost} is the output DC voltage overshoot response to voltage command, unit in volt. Reader could adjust the weight of T_{set} and V_{ost} by different emphases. For example, reader could replace (4-5) to $f(PI)' = T_{set} + V_{ost}/20$, when reducing overshoot is considered to be more important.

Table 4- 2 PI controller gains tuned by PSO based on (4-5)

k_{vp}	k_{vi}	K_{cp1}	K_{ci1}	K_{cp2}	K_{i2}
6.48	3.5	6.7	109	3.3	18

k_{vp}: proportional gain of outer voltage loop

k_{vi}: integral gain of outer voltage loop

k_{cp1}: proportional gain of inner active current loop

k_{ci1}: integral gain of inner active current loop

k_{cp2}: proportional gain of inner reactive current loop

k_{ci2}: integral gain of inner reactive current loop

CHAPTER 5

NPC RECTIFIER SIMULATION RESULT

Simulation tests could provide verification for the NPC rectifier system prior to real hardware experimentation. At the beginning of this chapter, a non-real-time simulation is showed in MATLAB/PLECS. Then a real-time simulation is tested with dSPACE and RTDS using Controller-Hardware-in-the-Loop (CHIL) methodology. CHIL could de-risk and debug the instantiation of the NPC rectifier from simulation test to real hardware test.

5.1 NPC Rectifier Non-real-time Simulation

The NPC rectifier main circuit in figure 2-1 is constructed in PLECS which is a third party power electronics block set for Simulink as showed in figure 5-1. Details about the simulation parameters are shown in table 4-1. The simulation process is explained as follows: 1) at 0 second, three phase switch closes and the NPC rectifier is in the diode-rectifier mode. The IBGT switches are not enabled, each DC capacitor is charged to about 25 V; 2) at 0.2 second, the IBGT switches are enabled and the command total output DC voltage is given as 100 V, input AC current performs sinusoid shape instead of double-hump which in the diode-rectifier mode; 3) at 1 second, the command total output DC voltage is changed from 100 V to 140 V. The PI controller in this MATLAB/PLECS simulation is not optimized.

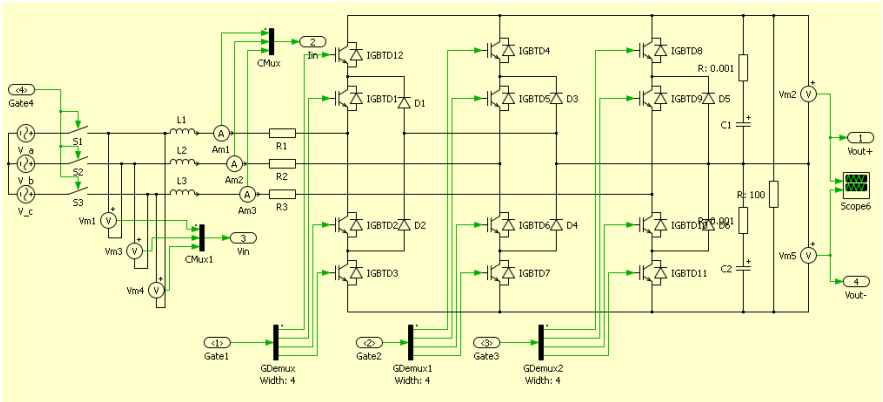
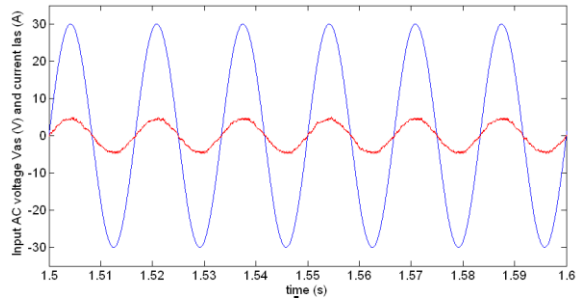
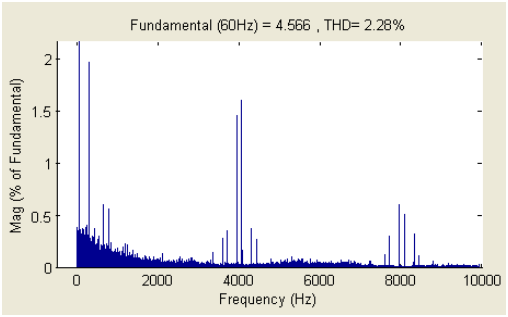


Figure 5- 1 NPC rectifier main circuit in MATLAB/PLECS

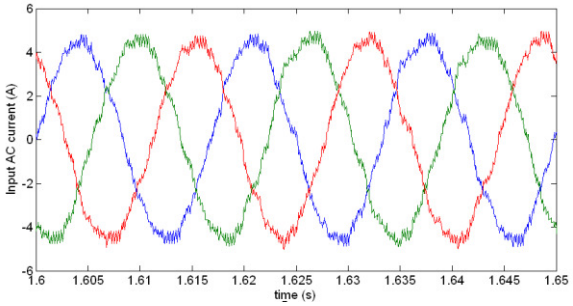
Figure 5-2 shows related graphs of the MATLAB/PLECS simulation results. Subplot (a) shows the phase A input voltage and current which is well sinusoidal shape. Since the reactive current command is zero during the whole simulation, we could see the unity power factor of NPC rectifier. Subplot (b) shows the low input current THD which means the NPC rectifier injects much less current harmonic into the grid compared to diode rectifier. Subplot (c) shows the three phase input AC currents in steady state. Subplot (d) shows the total output DC voltage which fast follows the command. Subplot (e) shows the input active current and reactive current in DQ0 reference frame. The active current has a prompt dynamic response when the voltage command changes. The reactive current could remain around zero in the transient state. Subplot (f) shows the voltage difference between two DC capacitor V_{dc1} and V_{dc2}. Three-level SVM could control the two voltage to be equal.



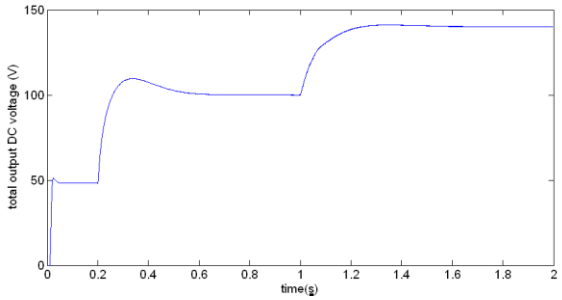
(a)



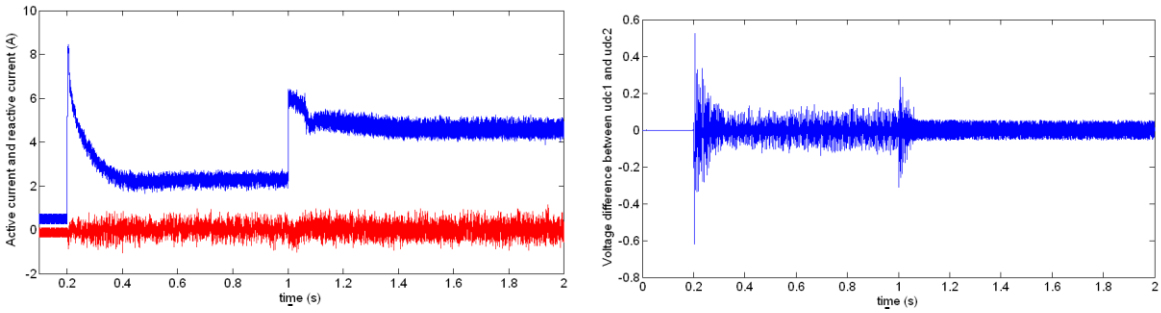
(b)



(c)



(d)



(e) (f)

Figure 5- 2 NPC rectifier MATLAB simulation results

5.2 NPC Rectifier Real-time Simulation

Before the illustration of NPC rectifier real-time simulation, it is necessary to describe Hardware-in-the-loop (HIL) and Controller-hardware-in-the-Loop (CHIL) [25].

HIL is a procedure that integrates a piece of equipment under test (HUT) into a large, virtually simulation system (VSS) through some coupling interface. It removes the inaccuracies of model simplification and linearization common to other simulation methods, as one or more actual device replace their modeled counterparts. Severe circumstances are analyzed with less risk or cost and precaution can then be taken before hidden defects which may cause the hardware experiment fail or damage.

Controller-hardware-in-the-loop [17] follows the HIL concept and implants a controller (dSPACE is the controller in this thesis), or part of it, as the HUT. It is then tested against a simulation of the system that it would normally control; the VSS (voltage and current in the NPC rectifier). CHIL [26] has many advantages over conventional simulation (only in MATLAB) controller tests. There is less truncation error, controller time delay and nonlinearities in CHIL. With CHIL, prospective controller problems are recognized and de-risked as protection design is more robustly test. The entire system is optimized via real controller hardware implantation. Figure 5-3 illustrates the CHIL methodology. A simple introduction of dPSACE and RTDS is needed for further explanation.

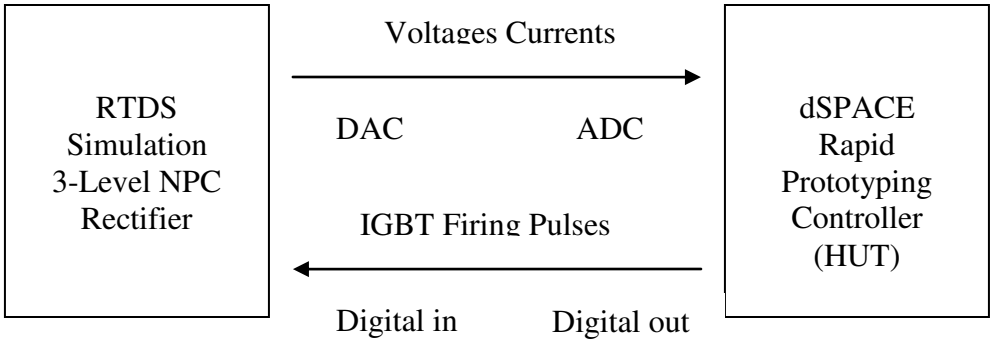


Figure 5- 3 CHIL methodology

Digital Signal Processing and Control Engineering (dSPACE) ACE 1103 [27], which is showed in figure 5-4, is the Rapid Prototyping Controller (RPC) used in the NPC rectifier test. The controller is instantiated via development in the MATLAB/Simulink environment and is compiled for use in the DSP via MATLAB's real-time interface. It doesn't require the user to spend tremendous time in coding the DSP (Digital Signal Processing) or FPGA (Field-programmable Gate Array). Experimental scenarios and data extraction are accomplished via the dSPACE^{TM} Control Desk environment. The user has real-time access to variable linked from Simulink when the model runs on the associated hardware processors. The dSPACE^{TM} I/O cards, which are optically connected to a VLT5000 V1.0 Aalborg Interface Control and Protection cards, sent the firing pulses signal to IGBT drivers. The dSPACE^{TM} takes system feedback, such as analogue voltage, current, torque signal, from its ADC channels with British naval connector (BNC) cable connected. In the CHIL test, NPC rectifier control is compiled into dSPACE^{TM}. It receives voltage and current signals and sends the IBGT firing pulses signal.

Figure 5- 4 dSPACE™ RPC

The real-time NPC rectifier circuit simulation is simulated in Real-time Digital Simulator™ (RTDS™) which is available at the Center for Advanced Power Systems (figure 5-5 (a)) [28]. The system consists of 14 racks, where the racks that were utilized contain 5 GPC cards that each contains two 750GX RISC-based processors. The NPC rectifier model is developed in the small time step environment (2μs). In figure 5-5 (b), gate drive pulses were transmitted to the digital I/O of the RTDS™ via a fiber optic link. Voltage and current measurements were transmitted via fiber optic cables to the DAC board in the lab interface which showed in figure 5-5 (c).

(a) (b) (c)

Figure 5- 5 RTDS™ (a) and its I/O interface (b), DAC interface(c)

RTDS™'s RSCAD develop environment provides a graphical user interface to model the NPC rectifier. After being built in RSCAD's Draft which is shown in figure 5-

6, the NPC rectifier main circuit could be compiled into Runtime which could run the real-time simulation.

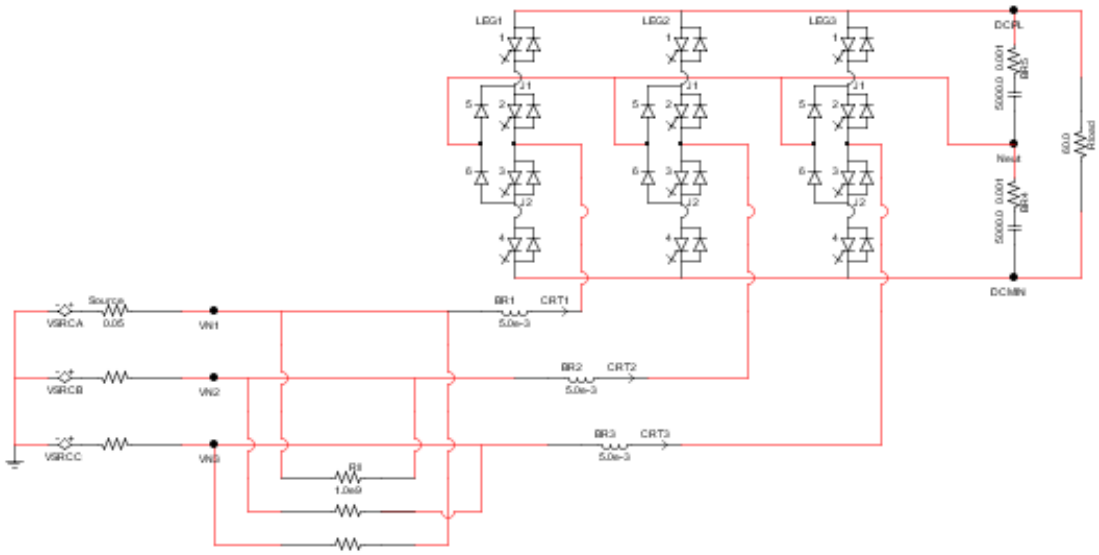
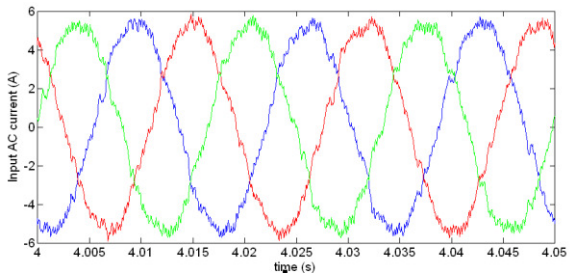


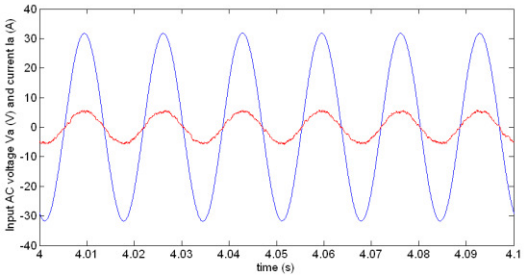
Figure 5- 6 NPC rectifier main circuit in RTDS^{TM}

In the CHIL test, dSPACE^{TM,} which is the NPC rectifier controller, plays the HUT role. With the main circuit model in RTDS^{TM}, the NPC rectifier system hardware controller ability was investigated very well before it connects to the real power electronic devices. It receives the virtual voltage and current signal from RTDS^{TM} DAC interface, also sends 12 firing pulses signals to the virtual IGBTs in RTDS^{TM} I/O interface. All control algorithms, such as PLL (Phase-Locked Loop); ABC to DQ0 transformation; PI control, 3-level SVM, was tested in real-time. It's easy for user to debug the control by checking data in dSPACE^{TM} Control Desk. When the system control debugging is finished, the RPC is ready to connect to the real power electronic devices which are shown in next chapter. The CHIL test circuit parameters from table 4-1 are still used in this test. In the CHIL test, the enable signal is given to IGBTs at about 1.8 second. The command total output DC voltage is 140V. Some CHIL test results are shown in figure5-7. They are similar to the MATLAB simulation results in figure 5-2, such as sinusoidal input AC currents and unity power factor; however the voltage difference between V_{dc1} and V_{dc2} in figure 5-2 (f) is zero in the diode rectifier mode (0 to 0.2 seconds) while in figure 5-7(f) it is not zero. Instead of ideal MATLAB simulation, the RTDS result seems more likely to the real world where the voltage difference exists because it's impossible

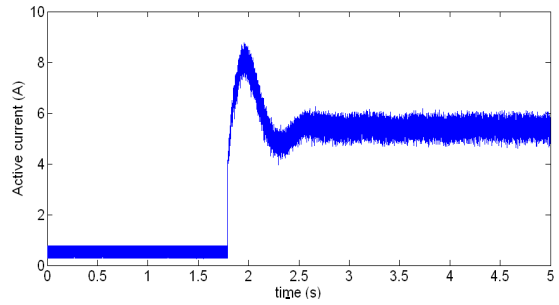
to find two capacitors value exactly the same to get exactly balanced voltage. Form figure 5-7(f), we know that 3-level NPC SVM algorithm could actively control the voltage difference in a very small range around zero. In the next chapter, result of CHIL test is compared to the result of real hardware test. We will investigate how close the CHIL methodology could simulate the real hardware experiment of the NPC rectifier system.



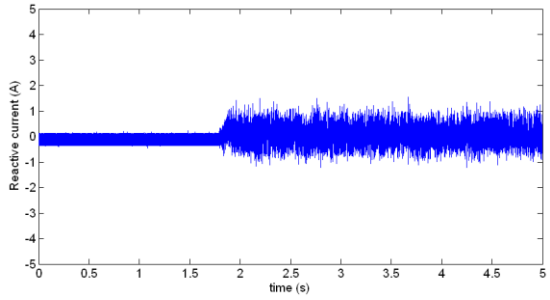
(a) Input AC currents

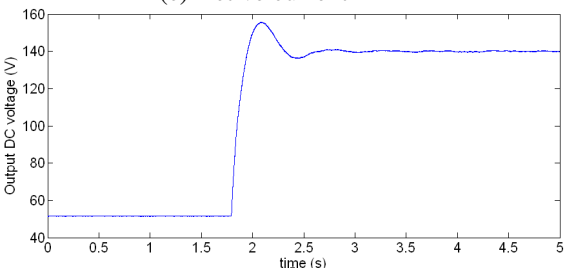


(b) Input AC voltage V_a and current I_a

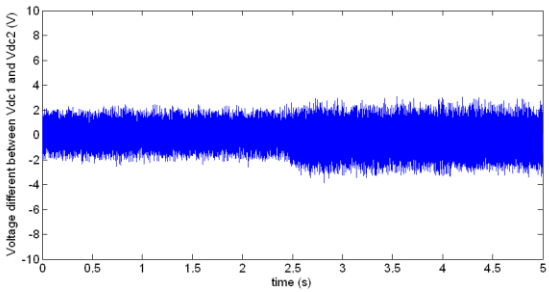


(c) Active current





(e) Output DC voltage (V)



(f) Voltage difference ΔV (V)

Figure 5- 7 NPC recitifier CHIL test results

CHAPTER 6

NPC RECTIFIER HARDWARE TEST RESULTS

6.1 Hardware Experimental Setup

In order to fully validate the 3-level NPC rectifier system and its control algorithm, a three-phase three-level NPC rectifier hardware test-bed is constructed. For users' safety, the test-bed won't test the full load which means operating above 1000V voltage across each IGBT and output power more than several kilo watts. The hardware test parameters remain the same as shown in table 4-1.

A POWERSTAT® 117CT-3 three-phase variable transformer is utilized to scale down the grid voltage of 110V line to neutral to 30V line to neutral which required from table 4-1. Figure 6-1(a) shows the variable transformer used for the test. At the beginning of the test, user could increase output voltage of the variable transformer from zero manually, just like soft starter to prevent high capacitor charging current.

Line reactors play an important role in the voltage source PWM rectifier. They make the rectifier boost characteristic; separate the sinusoidal AC input voltage and the nonlinear pulse voltage across semiconductors; reduce the AC currents harmonics as filters and so on. Figure 6-1(b) shows the Hammond heavy current 195G50 line reactors (Inductance: 5 mH, DC current: 50A) used for the test. When to select inductance value, engineers need to consider two sides: one is to ensure active and reactive power could flow from grid to load follow the command [5], engineers usually use (6-1) to limit the max value of inductance; another side is to satisfy the current dynamic response and reduce the current ripple to certain range, engineers usually use (6-2) to select inductance value to meet the ripple requirement. The inductance value in table 4-1, which is 5 mH, satisfies the NPC rectifier system if Δi_{max} is designed to be less than 0.2 A.

$$L_s \le \frac{V_{dc} - 2V_{sm}}{2I_m\omega} \quad (V_{dc} - 2V_{sm} > 0) \tag{6-1}$$

$$\frac{(2V_{dc} - 3V_{sm})V_{sm}T_s}{2V_{dc}\Delta i_{\max}} \le L_s \le \frac{2V_{dc}}{3I_m\omega} \quad (V_{dc} - 1.5E_m > 0) \tag{6-2}$$

where $V_{dc}= V_{dc1}+V_{dc2}$ in (2-4), which is total output DC voltage;

V_{sm} is peak value of grid AC input voltage;

I_m is peak value of AC input current;

Δi_{max} is the maximum value of the current ripple

The three-phase three-level bridges comprise of 6 Infineon® FF150R12ME3G dual IGBT modules (1200V/ 150A) and 3 POWEREX® CD61_16B dual diodes isolated modules (up to 2200V/160A). 6 CONCEPT® 2SD316EI dual-channel plug-and-play SCALE IGBT drivers are selected to drive the IGBTs. All above components are mounted on the H S MARSTON® heat-sink (size 300mm by 300mm). Figure 6-1 (c) shows the completed three-level bridges.

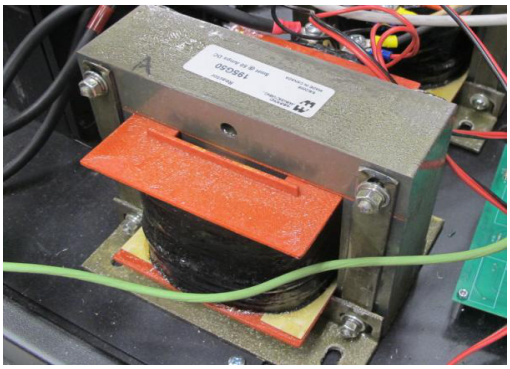
LEM® LA 55-P current sensors (I_{PN}=50A) and LEM® LV 20-P voltage sensors feedback currents and voltages signal to dSPACE™ ADC channels. They are sold on well-designed Print Circuit Boards (PCB) which shown in figure 6-1(d) and (e), respectively.

When to select DC capacitor value, engineers encounter a tradeoff problem [5]: on one hand, in order to obtain fast transient response, the capacitor value should be small, when the system is turned off, this also makes capacitor discharge fast which is safe to users; on the other hand, in order to reduce the voltage disturbance when there is a sudden load changes, and to decrease the DC voltage harmonic, the DC capacitor value should be big. Engineer use (6-3) to satisfy the first case which make sure the fast start-up performance, t_r is the settling-time from the switches are enabled to the system reach its steady state. (6-4) ensures that capacitor value is big enough to limit peak voltage ripple ΔV_L within designer's requirement during the sudden load change scenario (suppose the load is resistor load and its value is R_L). The capacitor value in table 4-1 satisfy if the ripple voltage ΔV_L=2 V. Figure 6-1(e) shows the three level DC capacitors.

$$C \le \frac{t_r}{0.74 R_L} \tag{6-3}$$

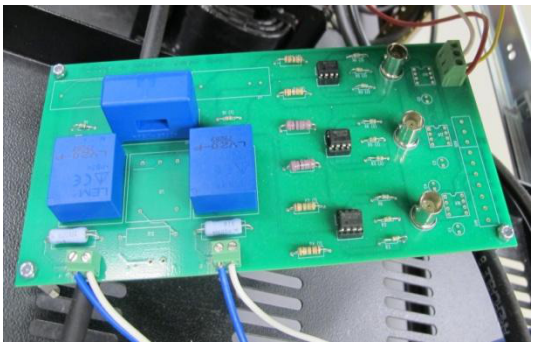
$$C > \frac{1}{2 \Delta V_m R_L} \tag{6-4}$$

(a)



(b)

(c)



(d)

(e)

Figure 6- 1 NPC rectifier hardware test-bed

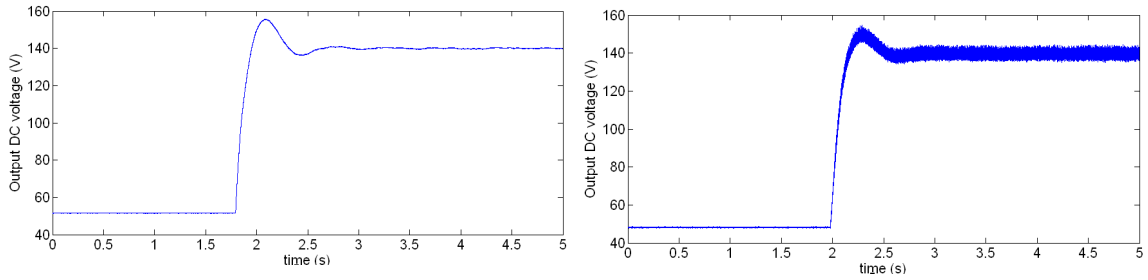
6.2 Hardware and CHIL Experimental Results.

Both hardware and CHIL experiment results are shown in this section. In order to test and compare how much the CHIL experiment could simulate the real hardware experiment. All the parameters of the NPC rectifier circuit are still remained as shown in table 4-1. This section is divided into to two sub-sections A and B. Sub-section A describes the testing and controller performance of the NPC rectifier start-up scenario

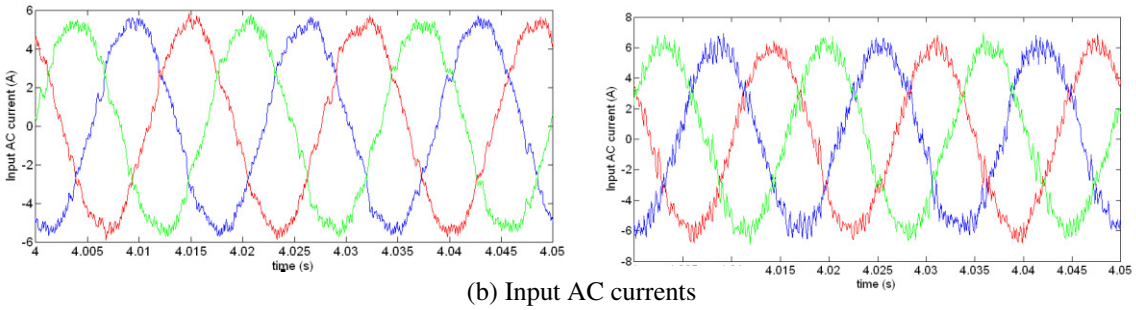
while sub-section B describes the step-command scenario. All data are records by dSPACE^{TM} Control Desk. PI controller gains in this section are not optimized.

A. Start-up Experimental Results.

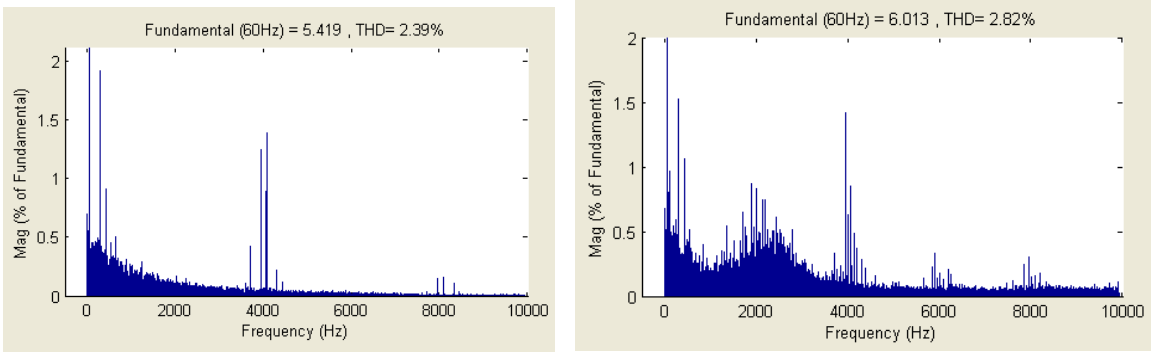
Figure 6-2 shows the NPC rectifier start-up scenario. The Graphs at left side are data from CHIL experiment while the graphs at right side are data from real hardware experiment. Before the IBGT given enable firing signal, the NPC rectifier is in the diode mode, the total output DC voltage V_{dc}=1.35V_{sm}. At about 2 seconds, enable signals are given to IGBTs. The command total output DC voltage is 140V.



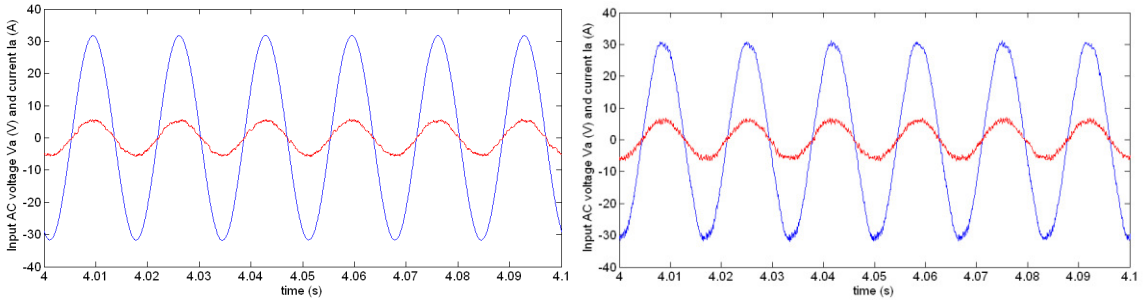
(a) Total output DC voltage



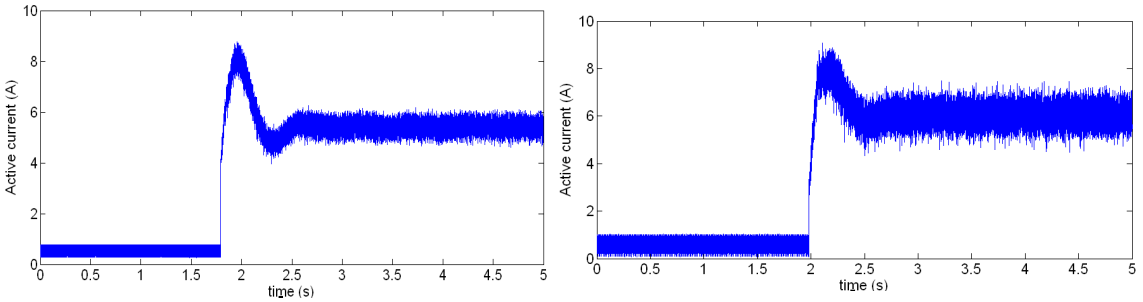
(b) Input AC currents



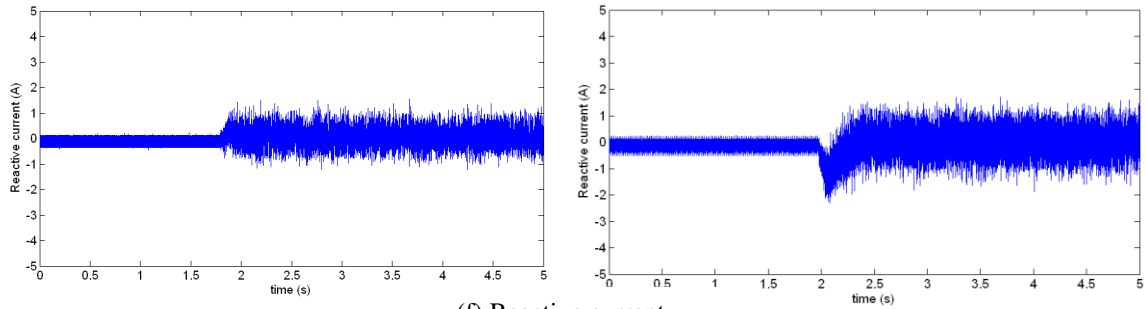
(c) Input AC current I_a THD



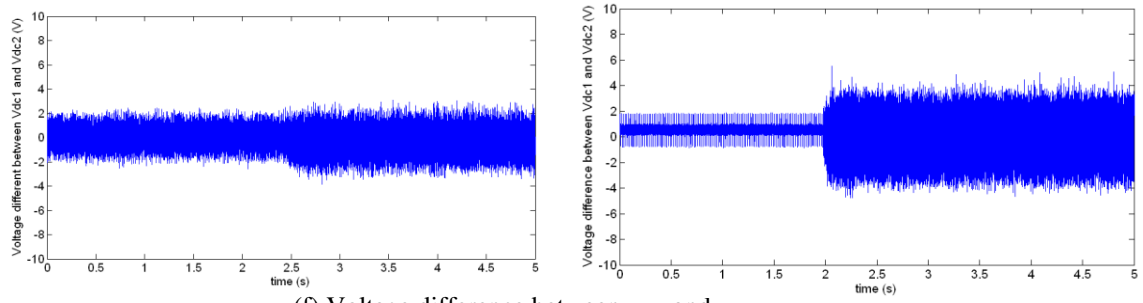
(d) Input AC voltage V_a and current I_a



(e) Active current



(f) Reactive current



(f) Voltage difference between u_{dc1} and u_{dc2}

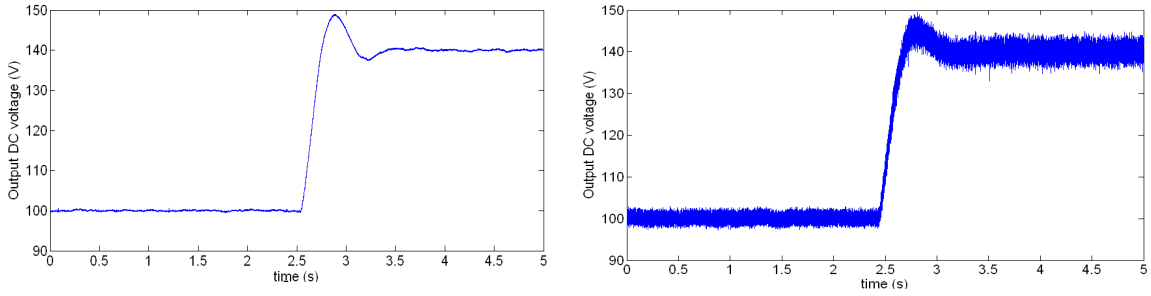
Figure 6- 2 CHIL and hardware results of NPC rectifier start-up scenario

Figure 6-2 (a) shows the output DC voltage. It could fast follow the command voltage 140 V. There is more noise and ripple in the right graph since the hardware test uses the real voltage sensors. Figure 6-2 (b) shows three-phase input currents. Since it's

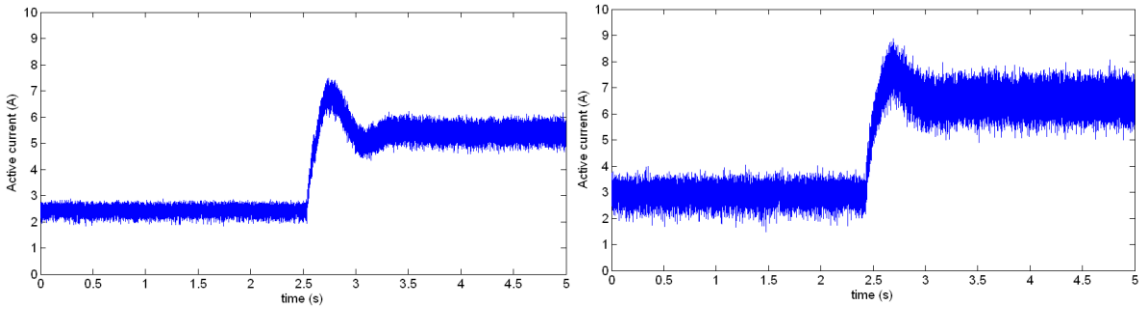
difficult to make the RTDS™ to simulate the loss of real hardware switches exactly the same, the peak value of currents in hardware is a little bigger than the value in the CHIL test. Figure 6-2 (c) shows the low current THD in steady state. Figure 6-2 (d) shows the Input AC voltage V_a and current I_a. Unity power factor is achieved in both graphs. It could see that the input AC voltage in hardware is not ideal sinusoidal due to the effect of variable transformer. Figure 6-2 (e) shows the good dynamic active current response to the changing voltage command. Figure 6-2 (f) shows that the reactive current could be controller to around zero even during the start-up transient. Figure 6-2 (f) shows that Voltages across two capacitors V_{dc1} and V_{dc2} could be controlled balanced by the NPC SVM. The error ripple of ΔV in the hardware test is a little bigger than the CHIL test.

B. Step-command Experimental Results.

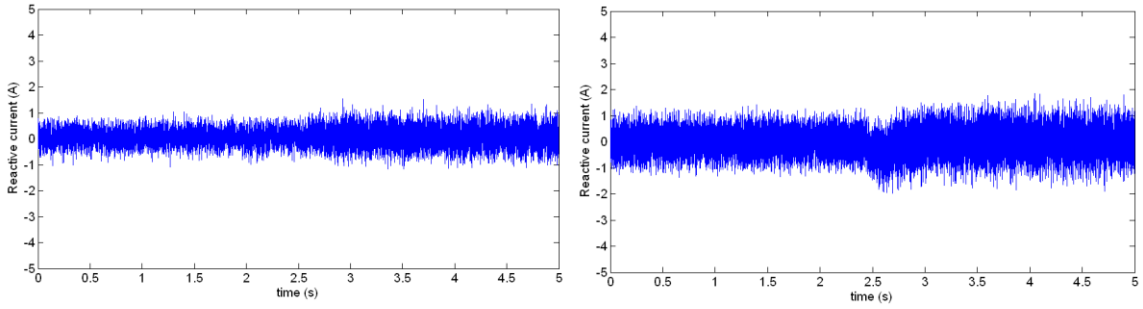
In this sub-section, another scenario called step-command has been analyzed. At the beginning of this scenario, the NPC rectifier is in the steady state where the output DC voltage is 100 V. At about 2.5 s, the output DC voltage command is suddenly changes to 140 V. Similar to sub-section A, the graphs at left side are data from CHIL experiment while the graphs at right side are data from real hardware experiment.



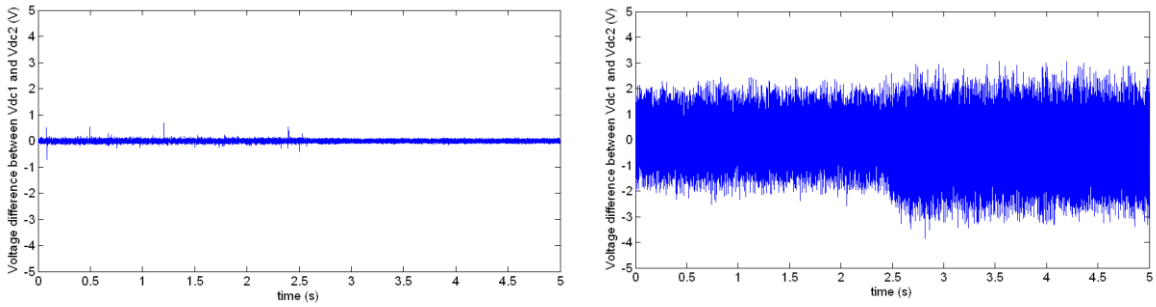
(a) Total output DC voltage



(b) Active current



(c) Reactive current



(d) Voltage difference between u_{dc1} and u_{dc2}

Figure 6- 3 CHIL and hardware results of NPC rectifier step-command scenario

As shown in figure 6-3, the NPC rectifier system could follow the sudden-change command and it has fast dynamic response. Although there are more noise and ripple in hardware test data than the CHIL test, two experiments are consistent to each other. The CHIL experiment is validated by the hardware. The real time simulation CHIL test could simulate the hardware performance in good accuracy.

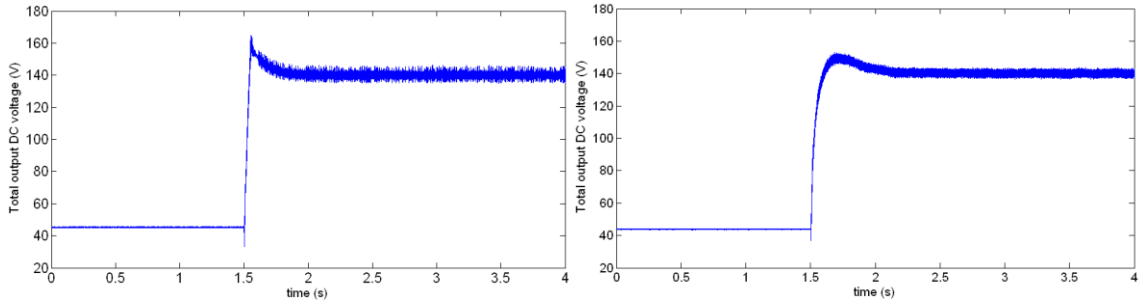
Sometimes when engineers finish the MATLAB non-real-time simulation, they begin to work in real hardware experiment directly. But due to the complexity of some power electronics device, such as the NPC rectifier, and the lack of accuracy of non-real-time simulation presenting the real world performance, the hardware test may fail or even cause some danger. Therefore, as CHIL test could debug the control algorithm in dSPACE^{TM} in the NPC rectifier system, it makes sense for engineers to have CHIL experiment prior to the hardware experiment.

The rapid prototyping CHIL environment is a successful and expedient methodology to de-risk the instantiation of advanced converter topologies. The methodology illustrates the use of real-time simulation to rigorously test the functionality of a control strategy and its performance prior to hardware implementation of the entire

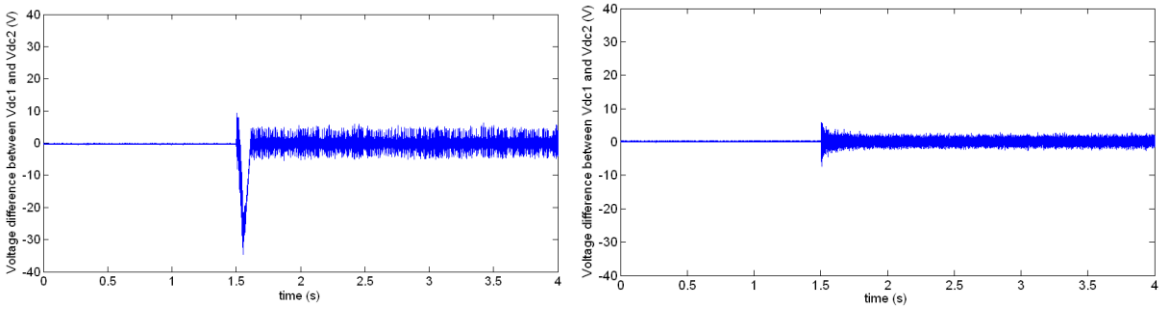
system. Provided a relatively well-defined model of the hardware is implemented in the real-time environment, there will be an almost seamless transition from the CHIL environment to the actual hardware testing and operation.

6.3 Particles Swarm Optimization Experimental Results.

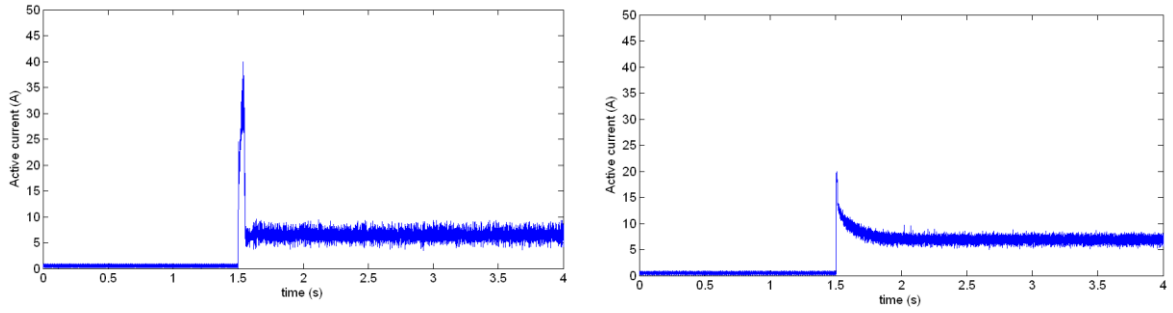
There are two PI controller tuning method mentioned in Chapter 4, one is conventional Nichols and Ziegler, another is PSO. The NPC rectifier system responses to these two tuning methods are compared in this section. All the experiment data come from hardware experiment test. Figure 6-4 illustrates that the start-up scenario which explained in the subsection 6.2-A. The left side waveform are experiment data from the system whose PI controller tuned by the classic Nichols and Ziegler methods, while right side waveform are experiment data from the system whose PI controller tuned by PSO. It could see from the figure, the PI controller tuned by PSO could improve the system performance compared to conventional Nichols and Ziegler tuning methods.



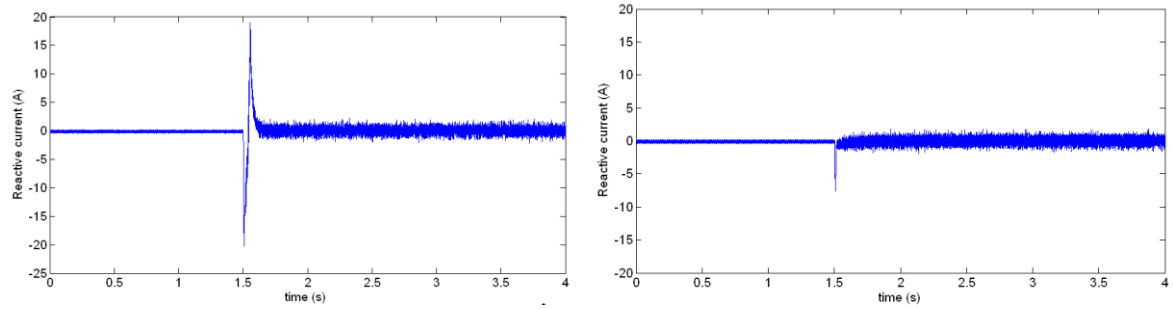
(a) Total output DC voltage



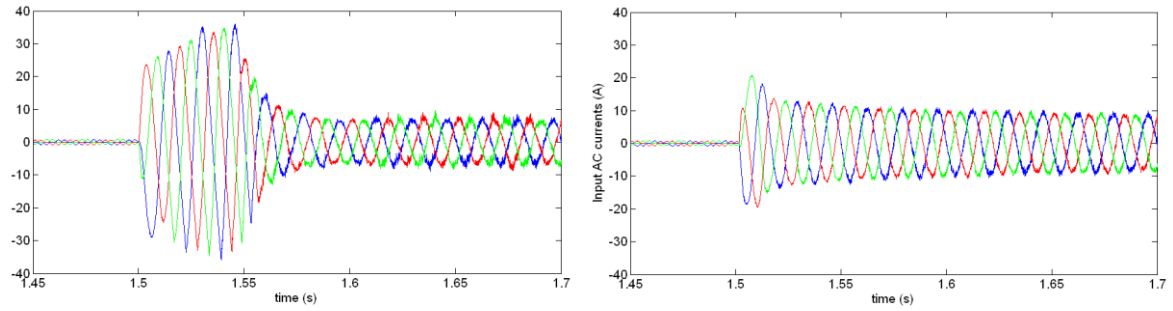
(b) Voltage difference between u_{dc1} and u_{dc2}



(c) Active current



(d) Reactive current



(e) Three phase input AC currents

Figure 6- 4 NPC rectifier's response to tuning methods of Nichols and Ziegler and PSO

As shown in figure 6-4 (a), the output total DC voltage overshoot of Nichols and Ziegler's tuning methods is bigger than PSO's. As shown in 6-4 (b), the voltage V_{dc1} and V_{dc2} suffer a big un-balance in the start-up transient whose controller tuned by Nichols and Ziegler's tuning methods. This voltage un-balance may cause the system lose its three-level advantage and increases the PWM wave harmonics. As shown in left figure of 6-4 (c) and (e): the big active current overshoot and transient AC currents overshoot may blow up fuse, cause breaker error and reduce the system service life. In figure 6-4 (d), we find that reactive current oscillates much more in the left graph than the right one which means the PI controller tuned by PSO could control the reactive current to zero better

than Nichols and Ziegler methods. Therefore, it's validated that PSO could use to improve tuning PI controller for the NPC rectifier.

In conclusion, PSO could further optimize the PI controller gains for the NPC rectifier system, which original tuned by Nichols and Ziegler methods, to improve the system dynamic performance. It success reduce the system transient overshoot and settling-time. The system will have less damage risk of over voltage and current and longer service life time.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

In this thesis, a three-phase three-level neutral point clamped rectifier system was presented. The circuit model was built in MATLAB/PLECS and the average math model without high switching was built in MATLAB to analyze the system control response. The neutral point voltage problem is solved by the bang-bang control algorithm which actively chooses or abandons redundant small vector. Double closed loop control, which original came from motor speed control, is used in the system and the dynamic response is satisfied. After non-real time simulation in MATLAB environment completed, the real-time simulation in RTDS was tested by CHIL methodology. The purpose of CHIL test is to de-risk and debug the control algorithm in rapid-prototyping controller dSPACE^{TM} in real-time before the dSPACE^{TM} actually controls the real hardware test devices. The NPC rectifier results from CHIL real-time simulation test and hardware test were compared in order to validate there is an almost seamless transition from the CHIL environment to the actual hardware. The rapid prototyping CHIL environment is a useful and expedient methodology to de-risk the instantiation of NPC rectifier system, and could use to other advanced converter topologies as well. Compared to classic Nichols and Ziegler method, a new method, which is base on Particle Swarm Optimization, is used for tuning PI controller gains in the double closed control loop. The improvement is approved in different models.

7.2 Future Work

For the future research, several improvements can be implemented. For the hardware configuration, the currently control was done in dSPACE^{TM} which had a time step limit of 50μs. The NPC rectifier switching frequency is only 2 kHz. The Texas Instruments TMS320F28335 DSP is prepared to replace dSPACE^{TM}'s control task in order to increase the switching frequency to above 10 kHz. More professional PCB boards which could reduce the EMI noise and obtain more accurate currents and voltages

signals measurement are built in process. With the improvement mentioned above, another NPC rectifier hardware test bed will built in the same lab, two NPC rectifiers will work in parallel to do further research of medium-voltage DC power systems on ships as showed in figure 1-1.

APPENDIX A

SPACE VECTOR MODULATION SEQUENCE

(a) SVM sequence for section D_1 to D_7

section	Neutral point voltage	Currents relationship	SVM sequence
D_1	$\Delta V_{NP}\geq 0$	$I_{sa}\text{-}i_{sc}\geq 0$	$S_2\rightarrow S_5\rightarrow S_4\rightarrow S_1\rightarrow S_1\rightarrow S_4\rightarrow S_5\rightarrow S_2$
		$i_{sa}\text{-}i_{sc}<0$	$S_2\rightarrow S_{10}\rightarrow S_{11}\rightarrow S_3\rightarrow S_3\rightarrow S_{11}\rightarrow S_{10}\rightarrow S_2$
	$\Delta V_{NP}<0$	$I_{sa}\text{-}i_{sc}\geq 0$	$S_2\rightarrow S_{10}\rightarrow S_{11}\rightarrow S_3\rightarrow S_3\rightarrow S_{11}\rightarrow S_{10}\rightarrow S_2$
		$I_{sa}\text{-}i_{sc}<0$	$S_2\rightarrow S_5\rightarrow S_4\rightarrow S_1\rightarrow S_1\rightarrow S_4\rightarrow S_5\rightarrow S_2$
D_2	$\Delta V_{NP}\geq 0$	$i_{sb}\text{-}is_c\geq 0$	$S_2\rightarrow S_5\rightarrow S_6\rightarrow S_1\rightarrow S_1\rightarrow S_6\rightarrow S_5\rightarrow S_2$
		$i_{sb}\text{-}i_{sc}<0$	$S_2\rightarrow S_{12}\rightarrow S_{11}\rightarrow S_3\rightarrow S_3\rightarrow S_{11}\rightarrow S_{12}\rightarrow S_2$
	$\Delta V_{NP}<0$	$i_{sb}\text{-}i_{sc}\geq 0$	$S_2\rightarrow S_{12}\rightarrow S_{11}\rightarrow S_3\rightarrow S_3\rightarrow S_{11}\rightarrow S_{12}\rightarrow S_2$
		$i_{sb}\text{-}i_{sc}<0$	$S_2\rightarrow S_5\rightarrow S_6\rightarrow S_1\rightarrow S_1\rightarrow S_6\rightarrow S_5\rightarrow S_2$
D_3	$\Delta V_{NP}\geq 0$	$i_{sb}\text{-}i_{sa}\geq 0$	$S_2\rightarrow S_7\rightarrow S_6\rightarrow S_1\rightarrow S_1\rightarrow S_6\rightarrow S_7\rightarrow S_2$
		$i_{sb}\text{-}i_{sa}<0$	$S_2\rightarrow S_{12}\rightarrow S_{13}\rightarrow S_3\rightarrow S_3\rightarrow S_{13}\rightarrow S_{12}\rightarrow S_2$
	$\Delta V_{NP}<0$	$i_{sb}\text{-}i_{sa}\geq 0$	$S_2\rightarrow S_{12}\rightarrow S_{13}\rightarrow S_3\rightarrow S_3\rightarrow S_{13}\rightarrow S_{12}\rightarrow S_2$
		$i_{sb}\text{-}i_{sa}<0$	$S_2\rightarrow S_7\rightarrow S_6\rightarrow S_1\rightarrow S_1\rightarrow S_6\rightarrow S_7\rightarrow S_2$
D_4	$\Delta V_{NP}\geq 0$	$i_{sc}\text{-}i_{sa}\geq 0$	$S_2\rightarrow S_7\rightarrow S_8\rightarrow S_1\rightarrow S_1\rightarrow S_8\rightarrow S_7\rightarrow S_2$
		$i_{sc}\text{-}i_{sa}<0$	$S_2\rightarrow S_{14}\rightarrow S_{13}\rightarrow S_3\rightarrow S_3\rightarrow S_{13}\rightarrow S_{14}\rightarrow S_2$
	$\Delta V_{NP}<0$	$i_{sc}\text{-}i_{sa}\geq 0$	$S_2\rightarrow S_{14}\rightarrow S_{13}\rightarrow S_3\rightarrow S_3\rightarrow S_{13}\rightarrow S_{14}\rightarrow S_2$
		$i_{sc}\text{-}i_{sa}<0$	$S_2\rightarrow S_7\rightarrow S_8\rightarrow S_1\rightarrow S_1\rightarrow S_8\rightarrow S_7\rightarrow S_2$
D_5	$\Delta V_{NP}\geq 0$	$i_{sc}\text{-}i_{sb}\geq 0$	$S_2\rightarrow S_9\rightarrow S_8\rightarrow S_1\rightarrow S_1\rightarrow S_8\rightarrow S_9\rightarrow S_2$
		$i_{sc}\text{-}i_{sb}<0$	$S_2\rightarrow S_{14}\rightarrow S_{15}\rightarrow S_3\rightarrow S_3\rightarrow S_{15}\rightarrow S_{14}\rightarrow S_2$
	$\Delta V_{NP}<0$	$i_{sc}\text{-}i_{sb}\geq 0$	$S_2\rightarrow S_{14}\rightarrow S_{15}\rightarrow S_3\rightarrow S_3\rightarrow S_{15}\rightarrow S_{14}\rightarrow S_2$
		$i_{sc}\text{-}i_{sb}<0$	$S_2\rightarrow S_9\rightarrow S_8\rightarrow S_1\rightarrow S_1\rightarrow S_8\rightarrow S_9\rightarrow S_2$
D_6	$\Delta V_{NP}\geq 0$	$i_{sa}\text{-}i_{sb}\geq 0$	$S_2\rightarrow S_9\rightarrow S_4\rightarrow S_1\rightarrow S_1\rightarrow S_4\rightarrow S_9\rightarrow S_2$
		$i_{sa}\text{-}i_{sb}<0$	$S_2\rightarrow S_{10}\rightarrow S_{15}\rightarrow S_3\rightarrow S_3\rightarrow S_{15}\rightarrow S_{10}\rightarrow S_2$
	$\Delta V_{NP}<0$	$i_{sa}\text{-}i_{sb}\geq 0$	$S_2\rightarrow S_{10}\rightarrow S_{15}\rightarrow S_3\rightarrow S_3\rightarrow S_{15}\rightarrow S_{10}\rightarrow S_2$
		$i_{sa}\text{-}i_{sb}<0$	$S_2\rightarrow S_9\rightarrow S_4\rightarrow S_1\rightarrow S_1\rightarrow S_4\rightarrow S_9\rightarrow S_2$

(b) SVM sequence for section D_8 to D_{12}

section	Neutral point voltage	Currents relationship	SVM sequence
D_7	$\Delta V_{NP}\geq 0$	$i_{sc}\geq 0$ $i_{sa}\geq 0$	$S_{11}\rightarrow S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_4\rightarrow S_4\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}\rightarrow S_{11}$
		$i_{sc}\geq 0$ $i_{sa}<0$	$S_{11}\rightarrow S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}\rightarrow S_{11}$
		$i_{sc}<0$ $i_{sa}\geq 0$	$S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_4\rightarrow S_4\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}$
		$i_{sc}<0$ $i_{sa}<0$	$S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}$
	$\Delta V_{NP}<0$	$i_{sc}\geq 0$ $i_{sa}\geq 0$	$S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}$
		$i_{sc}\geq 0$ $i_{sa}<0$	$S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_4\rightarrow S_4\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}$
		$i_{sc}<0$ $i_{sa}\geq 0$	$S_{11}\rightarrow S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}\rightarrow S_{11}$
		$i_{sc}<0$ $i_{sa}<0$	$S_{11}\rightarrow S_{10}\rightarrow S_{16}\rightarrow S_5\rightarrow S_4\rightarrow S_4\rightarrow S_5\rightarrow S_{16}\rightarrow S_{10}\rightarrow S_{11}$
D_8	$\Delta V_{NP}\geq 0$	$i_{sb}\geq 0$ $i_{sc}\geq 0$	$S_6\rightarrow S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{11}\rightarrow S_{11}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5\rightarrow S_6$
		$i_{sb}\geq 0$ $i_{sc}<0$	$S_6\rightarrow S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5\rightarrow S_6$
		$i_{sb}<0$ $i_{sc}\geq 0$	$S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{11}\rightarrow S_{11}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5$
		$i_{sb}<0$ $i_{sc}<0$	$S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5$
	$\Delta V_{NP}<0$	$i_{sb}\geq 0$ $i_{sc}\geq 0$	$S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5$
		$i_{sb}\geq 0$ $i_{sc}<0$	$S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{11}\rightarrow S_{11}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5$
		$i_{sb}<0$ $i_{sc}\geq 0$	$S_6\rightarrow S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5\rightarrow S_6$
		$i_{sb}<0$ $i_{sc}<0$	$S_6\rightarrow S_5\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{11}\rightarrow S_{11}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_5\rightarrow S_6$
D_9	$\Delta V_{NP}\geq 0$	$i_{sa}\geq 0$ $i_{sb}\geq 0$	$S_{13}\rightarrow S_{12}\rightarrow S_{18}\rightarrow S_7\rightarrow S_6\rightarrow S_6\rightarrow S_7\rightarrow S_{18}\rightarrow S_{12}\rightarrow S_{13}$
		$i_{sa}\geq 0$ $i_{sb}<0$	$S_{13}\rightarrow S_{12}\rightarrow S_{18}\rightarrow S_7\rightarrow S_7\rightarrow S_{18}\rightarrow S_{12}\rightarrow S_{13}$
		$i_{sa}<0$ $i_{sb}\geq 0$	$S_{12}\rightarrow S_{18}\rightarrow S_7\rightarrow S_6\rightarrow S_6\rightarrow S_7\rightarrow S_{18}\rightarrow S_{12}$
		$i_{sa}<0$	$S_{12}\rightarrow S_{18}\rightarrow S_7\rightarrow S_7\rightarrow S_{18}\rightarrow S_{12}$

		$i_{sb}<0$	
	$\Delta V_{NP}<0$	$i_{sa}\geq 0$ $i_{sb}\geq 0$	$S_{12}\rightarrow S_{18}\rightarrow S_{7}\rightarrow S_{7}\rightarrow S_{18}\rightarrow S_{12}$
		$i_{sa}\geq 0$ $i_{sb}<0$	$S_{12}\rightarrow S_{18}\rightarrow S_{7}\rightarrow S_{6}\rightarrow S_{6}\rightarrow S_{7}\rightarrow S_{18}\rightarrow S_{12}$
		$i_{sa}<0$ $i_{sb}\geq 0$	$S_{13}\rightarrow S_{12}\rightarrow S_{18}\rightarrow S_{7}\rightarrow S_{7}\rightarrow S_{18}\rightarrow S_{12}\rightarrow S_{13}$
		$i_{sa}<0$ $i_{sb}<0$	$S_{13}\rightarrow S_{12}\rightarrow S_{18}\rightarrow S_{7}\rightarrow S_{6}\rightarrow S_{6}\rightarrow S_{7}\rightarrow S_{18}\rightarrow S_{12}\rightarrow S_{13}$
D_{10}	$\Delta V_{NP}\geq 0$	$i_{sc}\geq 0$ $i_{sa}\geq 0$	$S_{8}\rightarrow S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{13}\rightarrow S_{13}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}\rightarrow S_{8}$
		$i_{sc}\geq 0$ $i_{sa}<0$	$S_{8}\rightarrow S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}\rightarrow S_{8}$
		$i_{sc}<0$ $i_{sa}\geq 0$	$S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{13}\rightarrow S_{13}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}$
		$i_{sc}<0$ $i_{sa}<0$	$S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}$
	$\Delta V_{NP}<0$	$i_{sc}\geq 0$ $i_{sa}\geq 0$	$S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}$
		$i_{sc}\geq 0$ $i_{sa}<0$	$S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{13}\rightarrow S_{13}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}$
		$i_{sc}<0$ $i_{sa}\geq 0$	$S_{8}\rightarrow S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}\rightarrow S_{8}$
		$i_{sc}<0$ $i_{sa}<0$	$S_{8}\rightarrow S_{7}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{13}\rightarrow S_{13}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{7}\rightarrow S_{8}$
D_{11}	$\Delta V_{NP}\geq 0$	$i_{sb}\geq 0$ $i_{sc}\geq 0$	$S_{15}\rightarrow S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{8}\rightarrow S_{8}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}\rightarrow S_{15}$
		$i_{sb}\geq 0$ $i_{sc}<0$	$S_{15}\rightarrow S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}\rightarrow S_{15}$
		$i_{sb}<0$ $i_{sc}\geq 0$	$S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{8}\rightarrow S_{8}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}$
		$i_{sb}<0$ $i_{sc}<0$	$S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}$
	$\Delta V_{NP}<0$	$i_{sb}\geq 0$ $i_{sc}\geq 0$	$S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}$
		$i_{sb}\geq 0$ $i_{sc}<0$	$S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{8}\rightarrow S_{8}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}$
		$i_{sb}<0$ $i_{sc}\geq 0$	$S_{15}\rightarrow S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}\rightarrow S_{15}$
		$i_{sb}<0$ $i_{sc}<0$	$S_{15}\rightarrow S_{14}\rightarrow S_{20}\rightarrow S_{9}\rightarrow S_{8}\rightarrow S_{8}\rightarrow S_{9}\rightarrow S_{20}\rightarrow S_{14}\rightarrow S_{15}$
D_{12}	$\Delta V_{NP}\geq 0$	$i_{sa}\geq 0$ $i_{sb}\geq 0$	$S_{4}\rightarrow S_{9}\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{15}\rightarrow S_{15}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_{9}\rightarrow S_{4}$

		$i_{sa}\geq 0$ $i_{sb}<0$	$S_4\rightarrow S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9\rightarrow S_4$
		$i_{sa}<0$ $i_{sb}\geq 0$	$S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{15}\rightarrow S_{15}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9$
		$i_{sa}<0$ $i_{sb}<0$	$S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9$
	$\Delta V_{NP}<0$	$i_{sa}\geq 0$ $i_{sb}\geq 0$	$S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9$
		$i_{sa}\geq 0$ $i_{sb}<0$	$S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{15}\rightarrow S_{15}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9$
		$i_{sa}<0$ $i_{sb}\geq 0$	$S_4\rightarrow S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9\rightarrow S_4$
		$i_{sa}<0$ $i_{sb}<0$	$S_4\rightarrow S_9\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{15}\rightarrow S_{15}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_9\rightarrow S_4$

(c) SVM sequence for section D_{13} to D_{24}

Section	Neutral point voltage	Current relationship	SVM sequence
D_{13}	$\Delta V_{NP}\geq 0$	$i_{sa}\geq 0$	$S_4\rightarrow S_{22}\rightarrow S_{16}\rightarrow S_{16}\rightarrow S_{22}\rightarrow S_4$
		$i_{sa}<0$	$S_{22}\rightarrow S_{16}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{16}\rightarrow S_{22}$
	$\Delta V_{NP}<0$	$i_{sa}\geq 0$	$S_{22}\rightarrow S_{16}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{16}\rightarrow S_{22}$
		$i_{sa}<0$	$S_4\rightarrow S_{22}\rightarrow S_{16}\rightarrow S_{16}\rightarrow S_{22}\rightarrow S_4$
D_{14}	$\Delta V_{NP}\geq 0$	$i_{sc}\geq 0$	$S_{11}\rightarrow S_{23}\rightarrow S_{16}\rightarrow S_{16}\rightarrow S_{23}\rightarrow S_{11}$
		$i_{sc}<0$	$S_{23}\rightarrow S_{16}\rightarrow S_5\rightarrow S_5\rightarrow S_{16}\rightarrow S_{23}$
	$\Delta V_{NP}<0$	$i_{sc}\geq 0$	$S_{22}\rightarrow S_{16}\rightarrow S_5\rightarrow S_5\rightarrow S_{16}\rightarrow S_{23}$
		$i_{sc}<0$	$S_{11}\rightarrow S_{23}\rightarrow S_{16}\rightarrow S_{16}\rightarrow S_{23}\rightarrow S_{11}$
D_{15}	$\Delta V_{NP}\geq 0$	$i_{sc}\geq 0$	$S_{11}\rightarrow S_{23}\rightarrow S_{17}\rightarrow S_{17}\rightarrow S_{23}\rightarrow S_{11}$
		$i_{sc}<0$	$S_{23}\rightarrow S_{17}\rightarrow S_5\rightarrow S_5\rightarrow S_{17}\rightarrow S_{23}$
	$\Delta V_{NP}<0$	$i_{sc}\geq 0$	$S_{23}\rightarrow S_{17}\rightarrow S_5\rightarrow S_5\rightarrow S_{17}\rightarrow S_{23}$
		$i_{sc}<0$	$S_{11}\rightarrow S_{23}\rightarrow S_{17}\rightarrow S_{17}\rightarrow S_{23}\rightarrow S_{11}$
D_{16}	$\Delta V_{NP}\geq 0$	$i_{sb}\geq 0$	$S_6\rightarrow S_{24}\rightarrow S_{17}\rightarrow S_{17}\rightarrow S_{24}\rightarrow S_6$
		$i_{sb}<0$	$S_{24}\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_{24}$
	$\Delta V_{NP}<0$	$i_{sb}\geq 0$	$S_{24}\rightarrow S_{17}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{17}\rightarrow S_{24}$
		$i_{sb}<0$	$S_6\rightarrow S_{24}\rightarrow S_{17}\rightarrow S_{17}\rightarrow S_{24}\rightarrow S_6$
D_{17}	$\Delta V_{NP}\geq 0$	$i_{sb}\geq 0$	$S_6\rightarrow S_{24}\rightarrow S_{18}\rightarrow S_{18}\rightarrow S_{24}\rightarrow S_6$
		$i_{sb}<0$	$S_{24}\rightarrow S_{18}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{18}\rightarrow S_{24}$
	$\Delta V_{NP}<0$	$i_{sb}\geq 0$	$S_{24}\rightarrow S_{18}\rightarrow S_{12}\rightarrow S_{12}\rightarrow S_{18}\rightarrow S_{24}$
		$i_{sb}<0$	$S_6\rightarrow S_{24}\rightarrow S_{18}\rightarrow S_{18}\rightarrow S_{24}\rightarrow S_6$
D_{18}	$\Delta V_{NP}\geq 0$	$i_{sa}\geq 0$	$S_{13}\rightarrow S_{25}\rightarrow S_{18}\rightarrow S_{18}\rightarrow S_{25}\rightarrow S_{13}$
		$i_{sa}<0$	$S_{25}\rightarrow S_{18}\rightarrow S_7\rightarrow S_7\rightarrow S_{18}\rightarrow S_{25}$
	$\Delta V_{NP}<0$	$i_{sa}\geq 0$	$S_{25}\rightarrow S_{18}\rightarrow S_7\rightarrow S_7\rightarrow S_{18}\rightarrow S_{25}$
		$i_{sa}<0$	$S_{13}\rightarrow S_{25}\rightarrow S_{18}\rightarrow S_{18}\rightarrow S_{25}\rightarrow S_{13}$
D_{19}	$\Delta V_{NP}\geq 0$	$i_{sa}\geq 0$	$S_{13}\rightarrow S_{25}\rightarrow S_{19}\rightarrow S_{19}\rightarrow S_{25}\rightarrow S_{13}$
		$i_{sa}<0$	$S_{25}\rightarrow S_{19}\rightarrow S_7\rightarrow S_7\rightarrow S_{19}\rightarrow S_{25}$
	$\Delta V_{NP}<0$	$i_{sa}\geq 0$	$S_{25}\rightarrow S_{19}\rightarrow S_7\rightarrow S_7\rightarrow S_{19}\rightarrow S_{25}$
		$i_{sa}<0$	$S_{13}\rightarrow S_{25}\rightarrow S_{19}\rightarrow S_{19}\rightarrow S_{25}\rightarrow S_{13}$
D_{20}	$\Delta V_{NP}\geq 0$	$i_{sc}\geq 0$	$S_8\rightarrow S_{26}\rightarrow S_{19}\rightarrow S_{19}\rightarrow S_{26}\rightarrow S_8$
		$i_{sc}<0$	$S_{26}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{26}$
	$\Delta V_{NP}<0$	$i_{sc}\geq 0$	$S_{26}\rightarrow S_{19}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{19}\rightarrow S_{26}$
		$i_{sc}<0$	$S_8\rightarrow S_{26}\rightarrow S_{19}\rightarrow S_{19}\rightarrow S_{26}\rightarrow S_8$
D_{21}	$\Delta V_{NP}\geq 0$	$i_{sc}\geq 0$	$S_8\rightarrow S_{26}\rightarrow S_{20}\rightarrow S_{20}\rightarrow S_{26}\rightarrow S_8$
		$i_{sc}<0$	$S_{26}\rightarrow S_{20}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{20}\rightarrow S_{26}$
	$\Delta V_{NP}<0$	$i_{sc}\geq 0$	$S_{26}\rightarrow S_{20}\rightarrow S_{14}\rightarrow S_{14}\rightarrow S_{20}\rightarrow S_{26}$
		$i_{sc}<0$	$S_8\rightarrow S_{26}\rightarrow S_{20}\rightarrow S_{20}\rightarrow S_{26}\rightarrow S_8$
D_{22}	$\Delta V_{NP}\geq 0$	$i_{sb}\geq 0$	$S_{15}\rightarrow S_{27}\rightarrow S_{20}\rightarrow S_{20}\rightarrow S_{27}\rightarrow S_{15}$

		$i_{sb}<0$	$S_{27}\rightarrow S_{20}\rightarrow S_9\rightarrow S_9\rightarrow S_{20}\rightarrow S_{27}$
	$\Delta V_{NP}<0$	$i_{sb}\geq 0$	$S_{27}\rightarrow S_{20}\rightarrow S_9\rightarrow S_9\rightarrow S_{20}\rightarrow S_{27}$
		$i_{sb}<0$	$S_{15}\rightarrow S_{27}\rightarrow S_{20}\rightarrow S_{20}\rightarrow S_{27}\rightarrow S_{15}$
D_{23}	$\Delta V_{NP}\geq 0$	$i_{sb}\geq 0$	$S_{15}\rightarrow S_{27}\rightarrow S_{21}\rightarrow S_{21}\rightarrow S_{27}\rightarrow S_{15}$
		$i_{sb}<0$	$S_{27}\rightarrow S_{21}\rightarrow S_9\rightarrow S_9\rightarrow S_{21}\rightarrow S_{27}$
	$\Delta V_{NP}<0$	$i_{sb}\geq 0$	$S_{27}\rightarrow S_{21}\rightarrow S_9\rightarrow S_9\rightarrow S_{21}\rightarrow S_{27}$
		$i_{sb}<0$	$S_{15}\rightarrow S_{27}\rightarrow S_{21}\rightarrow S_{21}\rightarrow S_{27}\rightarrow S_{15}$
D_{24}	$\Delta V_{NP}\geq 0$	$i_{sa}\geq 0$	$S_4\rightarrow S_{22}\rightarrow S_{21}\rightarrow S_{21}\rightarrow S_{22}\rightarrow S_4$
		$i_{sa}<0$	$S_{22}\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_{22}$
	$\Delta V_{NP}<0$	$i_{sa}\geq 0$	$S_{22}\rightarrow S_{21}\rightarrow S_{10}\rightarrow S_{10}\rightarrow S_{21}\rightarrow S_{22}$
		$i_{sa}<0$	$S_4\rightarrow S_{22}\rightarrow S_{21}\rightarrow S_{21}\rightarrow S_{22}\rightarrow S_4$

APPENDIX B

PSO NPC MATLAB M-FILE CODE

```
K=100; %%population of particles
ITER=100;  %%Iterations
iters=1;
particles=zeros(K,9); %%Initialization of martix
pbest=zeros(K,9);
vel=zeros(K,7);
W=1.0; %%Inertial weight
alpha=0.9; %%Inertia Factor
P=zeros(6,2);
P(1,1)=0;P(2,1)=0;P(3,1)=0;P(4,1)=0;P(5,1)=0;P(6,1)=0;
P(1,2)=10;P(2,2)=200;P(3,2)=10;P(4,2)=100;P(5,2)=10;P(6,2)=10;
%%Range of PSO searching areas
for i=1:K
   particles(i,1)=unifrnd(0,10);
   particles(i,2)=unifrnd(0,200);
   particles(i,3)=unifrnd(0,10);
   particles(i,4)=unifrnd(0,100);
   particles(i,5)=unifrnd(0,10);
   particles(i,6)=unifrnd(0,10);
end
%% Initialization the PSO with random particle locations
for i=1:K
   a=particles(i,1);b=particles(i,2);c=particles(i,3);d=particles(i,4);
   e=particles(i,5);f=particles(i,6);
   sim('NPC_math_apr_01'); %%simulate matlab NPC model
   t=OUT.time;
   Z=stepinfo(OUT.signals.values,t);
   err1=Z.SettlingTime;
   err2=Z.Overshoot;
   particles(i,7)=mean([err1 err2/10]);
   if(Z.SettlingMax>=200 || Z.SettlingMin<=60)
      particles(i,7)=1000;
   end
   particles(i,8)=err1;
   particles(i,9)=err2;
end
% Initial global best location
[gbest,j]=min(particles(:,7));
gbestW=particles(j,:);
for i=1:K
   pbest(i,1)=gbestW(1)+abs(normrnd(0,0.5));
```

```
    pbest(i,2)=gbestW(2)+abs(normrnd(0,0.5));
    pbest(i,3)=gbestW(3)+abs(normrnd(0,0.5));
    pbest(i,4)=gbestW(4)+abs(normrnd(0,0.5));
    pbest(i,5)=gbestW(5)+abs(normrnd(0,0.5));
    pbest(i,6)=gbestW(6)+abs(normrnd(0,0.5));
end
[gbest,j]=min(particles(:,7));
gbestW=particles(j,:);
% Setting initial pbest locations
for i=1:K
    a=pbest(i,1);b=pbest(i,2);c=pbest(i,3);d=pbest(i,4);
    e=pbest(i,5);f=pbest(i,6);
    sim('NPC_math_apr_01');
    t=OUT.time;
    Z=stepinfo(OUT.signals.values,t);
    err1=Z.SettlingTime;
    err2=Z.Overshoot;
    pbest(i,7)=mean([err1 err2/10]);
    if(Z.SettlingMax>=200 || Z.SettlingMin<=60)
        pbest(i,7)=1000;
    end
    pbest(i,8)=err1;
    pbest(i,9)=err2;
end
%% Starting the PSO algorithm
while(iters<=ITER)
    for i=1:K
        for j=1:6
            x=particles(i,:);
            vel(i,j)=vel(i,j)*W+2*unifrnd(0,1)*(pbest(i,j)-x(j))+2*unifrnd(0,1)*(gbestW(j)-
x(j));
            x(j)=x(j)+vel(i,j);
            if((x(j)<=P(j,2))&&((x(j)>=P(j,1))))
                particles(i,j)=x(j);
            end
        end
    end
    for i=1:K
        a=particles(i,1);b=particles(i,2);c=particles(i,3);d=particles(i,4);
        e=particles(i,5);f=particles(i,6);
        sim('NPC_math_apr_01');
        t=OUT.time;
        Z=stepinfo(OUT.signals.values,t);
        err1=Z.SettlingTime;
        err2=Z.Overshoot;
        particles(i,7)=mean([err1 err2/10]);
```

```
        if(Z.SettlingMax>=200 || Z.SettlingMin<=60)
            particles(i,7)=1000;
        end
        if(particles(i,7)<pbest(i,7))
            pbest(i,:)=particles(i,:);
        end
    end
    [gbest,j]=min(pbest(:,7));
    if(gbest<gbestW(7))
        gbestW=pbest(j,:);
    end
    W=2*W/(1+exp((iters*alpha)/ITER));
    iters=iters+1;
end
disp('the optimal answer is in the order:')
disp('first P value, first I, second K, second I')
optimal=[gbestW(1) gbestW(2) gbestW(3) gbestW(4) gbestW(5) gbestW(6)]
```

REFERENCES

[1] Read, J.C., “Mercury-arc rectifiers for medium-voltage application. A review of progress”, *IET Journals,* November 1952, vol.9, pp. 252

[2] Bimal K.Bose, “Modern Power Electronics and AC Drives”, Prentice Hall PTR Prentice-Hall, Inc, 2002

[3] IEEE Std 519-1992, IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems

[4] Bell, S.; Sung, J.; , "Will your motor insulation survive a new adjustable frequency drive?," *Petroleum and Chemical Industry Conference, 1996, Record of Conference Papers. The Institute of Electrical and Electronics Engineers Incorporated Industry Applications Society 43rd Annual* , vol., no., pp.125-130, 23-25 Sep 1996

[5] Chongwei Z, Xing Z, “PWM rectifier and its Control”, China Machine Press

[6] Nabae, Akira; Takahashi, Isao; Akagi, Hirofumi; , "A New Neutral-Point-Clamped PWM Inverter," *Industry Applications, IEEE Transactions on* , vol.IA-17, no.5, pp.518-523, Sept. 1981

[7] Tolbert, L.M.; Peng, F.Z.; , "Multilevel converters for large electric drives," *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual* , vol.2, no., pp.530-536 vol.2, 15-19 Feb 1998

[8] D. Grahame Holmes; Thomas A. Lipo, “Pulse Width Modulation for Power Converters”, IEEE Series on Power Engineering, 2003

[9] Escobar, G.; Leyva-Ramos, J.; Carrasco, J.M.; Galvan, E.; Portillo, R.C.; Prats, M.M.; Franquelo, L.G.; , "Modeling of a three level converter used in a synchronous rectifier application," *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* , vol.6, no., pp. 4306- 4311 Vol.6, 20-25 June 2004

[10] Wei Chen; Yunping Zou; Lijuan Xu; , "Direct power control for Neutral-point-clamped three-level PWM rectifier," *Industrial Technology, 2008. ICIT 2008. IEEE International Conference on* , vol., no., pp.1-6, 21-24 April 2008

[11] Celanovic, N.; Borojevic, D.; , "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual* , vol.1, no., pp.535-541 vol.1, 14-18 Mar 1999

[12] Paul C. Krause, Oleg Wasynczuk, Scott D. Sudhoff, “Analysis of Electric Machinery and Drive Systems”, Wiley-Interscience Publication, IEEE Press Power Engineering Series

[13] Robert W. Erickson, Dragan Maksimoic, “Fundamentals of Power Electronics” second edition, Springer Science+Business Media, LLC

[14] Katsuhiko Ogata, “Modern Control Engineering (Forth Edition)”, Pearson Education Asia Limited and Tsinghua University Press

[15] Andries P. Engelbrecht, “Fundamentals of Computational Swarm Intelligence”, John Wiley & Sons, Ltd

[16] Emami, S.A.; Poudeh, M.B.; Eshtehardiha, S.; , "Particle Swarm Optimization for improved performance of PID controller on Buck converter," *Mechatronics and Automation, 2008. ICMA 2008. IEEE International Conference on* , vol., no., pp.520-524, 5-8 Aug. 2008

[17] Edrington, C. S.; Liu, Y.; Leonard, J.; Henry, S.; Balathandayuthapani, S.; , "Rapid protyping CHIL methodology for advanced converter studies," *Electric Ship Technologies Symposium (ESTS), 2011 IEEE* , vol., no., pp.370-373, 10-13 April 2011

[18] Meng YongQing; Liu Zheng; Shen ChuanWen; Liang Yi; Su YanMin; Yu Ting; , "Study on Mathematical Model and Lyapunov-Based Control for Three-Level NPC Voltage-Source Rectifier," *Industrial Electronics, 2006 IEEE International Symposium on* , vol.2, no., pp.1949-1954, 9-13 July 2006

[19] Lei Lin; Yunping Zou; Zhan Wang; Hongyuan Jin; , "Modeling and Control of Neutral-point Voltage Balancing Problem in Three-level NPC PWM Inverters," *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th* , vol., no., pp.861-866, 16-16 June 2005

[20] N. Celanovic, “Space vector modulation and control of multilevel converters” Ph. D. Dissertation, Virginia Power Electronics Center (VPEC). Virginia Polytechnic Institute & State University, Blacksburg, VA (USA), 2000

[21] Wang Hui; Chen Jihua; Huang Shoudao; Wang Yaonan; , "The investigation of PWM rectifier control method," *Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International* , vol.2, no., pp.673-675 Vol.2, 14-16 Aug. 2004

[22] Wei Sun; Zhe Chen; Xiaojie Wu; , "Intelligent optimize design of LCL filter for three-phase voltage-source PWM rectifier," *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International* , vol., no., pp.970-974, 17-20 May 2009

[23] Banerjee, T.; Choudhuri, S.; Bera, J.; Maity, A.; , "Off-line optimization of PI and PID controller for a vector controlled induction motor drive using PSO," *Electrical and Computer Engineering (ICECE), 2010 International Conference on* , vol., no., pp.74-77, 18-20 Dec. 2010

[24] Chun-Yu Du; Gwo-Ruey Yu; , "Optimal PI Control of a Permanent Magnet Synchronous Motor Using Particle Swarm Optimization," *Innovative Computing, Information and Control, 2007. ICICIC '07. Second International Conference on* , vol., no., pp.255, 5-7 Sept. 2007

[25] Fleming Fletcher, "Development and Implementation of a 25 KVA Phasor-based Virtual Machine," Master thesis, Florida State University, Tallahassee, FL, USA, 2010

[26] Yu Liu; Zhengping Xi; Zhigang Liang; Wenchao Song; Bhattacharya, S.; Huang, A.; Langston, J.; Steurer, M.; Litzenberger, W.; Anderson, L.; Adapa, R.; Sundaram, A.; , "Controller hardware-in-the-loop validation for a 10 MVA ETO-based STATCOM for wind farm application," *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE* , vol., no., pp.1398-1403, 20-24 Sept. 2009

[27] dSPACE Inc, dSPACE™ 1103 V6.5 Manual, 2007

[28] RTD® Technologies, Real Time Digital Simulation for the Power Industry Manual Set for RSCDA V2.013.3, RTD®, 2009

BIOGRAPHICAL SKETCH

Yusi Liu (IEEE Student Member since 2009) was born in Changsha, Hunan Province, China on February 8, 1986. He received his B.S. degree in Electrical Engineering in June 2008 from Hunan University, in Changsha, Hunan Province, China. He worked in China CEC Engineering Corporation as an electrical engineer before he joined the Florida State University in 2009 to purse his MS in the department of Electrical and Computer Engineering. Since September 2009, he has been working as a graduate research assistant under Dr. Chris S. Edrington at the Center for Advanced Power Systems.