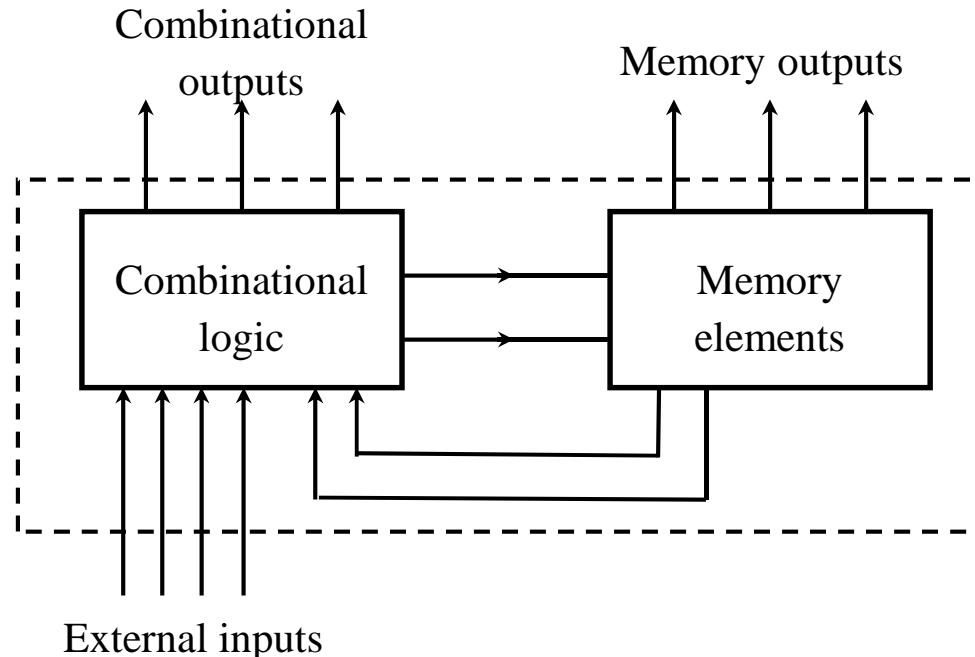


Digital Electronics and Microprocessors

Class 8

CHHAYADEVI BHAMARE

- A **sequential circuit** consists of a *feedback path*, and employs some *memory elements*.
-

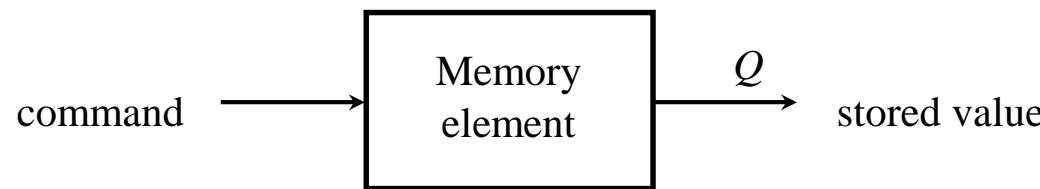


Sequential circuit = Combinational logic + Memory Elements



- There are two types of sequential circuits:
 - ❖ *synchronous*: outputs change only at specific time
 - ❖ *asynchronous*: outputs change at any time
- *Multivibrator*: a class of sequential circuits. They can be:
 - ❖ *bistable* (2 stable states)
 - ❖ *monostable* or *one-shot* (1 stable state)
 - ❖ *astable* (no stable state)
- Bistable logic devices: *latches* and *flip-flops*.
- Latches and flip-flops differ in the method used for changing their state.

■ **Memory element**: a device which can remember value indefinitely, or change value on command from its inputs.



■ **Characteristic table:**

Command (at time t)	$Q(t)$	$Q(t+1)$
Set	X	1
Reset	X	0
Memorise / No Change	0	0
	1	1

Q_n or $Q(t)$: **current state**

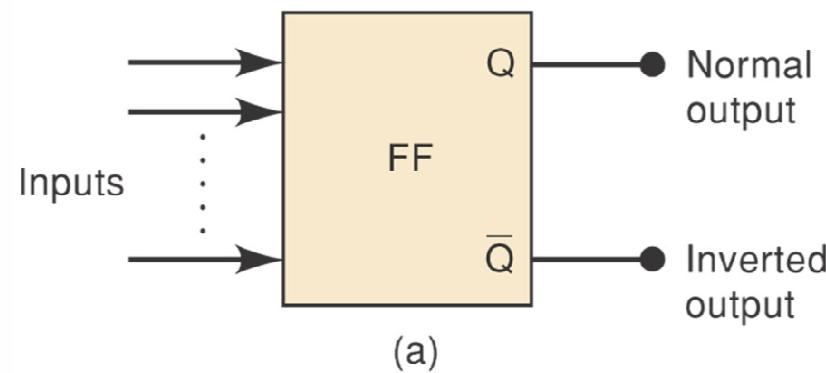
$Q(n+1)$ or $Q(t+1)$ or Q^+ : **next state**

Flip-Flops and their applications (Sequential Circuits) (Chapter5-T1)

- Logic circuits studied so far have outputs that respond immediately to inputs at some instant in time.
- We now introduce the concept of memory. The flip-flop, abbreviated FF, is a key memory element.
- The outputs of a flip flop are Q and Q'
- Q is understood to be the normal output, Q' is always the opposite.
- When the normal output (Q) is placed in the high or 1 state we say the FF has been set.
- When the normal output (Q) is placed in the low or 0 state we say the FF has been cleared or reset.



General flip-flop symbol and definition of its two possible output states.



Output states	
$Q = 1, \bar{Q} = 0:$	called HIGH or 1 state; also called SET state
$Q = 0, \bar{Q} = 1:$	called LOW or 0 state; also called CLEAR or RESET state

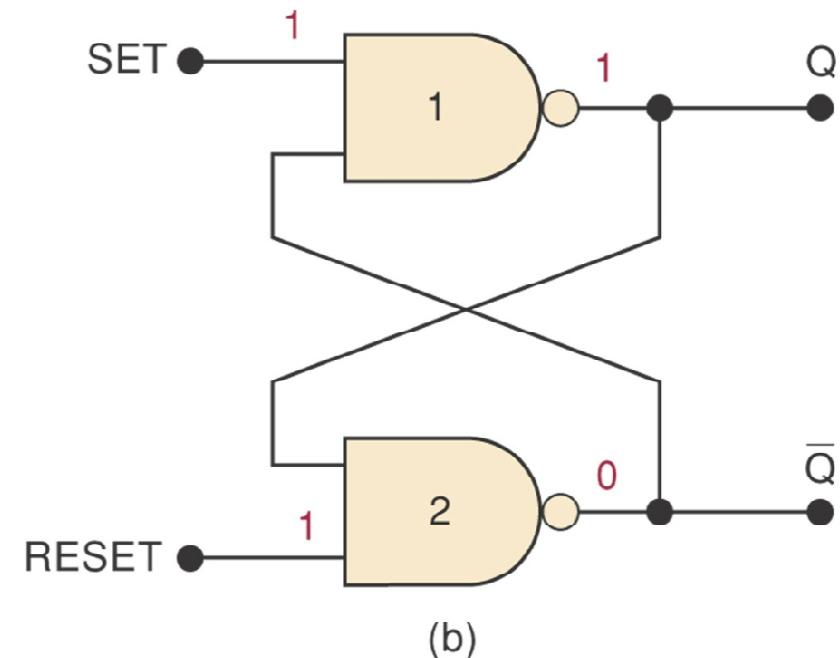
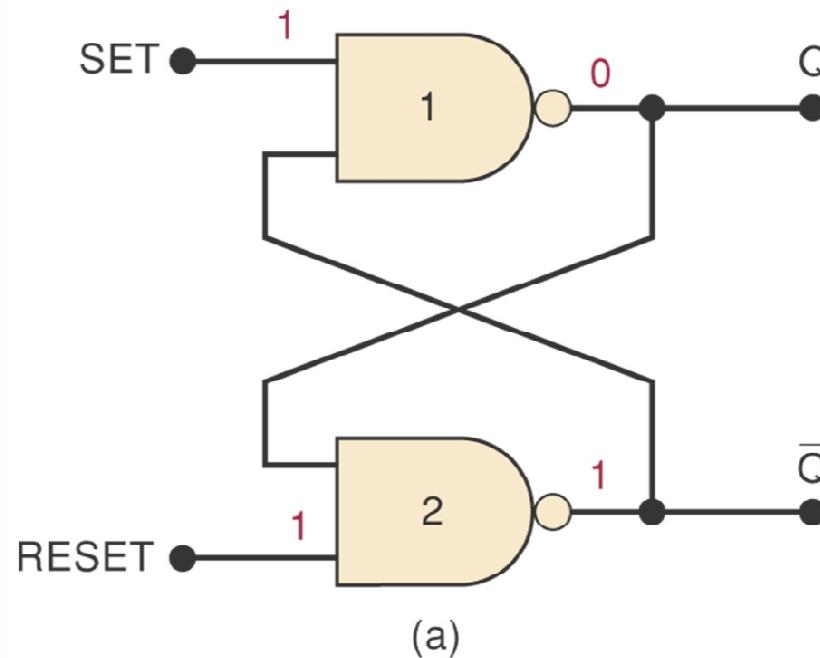
(b)

NAND Gate Latch

- The NAND gate latch or simply latch is a basic FF.
- The inputs are set and clear (reset)
- The inputs are active low, that is, the output will change when the input is pulsed low.
- When the latch is set
$$Q = 1 \text{ and } \bar{Q} = 0$$
- When the latch is clear or reset
$$Q = 0 \text{ and } \bar{Q} = 1$$

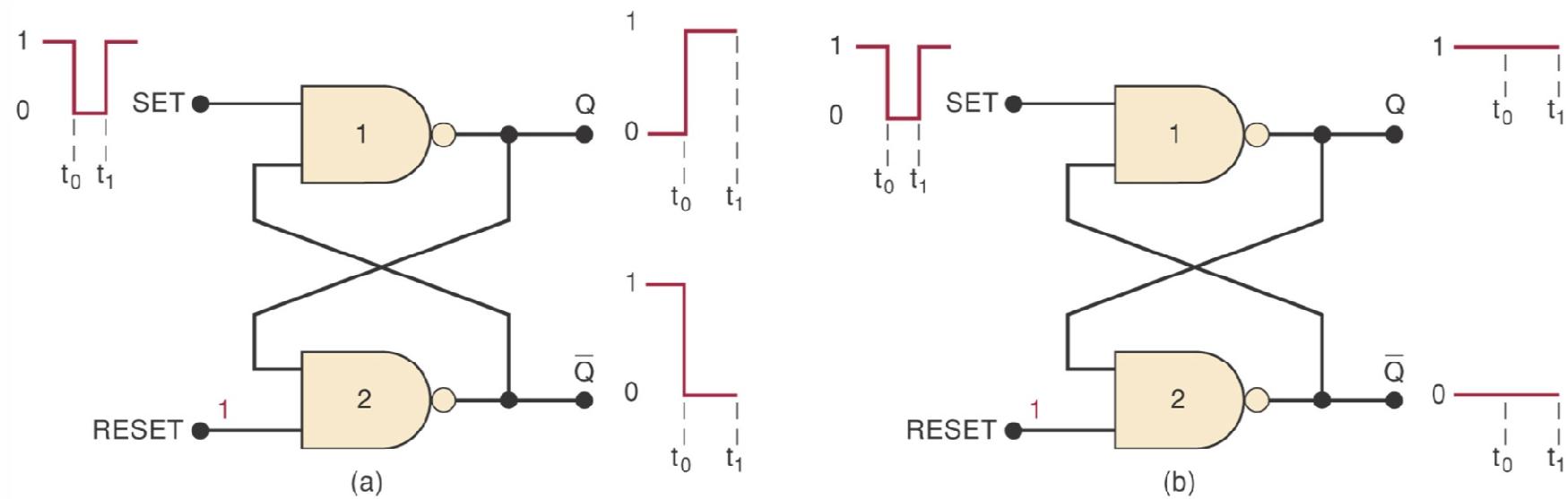


A NAND latch has two possible resting states when SET = RESET = 1.



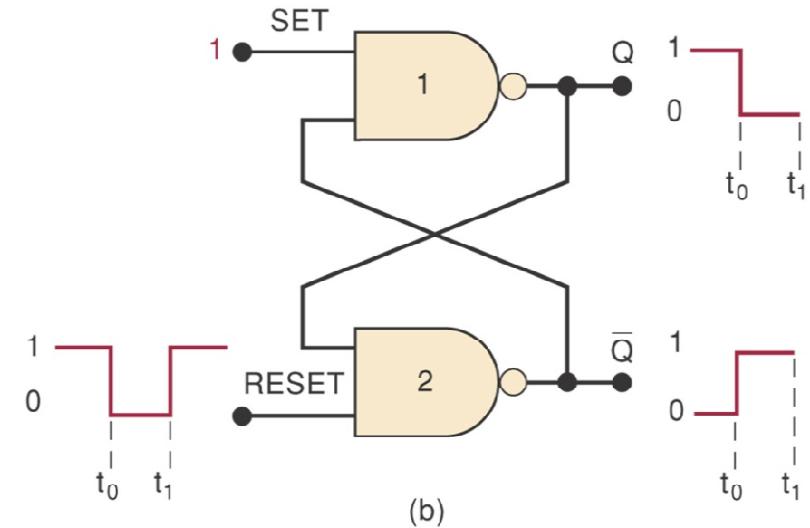
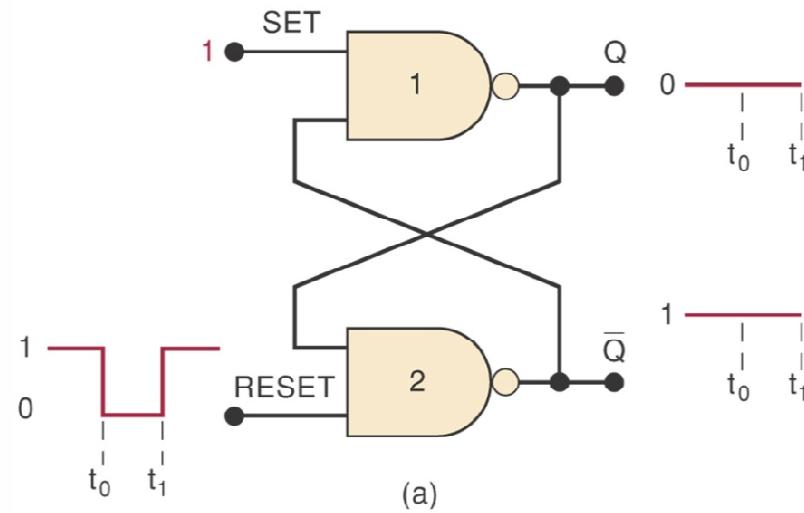


Pulsing the SET input to the 0 state when (a) $Q = 0$ prior to SET pulse; (b) $Q = 1$ prior to SET pulse. Note that, in both cases, Q ends up HIGH.



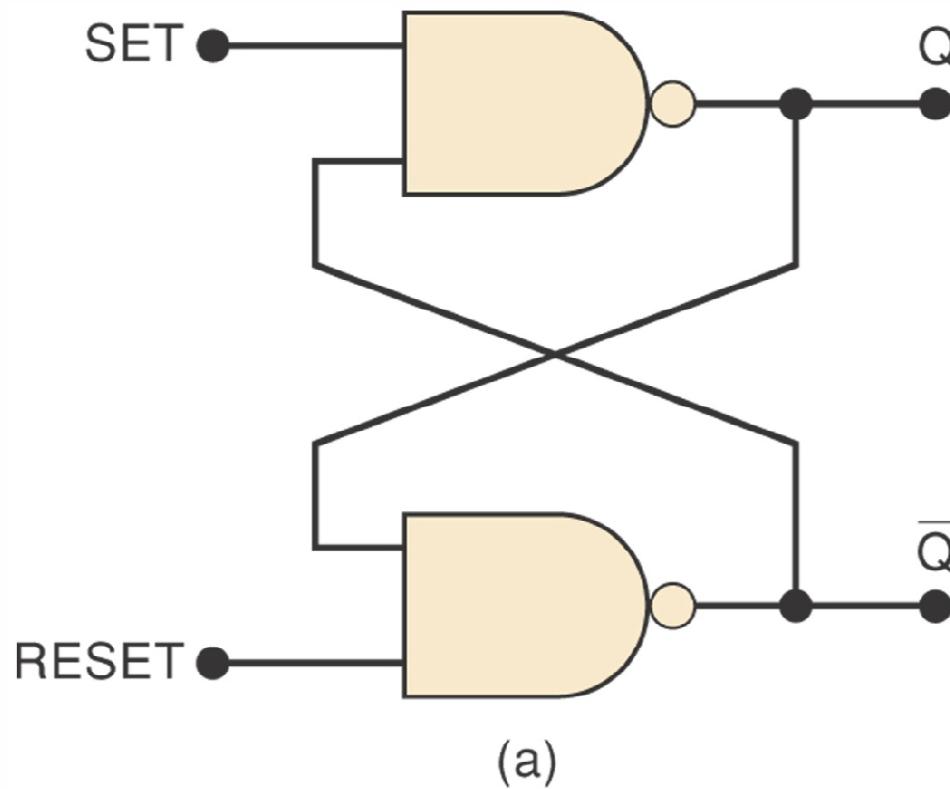


Pulsing the RESET input to the LOW state when (a) $Q = 0$ prior to RESET pulse; (b) $Q = 1$ prior to RESET pulse. In each case, Q ends up LOW.





(a) NAND latch; (b) function table.



Set	Reset	Output
1	1	No change
0	1	$Q = 1$
1	0	$Q = 0$
0	0	Invalid*

*Produces $Q = \bar{Q} = 1$.

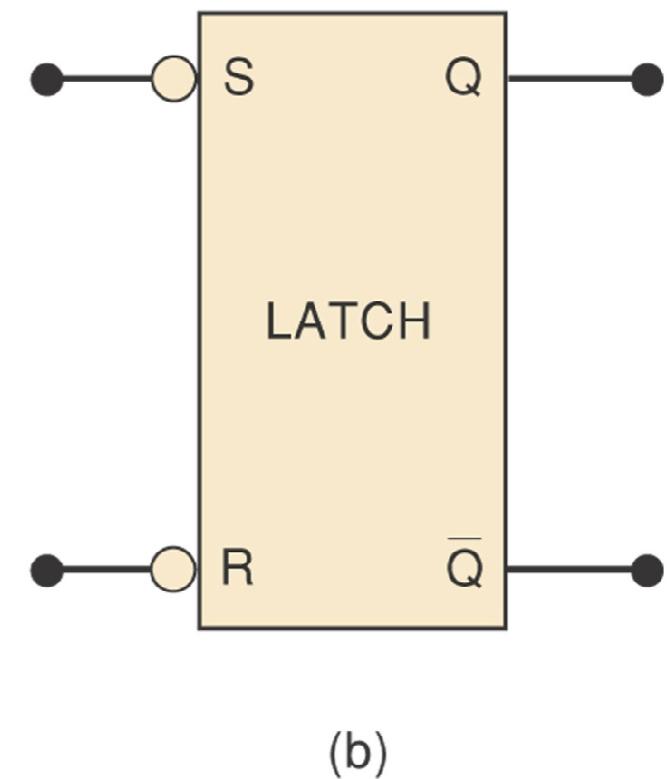
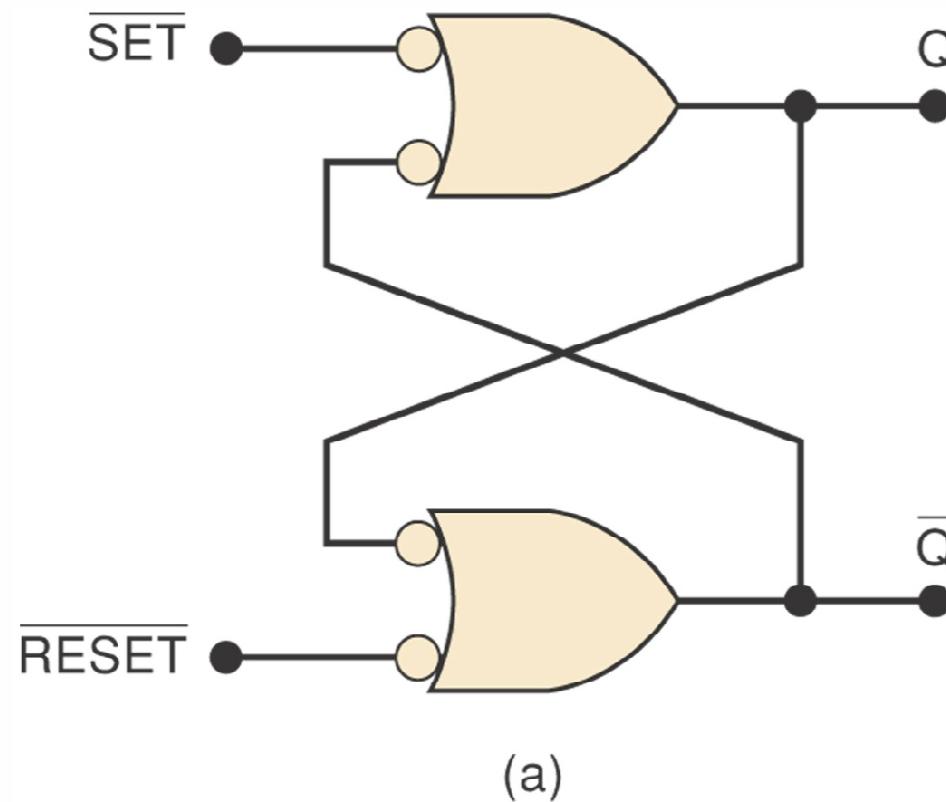
(b)

Summary of the NAND Gate Latch

- SET = RESET = 1. Normal resting state, outputs remain in state prior to input.
- SET = 0, RESET = 1. Q will go high and remain high even if the SET input goes high.
- SET = 0, RESET = 0. Q will go low and remain low even if the RESET input goes high.
- SET = RESET = 0. Output is unpredictable because the latch is being set and reset at the same time.



(a) NAND latch equivalent representation; (b) simplified block symbol.

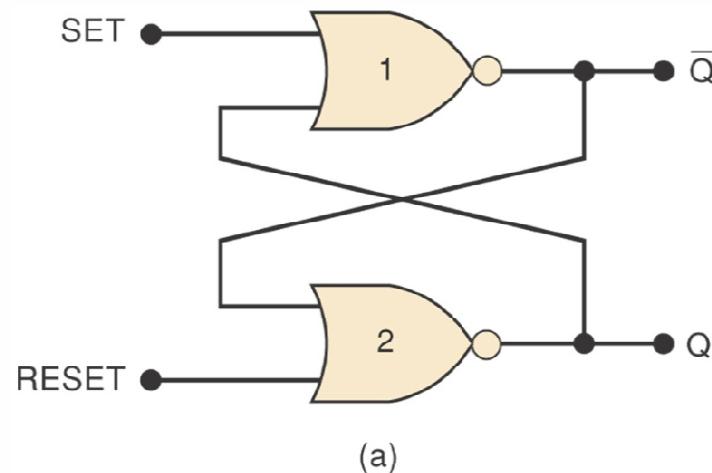


NOR Gate Latch

- The NOR latch is similar to the NAND latch except that the Q and \overline{Q} outputs are reversed.
- The SET and RESET inputs are active high, that is, the output will change when the input is pulsed high.
- In order to ensure that a FF begins operation at a known level, a pulse may be applied to the SET or RESET inputs when a device is powered up.



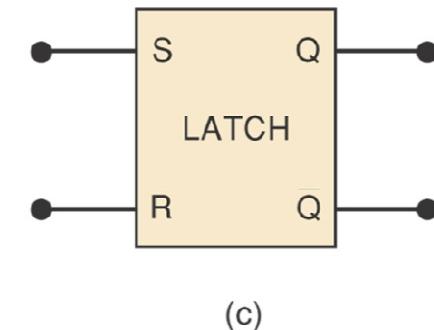
(a) NOR gate latch; (b) function table; (c) simplified block symbol.



Set	Reset	Output
0	0	No change
1	0	$Q = 1$
0	1	$Q = 0$
1	1	Invalid*

*Produces $Q = \bar{Q} = 0$.

(b)

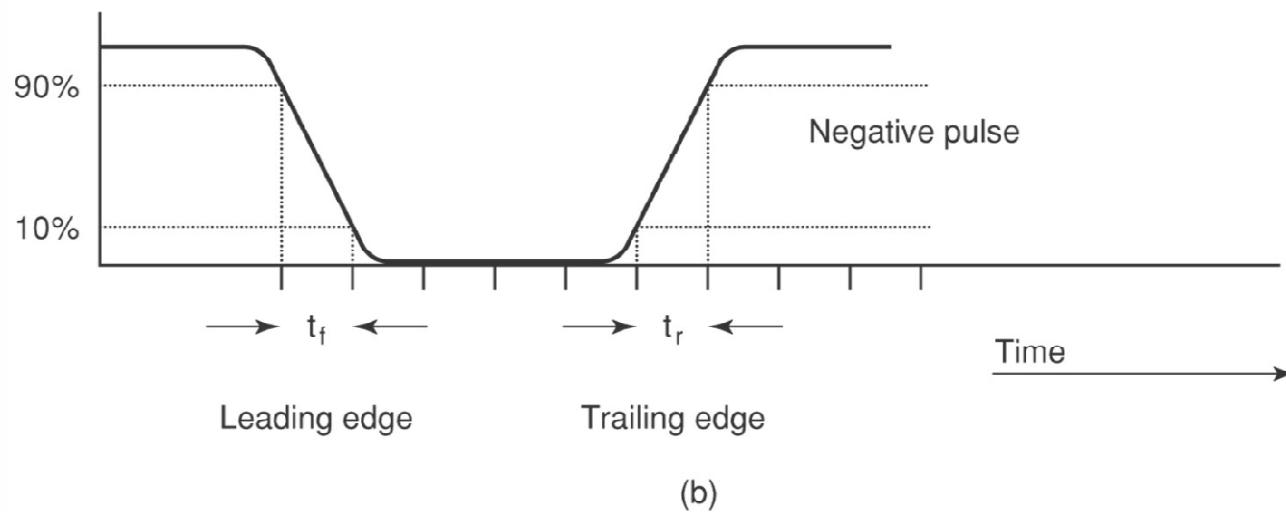
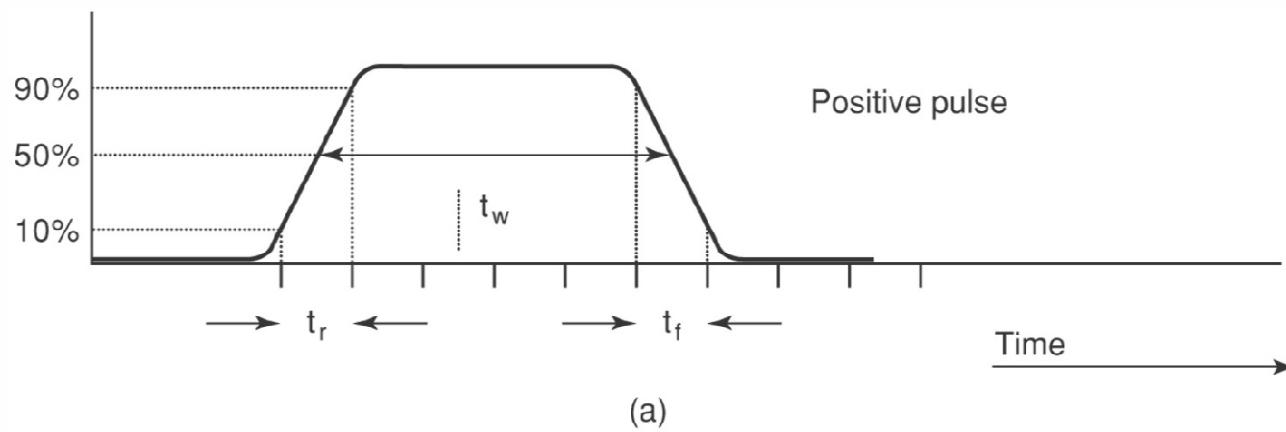


Digital Pulses

- Signals that switch between active and inactive states are called pulse waveforms.
 - A positive pulse has an active high level.
 - A negative pulse has an active low level.



(a) A positive pulse and (b) a negative pulse.



Digital Pulses

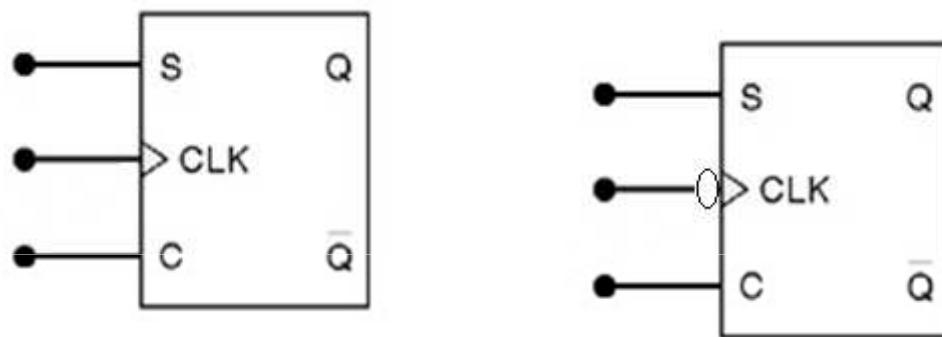
- The transition from low to high on a positive pulse is called rise time (t_r).
 - Rise time is measured between the 10% and 90% points on the leading edge of the voltage waveform.
- The transition from high to low on a positive pulse is called fall time (t_f).
 - Fall time is measured between the 90% and 10% points on the trailing edge of the voltage waveform.

Clock Signals and Clocked Flip-Flops

- Asynchronous digital system – outputs can change state at any time the input(s) change.
- Synchronous digital system – output can change state only at a specific time in the clock cycle.
 - The clock signal is a rectangular pulse train or square wave.
 - Positive going transition (PGT) – when clock pulse goes from 0 to 1.
 - Negative going transition (NGT) – when clock pulse goes from 1 to 0.
 - Transitions are also called edges.

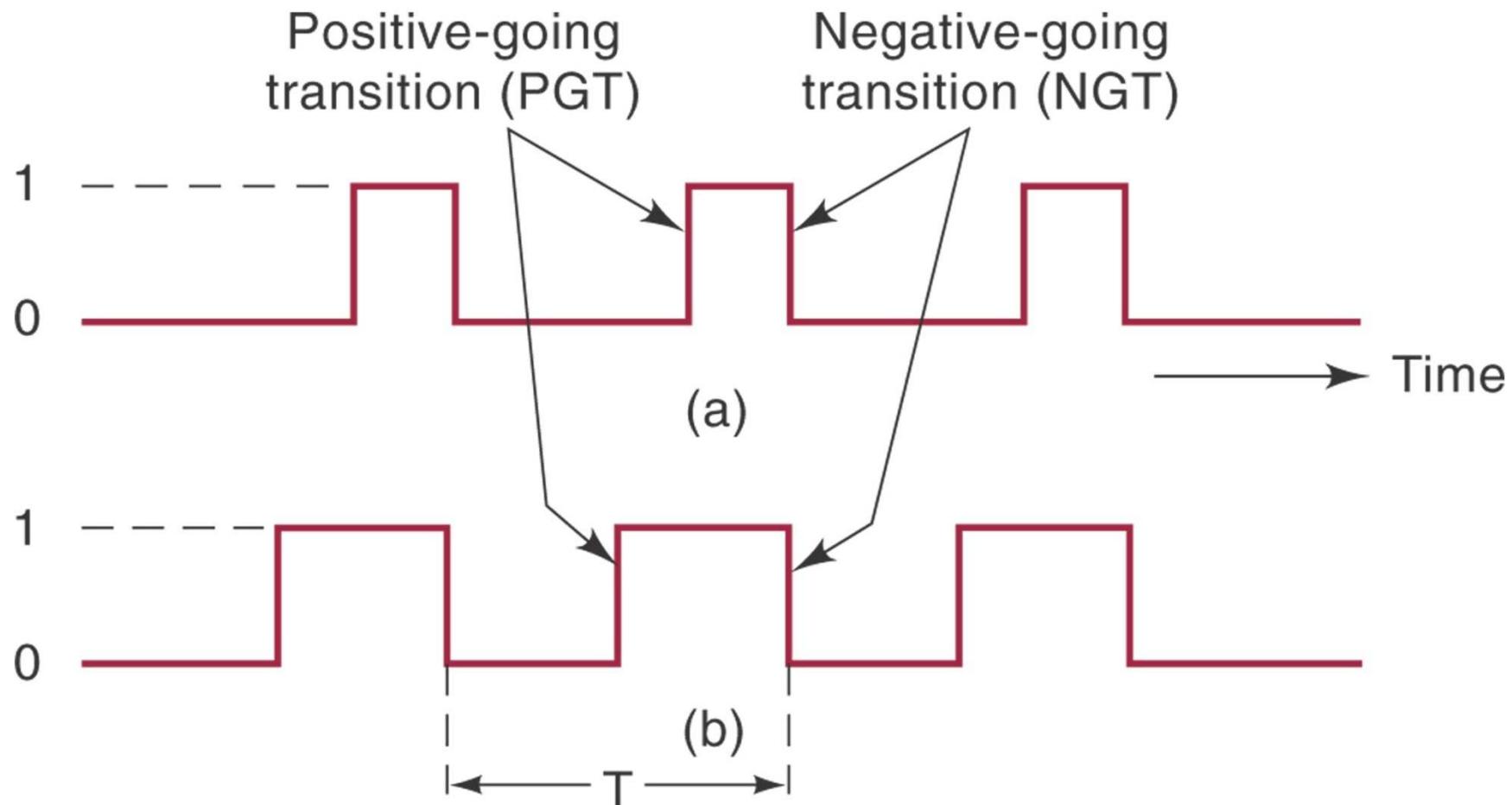
Clock Signals and Clocked Flip-Flops

- Clocked FFs change state on one or the other clock transitions. Some common characteristics:
 - Clock inputs are labeled CLK, CK, or CP.
 - A small triangle at the CLK input indicates that the input is activated with a PGT. 
 - A bubble and a triangle indicates that the CLK input is activated with a NGT.
 - Control inputs have an effect on the output only at the active clock transition (NGT or PGT). These are also called synchronous control inputs.
 - The control inputs get the FF outputs ready to change, but the change is not triggered until the CLK edge.





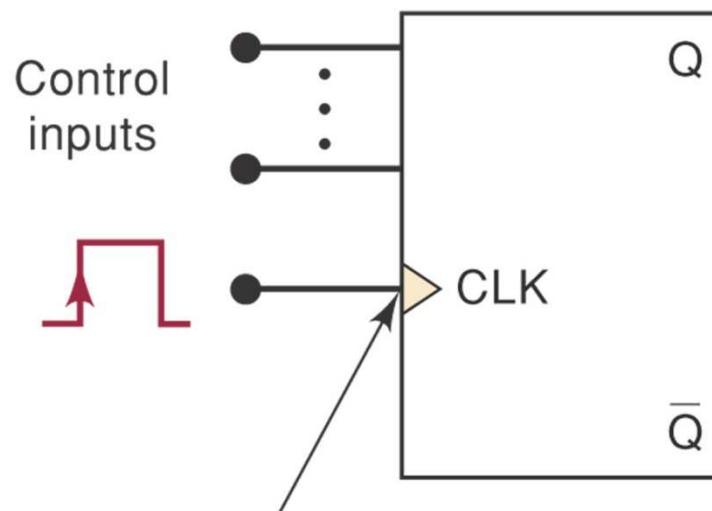
Clock signals.



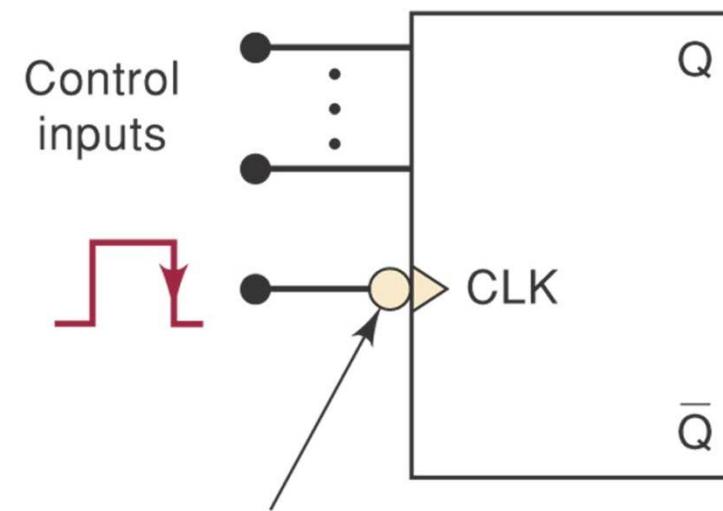
Clock Signals and Clocked Flip-Flops

- Setup time (t_S) is the minimum time interval before the active CLK transition that the control input must be kept at the proper level.
- Hold time (t_H) is the time following the active transition of the CLK during which the control input must be kept at the proper level.

Clocked FFs have a clock input (*CLK*) that is active on either (a) the PGT or (b) the NGT. The control inputs determine the effect of the active clock transition.



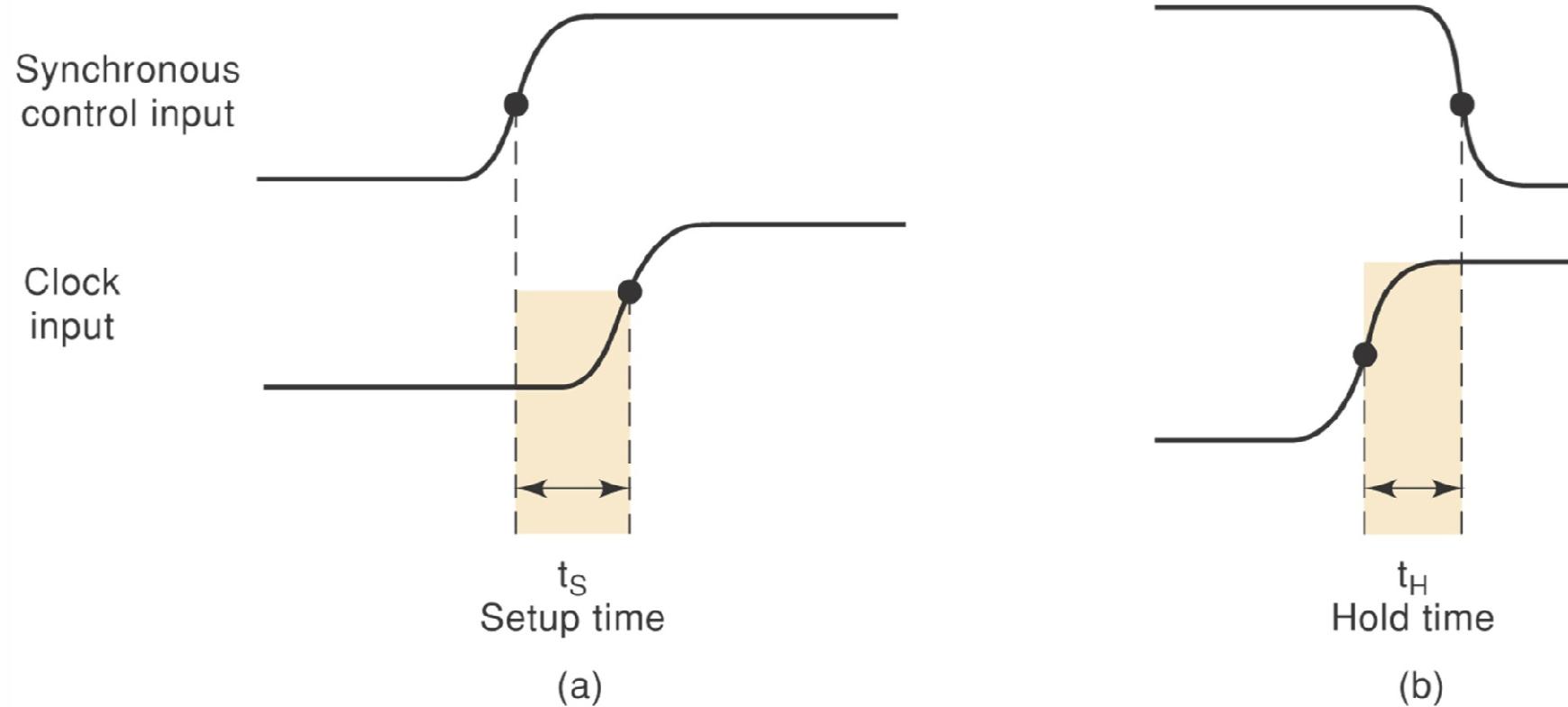
(a)



(b)

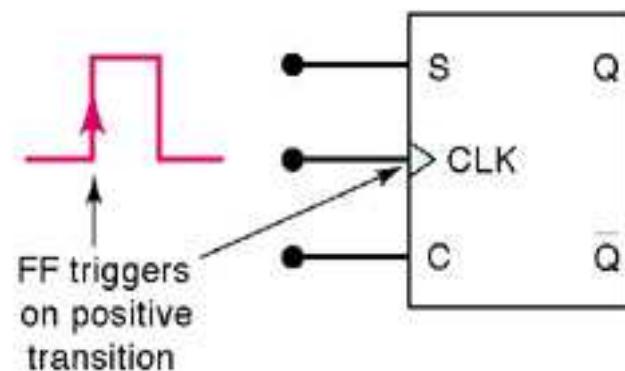


Control inputs must be held stable for (a) a time t_S prior to active clock transition and for (b) a time t_H after the active block transition.



Clocked S-R Flip-Flop

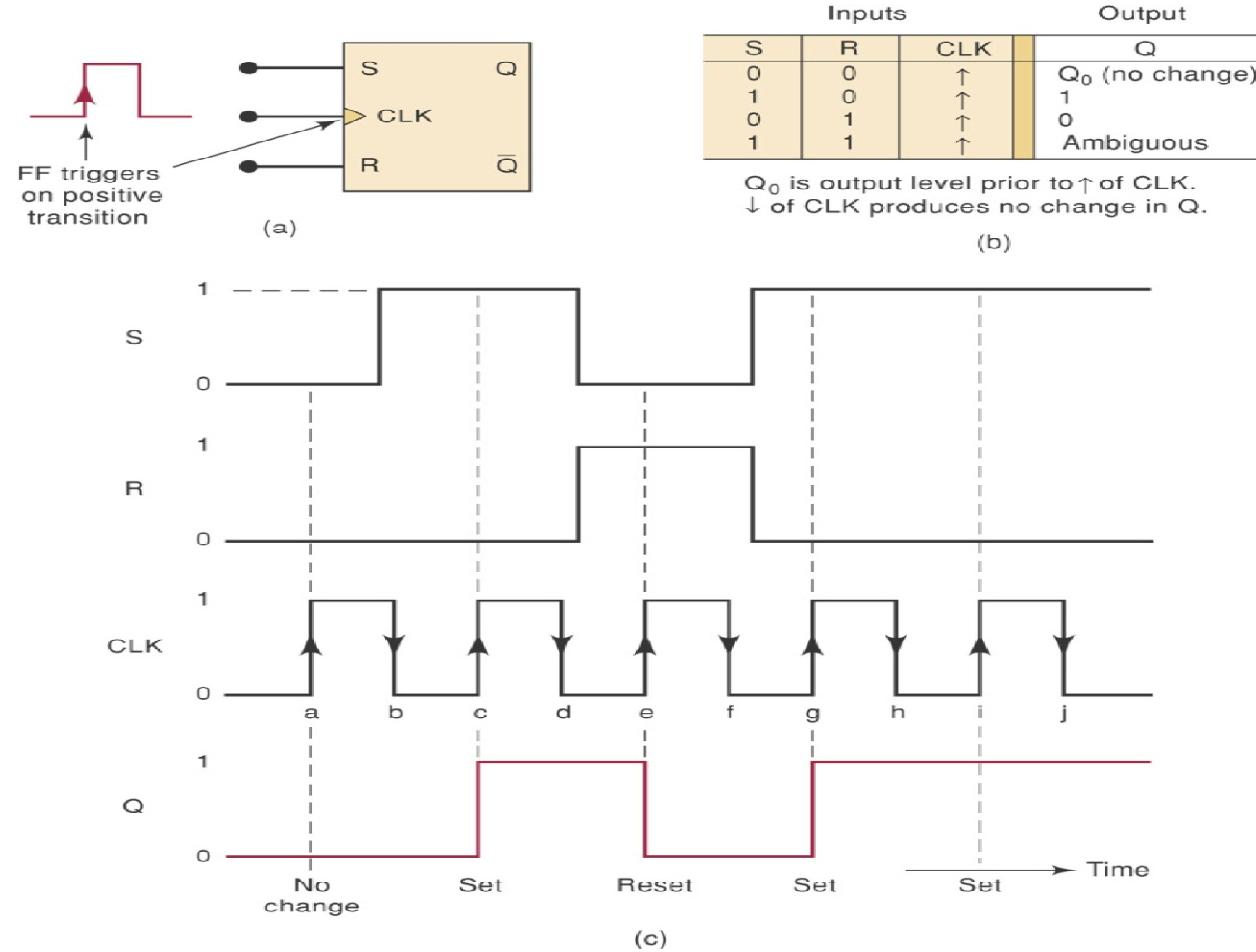
- The SET-RESET (or SET-CLEAR) FF will change states at the positive going or negative going clock edge.



Inputs			Output
S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

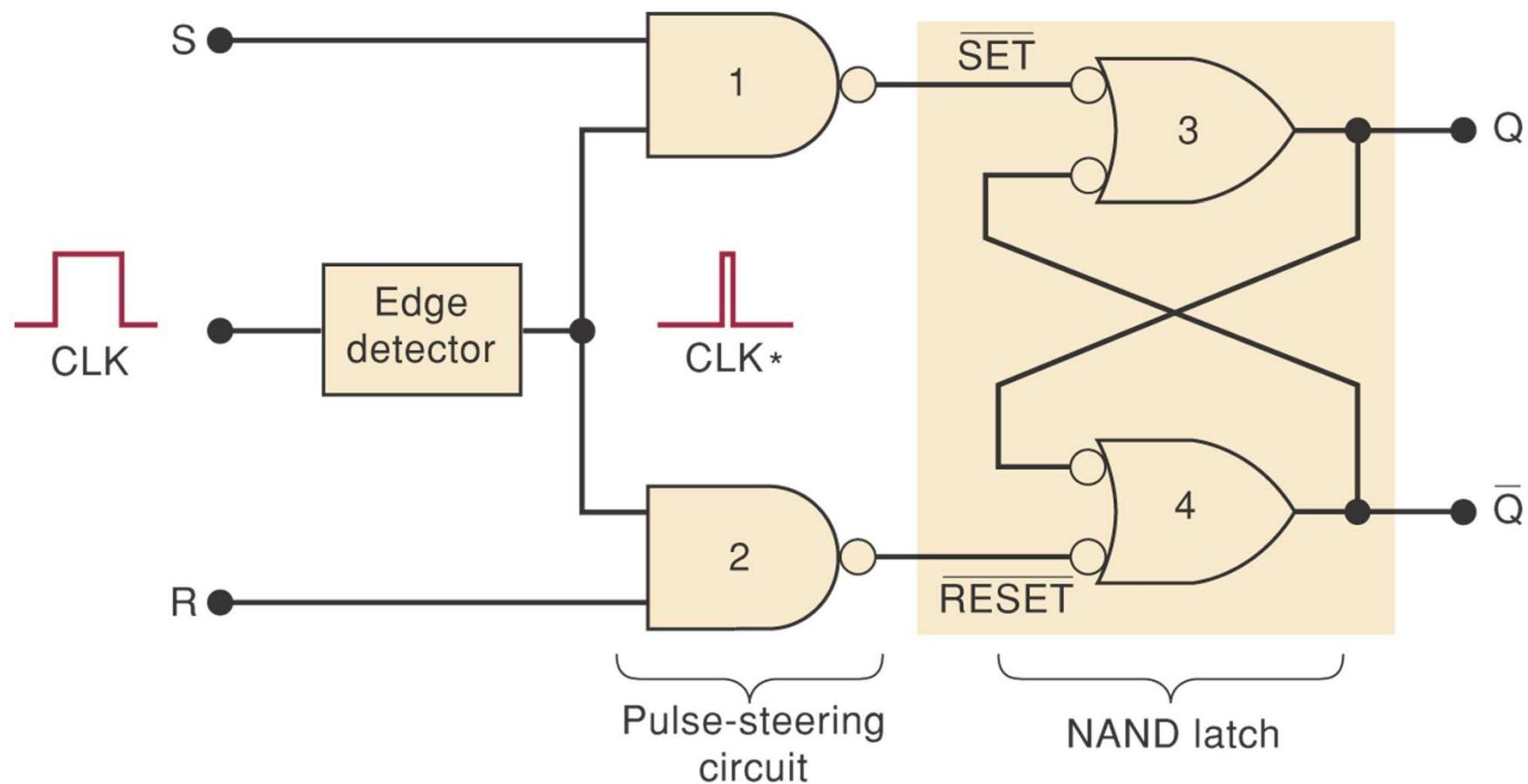
Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

(a) Clocked S-R flip-flop that responds only to the positive-going edge of a clock pulse; (b) function table; (c) typical waveforms.



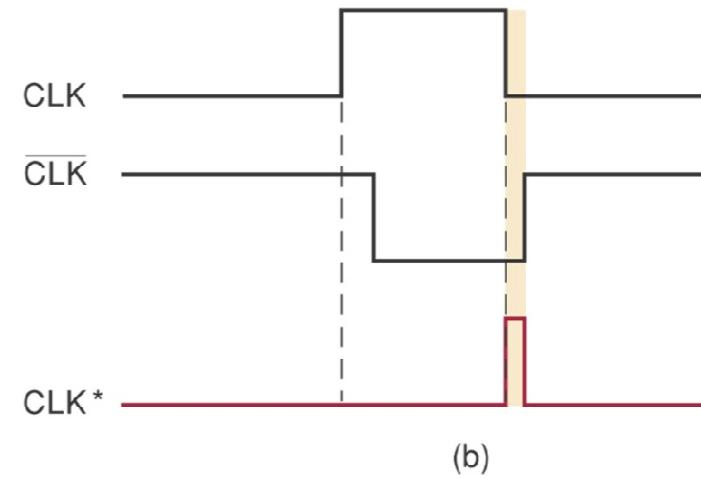
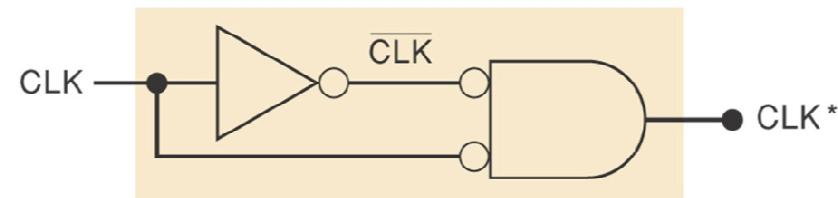
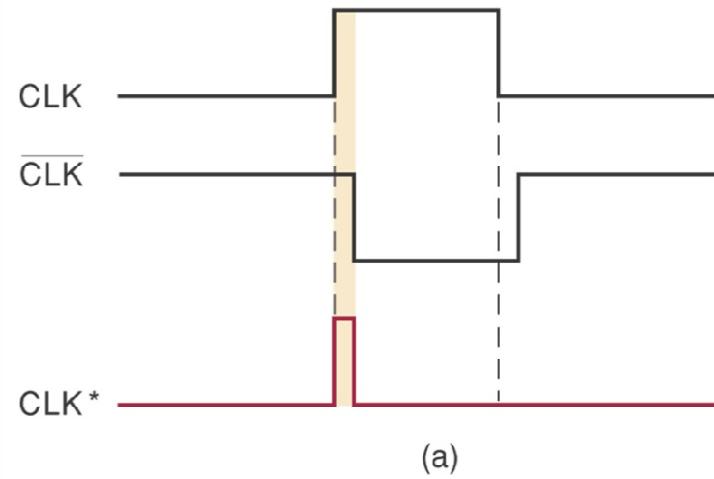
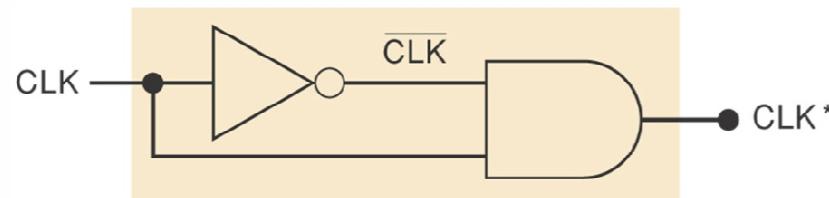


Simplified version of the internal circuitry for an edge-triggered S-R flip-flop.





Implementation of edge-detector circuits used in edge-triggered flip-flops: (a) PGT; (b) NGT. The duration of the CLK^* pulses is typically 2–5 ns.

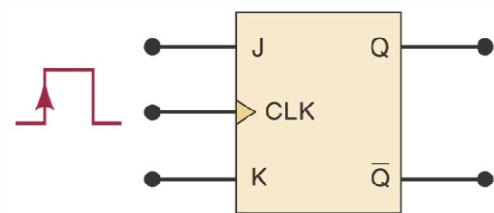


Clocked J-K Flip-Flop

- Operates like the S-C FF. J is set, K is clear.
- When J and K are both high the output is toggled from whatever state it is in to the opposite state.
- May be positive going or negative going clock trigger.
- Has the ability to do everything the S-C FF does, plus operate in toggle mode.

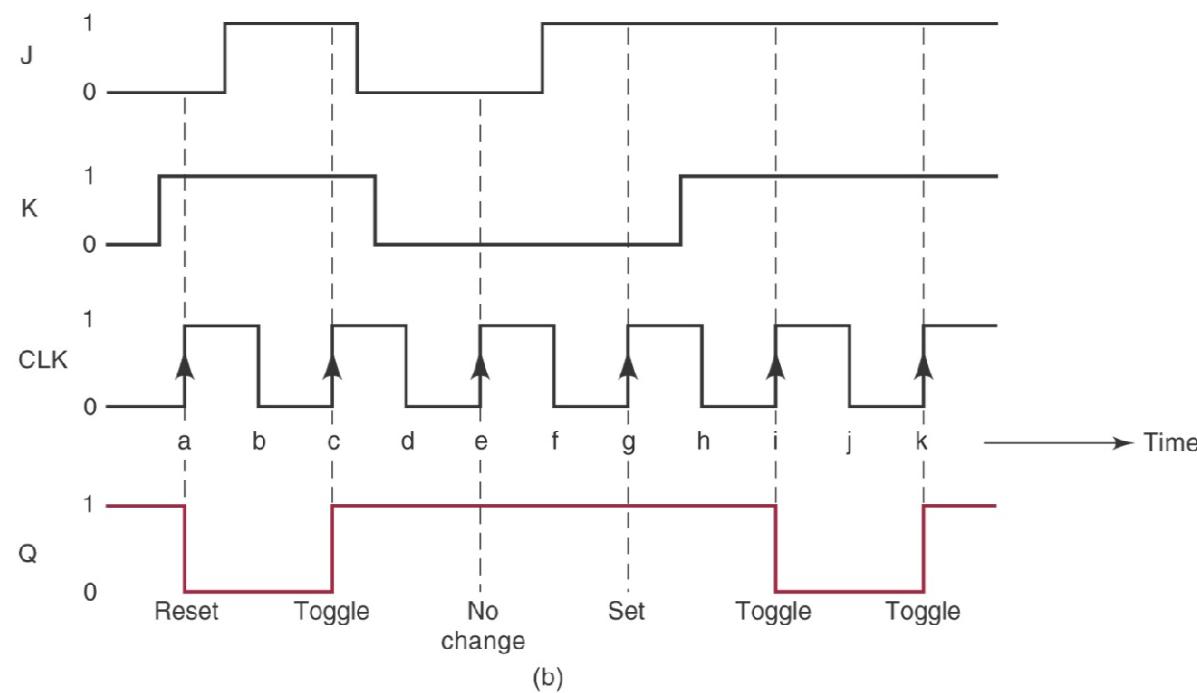


(a) Clocked J-K flip-flop that responds only to the positive edge of the clock; (b) waveforms.



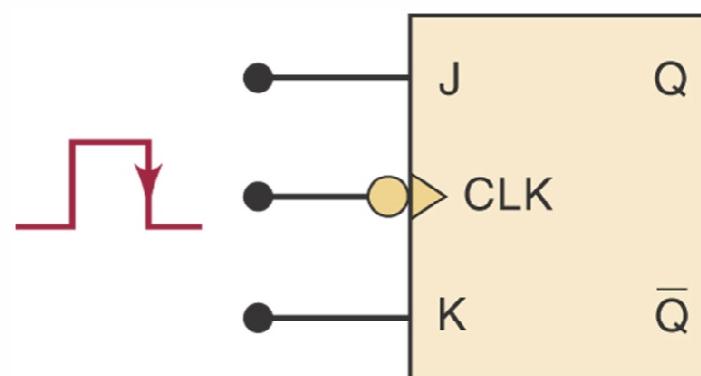
J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Q_0 (toggles)

(a)





J-K flip-flop that triggers only on negative-going transitions.



J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	\bar{Q}_0 (toggles)



Internal circuit of the edge-triggered J-K flip-flop.

