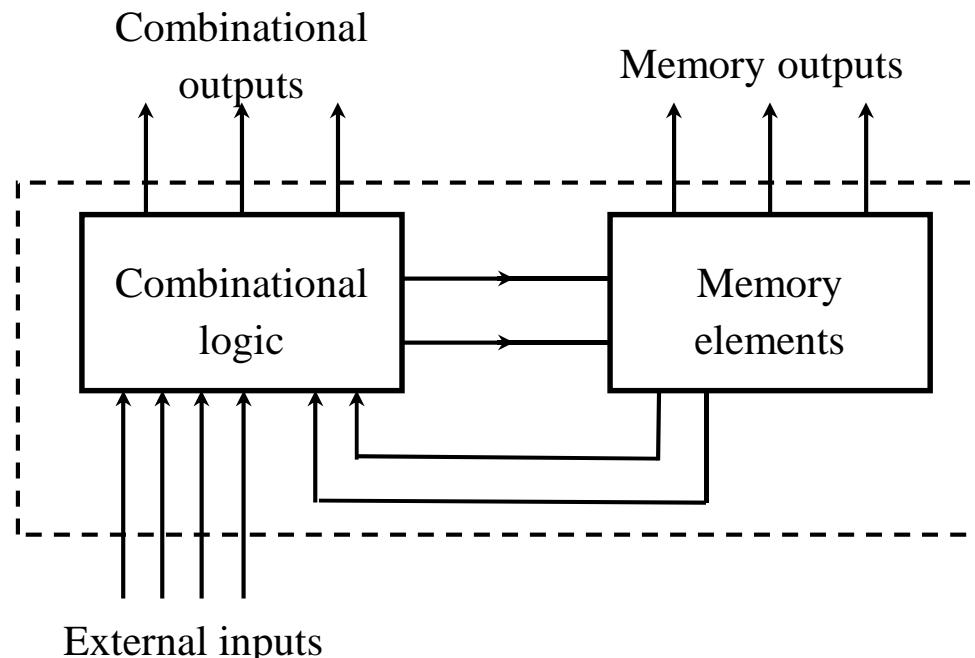


Digital Electronics and Microprocessors

Class 9

CHHAYADEVI BHAMARE

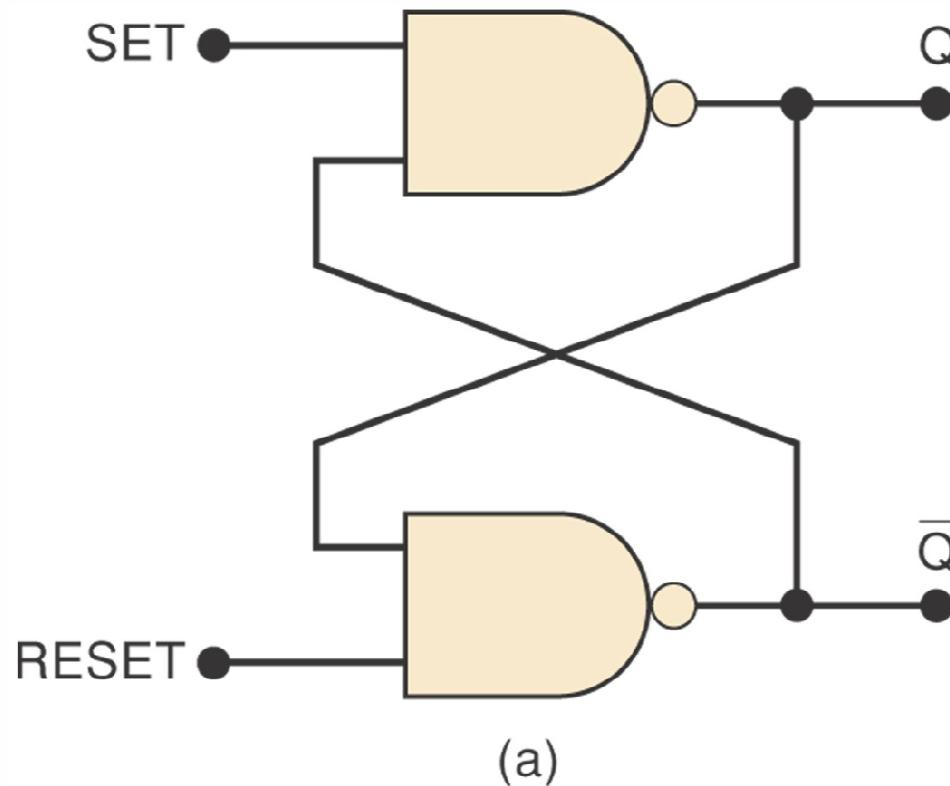
- A **sequential circuit** consists of a *feedback path*, and employs some *memory elements*.
-



Sequential circuit = Combinational logic + Memory Elements



(a) NAND latch; (b) function table.



A	B	NAND O/P
0	0	1
0	1	1
1	0	1
1	1	0

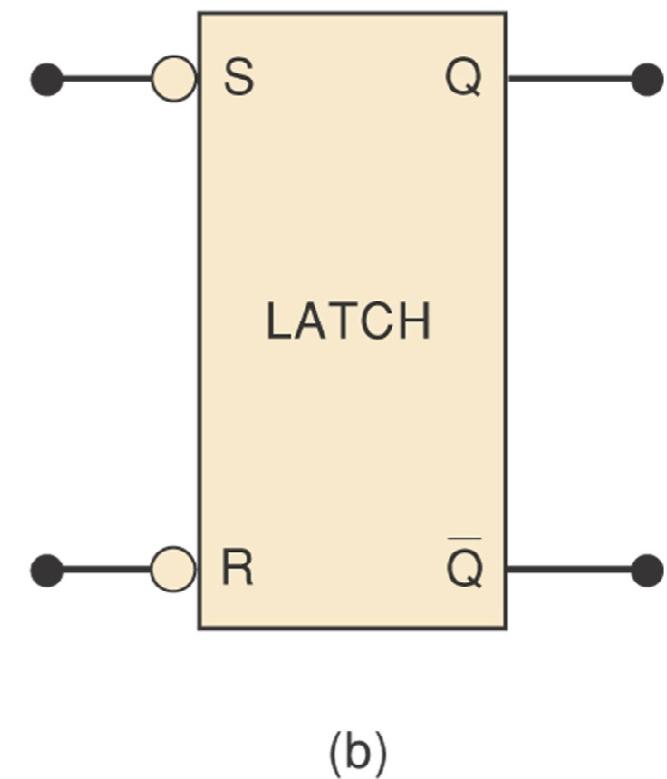
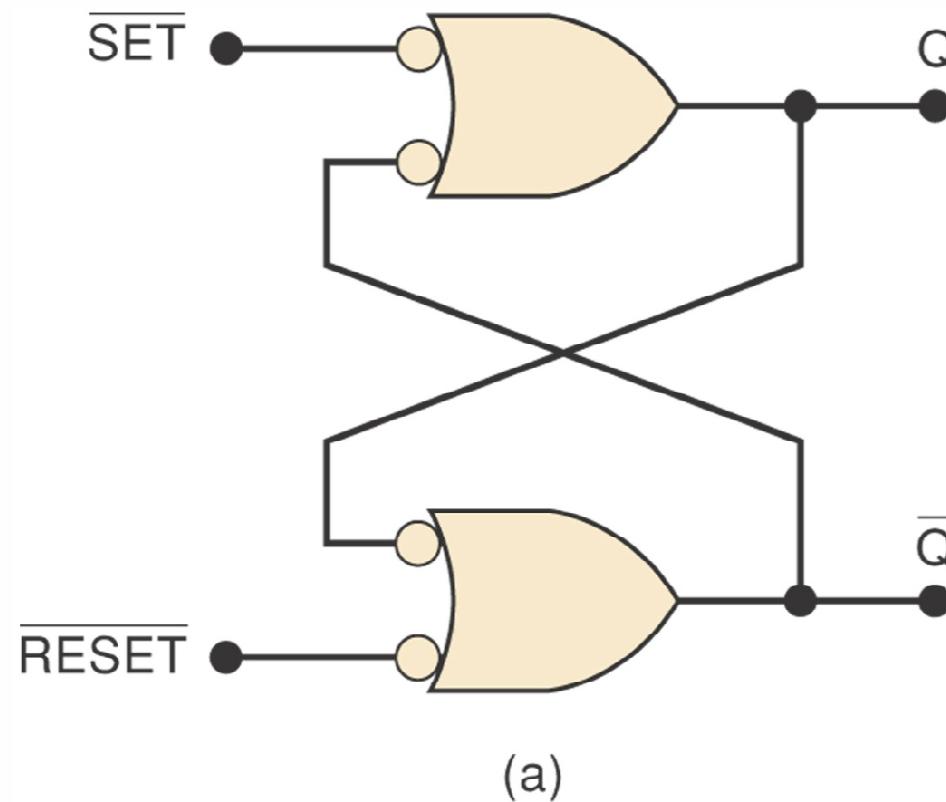
Set	Reset	Output
1	1	No change
0	1	$Q = 1$
1	0	$Q = 0$
0	0	Invalid*

*Produces $Q = \bar{Q} = 1$.

(b)

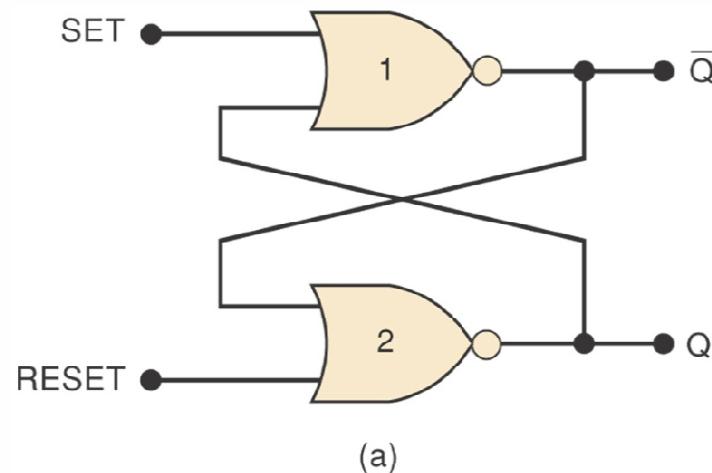


(a) NAND latch equivalent representation; (b) simplified block symbol.





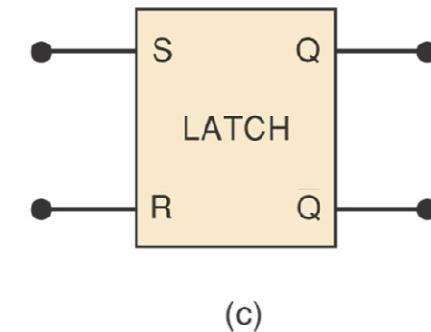
(a) NOR gate latch; (b) function table; (c) simplified block symbol.



Set	Reset	Output
0	0	No change
1	0	$Q = 1$
0	1	$Q = 0$
1	1	Invalid*

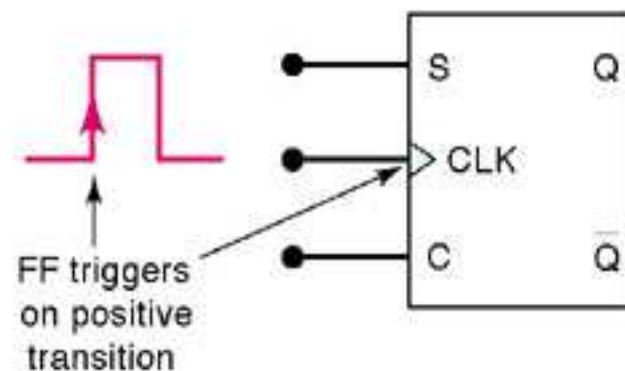
*Produces $Q = \bar{Q} = 0$.

(b)



Clocked S-R Flip-Flop

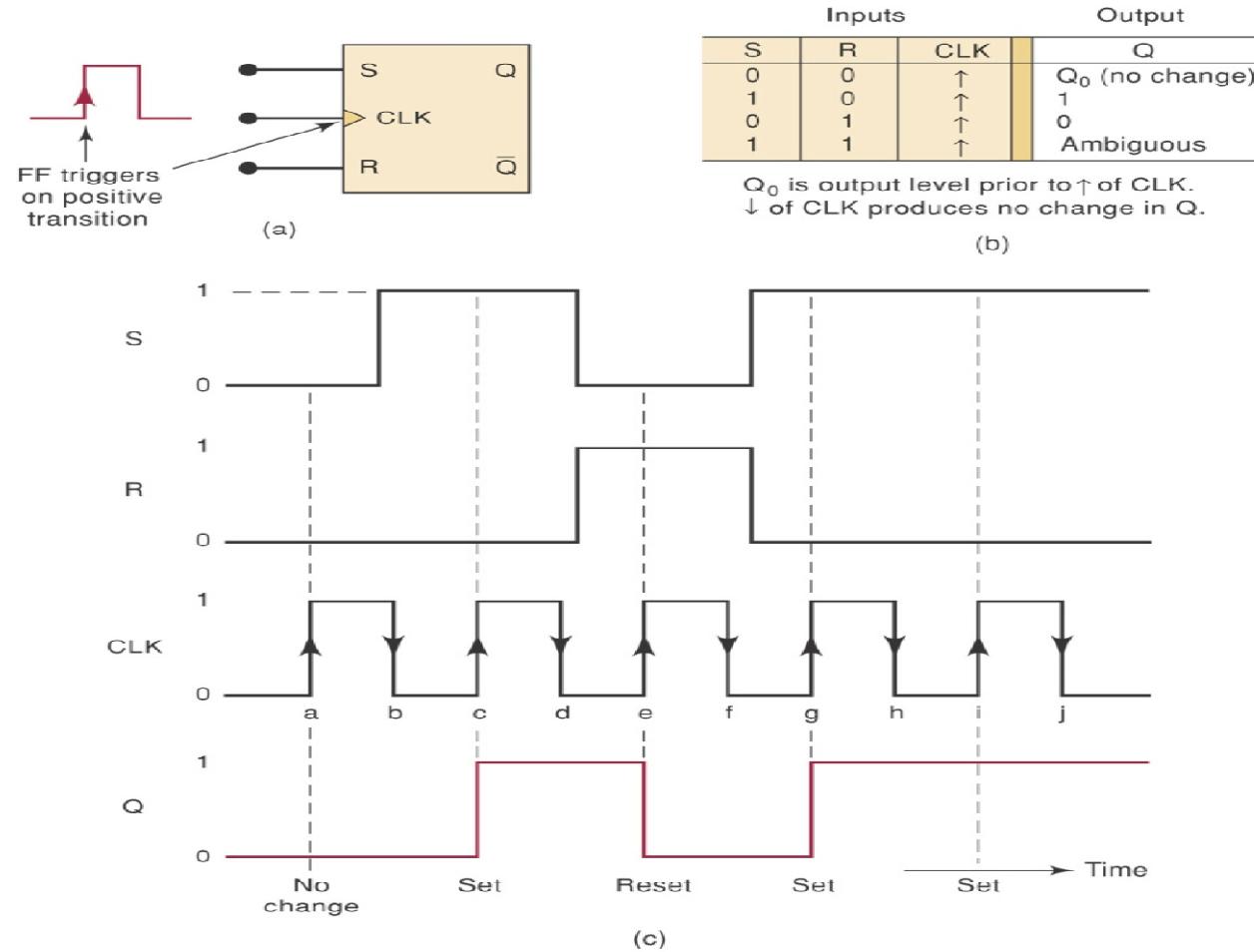
- The SET-RESET (or SET-CLEAR) FF will change states at the positive going or negative going clock edge.



Inputs			Output
S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

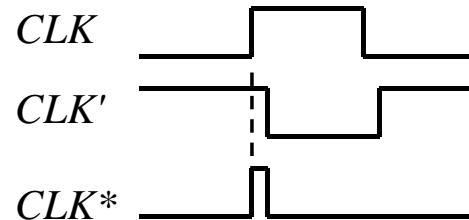
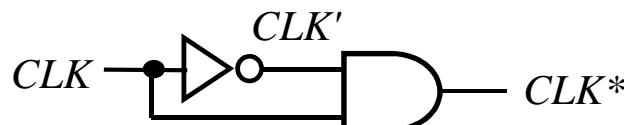
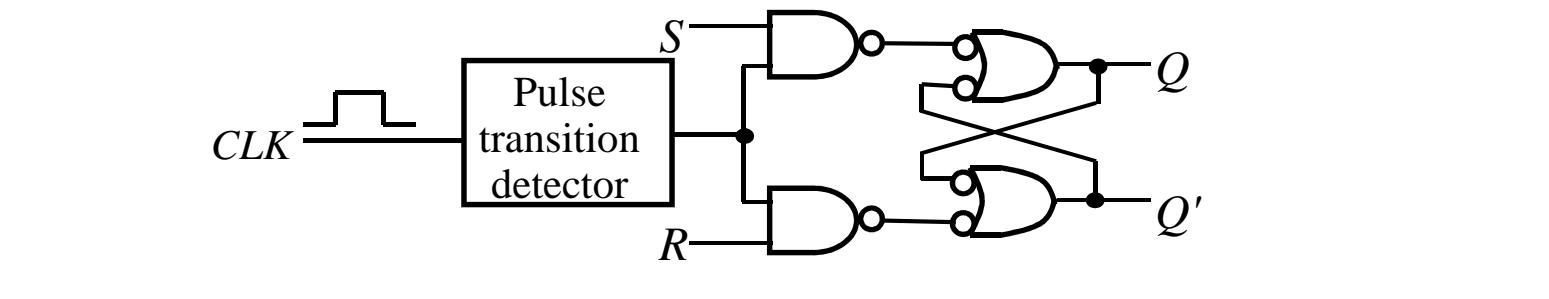
Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

(a) Clocked S-R flip-flop that responds only to the positive-going edge of a clock pulse; (b) function table; (c) typical waveforms.

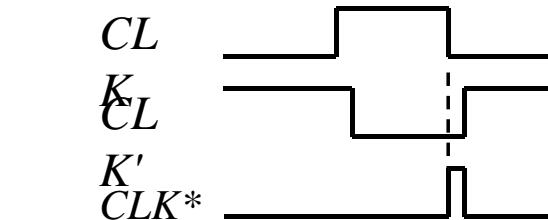
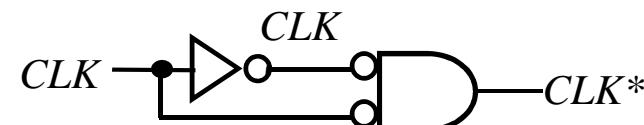


S-R Flip-flop

The pulse transition detector.



Positive-going transition
(rising edge)



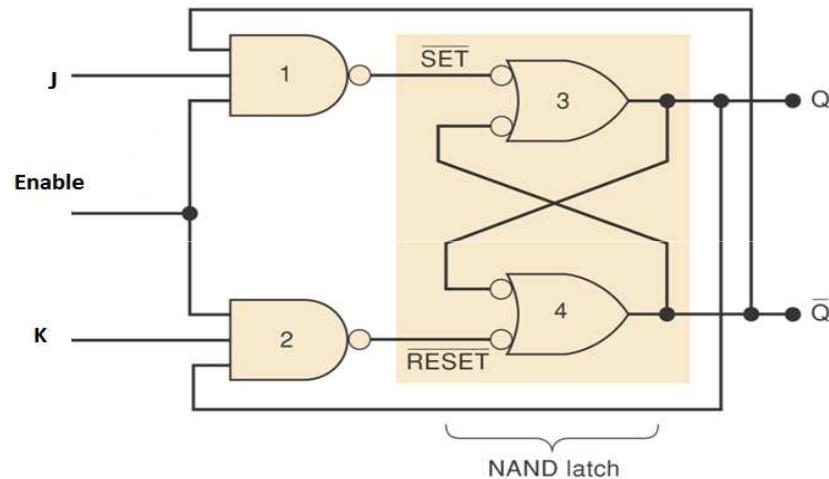
Negative-going transition
(falling edge)

Clocked J-K Flip-Flop

- Operates like the S-C FF. J is set, K is clear.
- When J and K are both high the output is toggled from whatever state it is in to the opposite state.
- May be positive going or negative going clock trigger.
- Has the ability to do everything the S-C FF does, plus operate in toggle mode.



Gated J K Latch



Case No	I/P'S			O/P'S		State
	E	J	K	Q_{n+1}	Q'_{n+1}	
Case I	0	X	X	Q_n	Q'_n	NC
Case II	1	0	0	Q_n	Q'_n	NC
Case III	1	0	1	0	1	Reset
Case IV	1	1	0	1	0	Set
Case V	1	1	1	Q'_n	Q_n	Toggle

Positive level triggered JK latch and its table

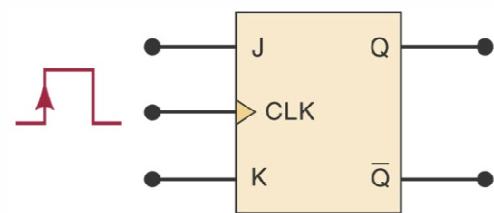


Negative level triggered JK latch

- Work for you

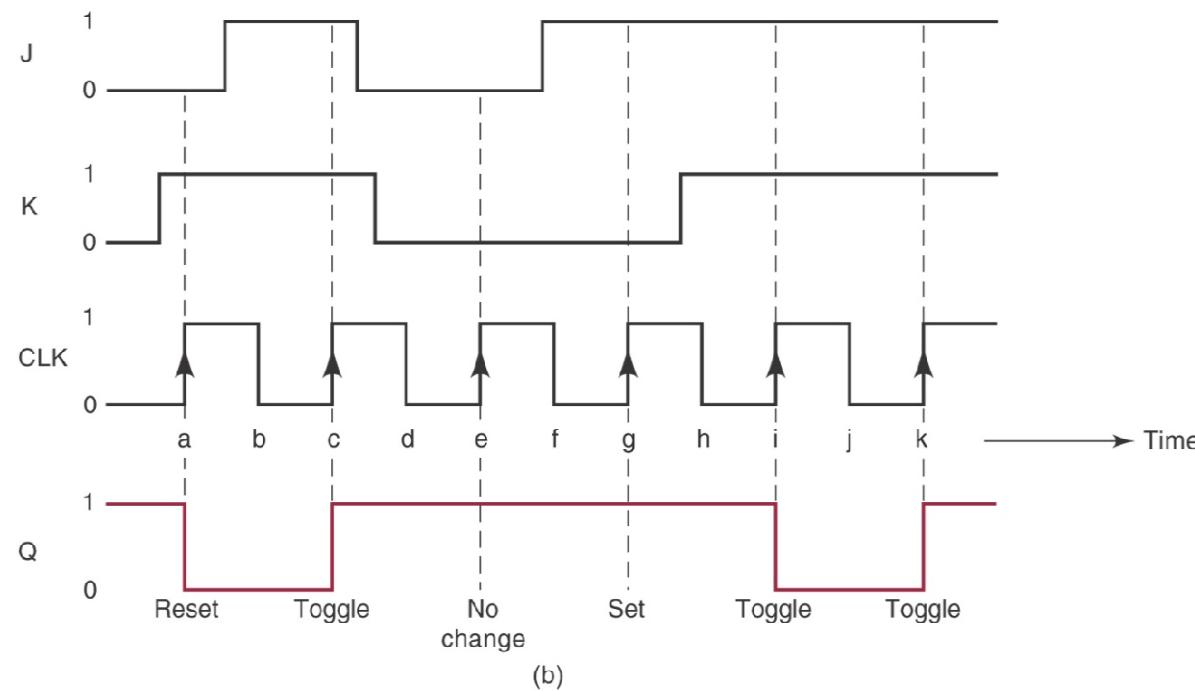


(a) Clocked J-K flip-flop that responds only to the positive edge of the clock; (b) waveforms.



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Q_0 (toggles)

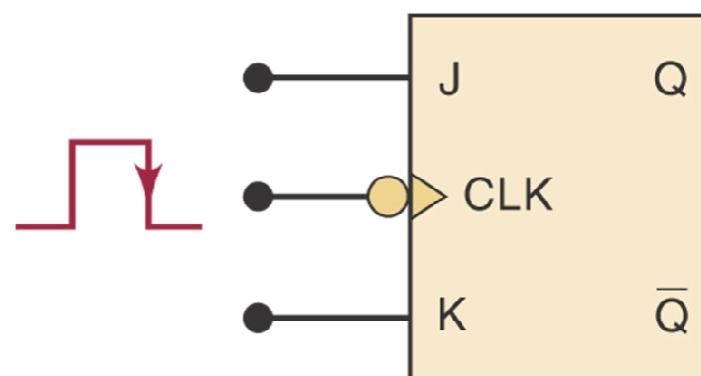
(a)



(b)



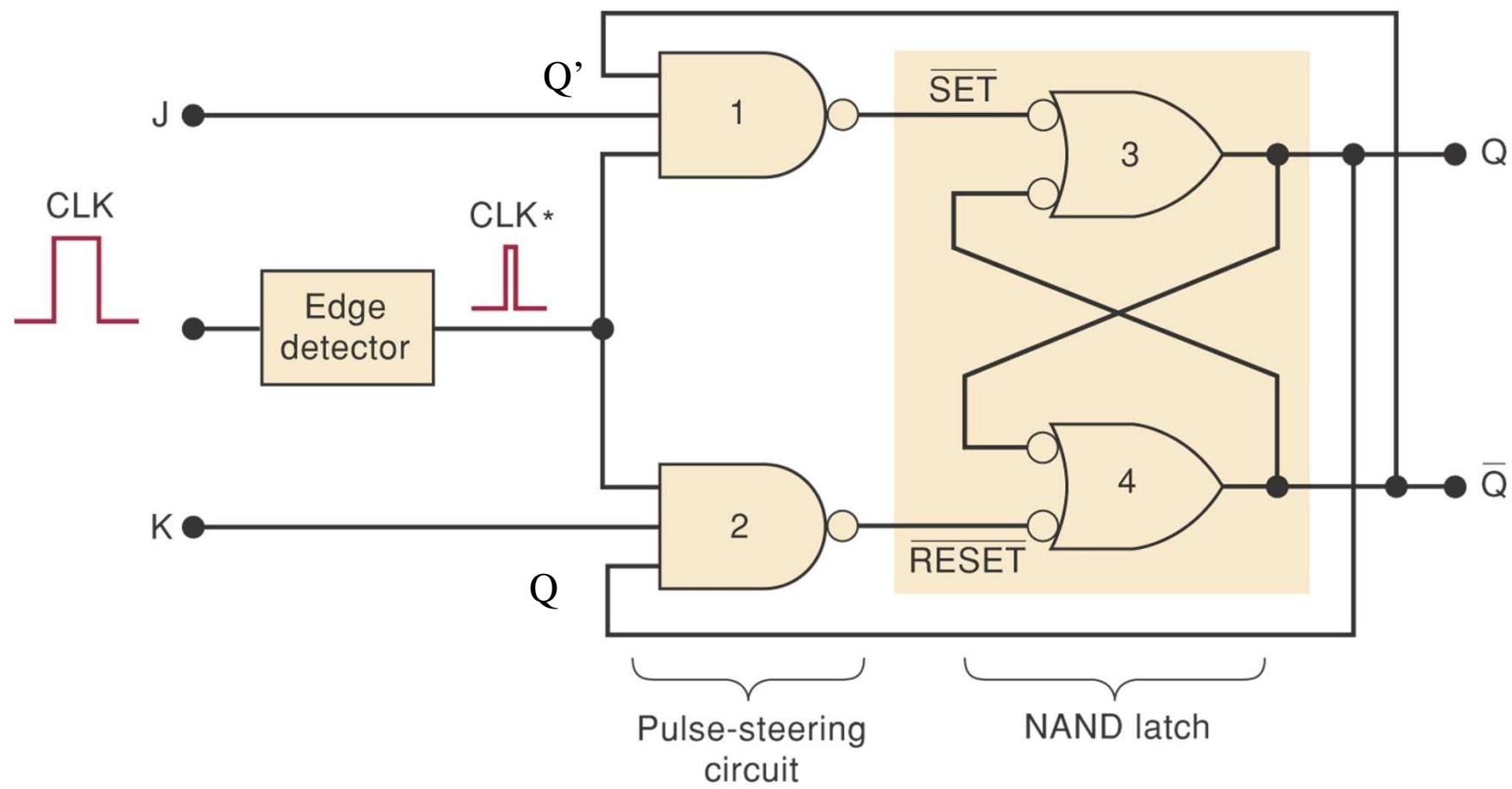
J-K flip-flop that triggers only on negative-going transitions.



J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	\bar{Q}_0 (toggles)

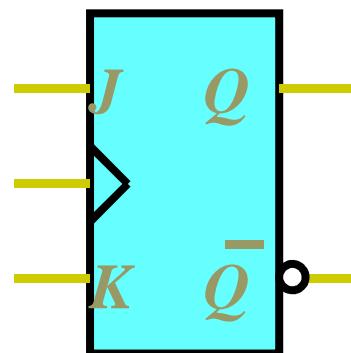


Internal circuit of the edge-triggered J-K flip-flop.





Flip-Flop Characteristic Equations



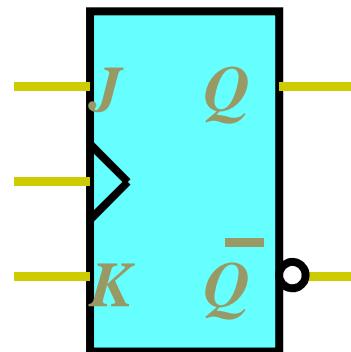
J	K	$Q(t)$	$Q(t+1)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

The table shows the characteristic equations for a JK flip-flop. The columns represent the inputs J , K , and the current state $Q(t)$. The rows show the next state $Q(t+1)$ for each combination of inputs. Brackets on the right side group the rows by output behavior:

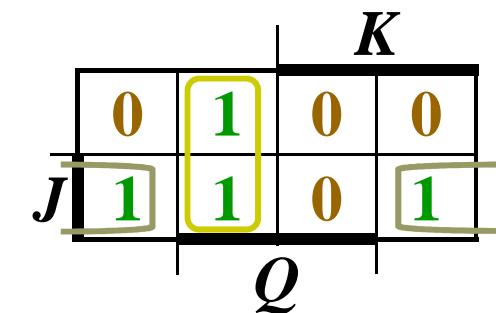
- No change (rows 1, 2, 5, 6)
- Reset (rows 3, 4)
- Set (rows 7, 8)
- Toggle (rows 9, 10)



Flip-Flop Characteristic Equations



J	K	$Q(t)$	$Q(t+1)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



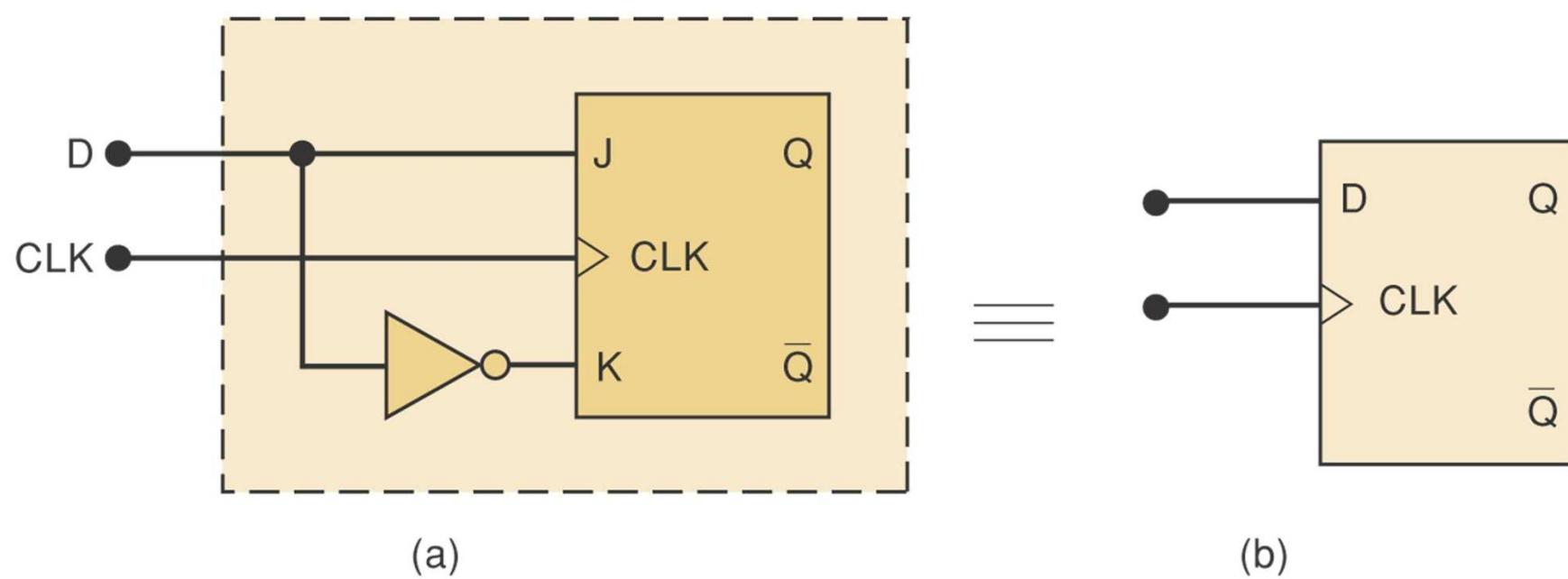
$$Q(t+1) = JQ' + K'Q$$

Clocked D Flip-Flop

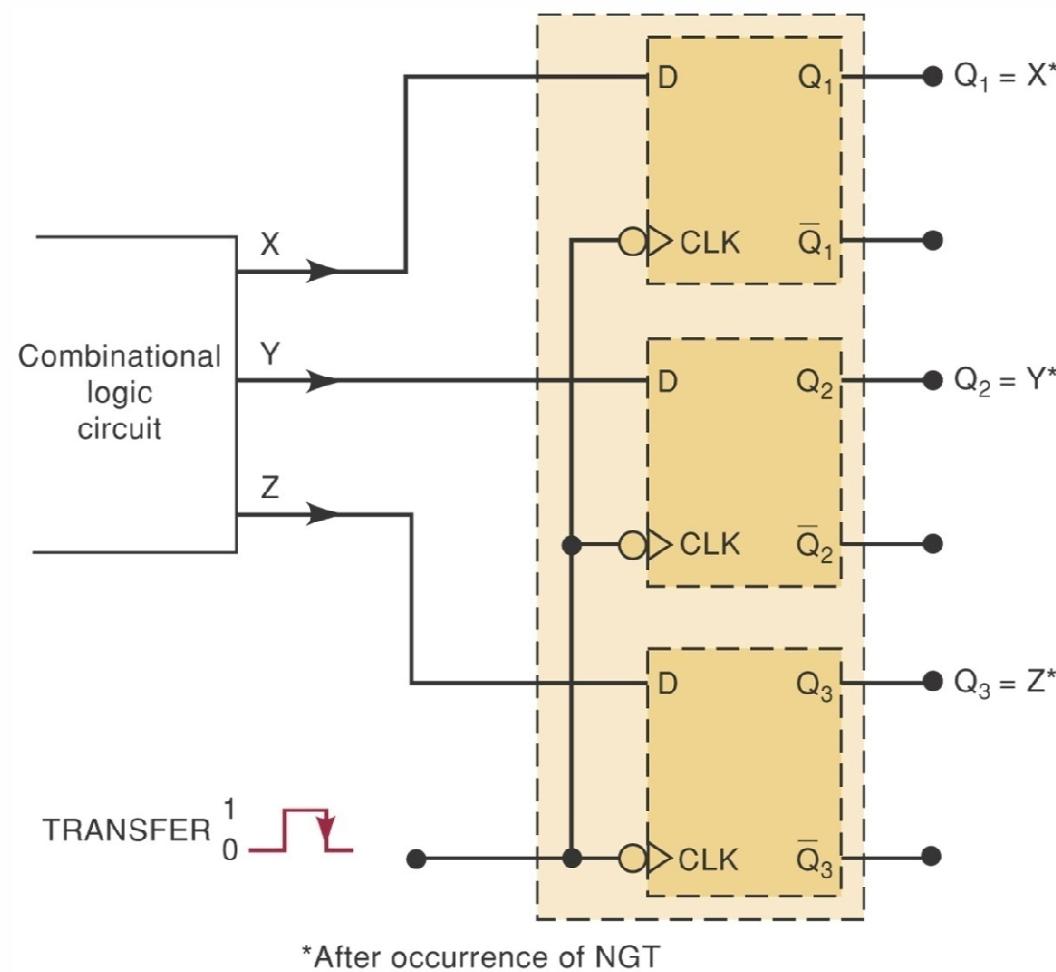
- One data input.
- The output changes to the value of the input at either the positive going or negative going clock trigger.
- May be implemented with a J-K FF by tying the J input to the K input through an inverter.
- Useful for parallel data transfer.



Edge-triggered D flip-flop implementation from a J-K flip-flop.



Parallel transfer of binary data using D flip-flops.

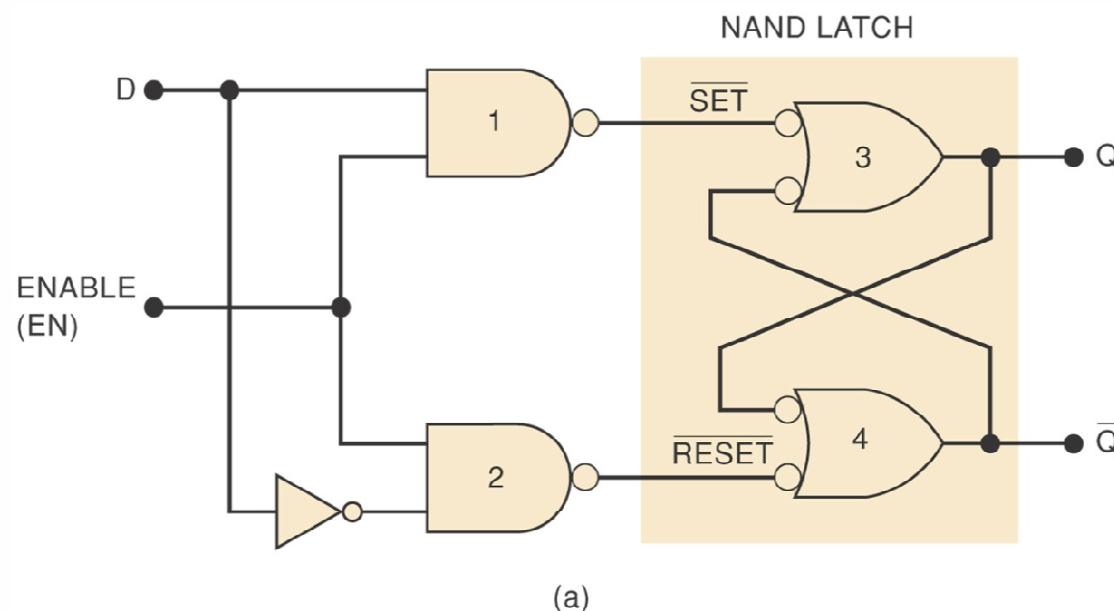


D Latch (Transparent Latch)

- One data input.
- The clock has been replaced by an enable line.
- The device is NOT edge triggered.
- The output follows the input only when EN is high.



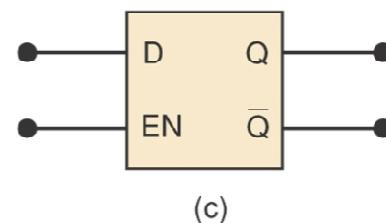
D latch: (a) structure; (b) function table; (c) logic symbol.



Inputs		Output
EN	D	Q
0	X	Q_0 (no change)
1	0	0
1	1	1

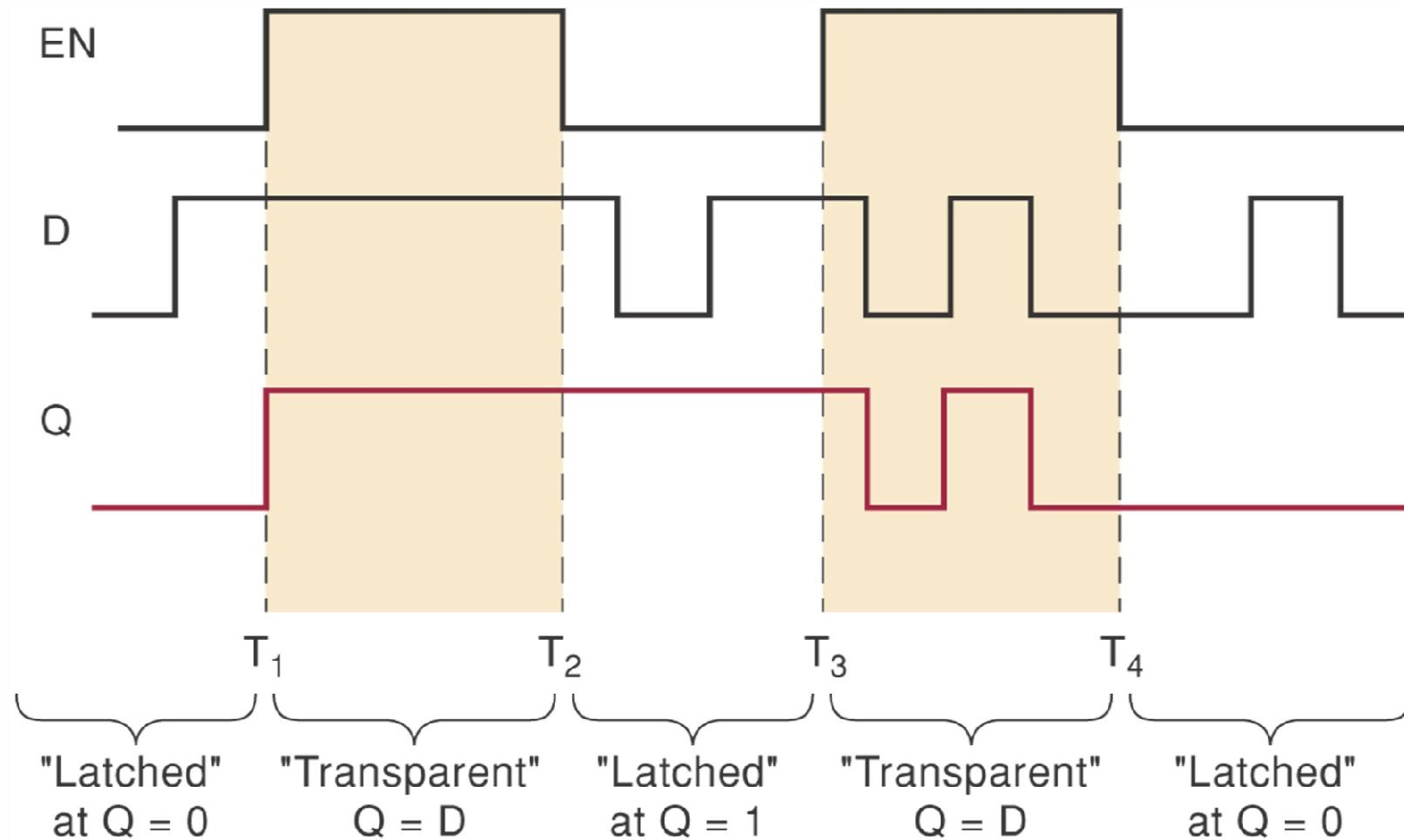
"X" indicates "don't care."
 Q_0 is state Q just prior to EN going LOW.

(b)





Waveforms for Example 5-8 showing the two modes of operation of the transparent D latch.

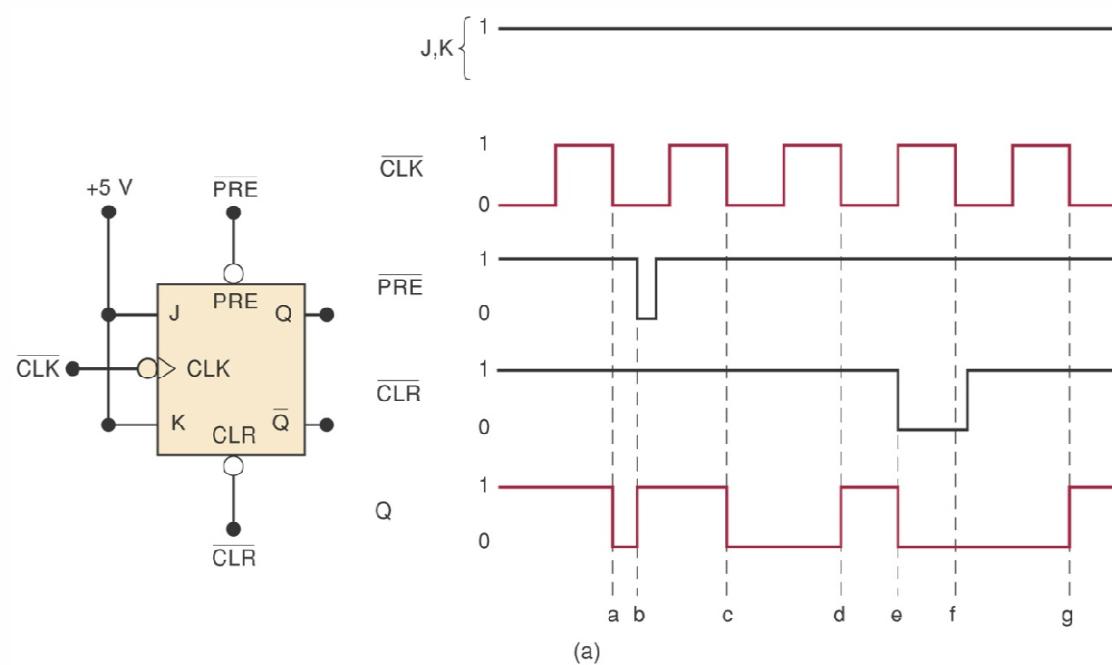


Asynchronous Inputs

- Inputs that depend on the clock are synchronous.
- Most clocked FFs have asynchronous inputs that do not depend on the clock.
- The labels PRE and CLR are used for asynchronous inputs.
- Active low asynchronous inputs will have a bar over the labels and inversion bubbles.
- If the asynchronous inputs are not used they will be tied to their inactive state.



Waveforms showing how a clocked flip-flop responds to asynchronous inputs.



Point	Operation
a	Synchronous toggle on NGT of \bar{CLK}
b	Asynchronous set on $\overline{PRE} = 0$
c	Synchronous toggle
d	Synchronous toggle
e	Asynchronous clear on $\overline{CLR} = 0$
f	\overline{CLR} overrides the NGT of \bar{CLK}
g	Synchronous toggle

(b)



Flip-Flop Applications

- Examples of applications:
 - Counting
 - Storing binary data
 - Transferring binary data between locations
- Many FF applications are categorized as sequential, which means that the output follows a predetermined sequence of states.

Frequency Division and Counting

- FFs are often used to divide a frequency. Here the output frequency is $1/8^{\text{th}}$ the input (clock) frequency.
- The same circuit is also acting as a binary counter. The outputs will count from 000_2 to 111_2 or 0_{10} to 7_{10}
- The number of states possible in a counter is the modulus or MOD number. The figure is a MOD-8 (2^3) counter. If another FF is added it would become a MOD-16 (2^4) counter.



J-K flip-flops wired as a three-bit binary counter (MOD-8).

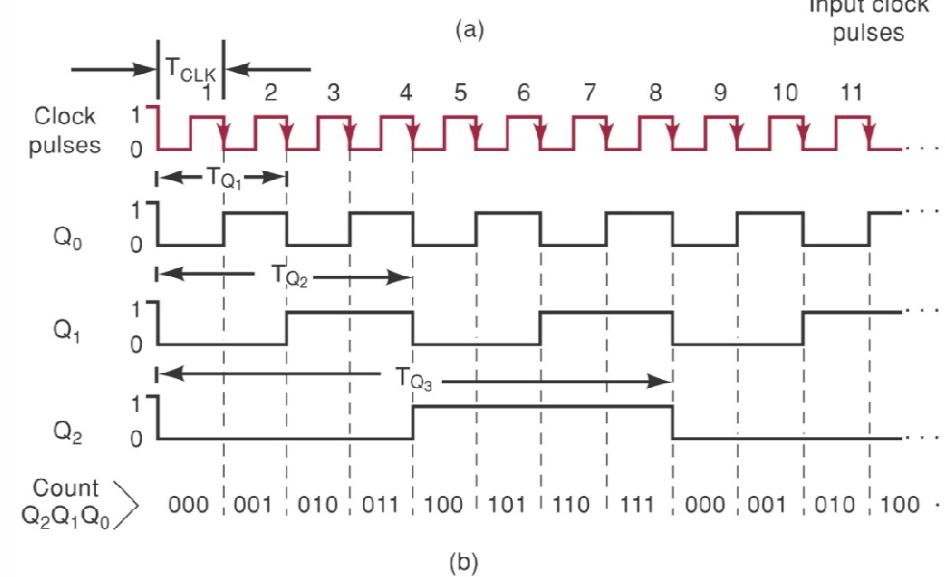
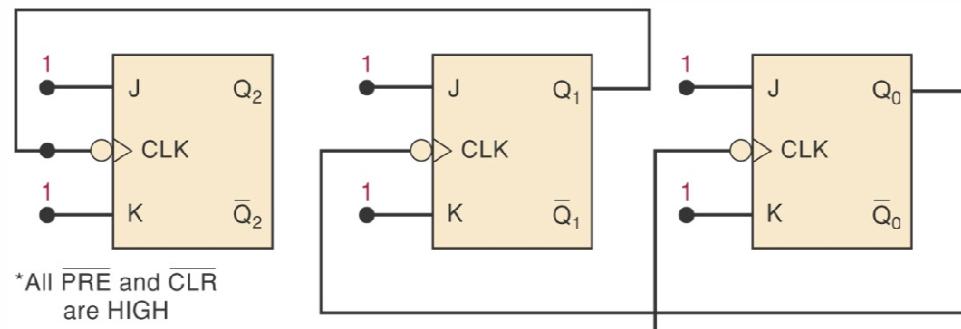
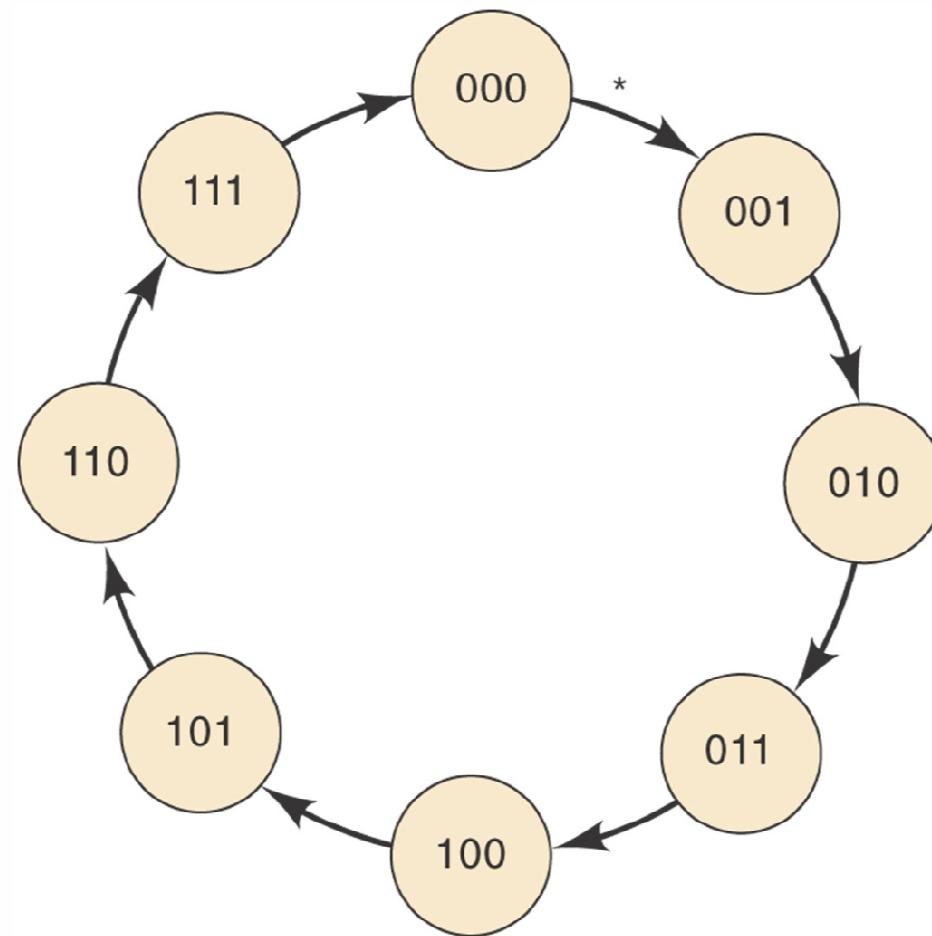




Table of flip-flop states shows binary counting sequence.

$\underline{2^2}$	$\underline{2^1}$	$\underline{2^0}$	
Q ₂	Q ₁	Q ₀	
0	0	0	Before applying clock pulses
0	0	1	After pulse #1
0	1	0	After pulse #2
0	1	1	After pulse #3
1	0	0	After pulse #4
1	0	1	After pulse #5
1	1	0	After pulse #6
1	1	1	After pulse #7
0	0	0	After pulse #8 recycles to 000
0	0	1	After pulse #9
0	1	0	After pulse #10
0	1	1	After pulse #11
.	.	.	.
.	.	.	.
.	.	.	.

State transition diagram shows how the states of the counter flip-flops change with each applied clock pulse.



* Note: each arrow represents the occurrence of a clock pulse