

**Gebze Technical University
Computer Engineering**

CSE 331 - 2019 Fall

ASSIGNMENT 2 REPORT

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1 INTRODUCTION

1.1 Problem Definition

Our problem was designing an ALU which includes 4x1 MUX module, 1-bit ALU module and 32-bit ALU module, which will be implemented in Verilog, with their own testbenches.

1.2 System Requirements

- XOR Gate Implementation
- 4x1 Multiplexer Implementation
- 1-Bit ALU Implementation which is described exactly how in the assignment document.
- 32-Bit ALU Implementation which is described exactly how in the assignment document.

1.3 Problem Solution Approach

I divide the problem into 4 section and create separate solutions for each of them:

1. **XOR Gate:** Based on logical circuits $Q = a'b + ab'$ equality, implemented an `exclusive_or.v` by using only 2 NOT, 2 AND, 1 OR gate
2. **4x1 Multiplexer:** Based on logical circuits $Q = x'y'A + xy'B + x'y'C + xyD$ equality, implemented an `mux_4to1.v` by using only 2 NOT, 4 AND, 1 OR gate
3. **1-Bit ALU:** Based on the given schema, implemented an `ALU_1bit.v` by using 1 XOR(`exclusive_or.v`), 1 4x1 MUX(`mux_4to1.v`), 2 NOT, 4 AND, 3 OR gate.
4. **32-Bit ALU:** Based on the given schema, implemented an `ALU_32bit.v` by using 32 `ALU_1bit.v`.

For each section, prepared testbenches and tested all them separately. All passed the requirements which you can see the screenshots at the next section of the report.

For the bonus part, I tried to organize pins and create a demo file by using resources on PS5 files. Due to only 10 switch inputs, I only used 2 less significant bits for the input A and B, 3 bits for ALU Control, 1 bit for carry input. Assigned LED's for 3 less significant bits of result and 1 LED for the carry output bit. Based on the videos, it should be working properly but I couldn't test it because I don't have any FPGA board.

2 RESULT

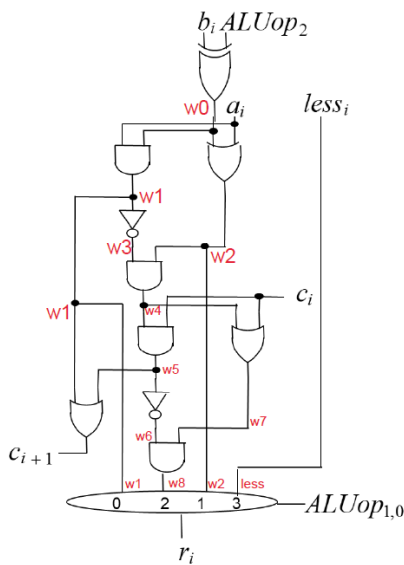
2.1 Test Cases & Running Result for the file : exclusive_or.v

```
# time = 0, a =0, b=0, x=0
# time = 20, a =1, b=0, x=1
# time = 40, a =0, b=1, x=1
# time = 60, a =1, b=1, x=0
```

2.2 Test Cases & Running Result for the file : mux_4to1.v

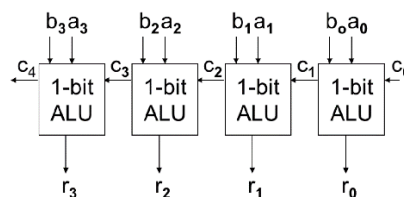
```
# time = 0, a =1, b=0, c =0, d=0, select=00, out=1
# time = 20, a =1, b=0, c =1, d=1, select=01, out=0
# time = 40, a =0, b=0, c =1, d=0, select=10, out=1
# time = 60, a =0, b=0, c =0, d=1, select=11, out=1
```

2.3 Test Cases & Running Result for the file : ALU_1bit.v



```
# time = 0, a =0, b=0, carry_in =0, less=0, ALU_op =000, carry_out =0, result=0
# time = 20, a =0, b=1, carry_in =0, less=0, ALU_op =000, carry_out =0, result=0
# time = 40, a =1, b=0, carry_in =0, less=0, ALU_op =000, carry_out =0, result=0
# time = 60, a =1, b=1, carry_in =0, less=0, ALU_op =000, carry_out =1, result=1
# time = 80, a =0, b=0, carry_in =0, less=0, ALU_op =001, carry_out =0, result=0
# time = 100, a =0, b=1, carry_in =0, less=0, ALU_op =001, carry_out =0, result=1
# time = 120, a =1, b=0, carry_in =0, less=0, ALU_op =001, carry_out =0, result=1
# time = 140, a =1, b=1, carry_in =0, less=0, ALU_op =001, carry_out =1, result=1
# time = 160, a =0, b=0, carry_in =0, less=0, ALU_op =010, carry_out =0, result=0
# time = 180, a =0, b=1, carry_in =0, less=0, ALU_op =010, carry_out =0, result=1
# time = 200, a =1, b=0, carry_in =0, less=0, ALU_op =010, carry_out =0, result=1
# time = 220, a =1, b=1, carry_in =0, less=0, ALU_op =010, carry_out =1, result=0
# time = 240, a =0, b=0, carry_in =1, less=0, ALU_op =010, carry_out =0, result=1
# time = 260, a =0, b=1, carry_in =1, less=0, ALU_op =010, carry_out =1, result=0
# time = 280, a =1, b=0, carry_in =1, less=0, ALU_op =010, carry_out =1, result=0
# time = 300, a =1, b=1, carry_in =1, less=0, ALU_op =010, carry_out =1, result=1
# time = 320, a =0, b=0, carry_in =0, less=0, ALU_op =011, carry_out =0, result=0
# time = 340, a =0, b=1, carry_in =0, less=0, ALU_op =011, carry_out =0, result=0
# time = 360, a =1, b=0, carry_in =0, less=0, ALU_op =011, carry_out =0, result=0
# time = 380, a =1, b=1, carry_in =0, less=0, ALU_op =011, carry_out =1, result=0
# time = 400, a =0, b=0, carry_in =1, less=0, ALU_op =011, carry_out =0, result=0
# time = 420, a =0, b=1, carry_in =1, less=0, ALU_op =011, carry_out =1, result=0
# time = 440, a =1, b=0, carry_in =1, less=0, ALU_op =011, carry_out =1, result=0
# time = 460, a =1, b=1, carry_in =1, less=0, ALU_op =011, carry_out =1, result=0
# time = 480, a =0, b=0, carry_in =0, less=0, ALU_op =111, carry_out =0, result=0
# time = 500, a =0, b=1, carry_in =0, less=0, ALU_op =111, carry_out =0, result=0
# time = 520, a =1, b=0, carry_in =0, less=0, ALU_op =111, carry_out =1, result=0
# time = 540, a =1, b=1, carry_in =0, less=0, ALU_op =111, carry_out =0, result=0
# time = 560, a =0, b=0, carry_in =0, less=1, ALU_op =111, carry_out =0, result=1
# time = 580, a =0, b=1, carry_in =0, less=1, ALU_op =111, carry_out =0, result=1
# time = 600, a =1, b=0, carry_in =0, less=1, ALU_op =111, carry_out =1, result=1
# time = 620, a =1, b=1, carry_in =0, less=1, ALU_op =111, carry_out =0, result=1
```

2.4 Test Cases & Running Result for the file : ALU_32bit.v



[illegible]