CMS RPC Upgrade Program

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Abstract

The LHC will be upgraded in several phases that will allow significant expansion of its physics program. The luminosity of the accelerator is expected to exceed 5×10^{34} $cm^{-2}s^{-1}$. In order to sustain the harsher conditions and to help maintaining good trigger efficiency and performance the Resistive Plate Chambers (RPC) system of the CMS experiment will be upgraded. The present RPC system would continue to operate, and it would be upgraded with new Link Boards system. In addition, the coverage of the RPC system would be increased up to pseudo rapidity of 2.4 by installing a new generation of improved RPCs (iRPCs). Their design and configuration are optimized to sustain higher rates and hence to survive the harsh background condition during HL-LHC operation. The iRPC are equipped with newly developed electronics designed to read out the detectors from both sides, allowing in this way a good spatial resolution along the strips O(cm). The status of the upgrade project is presented.

CMS RPC Upgrade

The CMS RPC upgrade for Phase-2 [1] compreehends **(1) the replacement of a the current Link System**, which connects the Front-End Boards (FEBs) to the trigger processors, by a new one, redesigned one from scratch and **(2) the extension of the pseudorapidity coverage of the RPC system**, by adding new chambers from $|\eta| = 1.9$ up to 2.4, namely stations RE3/1 and RE4/1. Those new chamber will be assembled with a Improved Resistive Plate Chambers (iRPC) technology, which does the readout of signals in both ends of the strip. The timing difference per hit and strip, is used by the iRPC Front-End electronics to estimate the spatial position of the hit in the longitudinal direction. The current RPC chambers can only read the transverse hit position.

Both upgrades are important in order to cope with expected high rate of the HL-LHC scenario, in which a Inst. Luminosity of 5×10^{34} $cm^{-2}s^{-1}$ would provide a background rate up to 700 Hz/cm^2 (for present chamber, already including a safety factor of 3). Also, the upgrades would enhance the redundancy of the CMS Muon System, resolve ambiguities in the Endcap triggering and allow improvements of the RPC system to Trigger and reconstruction. Figure 1 presents a quadrant of the CMS Muon system, showing Drift Tubes (DT) chambers in yellow, RPCs in light blue, and Cathode Strip Chambers (CSCs) in green. The locations of new forward muon detectors for the HL-LHC project are indicated in red for Gas Electron Multiplier (GEM) stations (ME0, GE1/1, and GE2/1) and violet for improved RPC stations (RE3/1 and RE4/1).

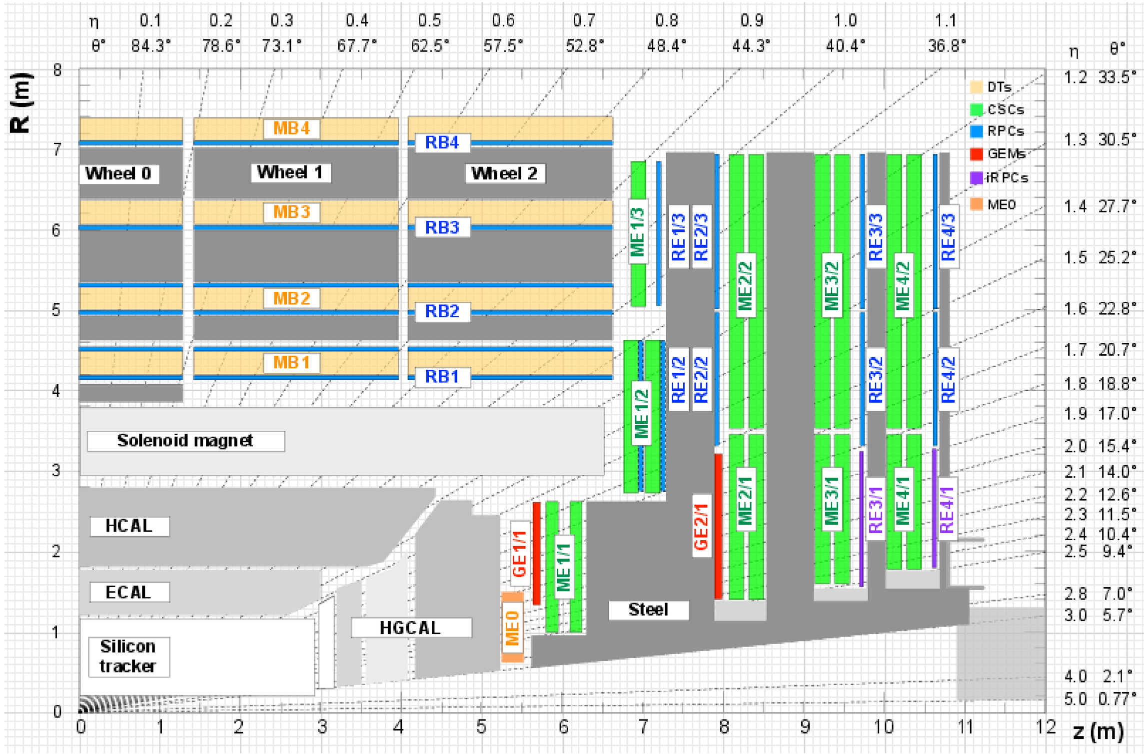


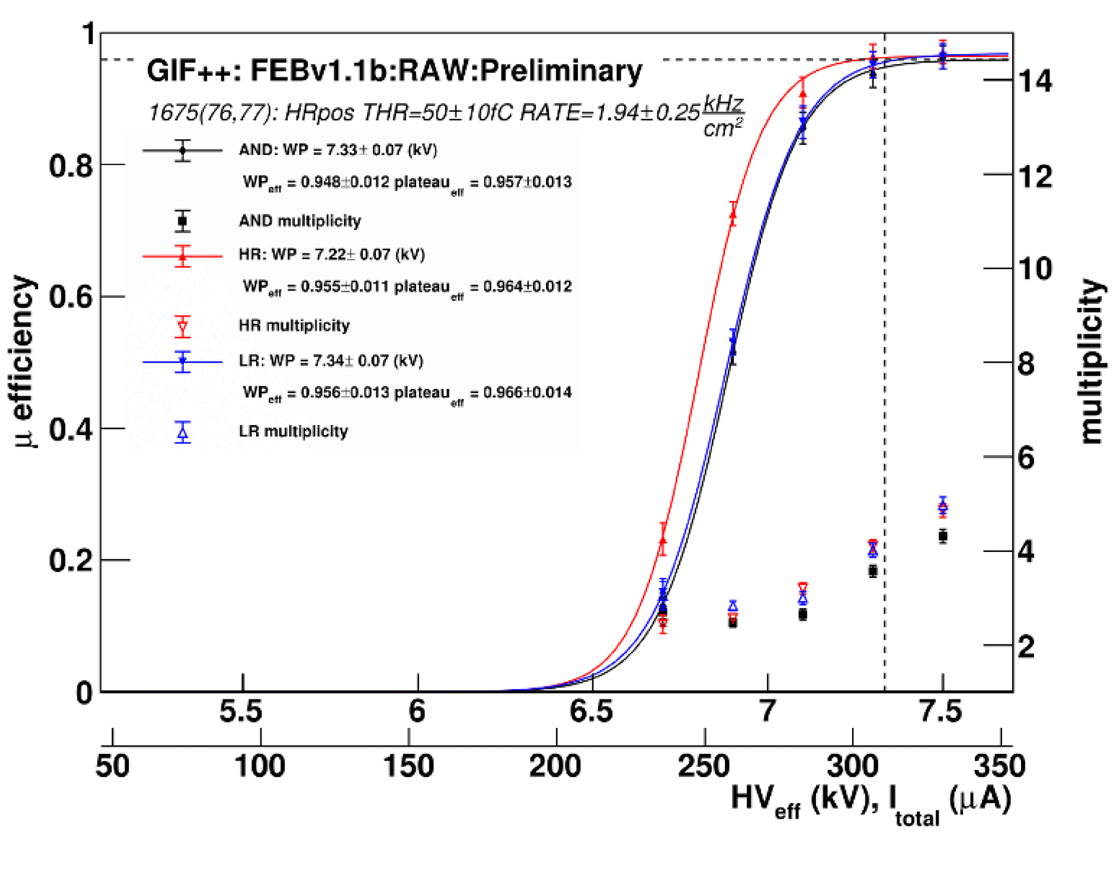
Figure 1: CMS Muon system for the Phase-2 Upgrade.

iRPC FEB

The iRPC chambers to be installed in stations RE3/1 and RE4/1 will demand changes, in comparison with the current chambers, in terms of design and electronics. The key design change is the finer gas gap thickness, from 2 mm to 1.4 mm [1], to reduce the intrinsic chamber threshold. In terms of electronics, a completely new FEB is being developed. This one should **(1) ensure the chamber efficiency in a high rate environment (up to 2 kHz/cm^2) and (2) provide information for a 2-dimensional readout**.

To achieve the requirements, the iRPC FEB will use PETIROC ASICs [2], with 32-channels each, for pre-amplification and discrimination of strip signals, providing low-jitter trigger with accurate charge and time measurements. Each strip end will be connected to one channel of the PETIROC. The digitized signal is sent to a FPGA (Field Programmable Gate Array), where a high resolution Time-to-Digital Converter (TDC) is implemented, allowing 2D measurement of the muon hit by measuring the arrival time difference of the two strip ends.

Figure 2: Muon Efficiency versus High Voltage Effective (HVeff) and Total Current for the second version of FEB with PETIROC2B (FEBv1b) and the mean value of multiplicity for each side. 'AND' efficiency showing without crosstalk impact. Scintillators placed in the HR of the chamber and covered about 20cm. This setup includes three protected with leads scintillators inside GIF++ (w/o outside scintillators). Thresholds: 50 ± 10 fC.



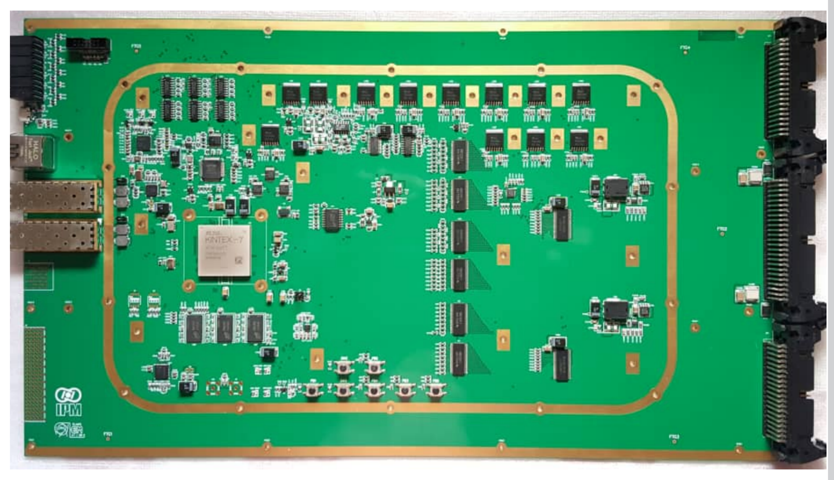
Currently there are two validated version of the iRPC FEB: FEBv0 (only one PETIROC2A and an Altera Cyclone II FPGA) and FEBv1 (with two PETRIOC2B and an Altera Cyclone V FPGA). Figure 3 shows the Muon Efficiency versus High Effective Voltage (HVeff, taking into account pressure and temperature effects) and the mean multiplicity, for cosmics data taken at GIF++ (CERN's Gamma Irradiation Facility - September-November 2019), considering the High Radius (HR), Low Radius (LR) strip ends and the logical AND of them. Future versions under development includes schematics closer to final version, radiation hard FPGA (PolarFire) and the possibility of a newer version of the PETIROC ASIC (2C, with automatic latching of individual channels).

New Link System

In the CMS experiment, the RPC chambers are readout, controlled and monitored through the Link System, which consists of 1592 electronics boards, divided in two kinds, known as the Link boards (LBs) and Control Boards (CBs), LBs can work as Master LB or Slave LB.

The HL-LHC high rates will required an increase of the available TX bandwidth and readout time resolution. The new link system is being developed around the use of modern components and FPGAs (Field Programmable Gate Array), following a radiation hard design. **The data transmission rate between the new Link system and RPC back-end electronics increases to 10.24 Gbps and resolution of the Muon hit time improves to 1.5 ns**, close to the RPC chamber intrinsic resolution, which is achieved by implementing a high resolution 96-channel Time-to-Digital Converter (TDC) in the link board FPGA. Each TDC channel comprised of 16 bins where each bin had a time scale of 25/16 ns. The experimental results showed that there existed a 1.56 ns resolution for the implemented TDC channels.

Figure 3: A RPC Link Board prototype for Phase-2 Upgrade.



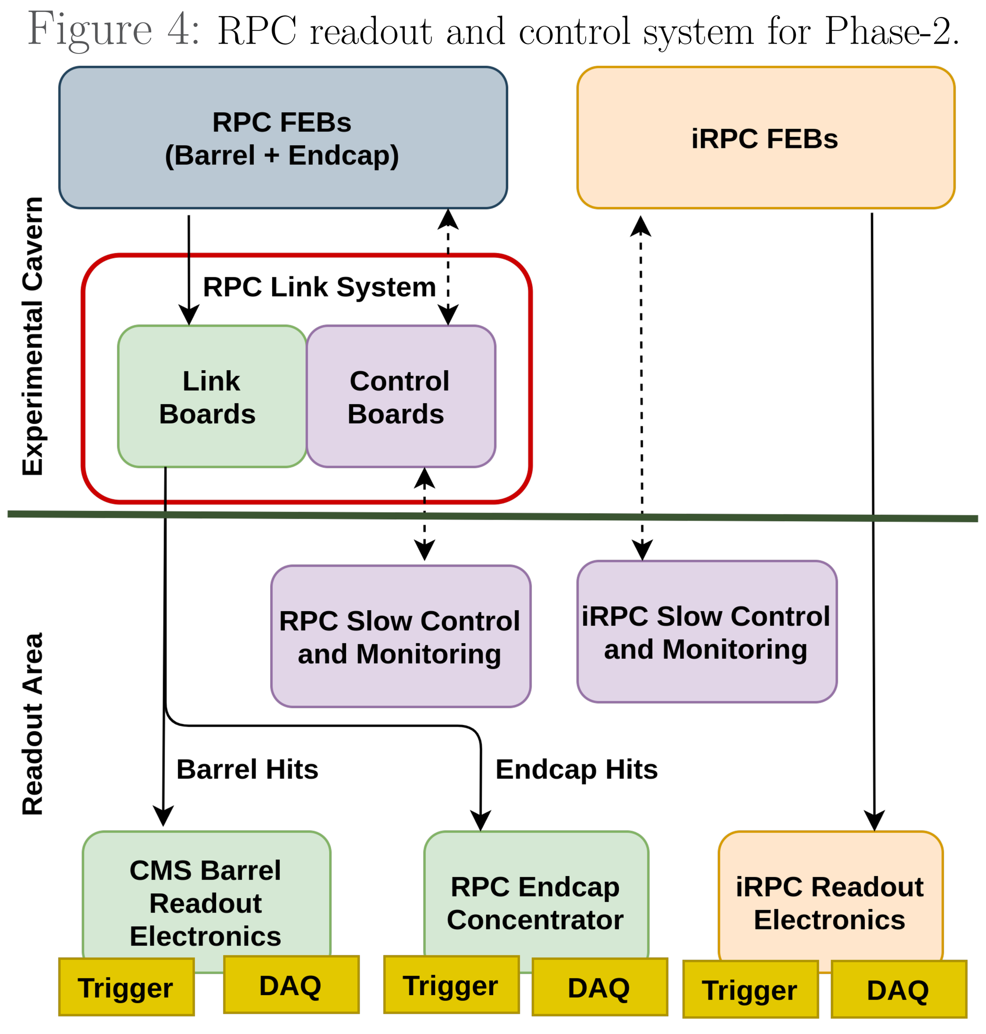
The high speed data transmissions is obtained by the use of a GTX transceivers of the FPGA, plus preprocessing of data before sending to the GTX transmitter.

Readout and Control Electronics

An extensive Phase-2 upgrade program is also scheduled for CMS Level-1 Trigger [3]. Since RPC is the only Muon detector present in both CMS Barrel and Endcap region, its contribution to CMS Level-1 Trigger upgrade program is important.

The readout and control system (also called back-end) of the RPC (Figure 4) system will be redesigned in order to **(1) include readout and control of new hardware; (2) cope with the requirements of the Level-1 Trigger Phase-2 design; (3) sustain maintainability of the system by replacing obsolete hardware.**

Figure 4: RPC readout and control system for Phase-2.



The new readout, control and monitoring hardware will be installed in the CMS Services Area, away from CMS radiation, and will follow the CMS specification of common hardware platforms for Phase-2, specifically, Serenity boards [4], with ATCA form factor. Its links will be composed by Slow Control/Monitoring channels (dashed lines) and readout channels (solid lines). Barrel RPC hits are expected to be distributed to a common CMS Barrel (RPC + DT) hardware, while Endcap and iRPC hits will go to dedicated RPC boards. Those hits will later be distributed to CMS Muon Track Finders and DAQ.

Conclusion

The status of the upgrade project was presented. For the next CMS data-taking period (Run3 - starting in 2022 - expected to double the integrated luminosity of Run 2), it is awaited that prototypes of the upgrade activities described above will be installed in CMS to take data concurrently with CMS, for validation propose. A thorough commissioning of prototypes is expected for the next years, in preparation for Phase-2 final upgrade hardware installation and operation.

References

[1] Thomas Hebbeker and Andrey Korytov. "The Phase-2 Upgrade of the CMS Muon Detectors". In: (Sept. 2017).

[2] J. Fleury et al. "Petiroc, a new front-end ASIC for time of flight application". In: *2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC)*. 2013, pp. 1–5.

[3] Alexandre Zabi et al. "The Phase-2 Upgrade of the CMS Level-1 Trigger". In: (2020).

[4] Andrew Rose et al. "Serenity: An ATCA prototyping platform for CMS Phase-2". In: *PoS* TWEPP2018 (2019), p. 115.