21

RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. (General) Degree in Applied Sciences
First Year - Semester II Examination – September / October 2020

COM 1308 – DIGITAL LOGIC DESIGN

Time: Three (03) hours

Instructions to Candidates:

1. This paper contains **SIX (06)** questions in **FOUR (04)** pages.
2. All questions carry equal marks.
3. Answer **ANY FIVE (05)** questions.

---

1. a. "A logic circuit implements logical operations on information to process them." Explain how the operation of a logic circuit is described.

(05 marks)

b. Show how an X-OR gate can be used to complement a single bit.

(05 marks)

c. Discuss the advantages of using universal gates in implementing logic circuits.

(05 marks)

d. Show how a NOT gate can be synthesized using NOR and NAND gates.

(05 marks)

2. a. Prove,

$$\overline{x + y} = \bar{x} \cdot \bar{y} \quad \text{and}$$

$$\overline{x \cdot y} = \bar{x} + \bar{y}$$

using truth tables.

What are these equations?

(05 marks)

b. Find the minimum sum-of-products expression for the function,

$$f = \bar{x}\bar{y}z + \bar{x}yz + x\bar{y}$$

using algebraic manipulation.

(05 marks)

c. Implement the minimum SOP expression you obtained in part b. using NOR gates.

(05 marks)

d. Prove that,

$$(\bar{x} + \bar{y} + \bar{z}).(\bar{x} + \bar{y} + z).(x + \bar{y} + \bar{z}).(x + \bar{y} + z) = \bar{y}$$

using Karnaugh Maps.

(05 marks)

3. a. Implement a half adder using NOR gates.

(05 marks)

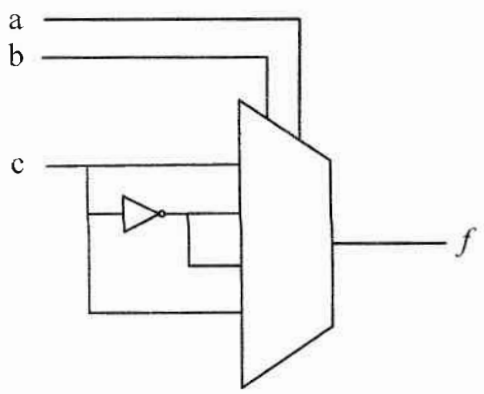
b. Implement a single-bit complementing circuit using NOR gates.

(05 marks)

c. Show how a single-bit subtractor can be implemented using two half adders. You may use additional gates as necessary.

(10 marks)

4. a. Show that the following circuit implements a 3-way switch.



(10 marks)

b. Design a binary-to-octal decoder.

(10 marks)

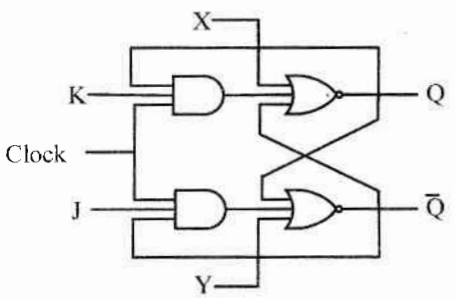
5. a. Using appropriate circuit diagrams show that one output of a simple latch is always the complement of the other.

(05 marks)

b. "Gated latches are only activated when the clock signal is 1." Using timing diagrams explain the operation of a gated S-R latch.

(05 marks)

c. Explain the use of the two signals X and Y in following circuit diagram. Use the characteristic table of a J-K flip for your explanation.



(10 marks)

6. a. Design and implement a synchronous decimal (divide-by-10) counter.

(20 marks)

---- End ----