RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. (General) Degree in Applied Sciences
FirstYear - Semester II Examination – Nov/Dec 2016

COM 1308 – DIGITAL LOGIC DESING

Time:Three hours

Instruction to candidates

- This is a closed book examination.
- There are THREE (3) pages in the question paper.
- Question paper consists of SIX (6) questions.
- Answer any FIVE (5) questions.
- All questions carry equal marks.

---

1. Question 01

a) Prove that x+x'·y=x+yusing perfect induction (4 marks)

b) Prove the given equation using algebraic manipulation. (5 marks)

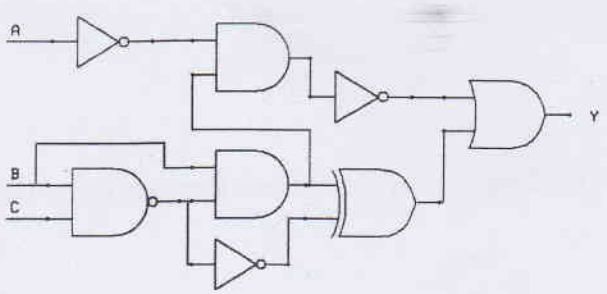
(X+A)(X'+A)(A+C)(A+D)X = AX

c) Simplify the given expressions using algebraic manipulation. (5 marks)

i. F(a,b) = ab+ab'

ii. F(x,y,z) = xy +x'z+yz

d) Write down the Boolean expression for the given circuit design. (3 marks)



e) Draw the circuit diagram of the given expression F(x,y,z) (3 marks)

$F(x,y,z) = xyz + xy' + yz' + x'y'$

(20 marks)

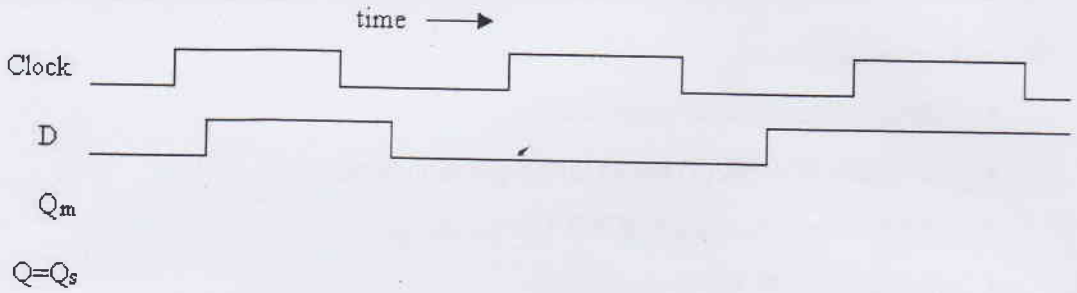
2. Question 02

a) Draw the Logic Implementations of D flip-flop and T flip-flop (3 marks)

b) Discuss the differences and similarities in the behavior of the flip-flops in part (a) (4 marks)

c) Design the Master Slave D flip-flop using two D flip-flops. (4 marks)

d) Complete the given timing diagram of a Master Slave D flip-flop. Q_m is the output at Master and $Q=Q_s$ the output at Slave. Consider that the flip-flops are positive edge triggered. (5 marks)



e) Draw the State transition diagrams of S-R and J-K Flip flops (4 marks)

(20 marks)

3. Question 03

a) Briefly describe the behavior of a Multiplexer. (3 marks)

b) Write the truth tables of Half Adder and Full Adder and state the difference between them. (6 marks)

c) Design a three bit adder using Full adders (5 marks)

d) State whether each of the following are Combinational components or Sequential components. (2 marks)

i. Decoder
ii. ROM
iii. Register
iv. Adder

e) Draw the design of a 4 bit Serial in Serial out Shift Register using flip-flops. (4 marks)

(20 marks)

4. Question 04

Design a car safety alarm considering four inputs; Door closed (D), Key in (K), Seat pressure (S), Seat belt closed (B). The alarm (A) should sound if the key is in and the door is not closed, or the door is closed and the key is in and the driver is in the seat and the seat belt is not closed

a) Create the Truth table for the car safety alarm system considering all the possibilities. (5 marks)

b) Obtain the POS expression for the created truth table in part (a). (4 marks)

c) Simplify the obtained expression using K- maps. (6 marks)

d) Draw the simplified circuit. (5 marks)

(20 marks)

Library
Applied Science
University of Sri Lanka

5. Question 05

a) Briefly explain the Programmable Logic Array. (3 marks)

b) Draw the gate level diagram for a programmed PLA that implement the function below (5 marks)

F=(A+B')(C+A'B)' G=AB'+C(A'+B).

c) Draw the schematic diagram for a programmed PLA that implements the functions in part (b). (4 marks)

d) Write the simplified truth table for a 1 bit 4x1Multiplexer. (4 marks)

e) Draw the circuit diagram for the Multiplexer in part (d). (4 marks)

(20 marks)

6. Question 06

a) Write the differences between Synchronous and Asynchronous counters. (3 marks)

b) Design a 3 bit Asynchronous Up Counter with T flip-flops (5 marks)

c) Draw the timing diagram for the Up Counter designed in part (b) (4 marks)

d) What are the three ways to model a digital system using VHDL? (3 marks)

e) Model a 3 bit shift register using VHDL in structural way. (5 marks)

(20 marks)

END