RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

Bachelor of Science in Applied Sciences
Third Year - Semester I Examination – July/August 2023

PHY 3212 – ELECTRONICS II

Time: Two (02) hours

Answer all Questions.

Calculators are not allowed.

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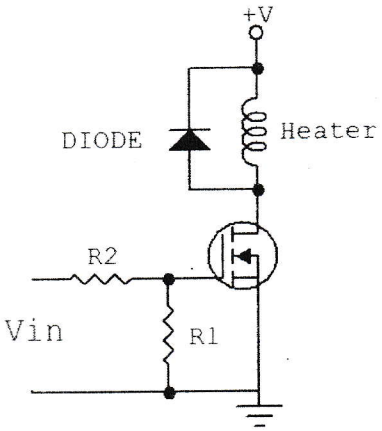
1) a) What are the advantages of using a metal oxide semiconductor field effect transistor (MOSFET), compared to a junction gate field effect transistor (JFET)?

(04 marks)

b) Explain the differences between the Depletion mode and the Enhancement mode of MOSFET.

(04 marks)

c) Use the given circuit to answer sub questions.



i. Identify the type of FET.
ii. Explain the functioning of FET circuit.
iii. Why a diode is placed in parallel with the load?

(06 marks)

d) State and briefly explain the four different regions of operations of a JFET.

(04 marks)

e) Is it possible to interchange Source and Drain of a FET? Explain your answer with an aid of a diagram.

(02 marks)

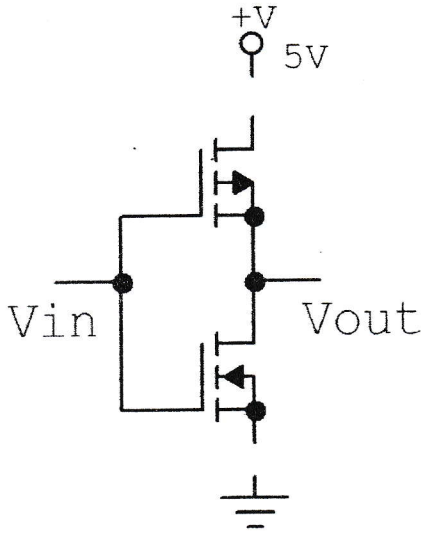
2) a) Convert the decimal 17.125 number into following forms.
   i. Binary form
   ii. Octal form
   iii. Hexadecimal form
   iv. Binary coded decimal (BCD) form

(04 marks)

b) Convert the following decimal numbers to 8-bit binary numbers using sign-magnitude and two's complement forms.
   i. + 21
   ii. - 19

(04 marks)

c) i. Explain the functioning of the MOSFET circuit shown below.



ii. What type of digital logic circuit is this?

(06 marks)

d) What is meant by following terms,
   i. Digital Logic States
   ii. Digital Logic Noise
   iii. Digital Logic Gate Noise Immunity

(06 marks)

3) A CCTV camera has following inputs; the camera image (A), an IR motion sensor (B), and the in-built battery voltage level (C). We intend to design an alarm that would go on (play a song) in following conditions. Define 0 as the low level and 1 as the high level.

- Battery voltage level is low.
- Human identification by the camera.
- Motion detection by the IR sensor and human identification by the camera.

a) Construct a truth table for the above system.

(05 marks)

Contd.

b) Obtain the sum of products, and the product of sums expressions from the truth table.
(05 marks)

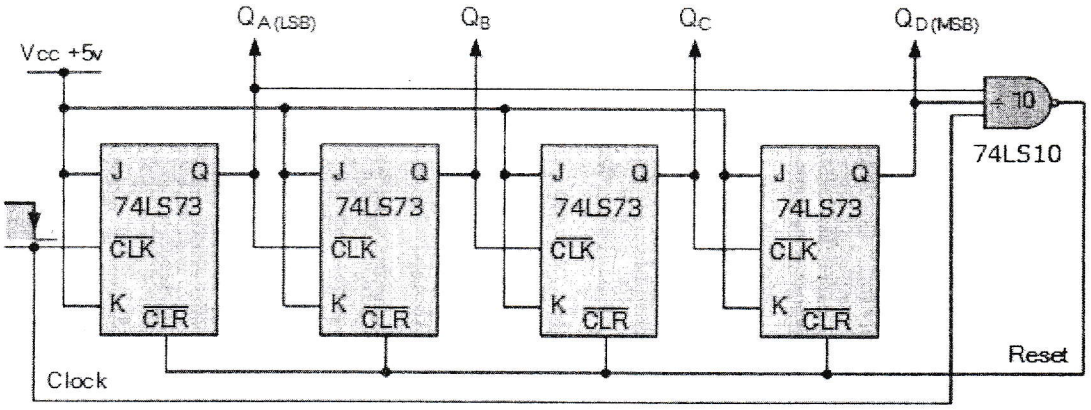
c) Construct a Karnaugh Map and obtain a Boolean expression for the results in part (b).
(05 marks)

d) Draw the logic circuit diagram for the Boolean expressions obtained in part (c).
(05 marks)

4) a) Compare the differences between SR, JK, T, D flip-flops.
(04 marks)

b) Solve following expressions using Boolean Algebra.
i. $Q = AB + BC(B + C)$
ii. $Q = \overline{ABC} + \bar{A}BC + \overline{AC}$
iii. $Q = \overline{(A \oplus B)} + ABC + \overline{AB}$
(06 marks)

c) Following figure shows an asynchronous counter (ripple counter), constructed from JK flip-flop.



i. Draw the output of Q_A, Q_B, Q_C, Q_D and input $\overline{CLR}$ with respect to Clock (up to 16 clock pluses).
(10 marks)

End.