51

RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. (General) Degree in Applied Sciences
First Year - Semester II Examination – February / March 2019

COM 1308 – DIGITAL LOGIC DESIGN

Time: Three (03) hours

Instructions to Candidates:

1. This paper contains **SIX (06)** questions in **FOUR (04)** pages.
2. All questions carry equal marks.
3. Answer **ANY FIVE (05)** questions.

---

1. a. Elaborate the requirement to use truth tables in explaining the operation of a logic circuit.

(05 marks)

b. Explain the operation of following logic gates using truth tables.

i. NAND
ii. NOR
iii. OR
iv. X-NOR
v. X-OR

(05 marks)

c. Using above truth tables, show how a NOT gate can be synthesized using other logic gates.

(05 marks)

d. Show that, $x + yz = (x + y).(x + z)$ using truth tables.

(05 marks)

2. a. State DeMorgan's theorem and prove it using truth tables.

(05 mark

b. Find the minimum sum-of-products expression for the function,

$$f = w\bar{x}\bar{y} + wxz + w\bar{x}y\bar{z}$$

using algebraic manipulation.

(05 mark

c. "NAND and NOR gates are universal gates". Discuss this statement explaining how the basic logic gates are synthesized using either NAND or NOR gates.

(05 mark

d. Prove that,

$$(\bar{x} + \bar{y} + \bar{z}).(\bar{x} + y + \bar{z}).(x + y + \bar{z}).(x + y + z) = \bar{x}z + x\bar{y}$$

using Karnaugh Maps.

(05 mark

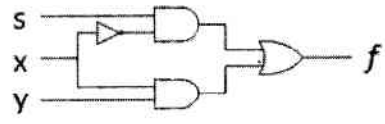
3. a. A digital lock is controlled by three fingerprint scanners. The fingerprint scanner produces when a defined fingerprint is identified. The lock opens when two persons present their fingerprints simultaneously. The lock will remain locked if all three persons press their fingers simultaneously. Design and implement a logic circuit to control the lock. Take the inputs from fingerprint scanners as f_1, f_2, and f_3 respectively.

(10 mark

b. Implement a full adder using NAND gates.

(10 mark

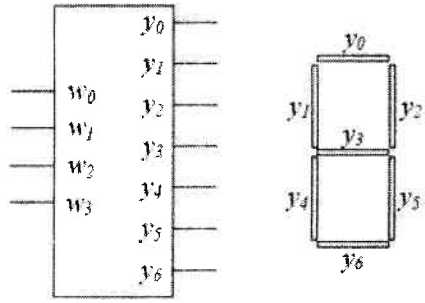
4. a. The following circuit shows the logical implementation of a 2-to-1 multiplexer.



Construct a 4-to-1 multiplexer using these circuits as building blocks.

(05 mark

b. A code converter is used to drive a 7-segment display according to the input from a decimal counter. In the figure, w_0, w_1, w_2, and w_3 denote the inputs from decimal counter. Outputs from the code converter, $y_0 - y_6$, corresponds to each segment of the display.



Design and implement the logical circuit required to produce the output y_4 of the converter.

(10 marks)

c. **"Encoders are used to reduce the number of bits needed to represent given information"**. Discuss this statement giving appropriate examples.

(05 marks)

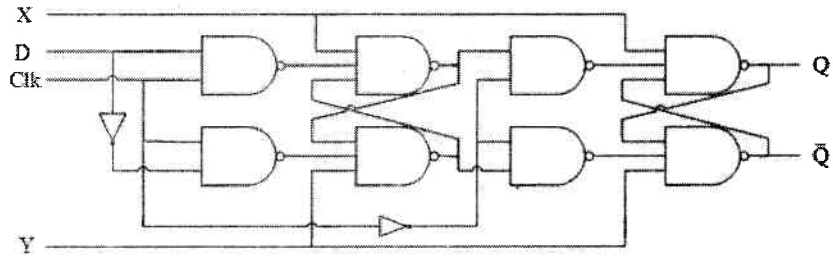
5. a. Using appropriate circuit diagrams show that a simple latch has two stable states.

(05 marks)

b. Elaborate how edge triggering is achieved in Master-Slave configuration using D Flip-Flops. Use timing diagrams to explain the operation.

(05 marks)

c. The following circuit shows a Master-Slave D Flip-Flop. Explain the use of the two signals X and Y.



(10 marks)

6. a. Design and implement a synchronous octal (divide-by-8) counter. (20 marks)

---- End ----