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RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. in Information Technology
First Year - Semester I Examination – March 2021

ICT 1303 – BASIC ELECTRONICS AND DIGITAL LOGIC DESIGN

Time: Three (03) hours

- There are six (06) questions in two (02) pages.
- All questions carry equal marks.
- Answer **ANY FIVE (05)** questions.

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1. a) Why cannot intrinsic semiconductors (semiconductors in their pure form) be used in electronic devices? (05 marks)

   b) Explain the operation of semiconductor diodes using suitable circuit diagrams as necessary.(

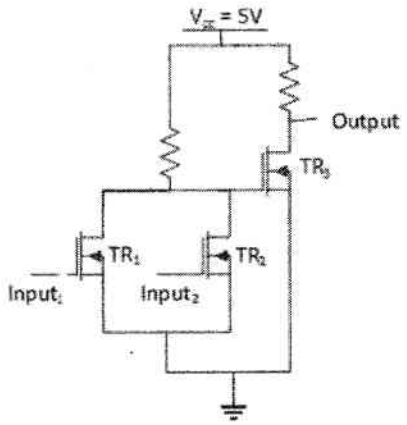
   c) Draw the circuit diagram of a full-wave bridge rectifier and explain its operation. (10 marks)

2. a) Discuss why it is required to dope the collector, base and emitter of a bipolar junction transistor at different levels. (05 marks)

   b) Explain why bipolar junction transistors are classified as current driven devices. (05 marks)

   c) Discuss the differences between Depletion Metal Oxide Semiconductor Field Effect Transistors (D-MOSFET) and Enhancement Metal Oxide Semiconductor Field Effect Transistors (E-MOSFET). (10 marks)

3. a) The following circuit shows an NMOS logic gate. Identify the gate by constructing its truth table.



(05 marks)

b) What is the function of the transistor TR_3 in the above circuit? (05 marks)

c) What changes are required to be done to the circuit to have the same functionality if TR_1 and TR_2 are replaced with PMOS FETs? (05 marks)

d) Discuss why it is always desirable to implement logic circuits using NAND and NOR (universal) gates. (05 marks)

4. A controller of a security system has four inputs and one output that drives the security system. The security system is activated when exactly three inputs are 1. Design the controller. You are required to write down the truth table, minterms and the Boolean expression. Then minimize the expression and draw the minimal circuit. Clearly state all assumptions you made. (20 marks)

5. a) Design a half adder using NAND gates. (10 marks)

b) Explain how a master-slave configuration achieves edge triggering. (05 marks)

c) Construct a JK flip-flop using a D flip-flop. (05 marks)

6. Design a modulo-8 (divide-by-8) synchronous up/down counter using D flip-flops. (20 marks)

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