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RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. (Information and Communication Technology) Degree
First Year - Semester I Examination – September/October 2019

ICT 1303 – BASIC ELECTRONICS AND DIGITAL LOGIC DESIGN

Time: Three (03) hours

Instructions to Candidates:

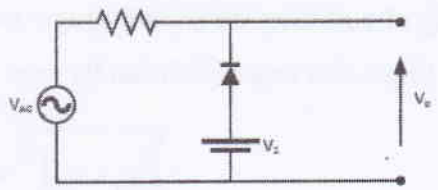
1. This paper contains **six (06)** questions in **three (03)** pages.
2. Answer any **five (05)** questions.

1.

a) Explain the difference between **intrinsic semiconductors** and **extrinsic semiconductors**. ***(05 Marks)***

b) Why do diodes only conduct current in one direction? ***(05 Marks)***

c) The following circuit shows a voltage clipper. Explain its operation using appropriate graphs of V_O versus time (Assume that $V_1 < V_m$, where V_m is the peak voltage of AC source). ***(10 Marks)***



2.

a) Explain the operation of an active bipolar junction transistor. ***(05 Marks)***

b) Explain the three small signal amplifier configurations and their applications.

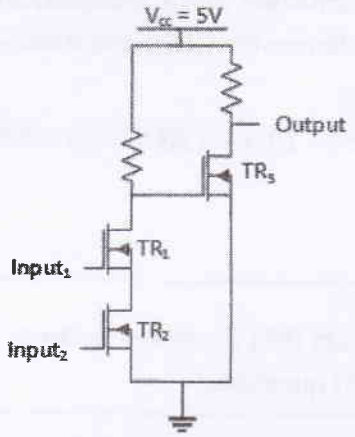
(05 Marks)

c) Discuss how **Field Effect Transistors** differ from **Bipolar Junction Transistors**.

(10 Marks)

3.

a) The following circuit shows an NMOS AND gate. Explain the operation of the transistor TR_3. ***(05 Marks)***



b) Minimize the following Boolean expression and draw the minimized circuit.

$$f(a, b, c) = \bar{a}\bar{b}c + a\bar{b}\bar{c} + a\bar{b}c + ab\bar{c}$$

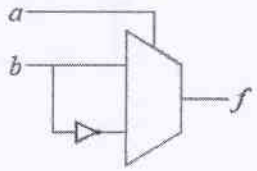
(10 Marks)

c) Implement the minimized logic circuit using NAND gates. ***(05 Marks)***

4.

a) Discuss how an X-OR gate can be used to complement a single bit. ***(05 Marks)***

b) The following circuit diagram shows a logic circuit implemented using a 2-to-1 multiplexer. Show that this circuit can be used to add two bits. ***(10 Marks)***

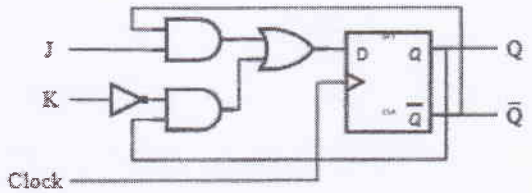


c) Draw a diagram to show a logic circuit you would build to add three bits using the circuit shown in (b) above as the building block. ***(05 Marks)***

5.

a) Explain what happens when both inputs of a Set-Reset (S-R) latch is set to 1. **(*05 Marks*)**

b) The following diagram shows a J-K flip-flop implemented using a D flip-flop. Explain its operation and build the characteristic table. **(*10 Marks*)**



c) Implement a T flip-flop using a D flip-flop. **(*05 Marks*)**

6.

a) Design a synchronous divide-by-12 up counter using T flip-flops. **(*20 Marks*)**

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