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RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. (General) Degree in Applied Sciences
Third Year - Semester I Examination – September / October 2019

PHY 3212 – ELECTRONICS II

Time: Two (02) hours

- **Answer all questions**
- A non-programmable calculator is permitted.
- All undefined symbols or terms appear below have their usual meanings.

1. a) Express + 44 and – 62 as an 8 bit binary number in

   i. sign magnitude

   ii. 1's complement method

   iii. 2's complement method **(04 marks)**

   b) In 16-bit 2's complement binary notation, add the maximum positive integer to the minimum negative integer. Express the answer in true binary. **(06 marks)**

   c) Convert the following decimal numbers to binary, multiply by partial products method, and divide by 2's complement method.

   i. -36 x 64 ii. 168 / (-14) **(08 marks)**

   d) Convert the following binary numbers to gray code, and draw a logic diagram for 6 bits binary- to- gray- code converter.

   i. 110010 ii. 010101001 **(07 marks)**

2. a) Design a parity generation circuit for a 5-bit data (4-bit message with an odd parity bit) to be transmitted by a computer. Give the following for the parity generation.

   i. the truth table, **(05 marks)**

   ii. Karnaugh map, **(05 marks)**

   iii. logic expression, and **(05 marks)**

   iv. logic diagram using only XOR and XNOR gates. **(06 marks)**

   b) State two practical advantages and disadvantages of using parity bits to detect errors. **(04 marks)**

3. a) Explain the universal property of NOR gate. **(06 marks)**

b) Use a Karnaugh map to find the minimum sum of products (SOP) form for the following expression.

$f(A,B,C,D) = A\,\bar{B}\,\bar{C}\,D + A\,C\,\bar{D} + B\,\bar{C}\,D + \bar{A}\,B\,C\,\bar{D}$ **(05 marks)**

c) Use a Karnaugh map to find the minimum product of sums (POS) form for the following expression.

$g(W,X,Y,Z) = (X + \bar{Y})(W + \bar{Z})(\bar{X} + \bar{Y} + \bar{Z})(W + X + Y + Z)$ **(05 marks)**

d) i. Convert the following POS expression to minimum SOP expression using a Karnaugh map.

$f(A,B,C,D) = (\bar{A} + B)(\bar{A} + \bar{B} + \bar{C})(B + \bar{C} + D)(A + \bar{B} + C + \bar{D})$

(05 marks)

ii. Draw the combinational logic circuit for the above minimum SOP expression in (d)(i). using only XNOR, AND and OR gates. **(04 marks)**

4. A code converter converts a BCD number ($A_3A_2A_1A_0$) to excess 3 code ($B_3B_2B_1B_0$) where A_0 and B_0 are LSBs.

a) Give the truth table for the conversion. **(05 marks)**

b) Obtain the SOP expressions for each bit of excess 3 code. **(04 marks)**

c) Map the expressions in (b) on Karnaugh maps. **(12 marks)**

(Please mark the six invalid codes of BCD as don't cares (X)).

d) Find the minimum SOP expressions. **(04 marks)**

(The don't cares (X) can only use to form groups if it simplifies logic. However there is no requirement to group all or any of the don't cares (X)).

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