RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

B.Sc. (General) Degree in Applied Sciences
First Year - Semester II Examination – Oct/Nov 2017

COM 1308 – DIGITAL LOGIC DESIGN

Time: Three(03) hours

Instruction to candidates

- This is a closed book examination.
- There are THREE (3) pages in the question paper.
- Question paper consists of SIX (6) questions.
- Answer any FIVE (5) questions.
- All questions carry equal marks.

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1. Question 01

a) Prove the given equation using perfect induction (5 marks)

$F(A,B,C,D) = A'B+BC'+BC+AB'C' = B+AC'$

b) Prove the given equation using algebraic manipulation. (5 marks)

$F(A,B,C) = A'B'C'+A'B+ABC'+AC = B+A'C'+AC$

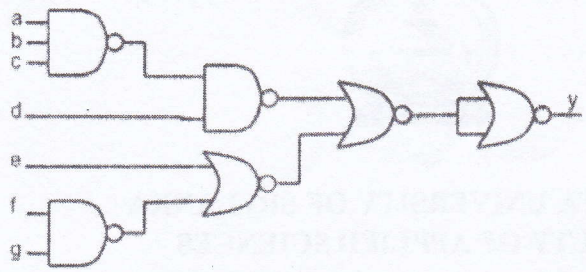
c) Simplify the given expression using a Karnaugh map. (4 marks)

$F(A,B,C,D) = A'B'C'D'+A'BC'D'+ABC'D'+AB'C'D'+ABC'D+AB'C'D$

d) Draw the circuit diagram of the given expression F(X,Y,Z) (3 marks)

$F(X,Y,Z) = (YZ+YZ')' +X'Y'Z$

e) Write down the Boolean expression for the given circuit. (3 marks)



(20 marks)

2. Question 02

a) Discuss the differences and similarities in the behavior of J-K flip-flop and T flip-flop.

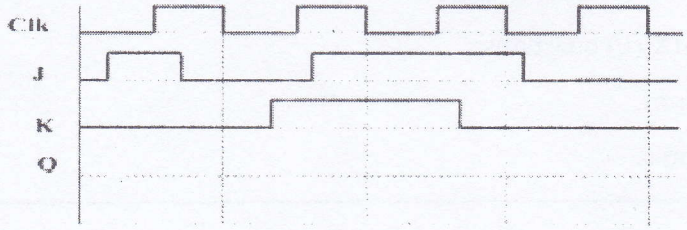
(4 marks)

b) Draw a circuit diagram of an S-R flip-flop using logic gates. (3 marks)

c) Briefly explain what happens when both inputs of an S-R flip-flop are logical one.

(5 marks)

d) Complete the given timing diagram of a J-K Flip Flop (5 marks)



e) Draw the State transition diagram of a D flip-flop. (3 marks)

(20 marks)

3. Question 03

a) Briefly describe the behavior of a Decoder explaining why it is said to have an "one hot" output

(4 marks)

b) Write down the truth table of a Full Adder. (4 marks)

c) State a sequential component which can be created using each of the given flip-flops.

(2 marks)

i. D flip-flops ii. T flip-flops

d) Design a 2-bit comparator with two inputs (A,B) and three outputs (A=B, A<B and A>B)

(6 marks)

e) Draw the design of a 4-bit Serial-In-Parallel-Out Register using flip-flops.

(4 marks)

(20 marks)

4. Question 04

Design a circuit with 4 inputs which takes a 4-bit binary number from 0 to 10 and have 3 outputs as Evan number, Odd number and Prime number. If the input number is an Evan number the Evan number output should be one. If the input number is an Odd number the Odd number output should be one. If the input number is a Prime number, the Prime number output should be one.

a) Create the truth table for the above system considering all the possibilities. (5 marks)

b) Obtain the POS expressions for the truth table created in part (a). (4 marks)

c) Simplify the obtained expressions using Karnaugh maps. (6 marks)

d) Draw the simplified circuit. (5 marks)

(20 marks)

5. Question 05

a) Compare and contrast a PLA(Programmable Logic Array) and PAL (Programmable Array Logic) (4 marks)

b) Draw the gate level diagram for a programmed PLA that implement the functions below (4 marks)

F=(A+B')(C+A'B)' G=AB'+C(A'+B)'.

c) Draw the schematic diagram for a programmed PLA that implements the functions in part (b). (4 marks)

d) Write the simplified truth table for a 2 bit 4x1Multiplexer. (4 marks)

e) Draw the circuit diagram using logic gates for the Multiplexer in part (d). (4 marks)

(20 marks)

6. Question 06

a) Briefly describe the operations of a shift register using a suitable diagram. (3 marks)

b) Design a 3 bit Synchronous Up Counter with T flip-flops (5 marks)

c) Draw the state transition diagram for the Up Counter designed in part (b) (4 marks)

d) Briefly explain how to model a digital system using VHDL? (3 marks)

e) Model a Half Adder using VHDL. (5 marks)

(20 marks)

END