RAJARATA UNIVERSITY OF SRI LANKA
FACULTY OF APPLIED SCIENCES

Bachelor of Science in Information Technology
Second Year - Semester II Examination – January / February 2023

ICT 2408 – COMPUTER ORGANIZATION AND ARCHITECTURE

Time: Three (03) hours

Instructions

- Answer **ALL** questions.
- This paper contains **five** (05) questions in **three** (03) pages.

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1. a) List four (04) characteristics of second generation computers.

(4 marks)

b) What do you mean by computer organization? Give two (02) examples for organizational attributes of a computer system.

(4 marks)

c) Explain the difference between an architectural design issue and an organizational design issue using an example.

(4 marks)

d) Explain why many computer manufacturers offer a family of computer models, all with the same architecture but with differences in organization.

(4 marks)

e) Distinguish between DRAM and SRAM.

(4 Marks)

2. a) What are program interrupts in instruction execution? Give two (02) examples.

(4 marks)

b) Using a suitable diagram, explain the basic instruction cycle with interrupts.

(6 marks)

c) Explain use of interrupts from the point of view of the user programs.

(4 marks)

d) List and briefly explain two (02) approaches to deal with multiple interrupts.

(6 marks)

3. a) Briefly explain the function of any two (02) "Control and Status Registers" that are used to move data between the CPU and main memory.

(4 marks)

b) Many processor designs include a register or set of registers, often known as the program status word (PSW). List four (04) common fields that can be included in a PSW. State the uses of two (02) of them.

(6 marks)

c) What are the typical elements of a machine instruction?

(4 marks)

d) The main memory of a computer has 256 K words of 32 bits each. The instruction set of the CPU of the computer consists of 150 different operations. All instructions have an operation code and two (02) equal operand fields. The length of each instruction in the instruction set is equal to a memory word. Draw the instruction format and specify the number of bits in each field.

(6 marks)

4. a) Briefly explain the following with respect to the bus interconnection structure of a computer:

i. Address bus.

ii. Bus width.

(4 marks)

b) Consider a hypothetical microprocessor generating a 16-bit address and having a 16-bit data bus.

i. What is the maximum memory address space that the processor can access directly if it is connected to an 8-bit memory?

ii. If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support?

(4 marks)

c) Briefly explain the following memory access methods:

i. Random Access.

ii. Associative Access.

(4 marks)

d) Briefly define the following techniques for performing I/O operations.

i. Programmed I/O.

ii. Interrupt-driven I/O.

(4 marks)

e) Assume an instruction pipeline with four (04) stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a timing diagram for the execution of four (04) instructions. Assume all stages are of equal duration and there are no branch instructions.

(4 marks)

5. a) Explain the function of MUL assembly language instruction.

(4 marks)

b) Write assembly language instructions to perform each of the following tasks:

i. Set register CX equal to zero (0).

ii. Save the content of the memory location pointed by the register BX in register AX.

iii. Test the contents of register AX and variable A.

iv. Branch to the label TEST if the content of register AX is greater than or equal to the content of variable A.

v. Add one (01) to register CX.

vi. Compare the content of register CX with the value ten (10). Label the instruction as TEST.

vii. Branch to the label OUT if the content of register CX is equal to ten (10).

(7 marks)

c) Describe the following input/output operations in assembly language:

i. Input a character from the keyboard without echo.

ii. Send a character to the monitor.

(4 marks)

d) Assume the three symbolic variables N1, N2, N3 contain integer values. Write an assembly language code fragment that moves the largest value among N1, N2, and N3 into the register AX. Use only the instructions MOV, CMP, and JBE (jump if below or equal).

(5 marks)

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