硬體描述語言作業一

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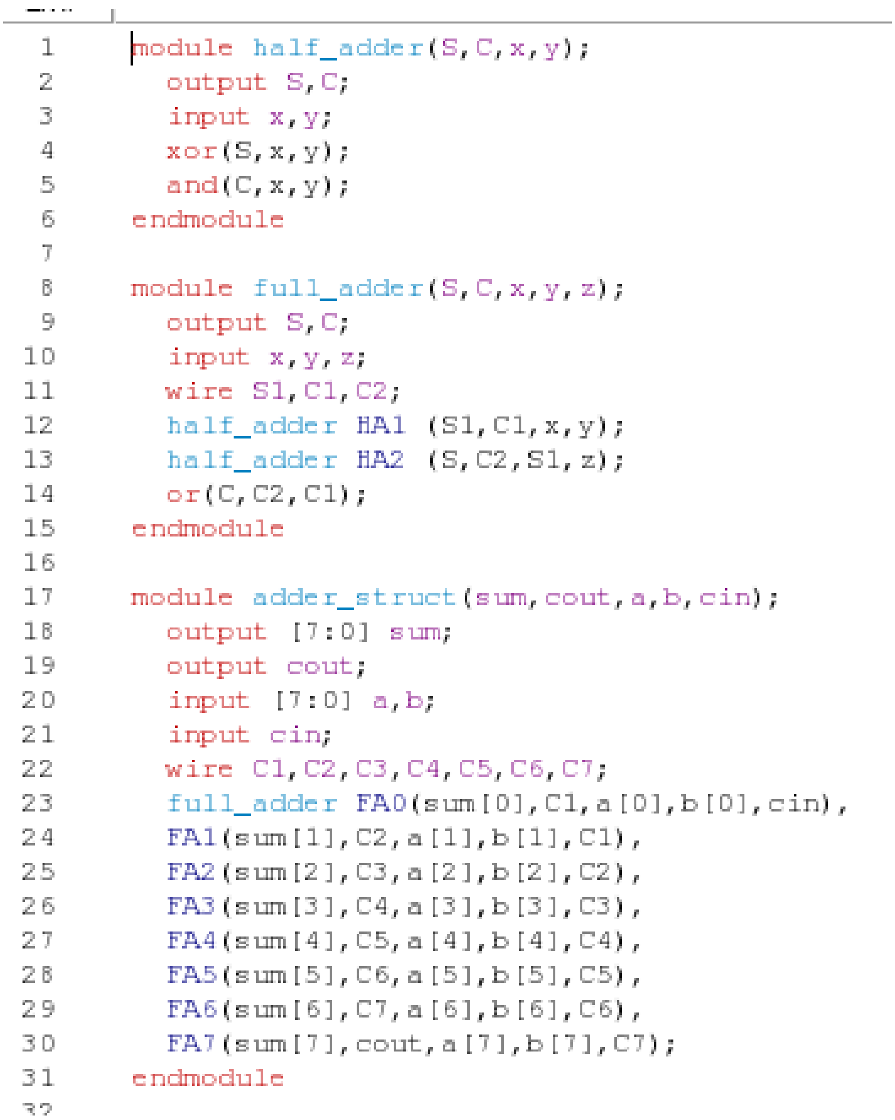
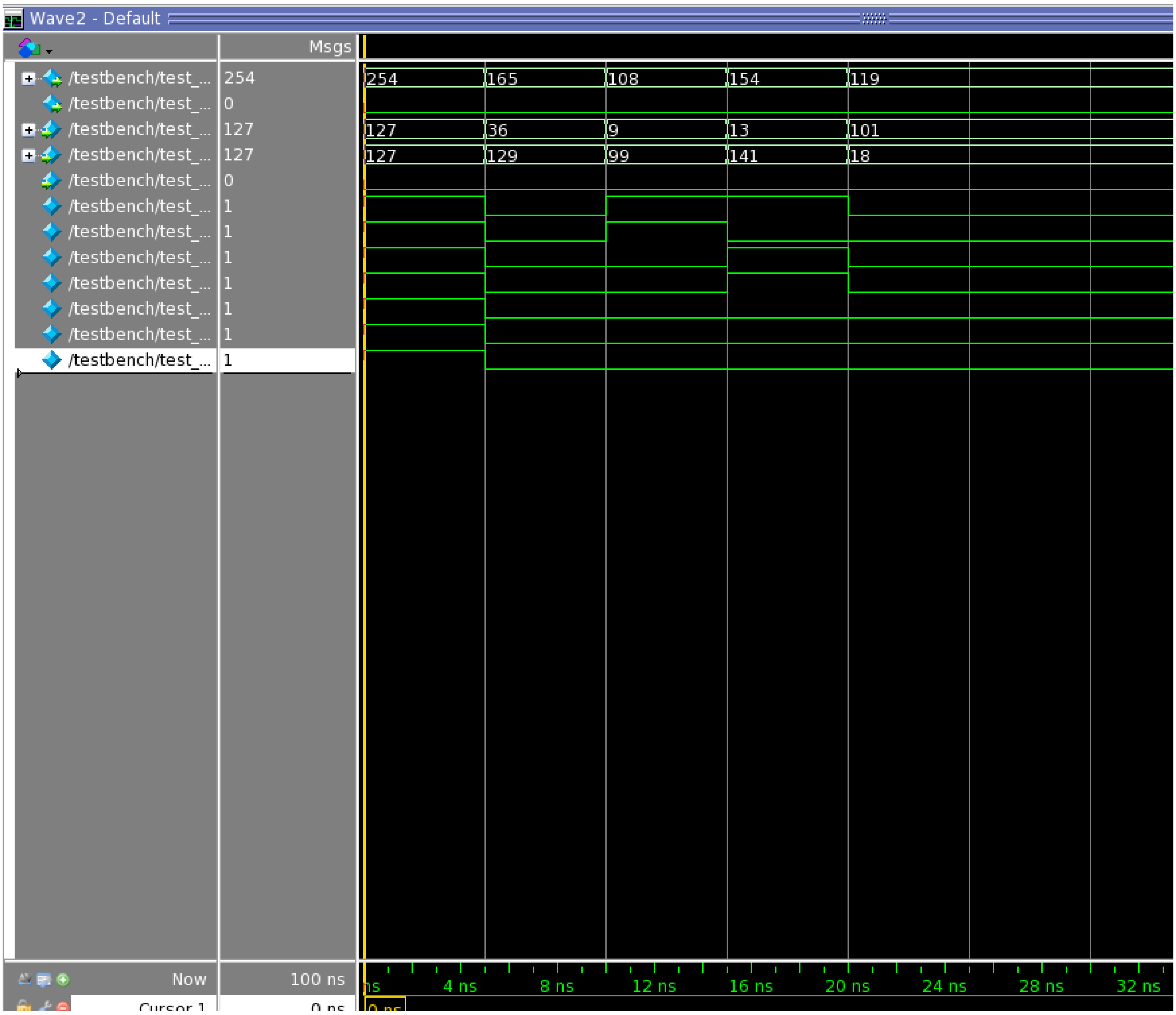
Structure-Level modeling

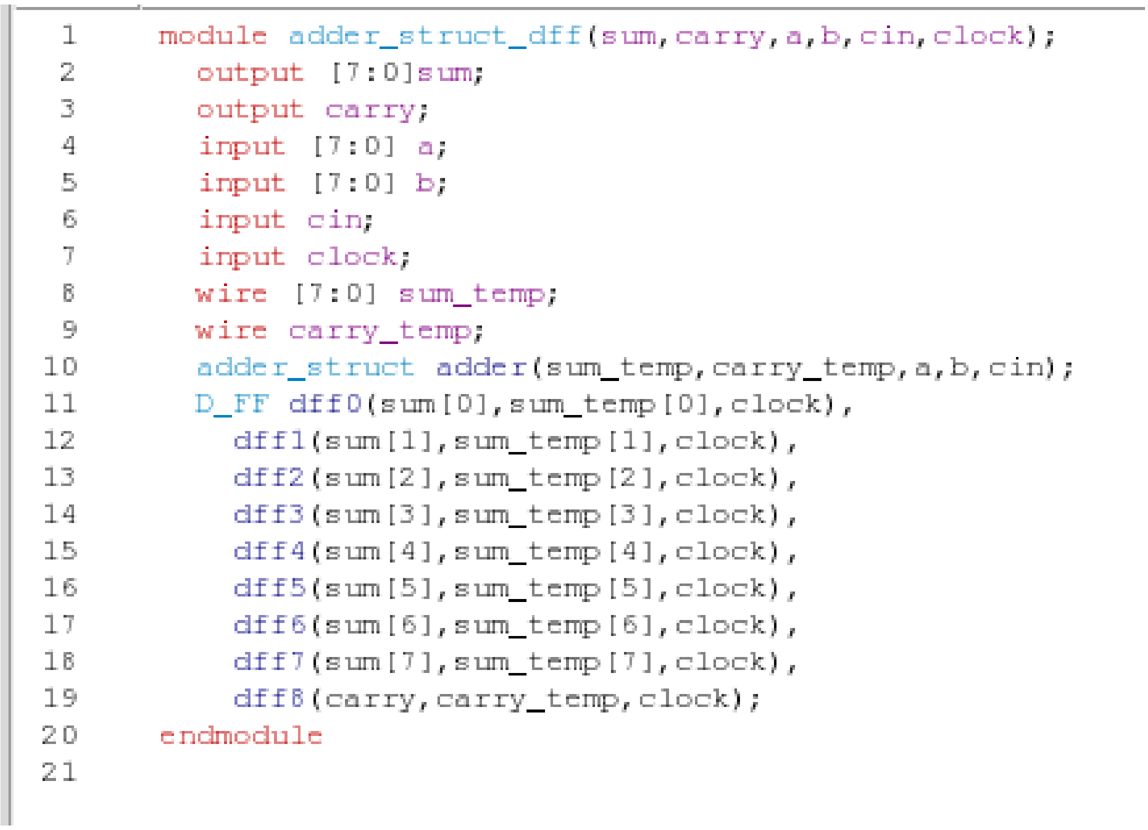


```
module half_adder(S,C,x,y);
  output S,C;
  input x,y;
  xor(S,x,y);
  and(C,x,y);
endmodule

module full_adder(S,C,x,y,z);
  output S,C;
  input x,y,z;
  wire S1,C1,C2;
  half_adder HA1 (S1,C1,x,y);
  half_adder HA2 (S,C2,S1,z);
  or(C,C2,C1);
endmodule

module adder_struct(sum,cout,a,b,cin);
  output [7:0] sum;
  output cout;
  input [7:0] a,b;
  input cin;
  wire C1,C2,C3,C4,C5,C6,C7;
  full_adder FA0(sum[0],C1,a[0],b[0],cin),
  FA1(sum[1],C2,a[1],b[1],C1),
  FA2(sum[2],C3,a[2],b[2],C2),
  FA3(sum[3],C4,a[3],b[3],C3),
  FA4(sum[4],C5,a[4],b[4],C4),
  FA5(sum[5],C6,a[5],b[5],C5),
  FA6(sum[6],C7,a[6],b[6],C6),
  FA7(sum[7],cout,a[7],b[7],C7);
endmodule
```

產生的波形圖

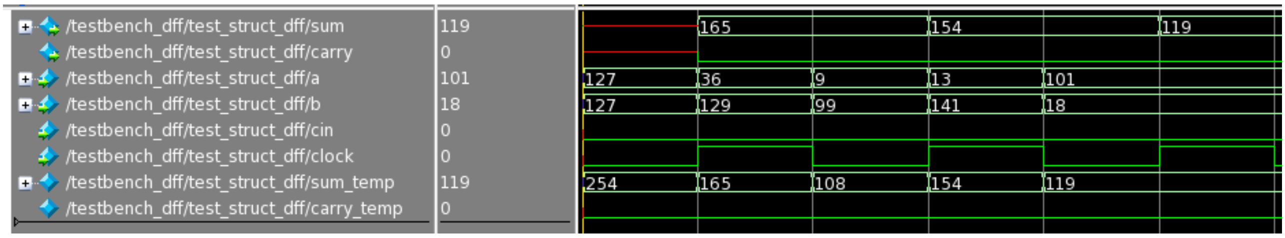

Wave2 - Default
Msgs
/testbench/test_... 254
/testbench/test_... 0
/testbench/test_... 127
/testbench/test_... 127
/testbench/test_... 0
/testbench/test_... 1
/testbench/test_... 1
/testbench/test_... 1
/testbench/test_... 1
/testbench/test_... 1
/testbench/test_... 1
/testbench/test_... 1
254 165 108 154 119
127 36 9 13 101
127 129 99 141 18
Now 100 ns
Cursor 1 0 ns
ns 4 ns 8 ns 12 ns 16 ns 20 ns 24 ns 28 ns 32 ns
0 ns

加上 D-Flip-Flop



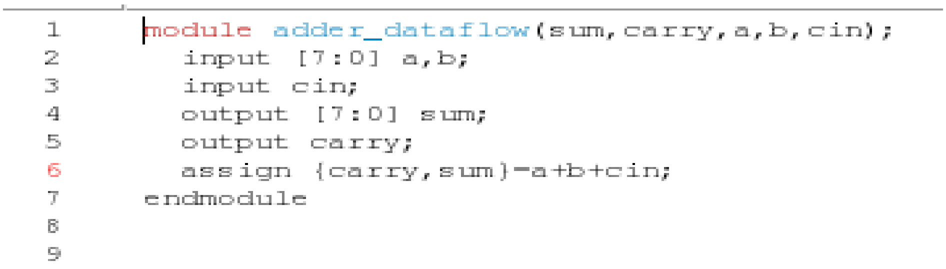
```
module adder_struct_dff(sum,carry,a,b,cin,clock);
  output  [7:0]sum;
  output carry;
  input  [7:0] a;
  input  [7:0] b;
  input cin;
  input clock;
  wire  [7:0] sum_temp;
  wire carry_temp;
  adder_struct adder(sum_temp,carry_temp,a,b,cin);
  D_FF dff0(sum[0],sum_temp[0],clock),
    dff1(sum[1],sum_temp[1],clock),
    dff2(sum[2],sum_temp[2],clock),
    dff3(sum[3],sum_temp[3],clock),
    dff4(sum[4],sum_temp[4],clock),
    dff5(sum[5],sum_temp[5],clock),
    dff6(sum[6],sum_temp[6],clock),
    dff7(sum[7],sum_temp[7],clock),
    dff8(carry,carry_temp,clock);
endmodule
```

把結果先存到 flip flop 裡面，等到 clock 為正時產生結果

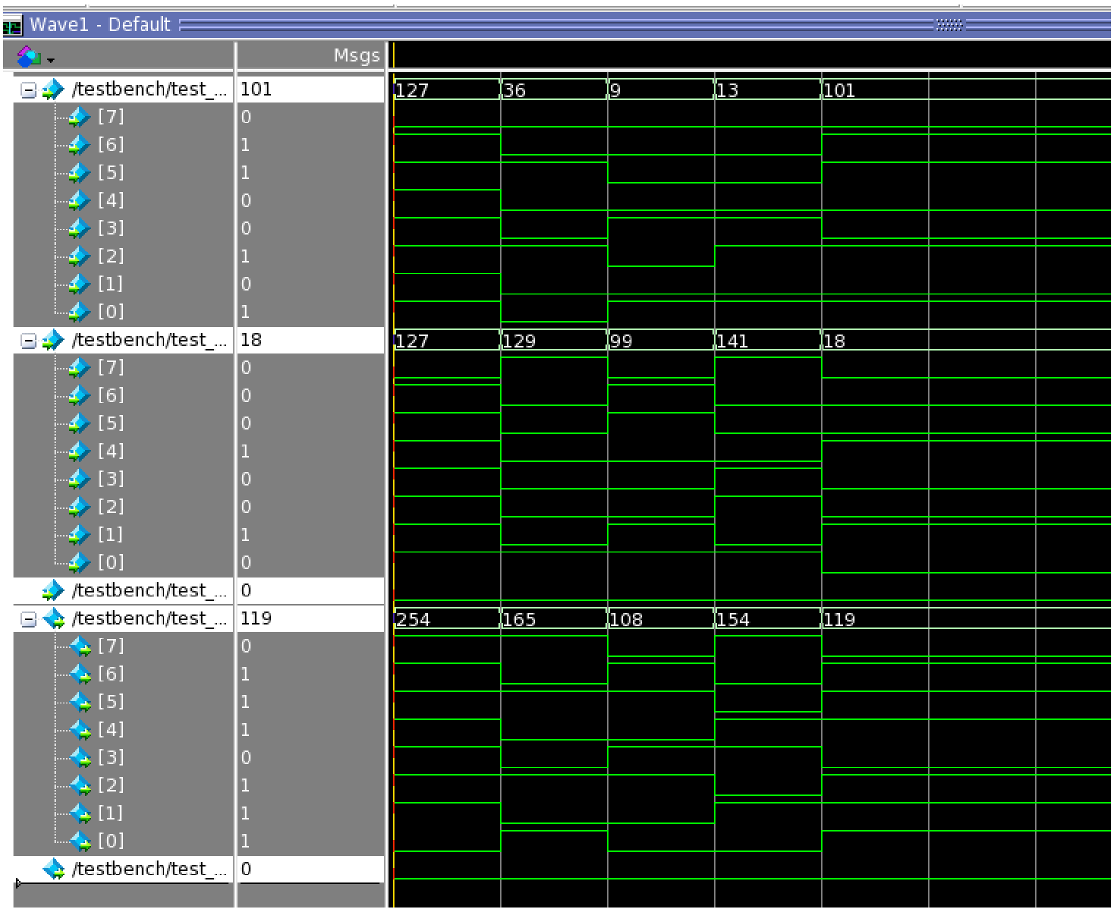


```
/testbench_dff/test_struct_dff/sum         119   165 154 119
/testbench_dff/test_struct_dff/carry       0
/testbench_dff/test_struct_dff/a           101   127 36 9 13 101
/testbench_dff/test_struct_dff/b           18    127 129 99 141 18
/testbench_dff/test_struct_dff/cin         0
/testbench_dff/test_struct_dff/clock       0
/testbench_dff/test_struct_dff/sum_temp    119   254 165 108 154 119
/testbench_dff/test_struct_dff/carry_temp  0
```

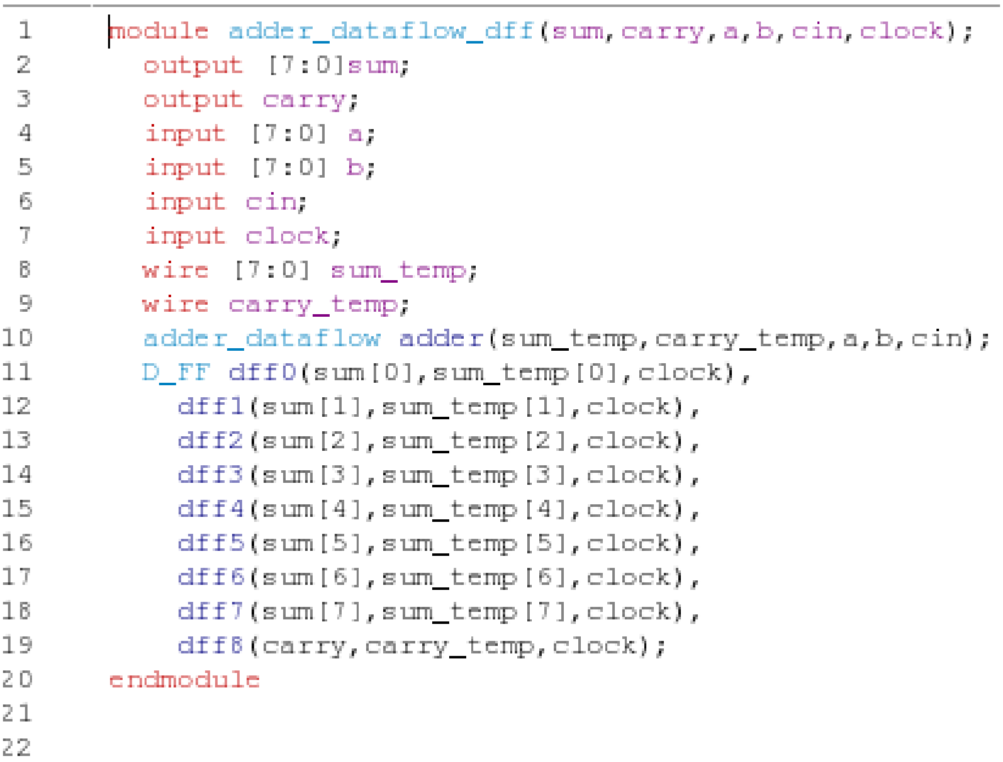
Data flow



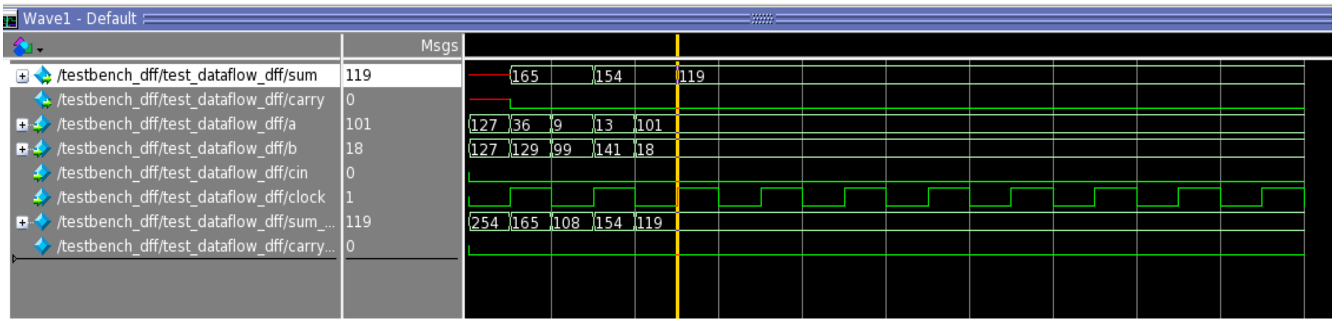
```
module adder_dataflow(sum,carry,a,b,cin);
  input  [7:0]  a,b;
  input  cin;
  output  [7:0]  sum;
  output  carry;
  assign {carry,sum}=a+b+cin;
endmodule
```



配上 DFF

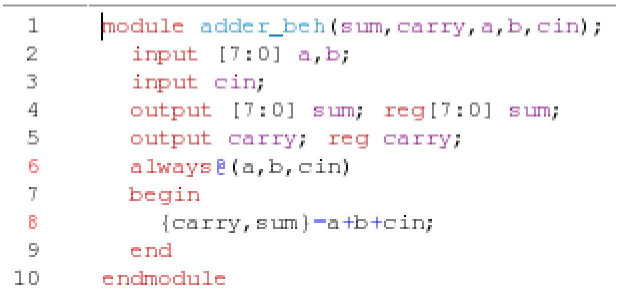


```
module adder_dataflow_dff(sum,carry,a,b,cin,clock);
  output  [7:0]sum;
  output carry;
  input  [7:0] a;
  input  [7:0] b;
  input cin;
  input clock;
  wire  [7:0] sum_temp;
  wire carry_temp;
  adder_dataflow adder(sum_temp,carry_temp,a,b,cin);
  D_FF dff0(sum[0],sum_temp[0],clock),
    dff1(sum[1],sum_temp[1],clock),
    dff2(sum[2],sum_temp[2],clock),
    dff3(sum[3],sum_temp[3],clock),
    dff4(sum[4],sum_temp[4],clock),
    dff5(sum[5],sum_temp[5],clock),
    dff6(sum[6],sum_temp[6],clock),
    dff7(sum[7],sum_temp[7],clock),
    dff8(carry,carry_temp,clock);
endmodule
```

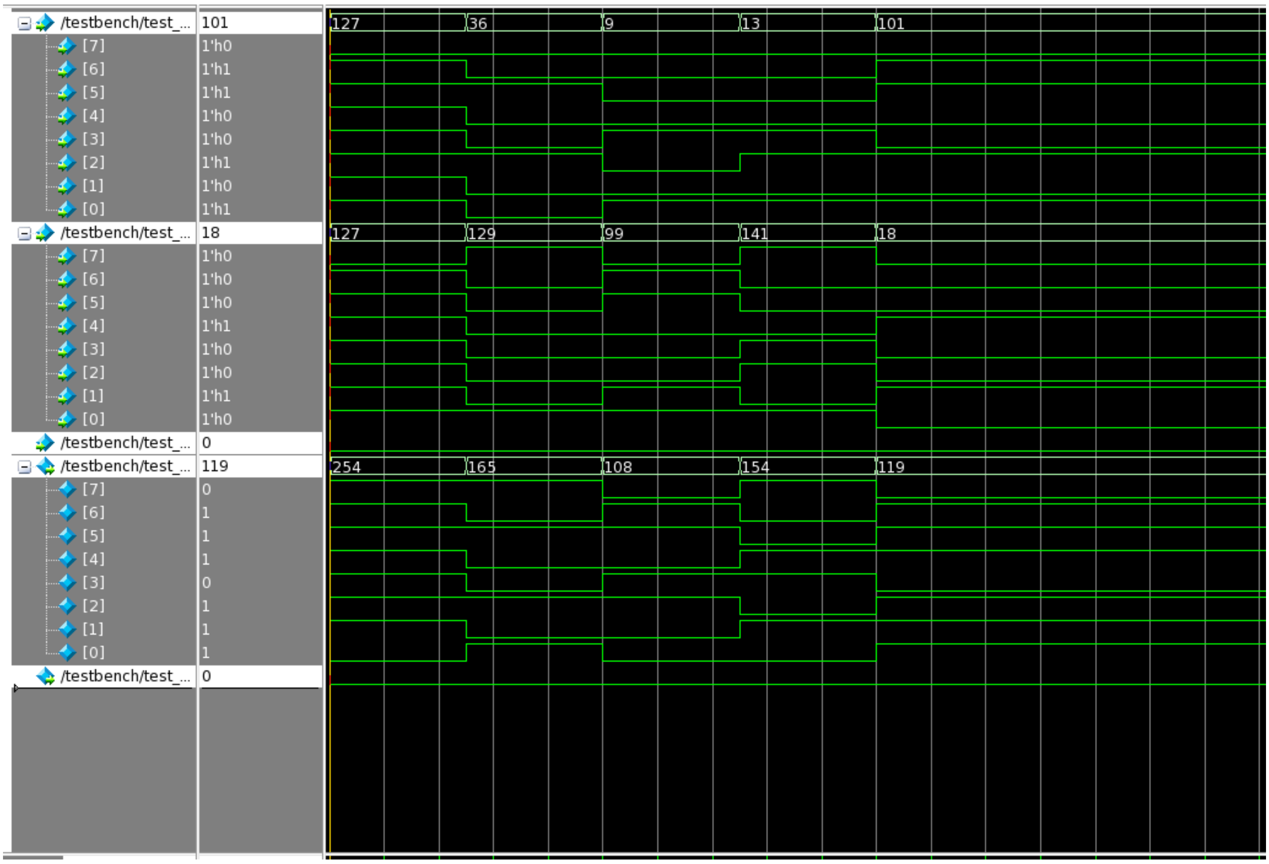


```
/testbench_dff/test_dataflow_dff/sum       119
/testbench_dff/test_dataflow_dff/carry     0
/testbench_dff/test_dataflow_dff/a         101
/testbench_dff/test_dataflow_dff/b         18
/testbench_dff/test_dataflow_dff/cin       0
/testbench_dff/test_dataflow_dff/clock     1
/testbench_dff/test_dataflow_dff/sum_...   119
/testbench_dff/test_dataflow_dff/carry...  0
```

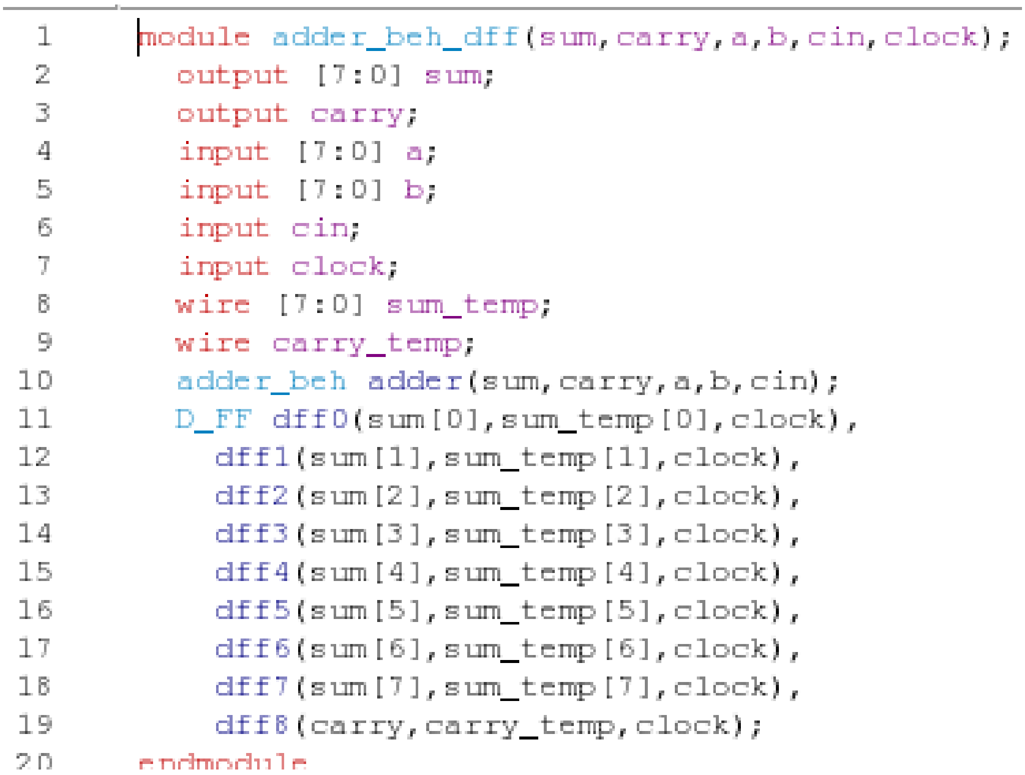
Behavioral modeling



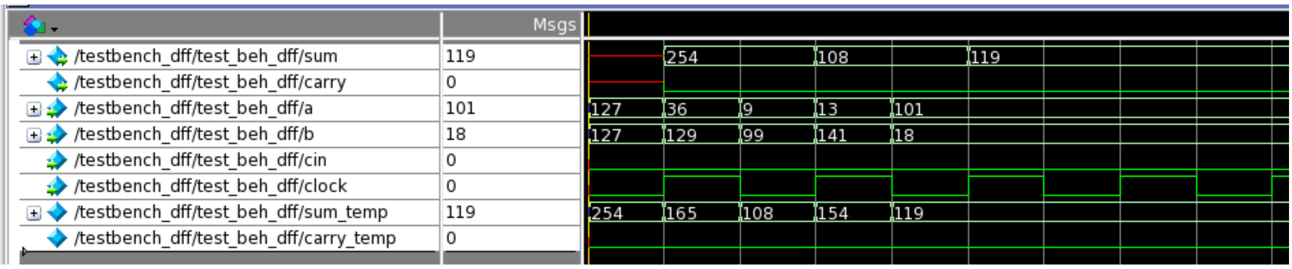
```
module adder_beh(sum,carry,a,b,cin);
  input  [7:0] a,b;
  input cin;
  output  [7:0] sum;  reg[7:0] sum;
  output carry;  reg carry;
  always@(a,b,cin)
  begin
    {carry,sum}=a+b+cin;
  end
endmodule
```



配上 DFF

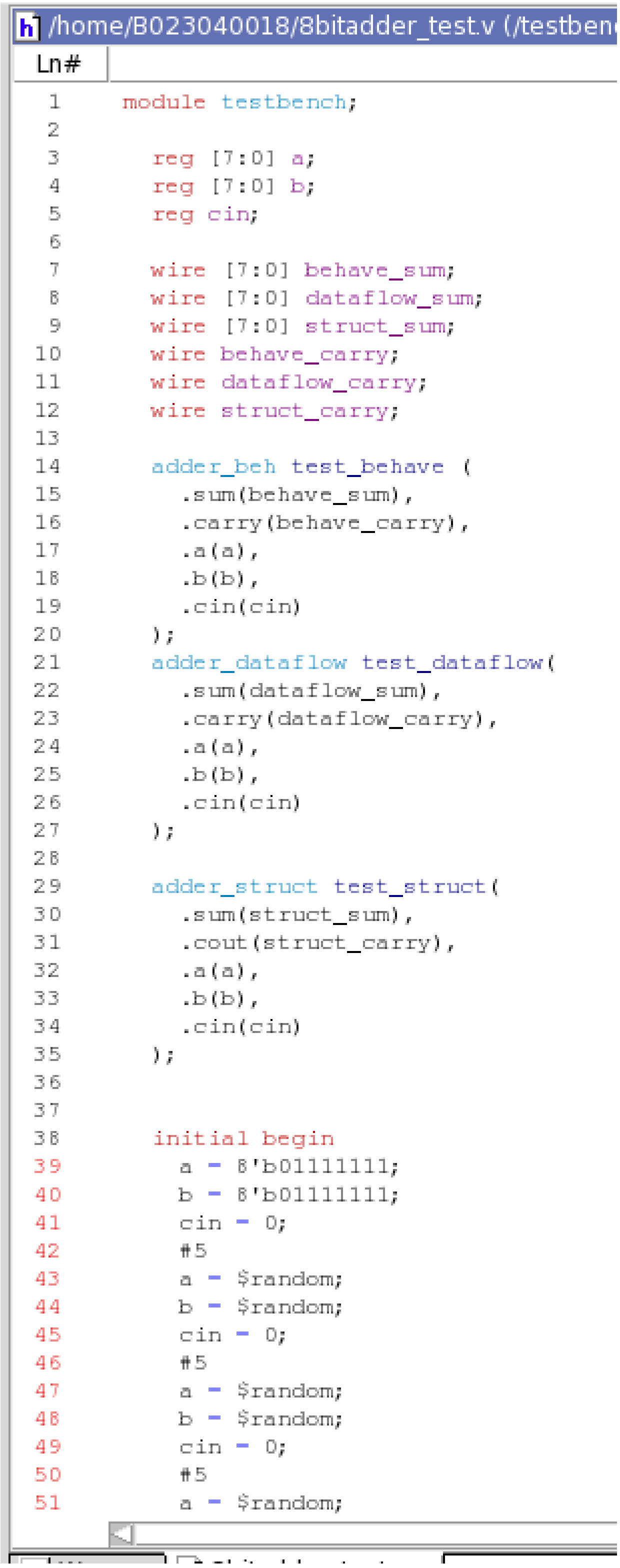


```
module adder_beh_dff(sum,carry,a,b,cin,clock);
  output [7:0] sum;
  output carry;
  input [7:0] a;
  input [7:0] b;
  input cin;
  input clock;
  wire [7:0] sum_temp;
  wire carry_temp;
  adder_beh adder(sum,carry,a,b,cin);
  D_FF dff0(sum[0],sum_temp[0],clock),
    dff1(sum[1],sum_temp[1],clock),
    dff2(sum[2],sum_temp[2],clock),
    dff3(sum[3],sum_temp[3],clock),
    dff4(sum[4],sum_temp[4],clock),
    dff5(sum[5],sum_temp[5],clock),
    dff6(sum[6],sum_temp[6],clock),
    dff7(sum[7],sum_temp[7],clock),
    dff8(carry,carry_temp,clock);
endmodule
```



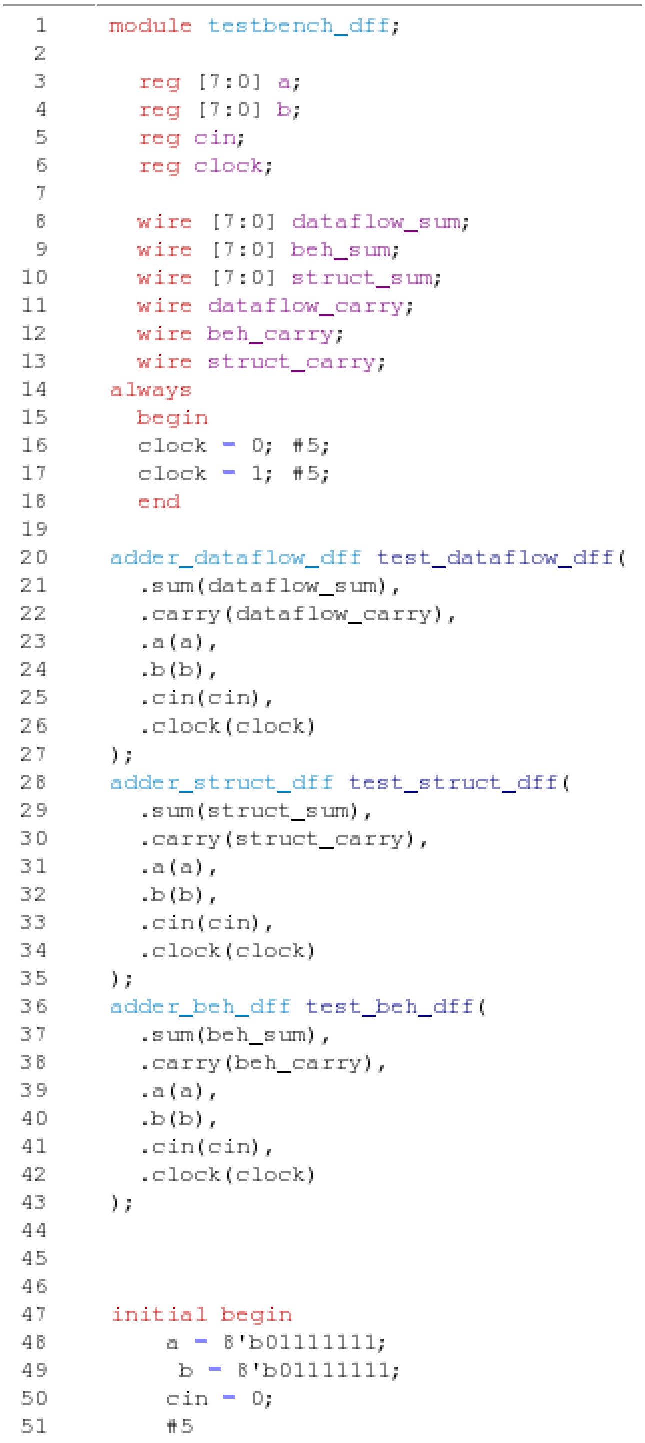
	Msgs
/testbench_dff/test_beh_dff/sum	119
/testbench_dff/test_beh_dff/carry	0
/testbench_dff/test_beh_dff/a	101
/testbench_dff/test_beh_dff/b	18
/testbench_dff/test_beh_dff/cin	0
/testbench_dff/test_beh_dff/clock	0
/testbench_dff/test_beh_dff/sum_temp	119
/testbench_dff/test_beh_dff/carry_temp	0

附上 Testbench



```
module testbench;

  reg [7:0] a;
  reg [7:0] b;
  reg cin;

  wire  [7:0] behave_sum;
  wire  [7:0] dataflow_sum;
  wire  [7:0] struct_sum;
  wire behave_carry;
  wire dataflow_carry;
  wire struct_carry;

  adder_beh test_behave (
    .sum(behave_sum),
    .carry(behave_carry),
    .a(a),
    .b(b),
    .cin(cin)
  );
  adder_dataflow test_dataflow(
    .sum(dataflow_sum),
    .carry(dataflow_carry),
    .a(a),
    .b(b),
    .cin(cin)
  );

  adder_struct test_struct(
    .sum(struct_sum),
    .cout(struct_carry),
    .a(a),
    .b(b),
    .cin(cin)
  );


  initial begin
    a = 8'b01111111;
    b = 8'b01111111;
    cin = 0;
    #5
    a = $random;
    b = $random;
    cin = 0;
    #5
    a = $random;
    b = $random;
    cin = 0;
    #5
    a = $random;
```

DFF 的 testbench



```
module testbench_dff;

  reg [7:0] a;
  reg [7:0] b;
  reg cin;
  reg clock;

  wire [7:0] dataflow_sum;
  wire [7:0] beh_sum;
  wire [7:0] struct_sum;
  wire dataflow_carry;
  wire beh_carry;
  wire struct_carry;
always
  begin
  clock = 0; #5;
  clock = 1; #5;
  end

adder_dataflow_dff test_dataflow_dff(
  .sum(dataflow_sum),
  .carry(dataflow_carry),
  .a(a),
  .b(b),
  .cin(cin),
  .clock(clock)
);
adder_struct_dff test_struct_dff(
  .sum(struct_sum),
  .carry(struct_carry),
  .a(a),
  .b(b),
  .cin(cin),
  .clock(clock)
);
adder_beh_dff test_beh_dff(
  .sum(beh_sum),
  .carry(beh_carry),
  .a(a),
  .b(b),
  .cin(cin),
  .clock(clock)
);



initial begin
    a = 8'b01111111;
     b = 8'b01111111;
    cin = 0;
    #5
```