Fuad Ismail

+62-838-9937-3595 | fuad1502@gmail.com | github.com/fuad1502

Summary

I am an ex-R&D Hardware Engineer from Keysight Technologies Malaysia with over 4 years of experience in the hardware industry (RF, electronics, embedded, and communication systems). Despite that, I am also acquinted with software development, as my work frequently require me to develop softwares, such as embedded software, mathematical simulation, and computational libraries.

I took a career break since August 2023 due to personal reasons. I am currently self studying Computer Science to break into the industry. See github.com/fuad1502/self-study-cs to know what I've achieved throughout my 7-months career break.

I am mainly interested in Systems Software (OS, Database, Distributed and Embedded Systems) and Computing Hardware. My goal is to consistently contribute to the OSS ecosystem by contributing to public repositories and building my own OSS projects. Currently, I have contributed to Verilator, an open-source SystemVerilog simulator and lint system. (Pull request #5006, #4966)

I am a passionate learner committed to continuous learning and have a track record of showing initiative at the workplace and deeply care about my work.

Education

Bandung Institute of Technology Bandung, Indonesia
Electrical Engineering (BS), ABET Accredited, GPA 3.81/4.0 *2014 - 2018*

Technical Skills

Programming Languages: SystemVerilog/Verilog, C, C++, MATLAB, Rust, Go, Java, JavaScript, Python, SQL
Softwares: Vivado, Quartus/ModelSim, Verilator, KiCad, Mentor Graphics Xpedition
Hardwares: Xilinx Zynq APSoC, STMicroelectronics STM32
Developer Tools: Git, Docker/Podman, CMake, Make

Projects

RVSV November 2023 – Present
github.com/fuad1502/rvsv

RVSV is a SystemVerilog implementation of a 5-stage pipelined RISC-V CPU. Verification code is written in C++ using Verilator and Rubbler.

Rubbler November 2023 – Present
github.com/fuad1502/rubbler

Rubbler is a RISC-V assembler written in Rust. This library was written with the main purpose of embedding a simple RISC-V assembler inside of a RISC-V CPU test bench code written with Verilator.

NAALG: Network Analyzer Algorithms C++ Library
Associated with Keysight Technologies

I initiated the development of NAALG due two things. First, I was tasked with developing a novel Time Domain Reflectometry (TDR) calculation from Vector Network Analyzer (VNA) measurements. Second, on a different project, I had just implemented a new calibration algorithm for an embedded VNA. Since both of this project involves calculation on VNA measurements, I realize that it would be nice to have a library that provides all of these VNA algorithms in one place. NAALG is similar to scikit-rf, but uses high performant implementation in C++ to enable usage in embedded real-time measurement applications.

Custom Telecommunication Device (GMSK + TDM Transceiver)
Associated with Hariff Daya Tunggal Engineering

My team was tasked with developing a fully custom telecommunication device. My role was in evaluating system level design tradeoffs using MATLAB and developing the physical (PHY) and medium access control (MAC) layer on an *All Programmable SoC (APSoC)*. The PHY layer consists of, but not limited to, baseband modulator, channel impulse response estimator, and Viterbi equalizer. The PHY layer is written in Verilog, while the MAC layer is written in C. Communication between the two layers uses Direct Memory Access (DMA).

Automatic Identification System Search and Rescue Transponder
Associated with Labs247

Automatic Identification System (AIS) Search and Rescue Transponder (SART) is a radio device used to locate distressed vessels. My role was in developing all of the electronic and embedded software aspect of the device, and production. We use FreeRTOS Real-Time Operating System to enable low power usage and multiple tasks management. Up till now the device is still in production.

Physical, Data Link, and Network Layer Implementation for Visible Light Communication
Associated with Institut Teknologi Bandung

Visible Light Communication (VLC), or sometimes referred as LiFi, is a communication system that aims to use regular LEDs used in for lighting as an internet access point. An IEEE standard has been released to accommodate the standardization of this emerging technology, namely IEEE 802.15.7. In this project we have made a fully functional VLC access point for a single user that has a data rate of around 500 kbps, enabling streaming YouTube videos in 144p. My workload was to create the baseband signal processing on an All Programmable SoC, which meant the design utilizes both an FPGA and a processor. The network and data link layer are implemented with a program written in C. The physical layer was designed based on the IEEE 802.15.7 standard, which includes VPPM encoding, CRC append and check, and Reed-Solomon FEC. The physical layer ran on the FPGA substrate and was written in Verilog. I also integrated a Xillybus IP core for the interconnection between the FPGA and the processor.

Experience

R&D Hardware Engineer January 2022 – August 2023
Keysight Technologies *Penang, Malaysia*

- Initiated the development of NAALG (*see above*), a network analyzer algorithms C++ library.
- Significantly improve the measurement accuracy of an embedded VNA product by introducing and implementing a better calibration algorithm.
- Successfully extend the measurement bandwidth of an embedded VNA product by suggesting improvements to the RF layout.
- Fixed an RF technical issue in an embedded VNA product and wrote a technical paper on it.
- Demonstrated iniatiative by voluntarily improving an internal software tool used by our team.
- Demonstrated initiative by introducing a better software development workflow.
- Collaborate in a team from various time zones (USA, Europe, and Malaysia).

Software Engineer February 2021 - October 2021
Lumina Industries *Jakarta, Indonesia*

- Wrote the Windows middleware for a Virtual Camera software using Win32 API.
- Developed image processing features using C++ with OpenCV.
- Worked remotely with a medium-sized team from various nationalities (USA, Taiwan, and Indonesia).

R&D Radio Frequency Engineer August 2020 – February 2021
Hariff Daya Tunggal Engineering *Bandung, Indonesia*

- Wrote MATLAB simulations to evaluate system-level design tradeoffs for the development of a fully custom telecommunication device (*see above*).
- Implemented the PHY and MAC layer of a fully custom telecommunication device on an APSoC using Verilog and C.
- Designed a schematic for a fully custom telecommunication device.

R&D Electronic Design Engineer August 2018 – August 2020
Labs247 *Jakarta, Indonesia*

- Lead the development of telecommunication product (Automatic Identification System Search and Rescue Transponder, *see above*) which is still in production up till now.
- Involved in the development of medical product (CPAP BiPAP machine).
- Demonstrated initiative by suggesting cost-saving solutions that avoids vendor lock in and introduced an efficient production workflow.