

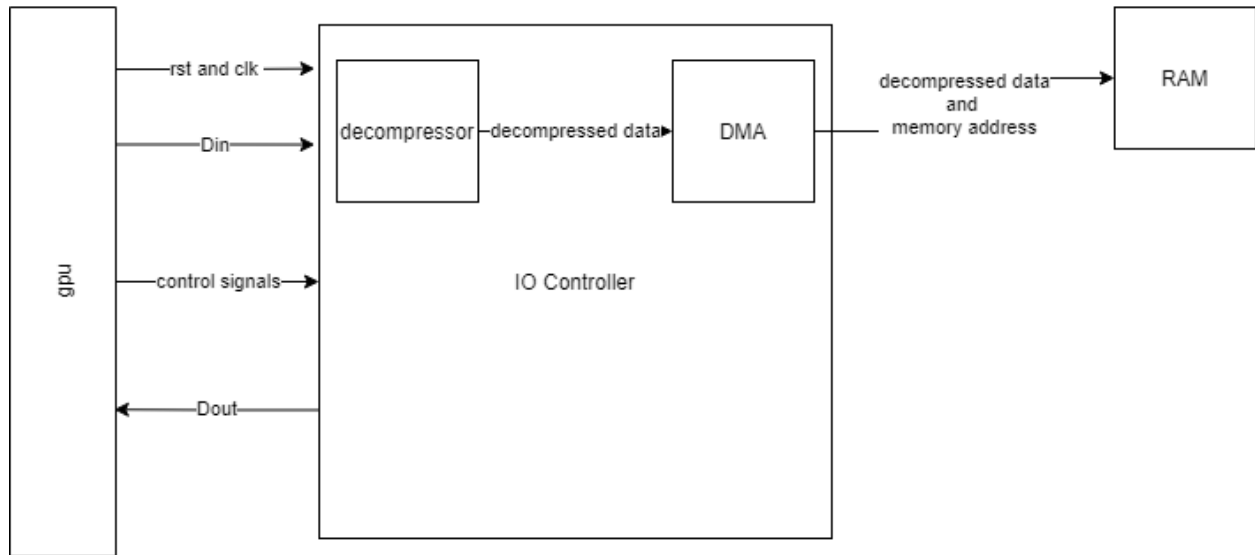
VLSI project  
IO subteam

# Participants

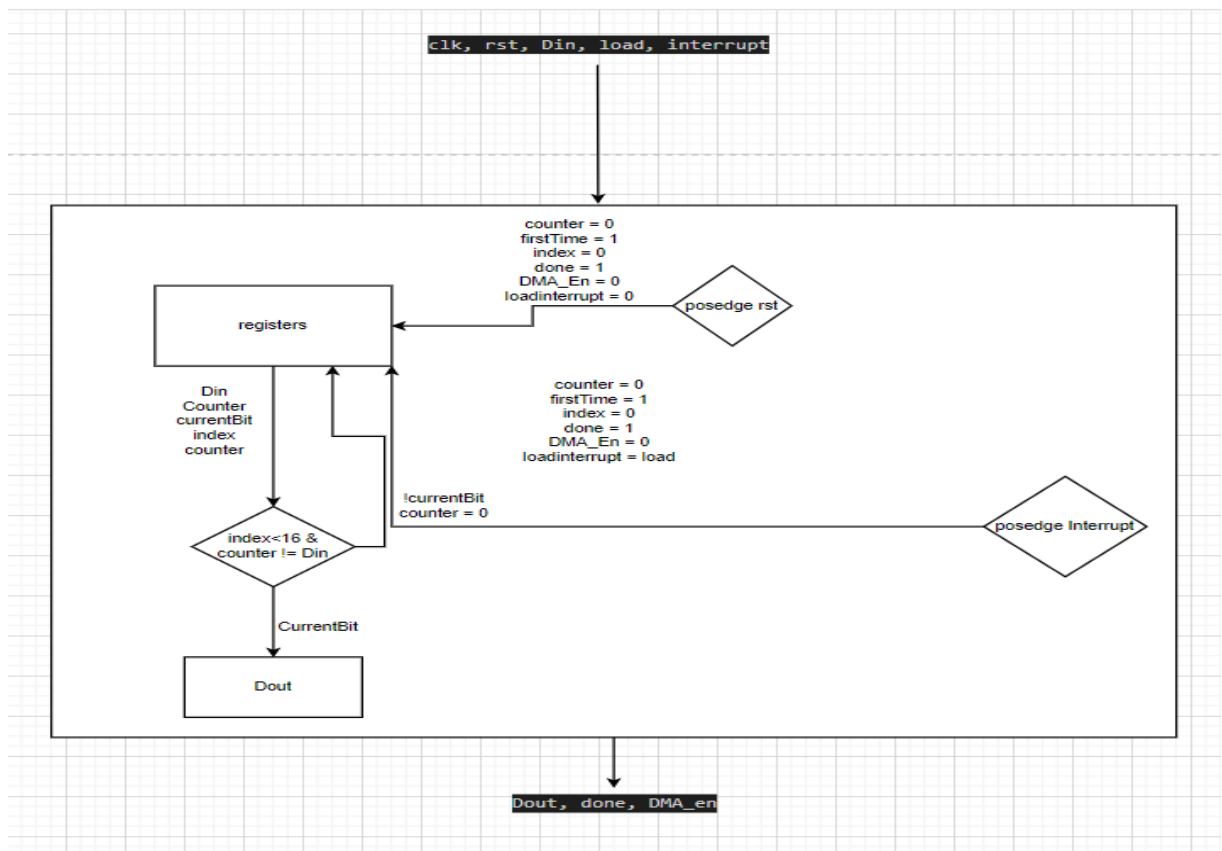
1. Ahmed Walid Fathy , section 1 , bench number 10
2. Abdelrahman Tarek , section 1 ,bench number 35
3. Ali Abdelhaleem , section 2, bench number 5

# Unit architecture

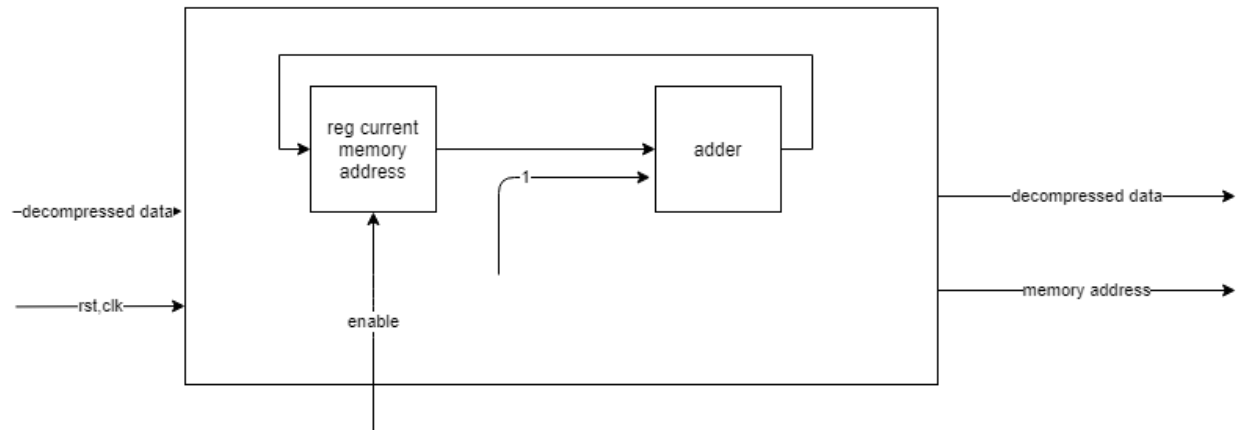
## Whole IO unit



## decompressor



## DMA



## Assumptions

- 1- Compressed file is in the form of block 16 bits width
- 2- The compressed file is compressed with RLE algorithm