Technische Universität München
Lehrstuhl für Rechnertechnik und Rechnerorganisation

Carsten Trinitis

Course IN2075: Microprocessors

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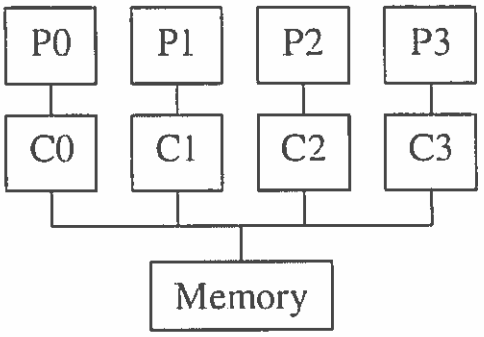
Exercise 3: Cache Coherency

In these exercises, we will be covering cache coherency, specifically the MESI protocol.

On the right, a system with four processors and shared memory is illustrated.
Each processor P0, P1, P2 and P3 has a local cache C0, C1, C2 and C3, respectively.



Exercise 3.1: Memory Overhead

Given a cache line size of 64 bytes and a cache size of 30MB per processor, how much additional memory is needed to support the MESI protocol?

$\frac{30\,MB}{64B} = 491.520\ lines \Rightarrow 491.520 \cdot 2\ bits = 122.880\ Bytes = 120\,kB$

Exercise 3.2: Valid State Combinations

Sketch all valid state combinations for a single cache line in two caches, i.e. if it is e.g. marked as modified (M) in one cache, which states are valid in the other cache?

- M: I
- E: I
- S: S, I
- I: M, E, S

Exercise 3.3: Sequence of Operations and States

The table below successively lists operations by different processors on a single data item. Initially, the corresponding cache line is marked invalid (I) at each cache.
Complete the table by filling in the respective states at the individual processor caches, explain why the operation resulted in the respective change and what signals are set due to snooping.

Step	Operation (Processor)	C0	C1	C2	C3	Comments
0		I	I	I	I	
1	Read (P0)	E	I	I	I	P0: BusRd
2	write (P0)	M	I	I	I	—
3	read (P1)	S	S	I	I	P1: BusRd P0: Flush
4	write (P2)	I	I	M	I	P2: BusRdX
5	read (P2)	I	I	M	I	—
6	Read (P3)	I	I	S	S	P3: BusRd P2: Flush
7	write (P0)	M	I	I	I	P0: BusRdX
8	write (P1)	I	M	I	I	P1: BusRdX
9	read (P0)	S	S	I	I	P0: BusRd P1: Flush