# Cpppc Project: Microfluidic-Large-Scale-Integration (mLSI) Simulator

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## 1 Introduction

Microfluidic Large-Scale Integration (mLSI) is a promising platform for biological/biochemical applications. An mLSI chip has a multi-layered structure consisting of micro-channels and micro-mechanical valves. The flow layer is responsible for fluid transportation and operation execution, and the control layer is responsible for valve actuation that manipulates the direction of the fluid-flow. Figure 1 shows a photo of an mLSI chip where control channels are filled with green food dye and flow channels are filled with red food dye.

MLSI is a developing research filed. Currently there is no simulation tool that can predicts the flow status on an mLSI chip. Different from existing microfluidic simulators, the main objective of which is to accurately predict the movement of small fluid particles, mLSI simulation should focus on the correlating valves and channels. More specifically, it should predict the channel status, i.e. whether a channel is blocked, vacant, or filled with fluids at a specific time point. In other world, mLSI simulation predicts the fluid behavior on a system-level.

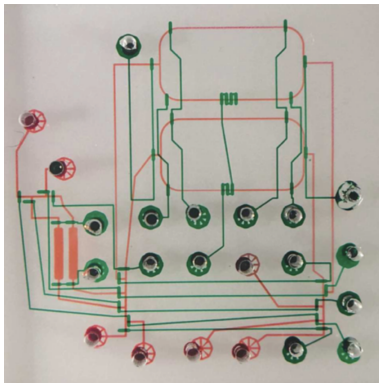
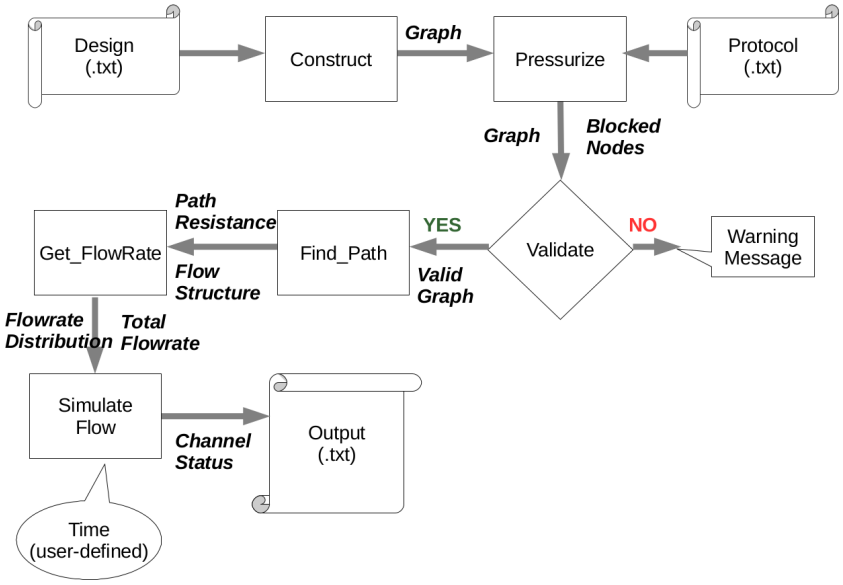


Figure 1: An mLSI chip for kinase activity applications.

Figure 2: System diagram of the Project




# 2 Overview of the Project

This project aims to develop a prototype of mLSI simulator. Formally:

### Input

- A description of the physical structure of an mLSI chip (.txt file);
- A description of the application protocols (txt.file);
- A specific time point (a floating point number).

### Output

- The channel status, i.e. whether it is blocked, vacant or filled with fluids, at a specific time point (txt.file).

Figure 2 shows the system diagram of the simulator. The simulator first takes a description of the chip *design* as its input, and *constructs* a **graph** structure consisting of nodes and edges. Each node may represent an inlet, an outlet, a valve, or a channel branching point of the mLSI chip, and each edge represents a channel segment that connects two nodes. After that, the simulator reads a description of application *protocols*, based on which some of the control channels will be *pressurize*d, and thus some nodes will be blocked. The **graph** and the **blocked nodes** are then fed to the next process that *validate*s whether

there is any feasible flow paths on the chip. If there is no feasible flow path, the simulator will output a *warning message* and terminate. If there is one or more feasible flow paths, the simulator will generate a **valid graph** where blocked nodes and channels are removed.