LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

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Parallel Computing

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Session 2: Pipelining

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Recap

Which pipelining stages do you remember from the lecture?

Recap

Explain the following pipelining stages:

IF	Instruction Fetch
ID	Instruction Decode
EX	Execute, Addr. Calc
MEM	Memory Access
WB	Write Back

Explain the term “Instruction Latency”

Explain the term “Instruction Latency”

Instr. No.	Pipeline Stage						
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

Discuss hidden parallelism in this snippet:

```
var1:   .word  23
lw      $t0 var1        # lw:  load maddr (reg_dest, addr)
                        #      copy content of RAM location into
                        #      register $t0
li      $t1 5           # li:  load value (reg_dest, val)
                        #      $t1 = 5
add     $t2 $t1 $t0     # add: (reg_dest, reg_op, reg_op)
                        #      $t2 = $t1 + $t0
sw      $t2 var1        # sw:  store maddr (reg_dest, addr)
                        #      write content of register $t1 into
                        #      RAM location
```

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2.1. Pipelining I

Assuming pipeline stages have the following durations:

IF	= 20ns
ID	= 10ns
EX	= 20ns
MEM	= 35ns
WB	= 10ns

Q: *What is the processor's maximum clock frequency?*

Assuming pipeline stages have the following durations:

IF = 20ns
ID = 10ns
EX = 20ns
MEM = 35ns slowest
WB = 10ns

F_{max} = 1 / 35 ns
= 1 / (35 · 1.0^{e}-9 s)
= ~ 28 571 428 Hz
= **~ 28 MHz**

Assuming pipeline stages have the following durations:

IF	= 20ns
ID	= 10ns
EX	= 20ns
MEM	= 35ns
WB	= 10ns

Q: *How could we achieve a performance gain in the next processor generation?*

Assuming pipeline stages have the following durations:

IF	= 20ns
ID	= 10ns
EX	= 20ns
MEM	= 35ns
WB	= 10ns

- Reduce latency of pipeline stages (Q: which one?)
- Add pipeline stages (Q: prerequisites?)
- Branch prediction
- …

Assuming pipeline stages have the following durations:

IF	= 20 ns
ID	= 10 ns
EX	= 20 ns
MEM	= 35 ns
WB	= 10 ns

Q: 50 pipeline stages advertised it to yield 10x performance increase compared to 5 stages:

- How can this statement be argued?

- How can we counter this argument?

Assuming pipeline stages have the following durations:

IF	= 20 ns
ID	= 10 ns
EX	= 20 ns
MEM	= 35 ns
WB	= 10 ns

- Stage with highest latency is decisive limit.
- So this implies …?
- What about hazards?

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2.2. Pipelining II

Floating-Point Multiplication

Involves the following three major steps in FPU:

1. Multiplication of fractions
2. Addition of exponents
3. Normalization of the result

Since fractions and exponents are fixed-point numbers, steps 1 & 2 can be implemented using fixed-point arithmetic.

Normalization step can be implemented as given in the floating point addition.

Floating-Point Division

- Less frequent in programs compared to addition, subtraction, and multiplication
- Separate pipeline unit for division is seldom implemented in FPUs.

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2.3. ILP, DLP

Conceptual differences between

- Pipelining
- Vector processing
- Multi-threading

Which ones are ILP / DLP?

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