EE 577a Lab2

Spring 2017

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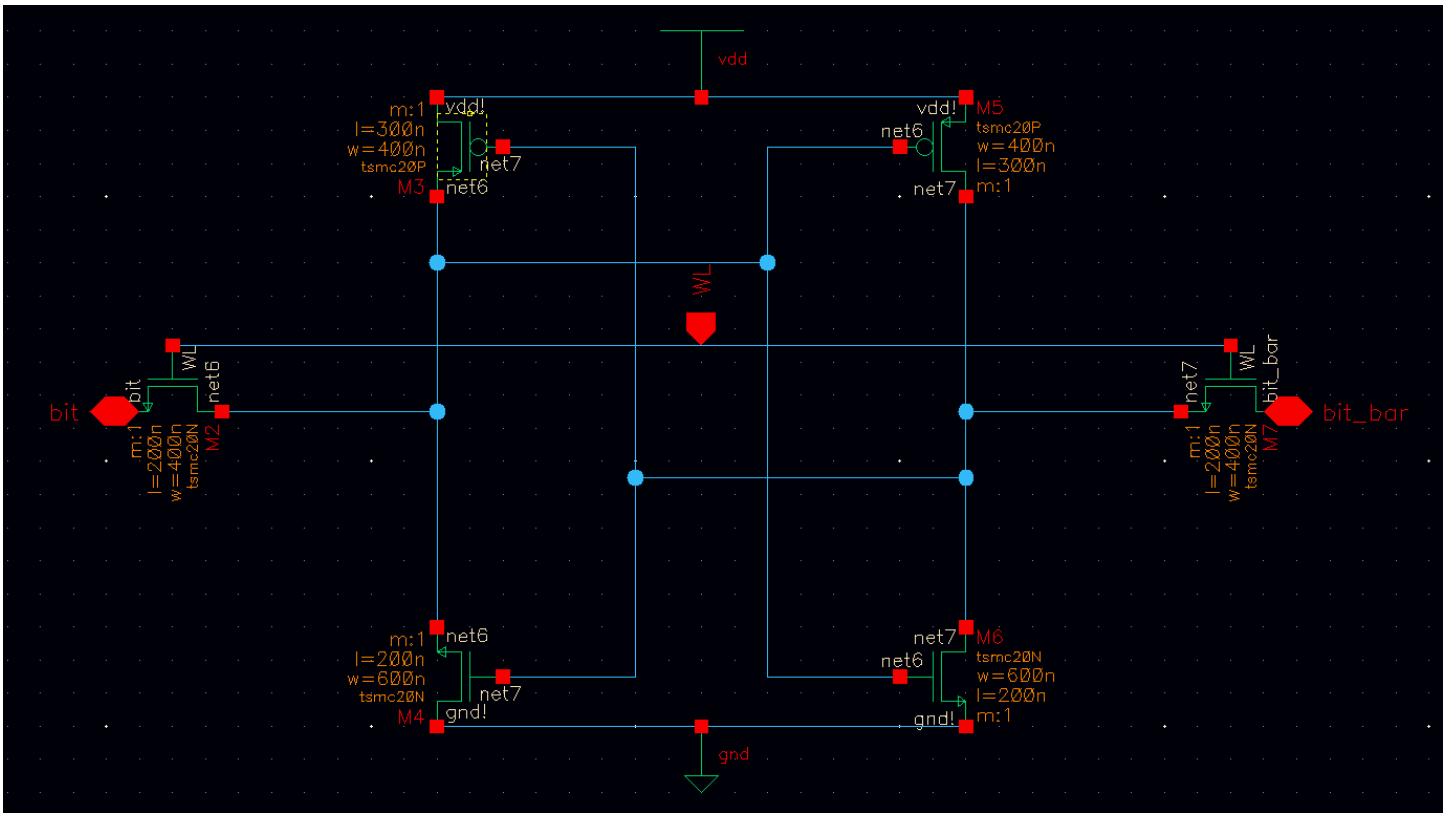
2/17/2017

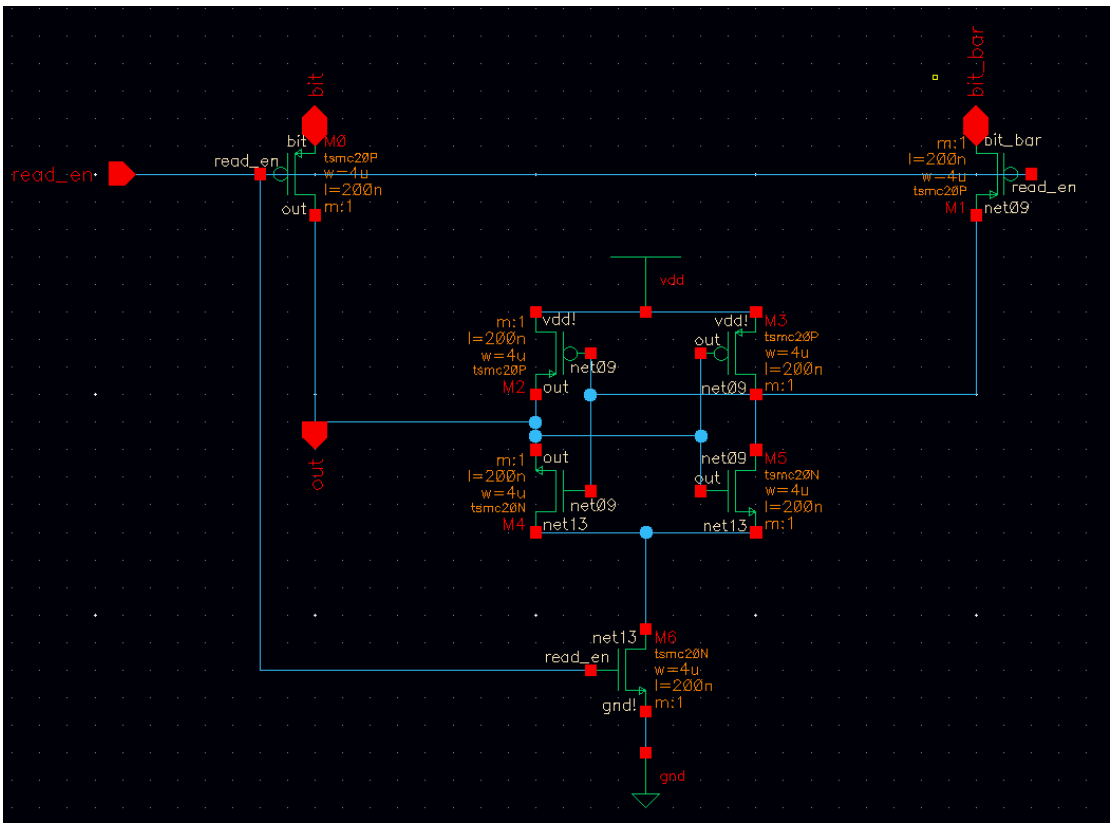
PartA:

A. Schematic of 512 bits SRAM

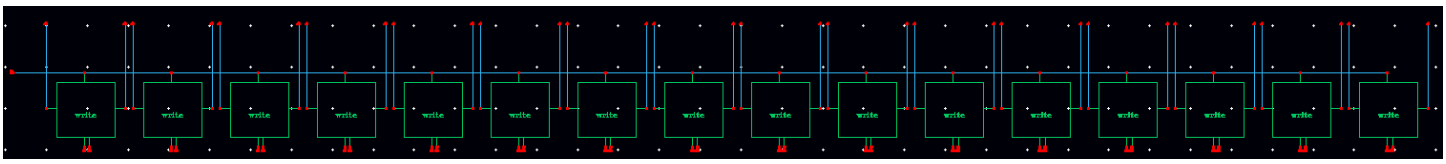
1. SRAM cell:



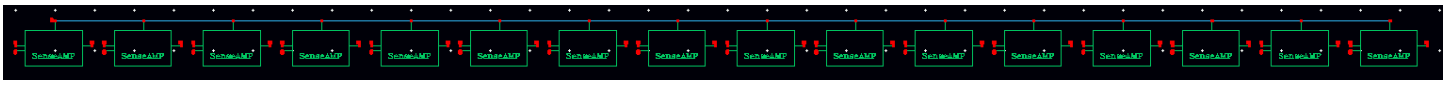
2. Sense Amplifier:



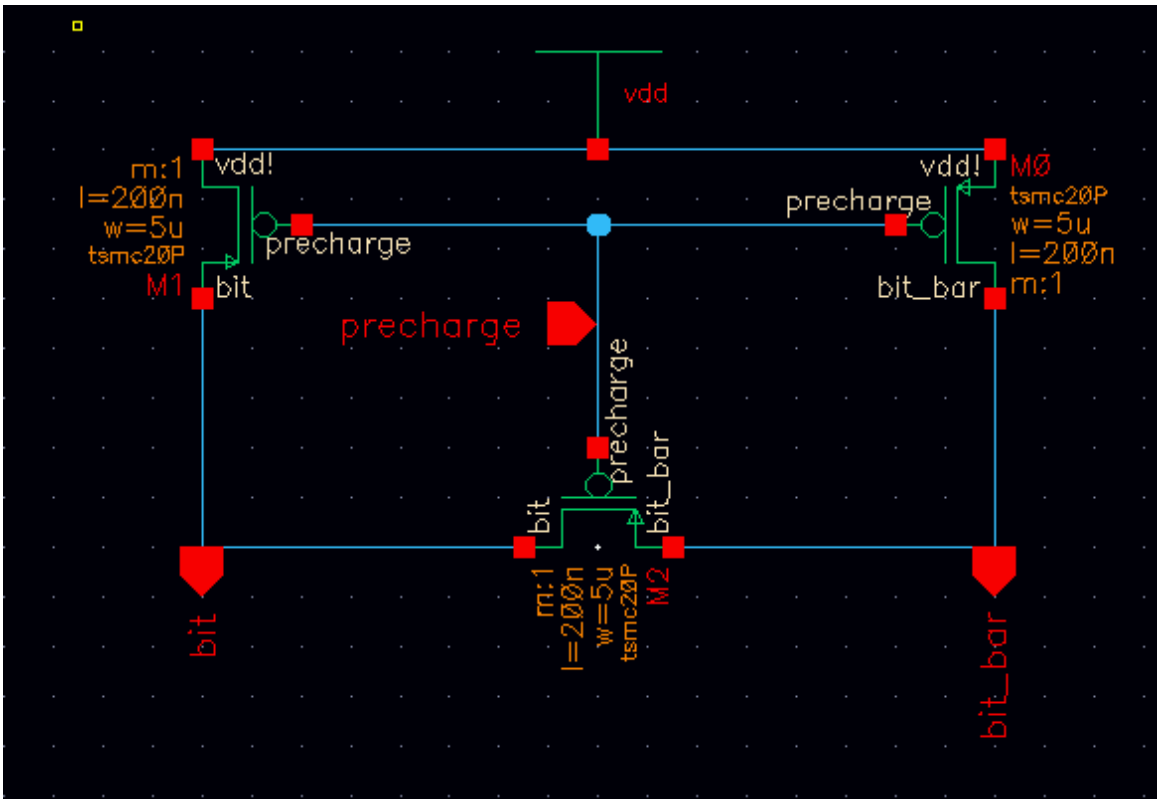
3. Write Circuit:



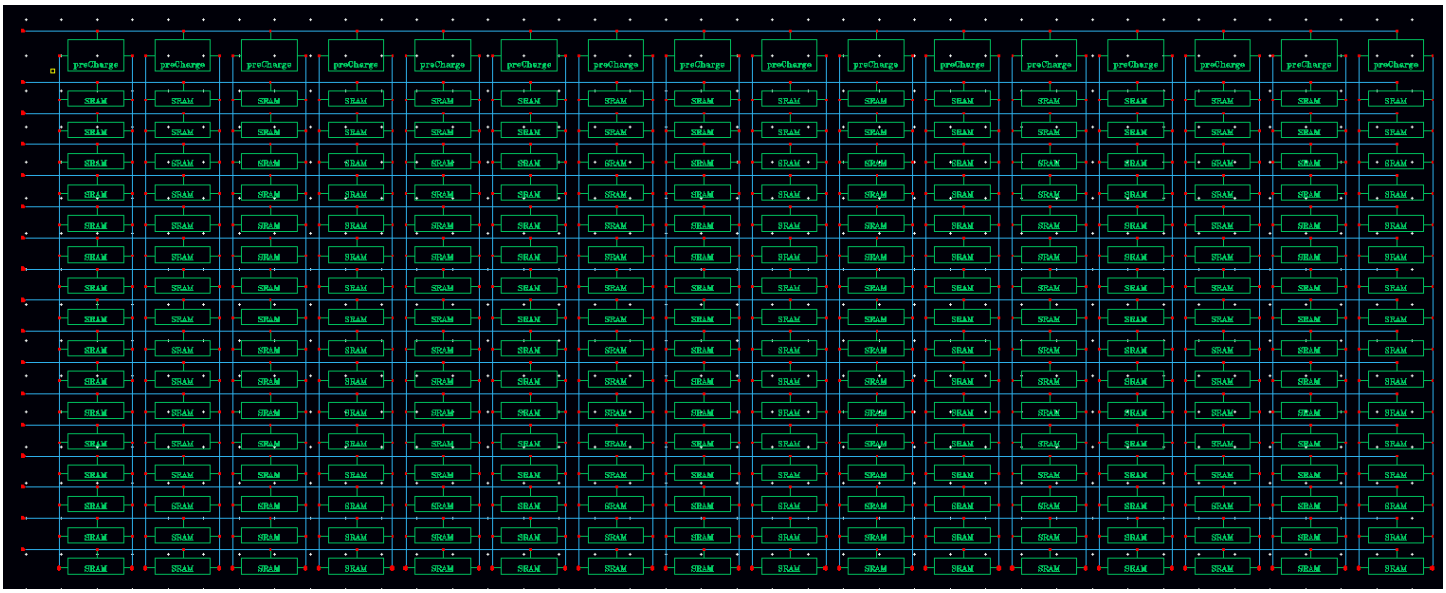
4. Read Circuit:



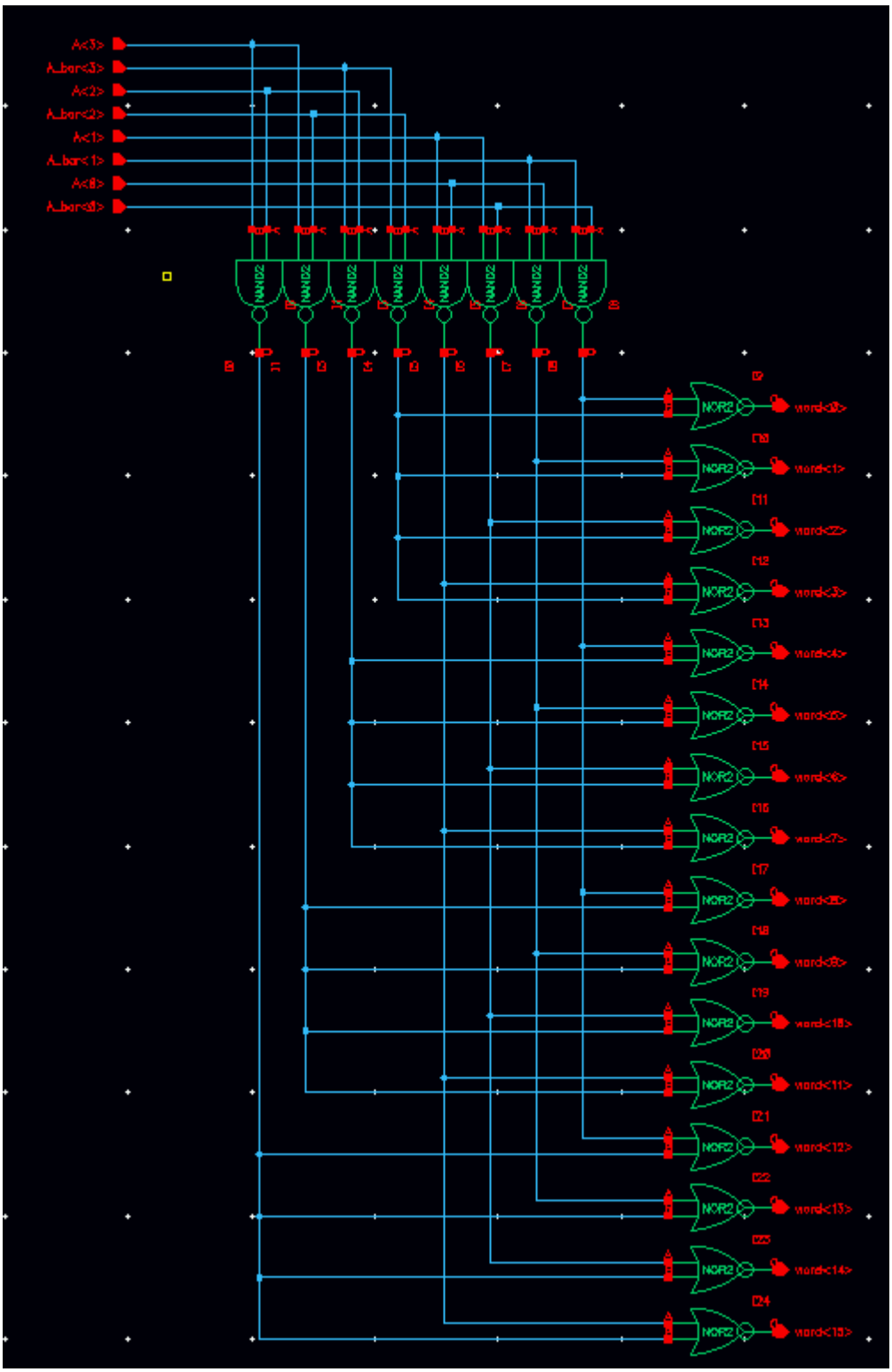
5. Pre-charge Circuit:



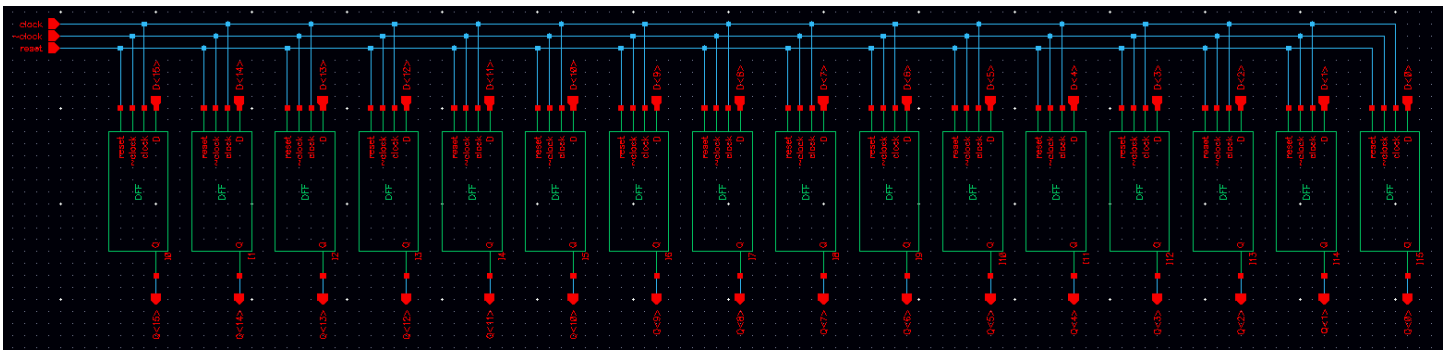
6. Bank schematic:



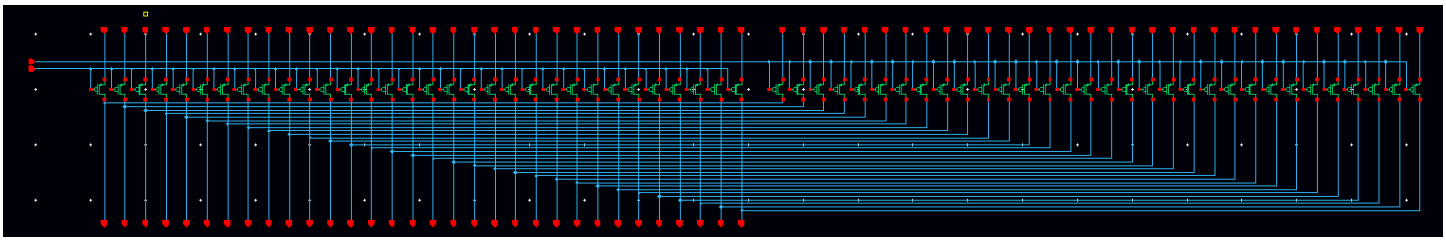
7. Decoder:


A<3>
A_bar<3>
A<2>
A_bar<2>
A<1>
A_bar<1>
A<0>
A_bar<0>
NOR2
word<0>
word<1>
word<2>
word<3>
word<4>
word<5>
word<6>
word<7>
word<8>
word<9>
word<10>
word<11>
word<12>
word<13>
word<14>
word<15>

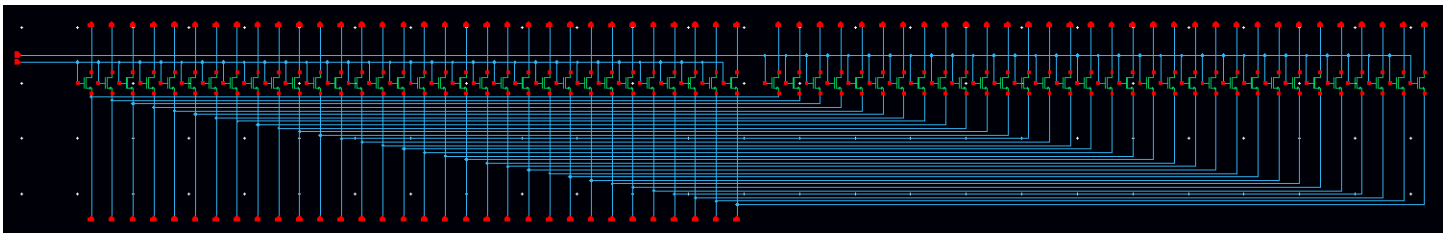
8. Output Register:



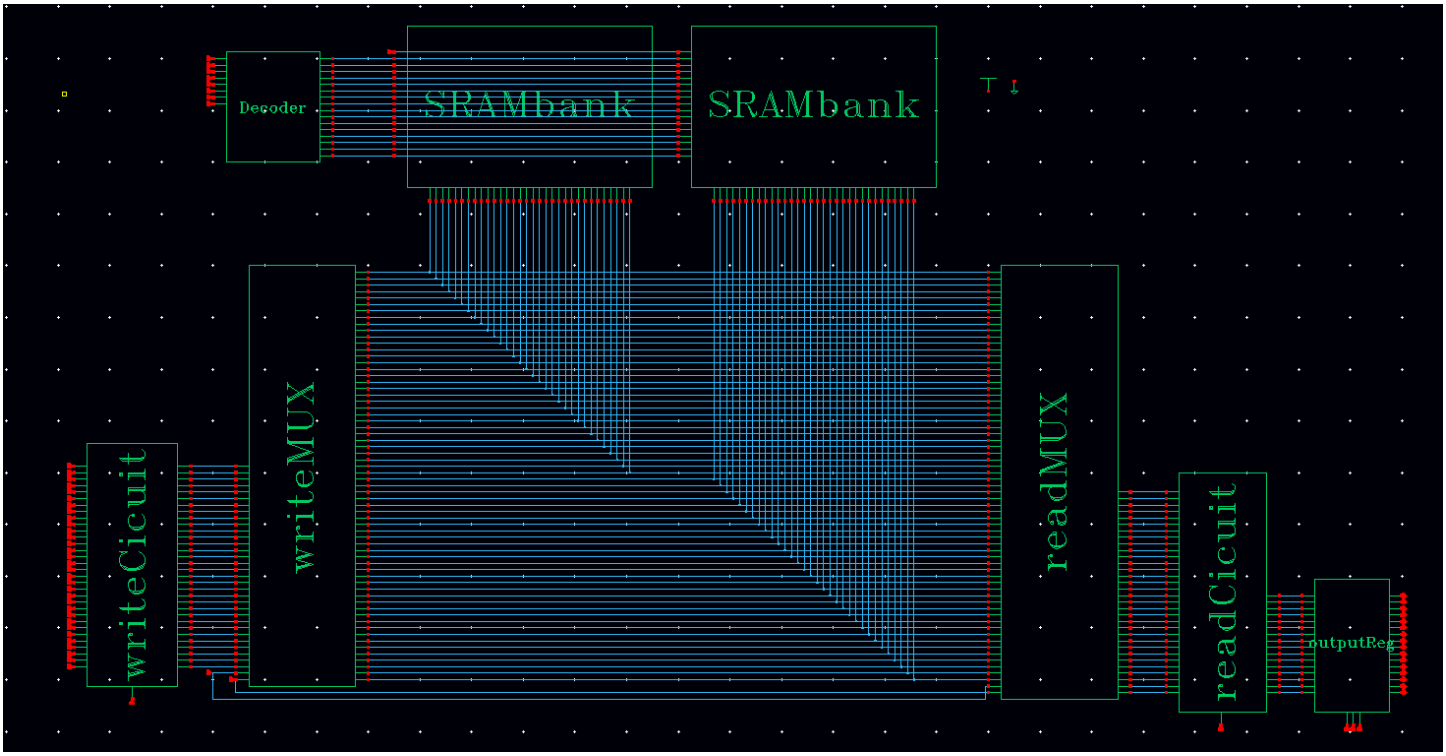
9. Read Mux:



10. Write Mux



11. Overall schematic:



B. Briefly explain your design

The design a 512-bit SRAM with two256-bit banks. And the design is based on the design2 which was discussed in discussion session.

In the bank design. There is 8 modules: Decoder, SRAMbank*2, readMUX, writeMUX, readCircuit, outputReg and writeCircuit.

readMUX contains 16 SenseAMP and writeMUX contains 16 write cell.

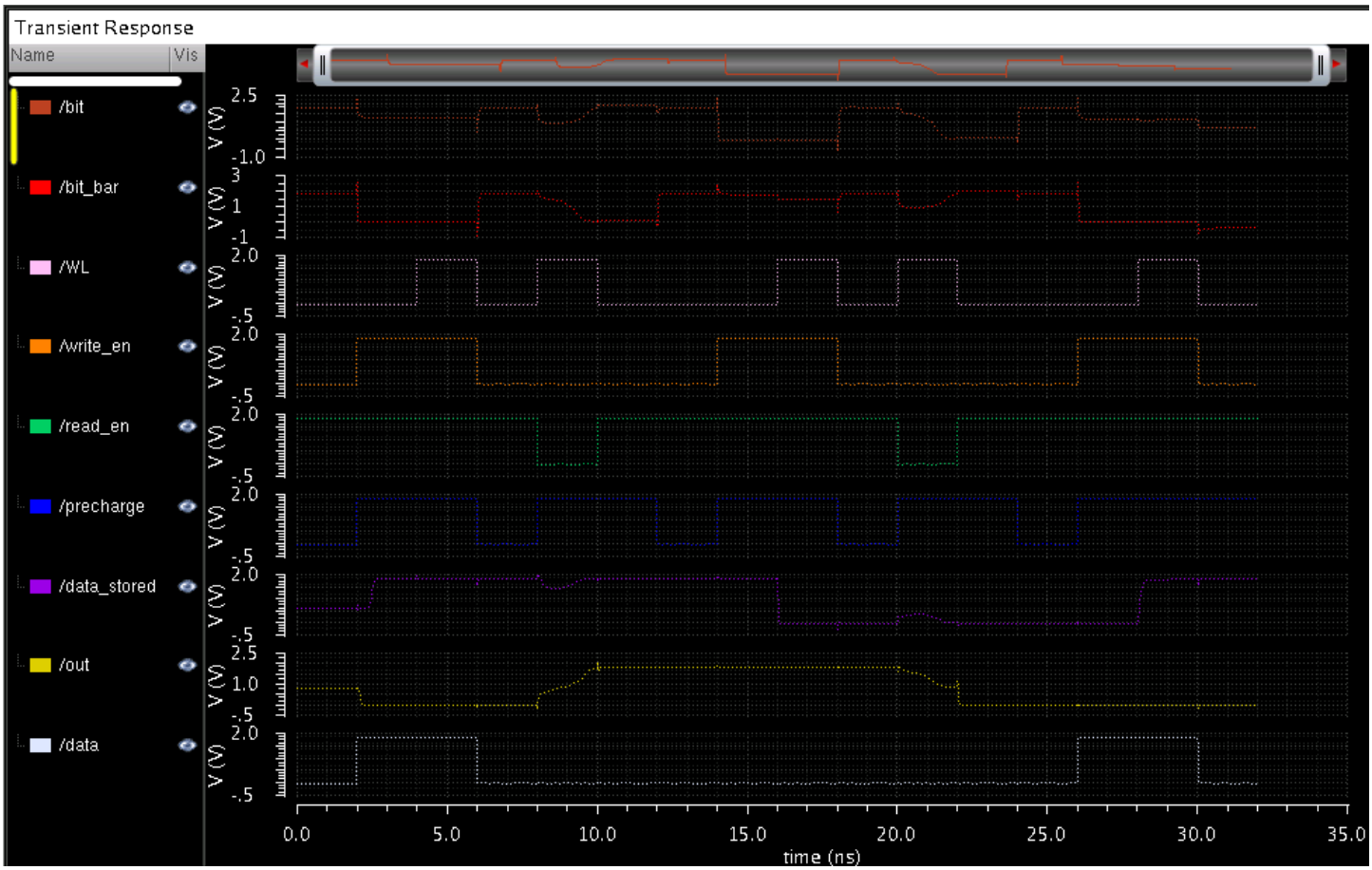
The readMUX is in between SRAMbank and readCircuit, which saves 16 SenseAMP.

The writeMUX is in between SRAMbank and writeCircuit, which saves 16 wirte cell.

Decoder decodes A[4:1] to the word line. And A[0] is connected to the readMUX and writeMUX to select bank.

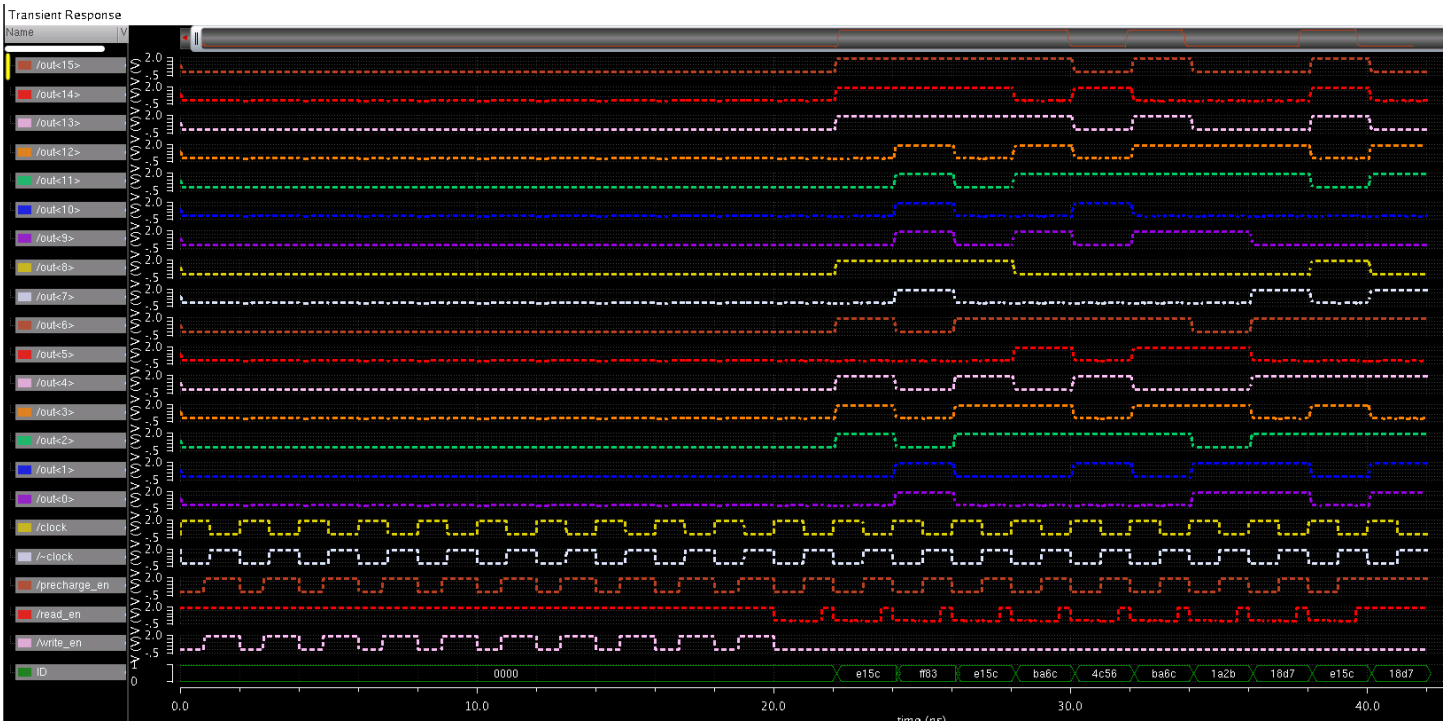
writeCircuit is connected to data[15:0] and output register is connected to out[15:0].

C. Show and explain the waveforms of the following operations to a single cell:



write 1 at 4 ns, read at 8ns and output stable at 1 at 10ns. Then write 0 at 16ns data stored changed to 0, at 20 ns read, output stable at 0 at 22ns. Write 1 at 28ns. Data stored change to 1.

D. Do the functional test for consecutive read and write operations and show the waveforms:



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E15c ff83 e15c ba6c 4c56 ba6c 1a2b 18d7 e15c 18d7

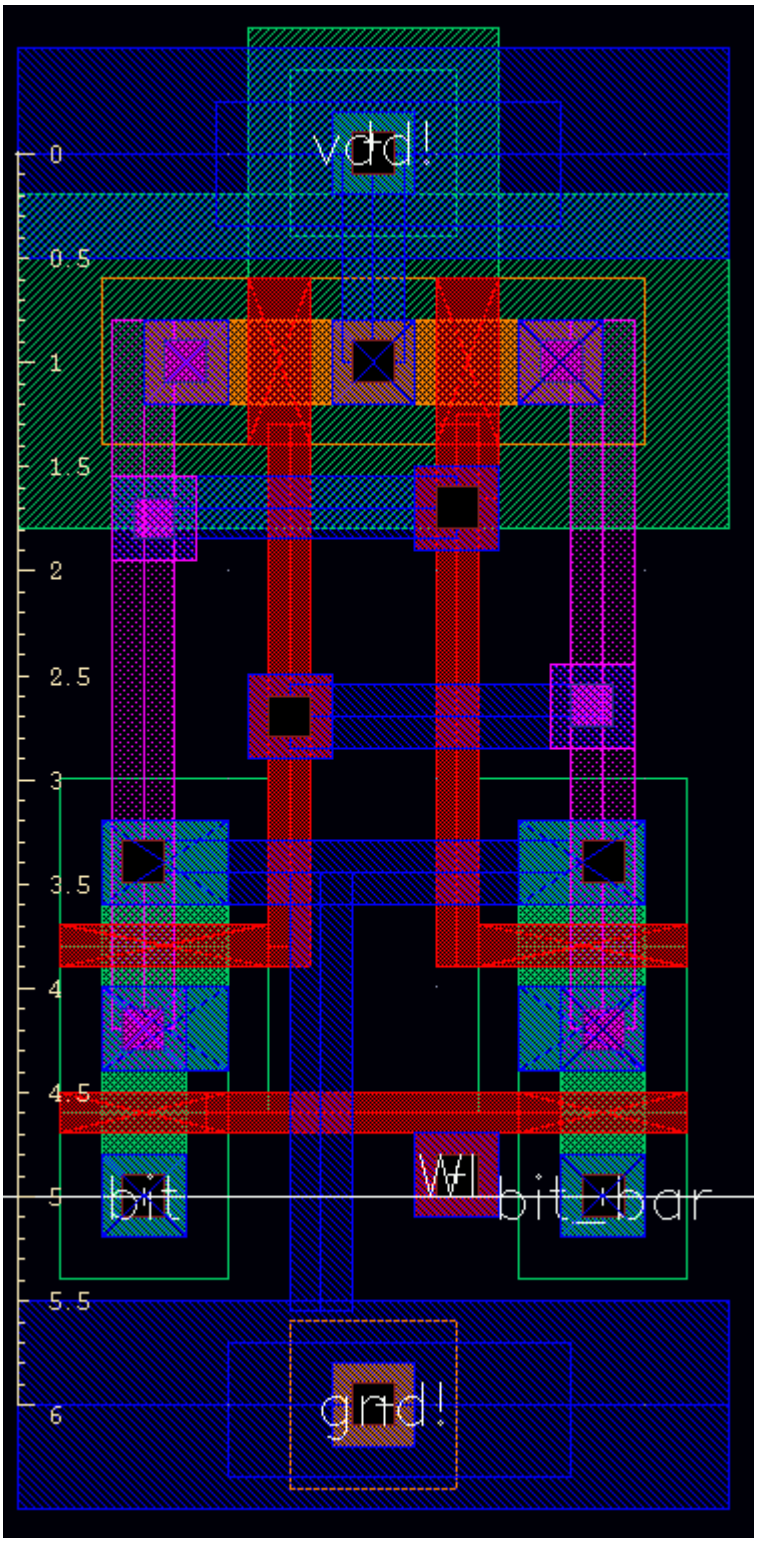
4 7 4 5 3\ 5 9 8 4 8

sequence 1 is overwritten by sequence 3 therefor my number1 turns to number3.

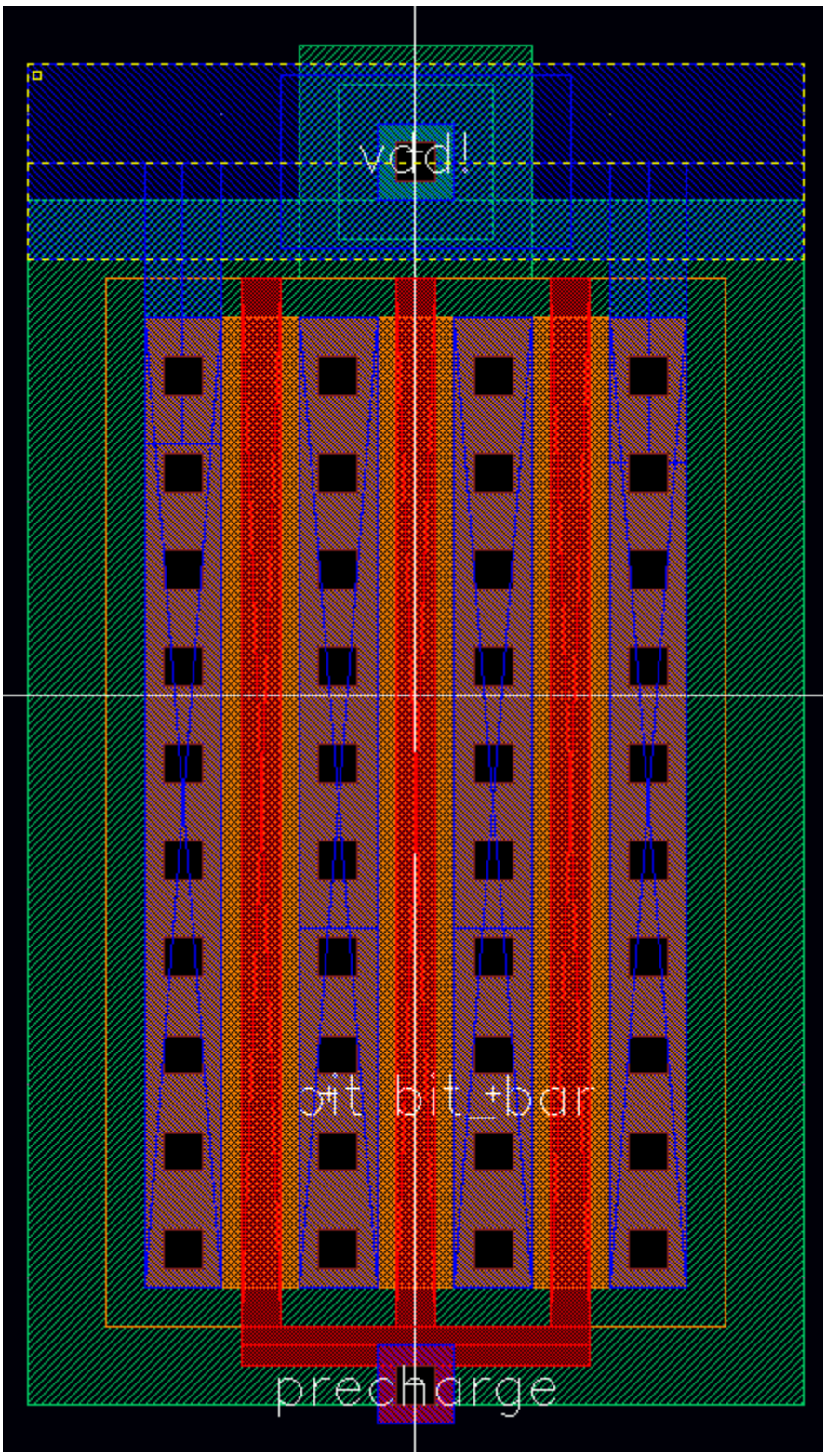
Part B:

A. Layout:

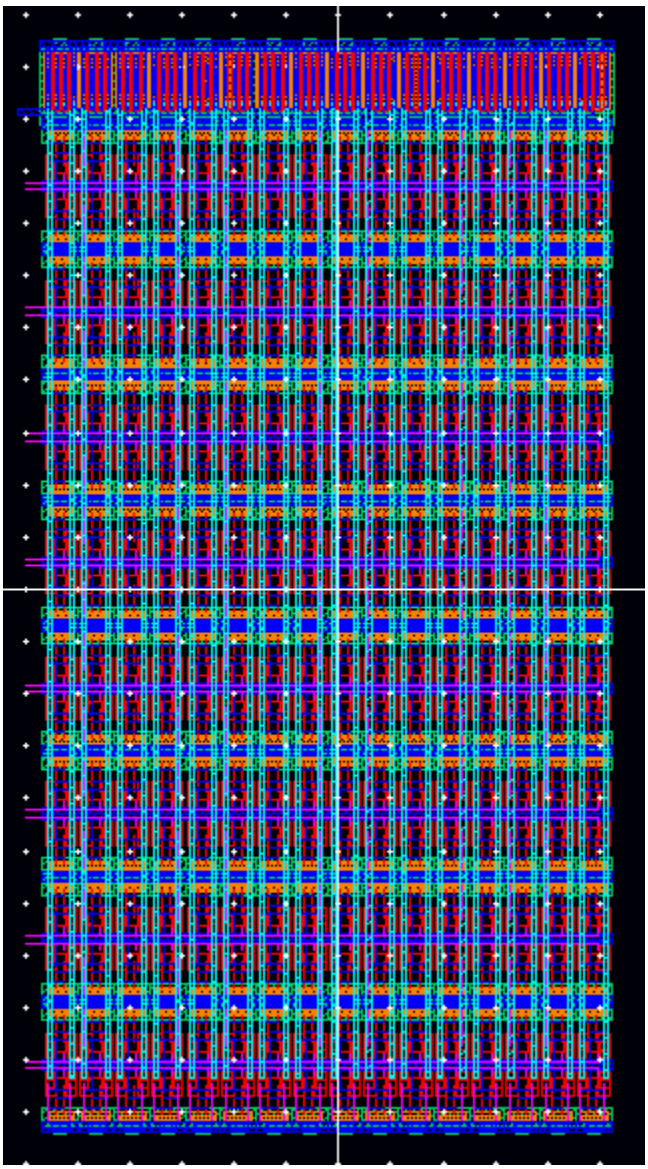
1. SRAM



2. PreCharge



3. SRAMbank



B. LVS

1. SRAM

2. preCharge