EE577
LAB1 Part2
Report

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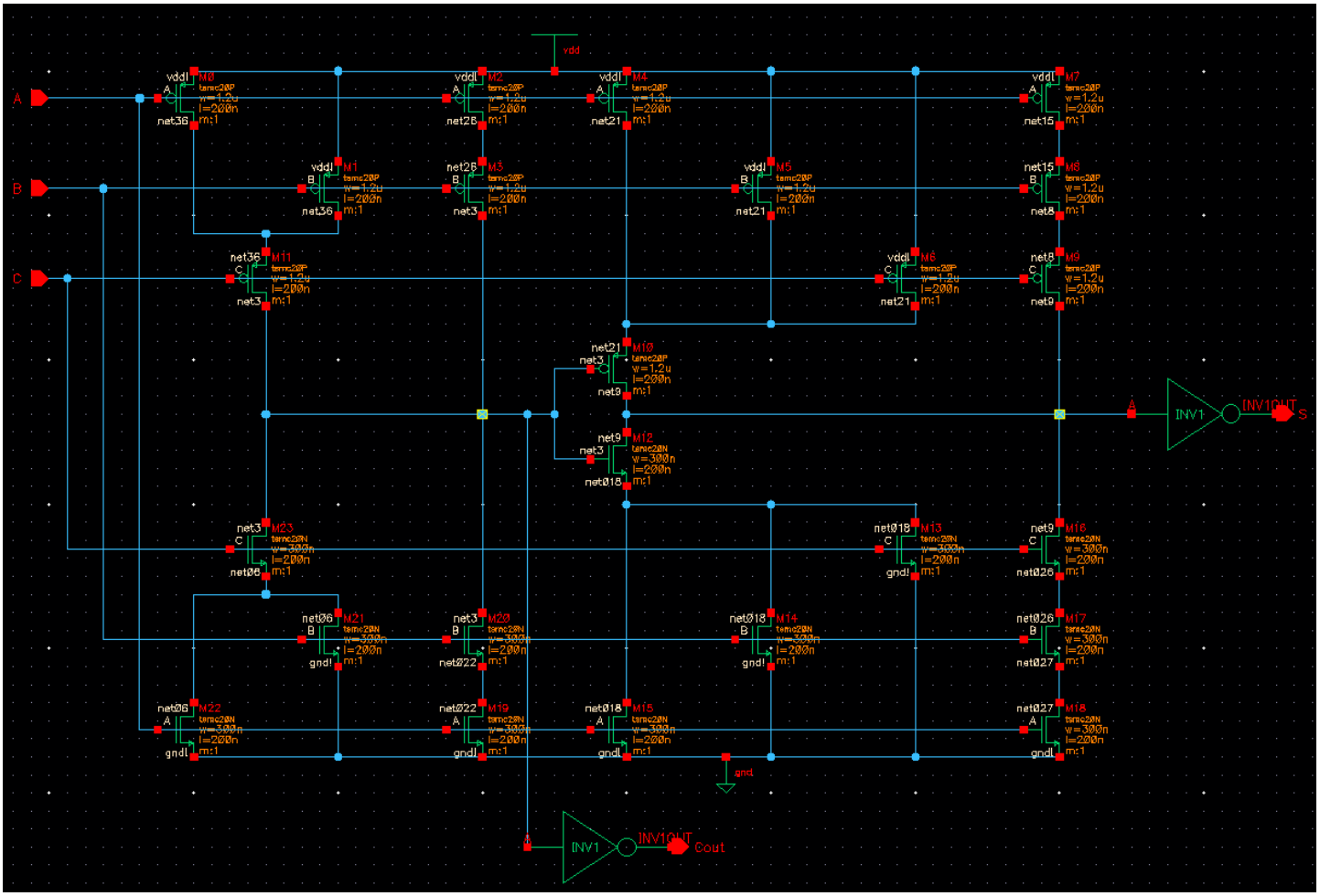
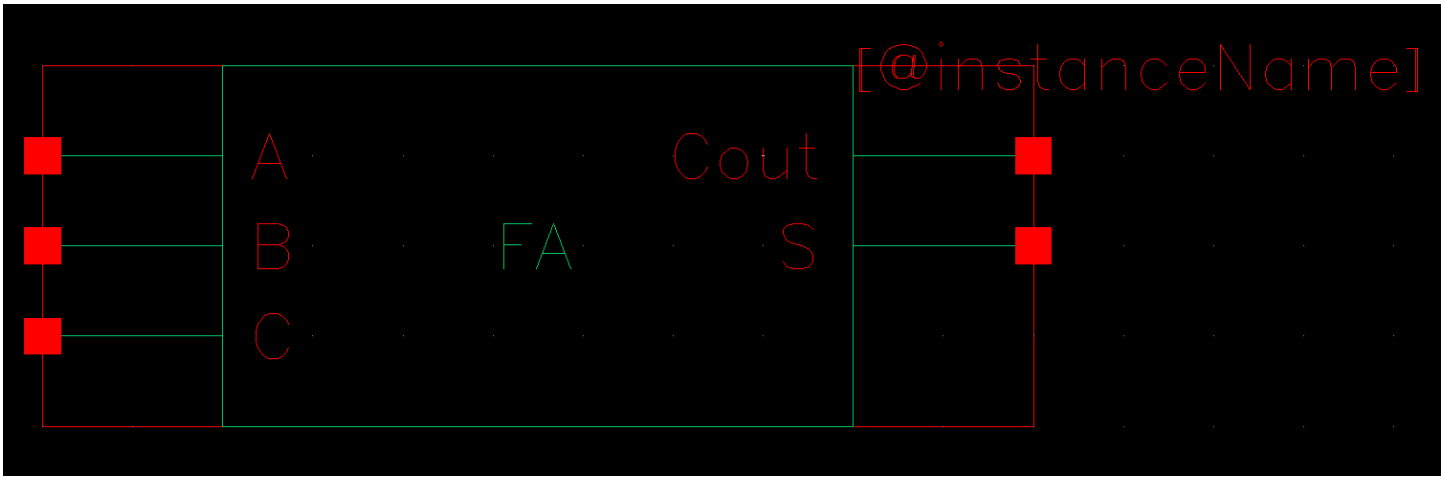
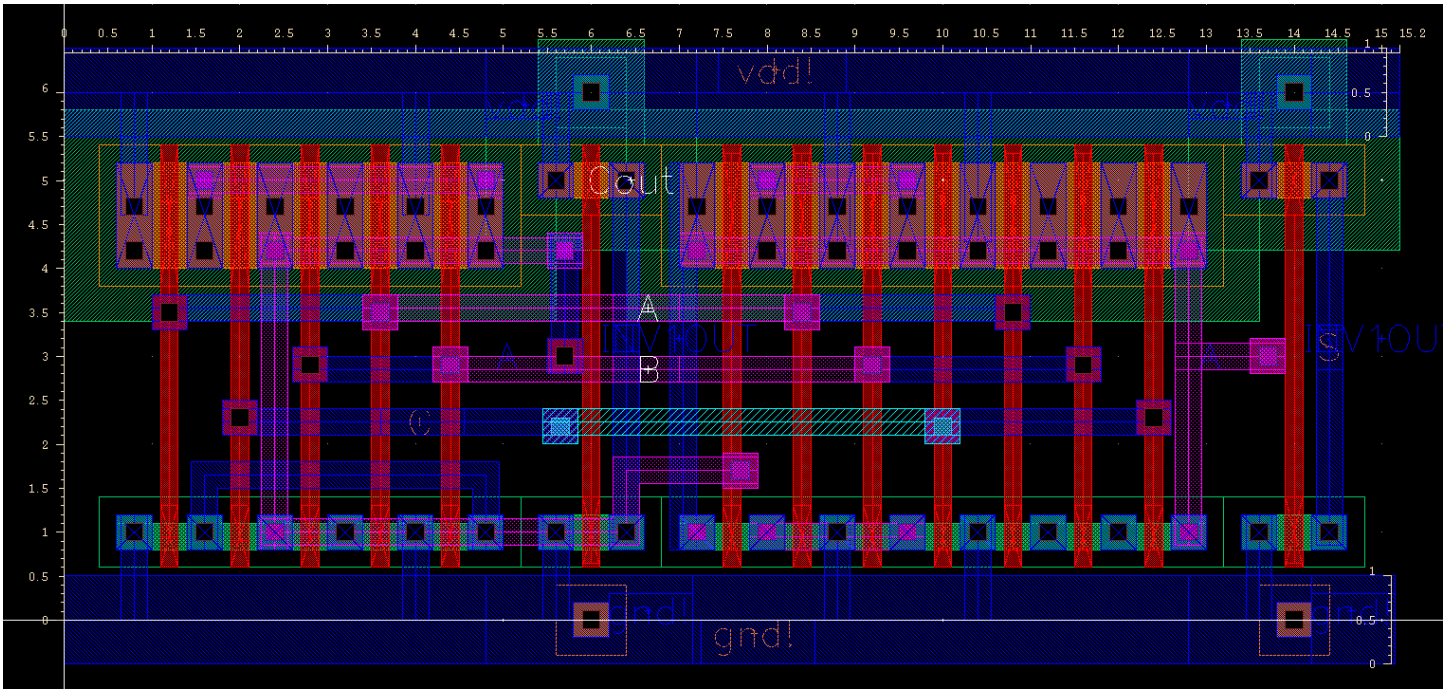
2/3/2017

1- bit Full Adder

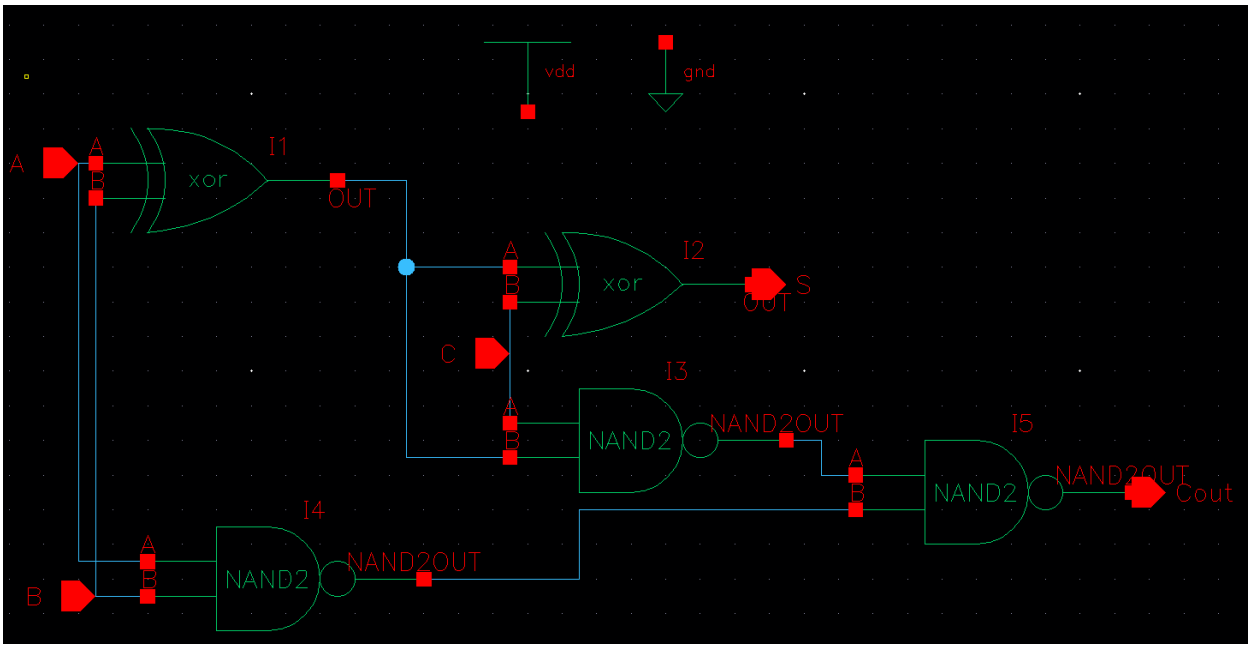
1. Schematic, symbol and layout.
   a. Standard full adder

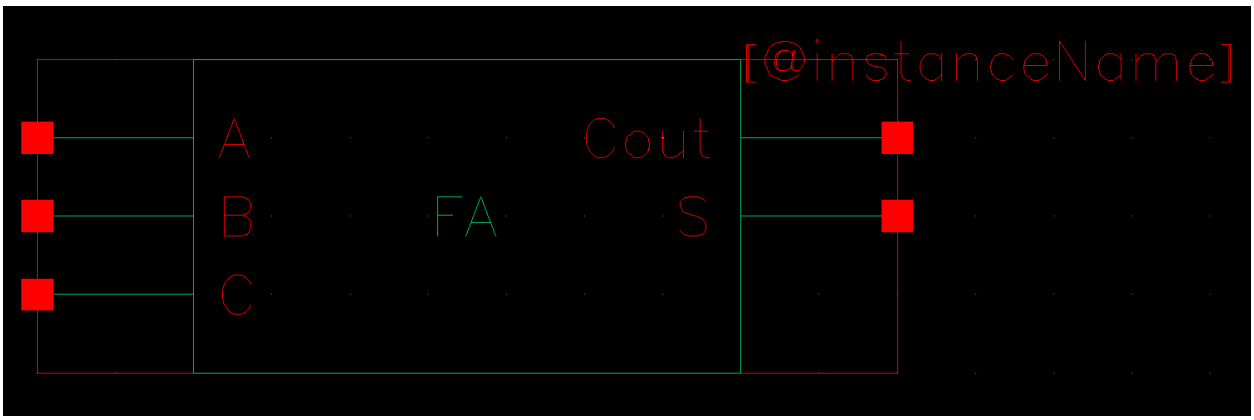


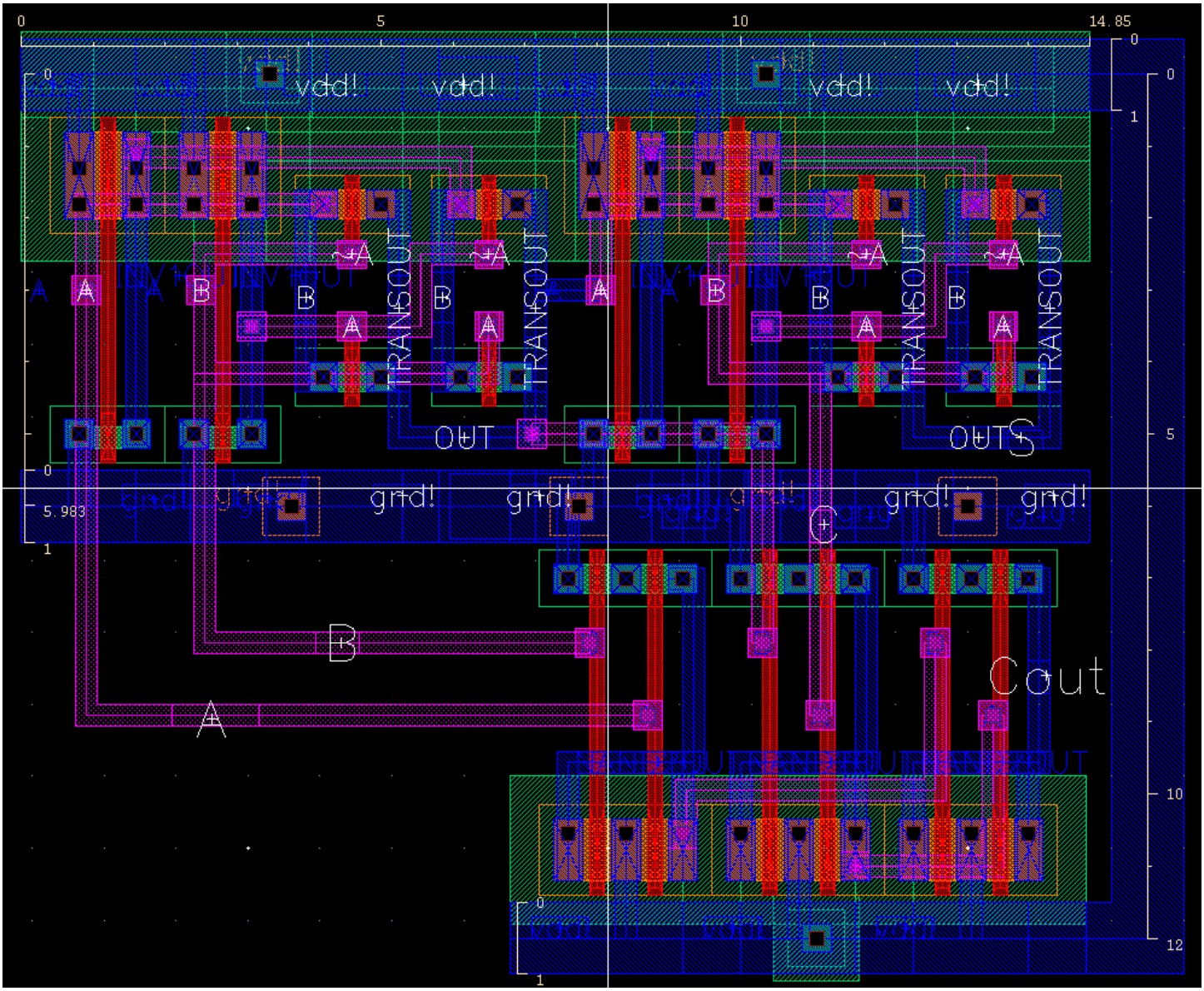




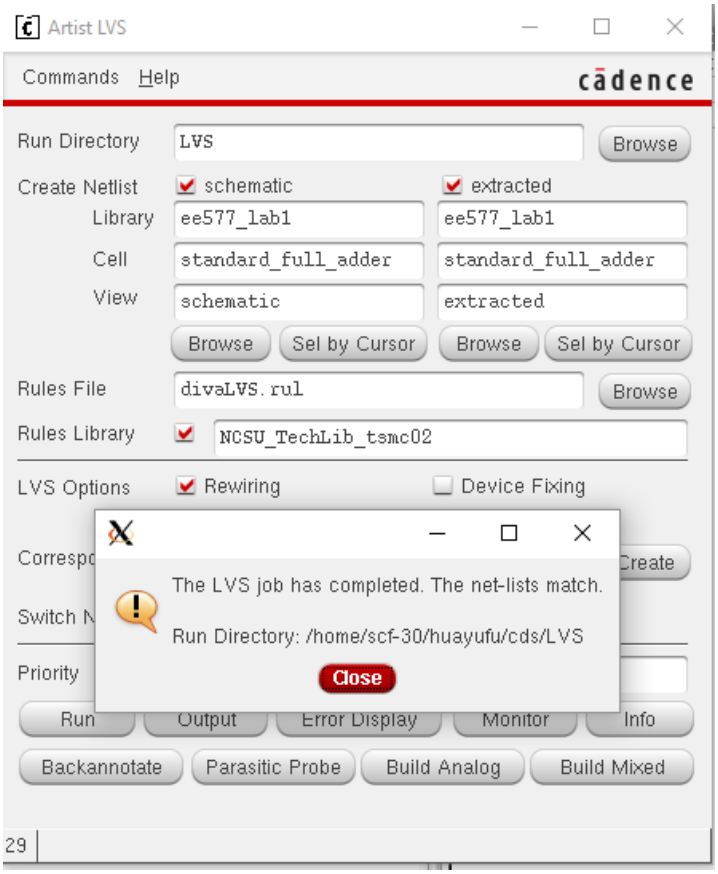
b. Gate level full adder



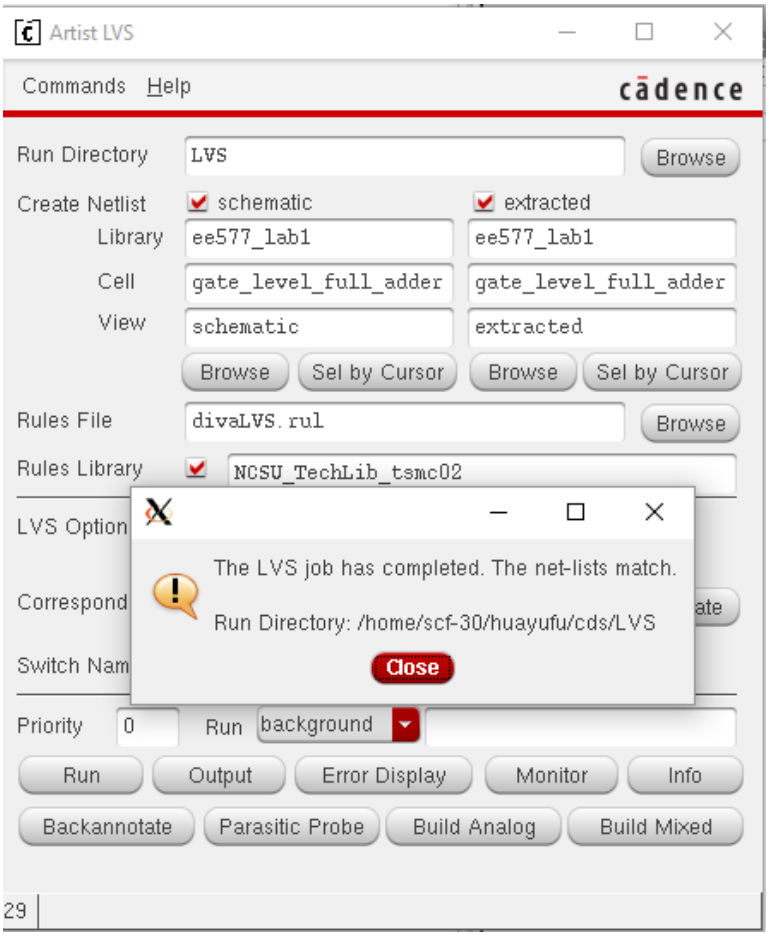




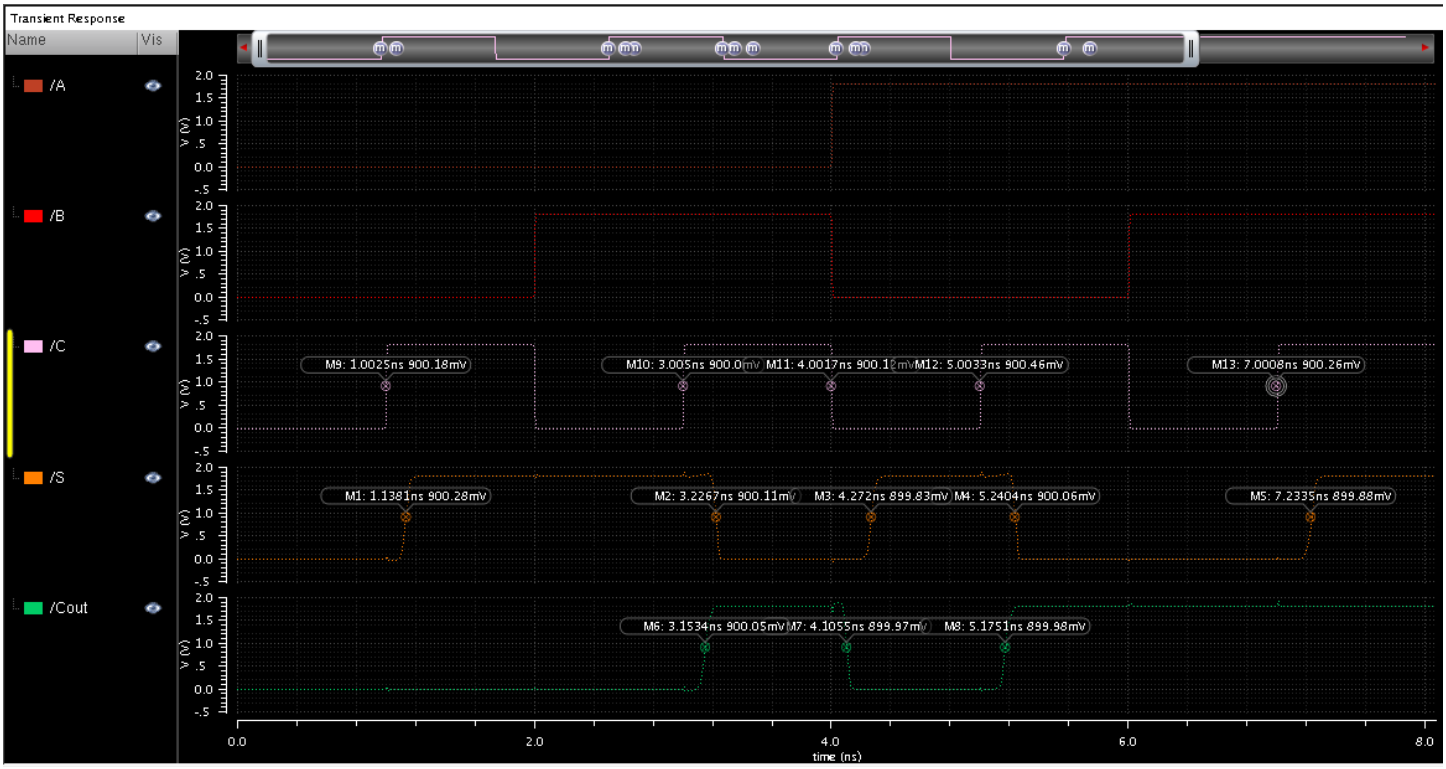
2. Metal width=1 um, height of cell=6 um
   a. Standard full adder
      Total area=15.2*6=91.2 um^2
   b. Gate level full adder
      Total area=14.85*12=178.2 um^2
3. LVS
   a. Standard full adder



b. Gate level full adder



4. Function test
    a. Standard full adder



    b. Gate level full adder

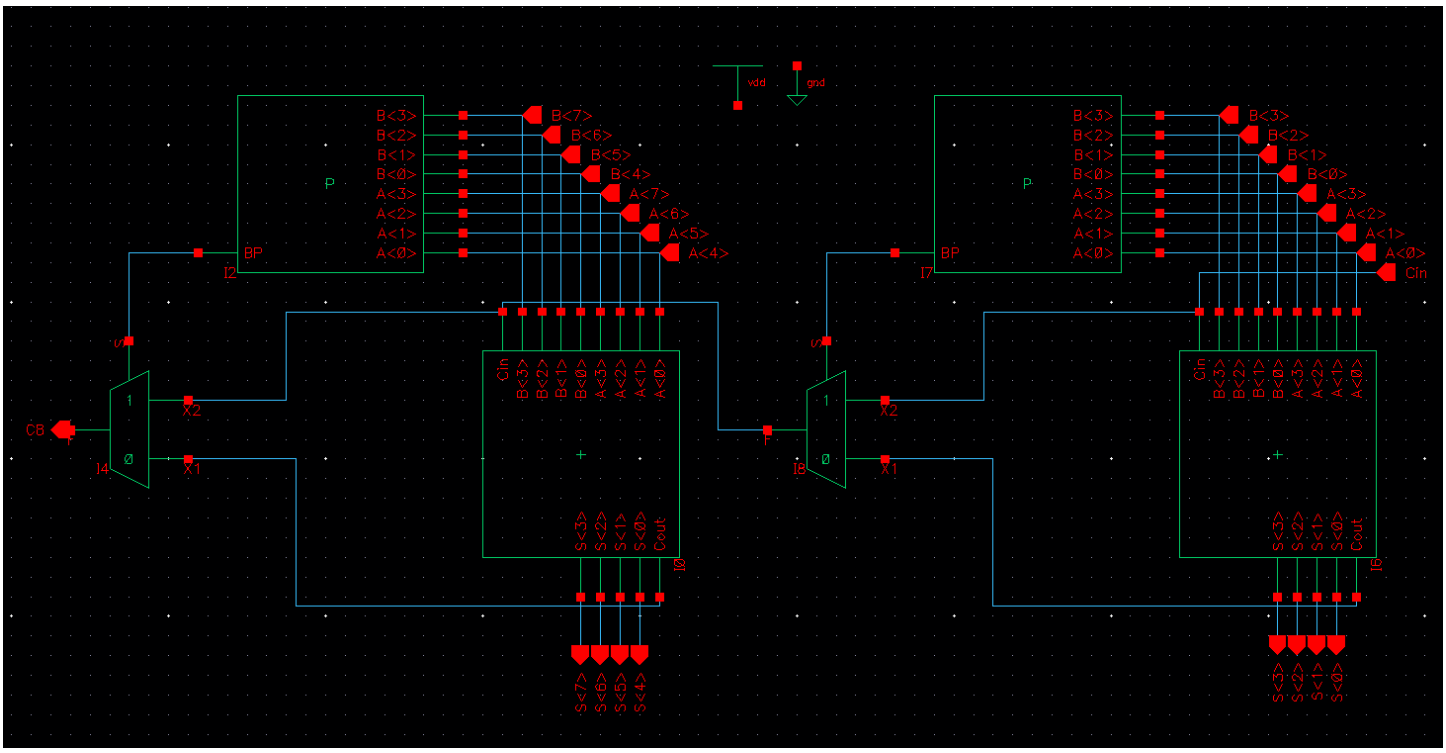
5. Comparison results and explanation.

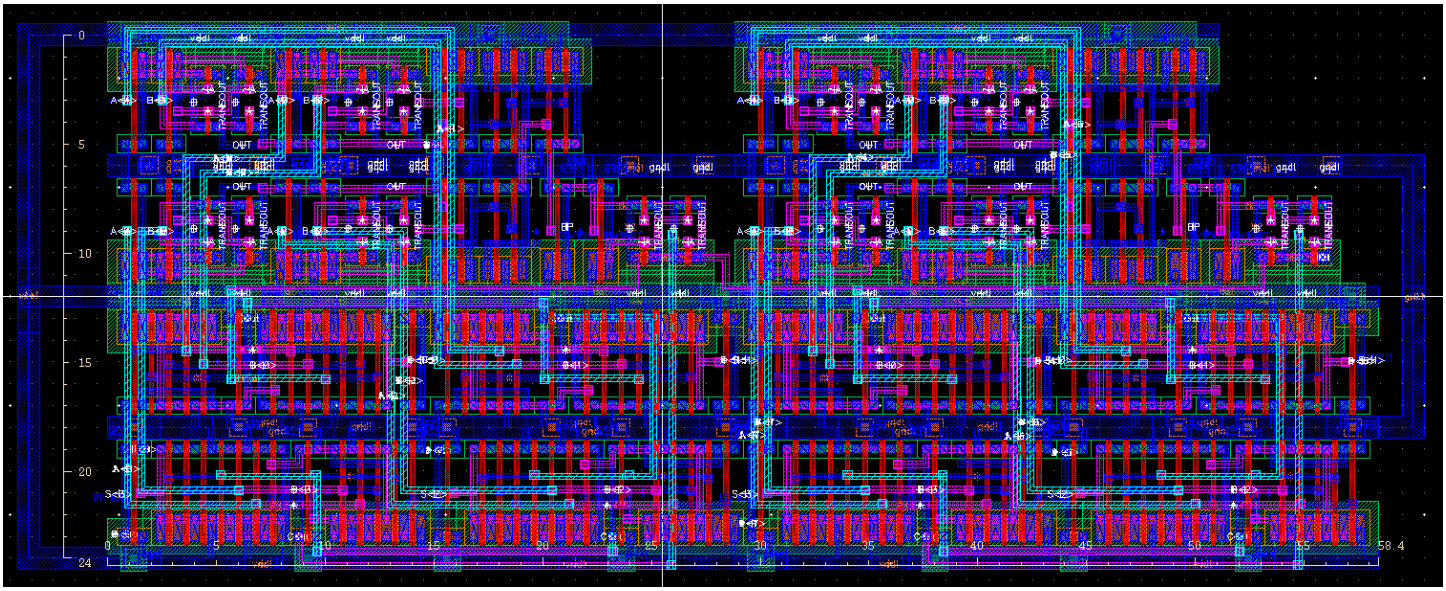
Standard Full Adder					Gate level Full adder				
C	S	S delay	Cout	Cout delay	C	S	S delay	Cout	Cout delay
1.0025	1.1381	0.1356			1.0025	1.0651	0.0626		
3.005	3.2267	0.2217	3.1534	0.1484	3.005	3.0293	0.0243	3.1004	0.0954
4.0017	4.272	0.2703	4.1105	0.1088	4.0017	4.0472	0.0455	4.093	0.0913
5.0033	5.2404	0.2371	5.1751	0.1718	5.0033	5.0295	0.0262	5.1004	0.0971

Conclusion, the gate level design has smaller delay, but the output signal is not smooth during the input changes. The reason for gate level design have smaller delay may because it has smaller capacitance to charge. Each gate is separated.

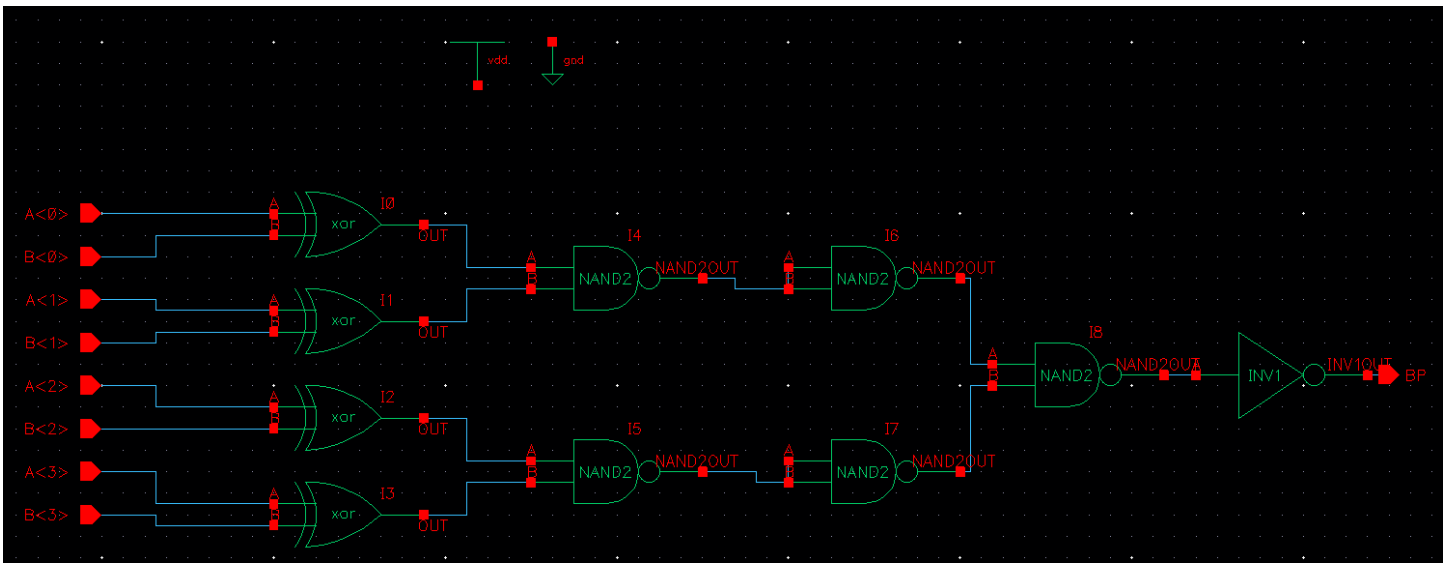
8-biiit Carry-Skip adder

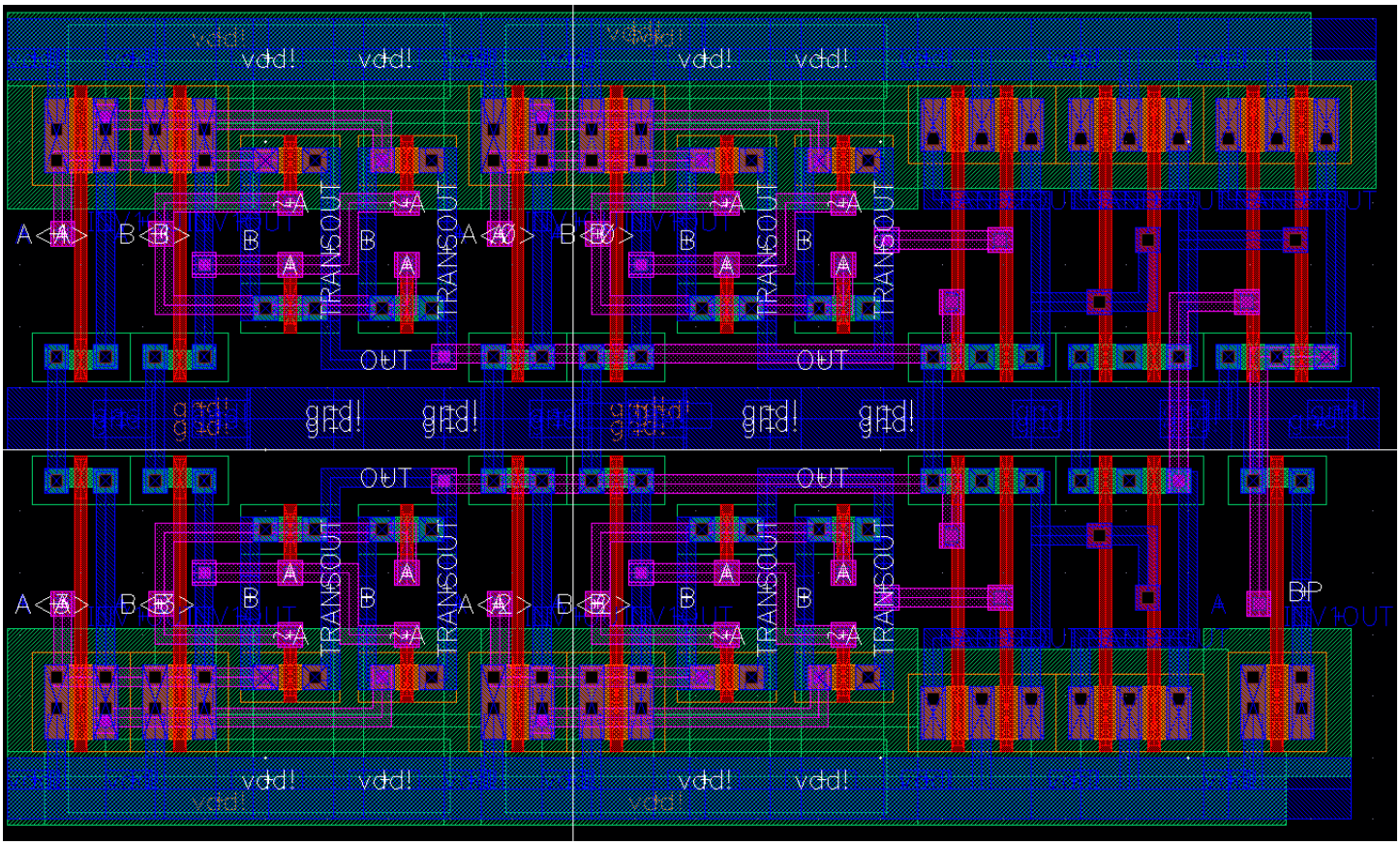
6. Schematic and layout



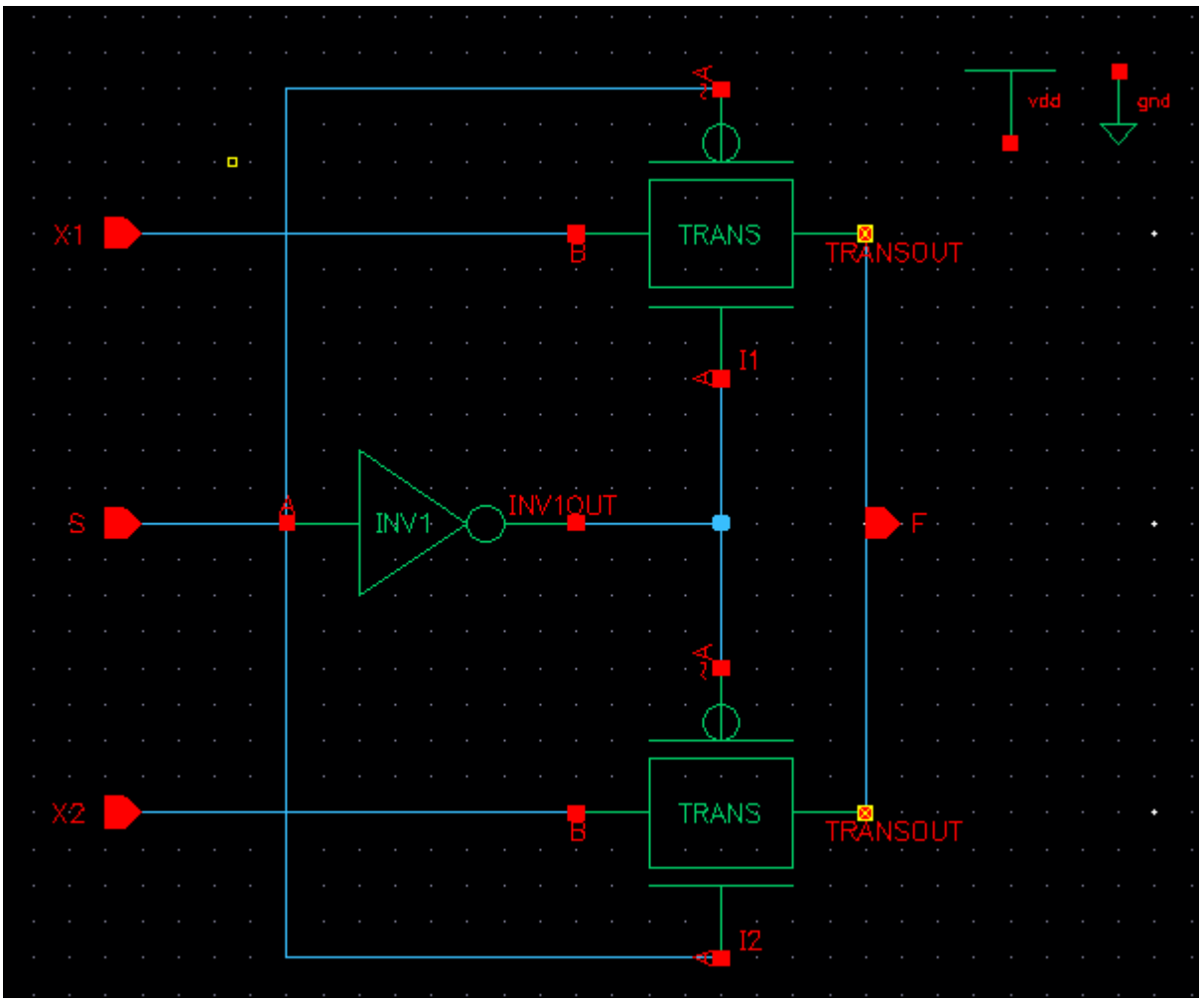


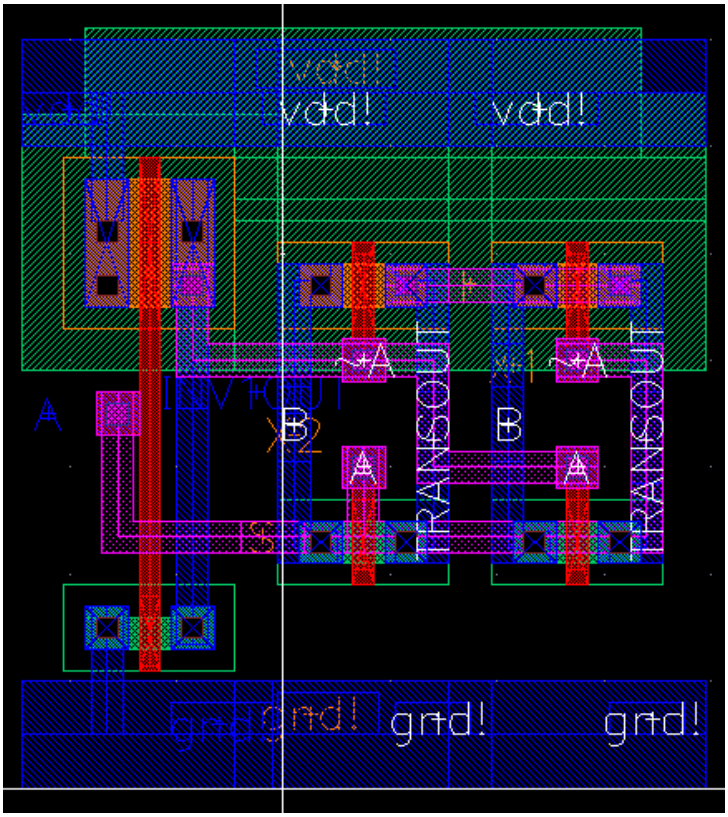
P module


vdd
gnd
A<0>
B<0>
A<1>
B<1>
A<2>
B<2>
A<3>
B<3>
xor
I0
I1
I2
I3
OUT
I4
I5
I6
I7
NAND2
NAND2OUT
I8
INV1
INV1OUT
BP

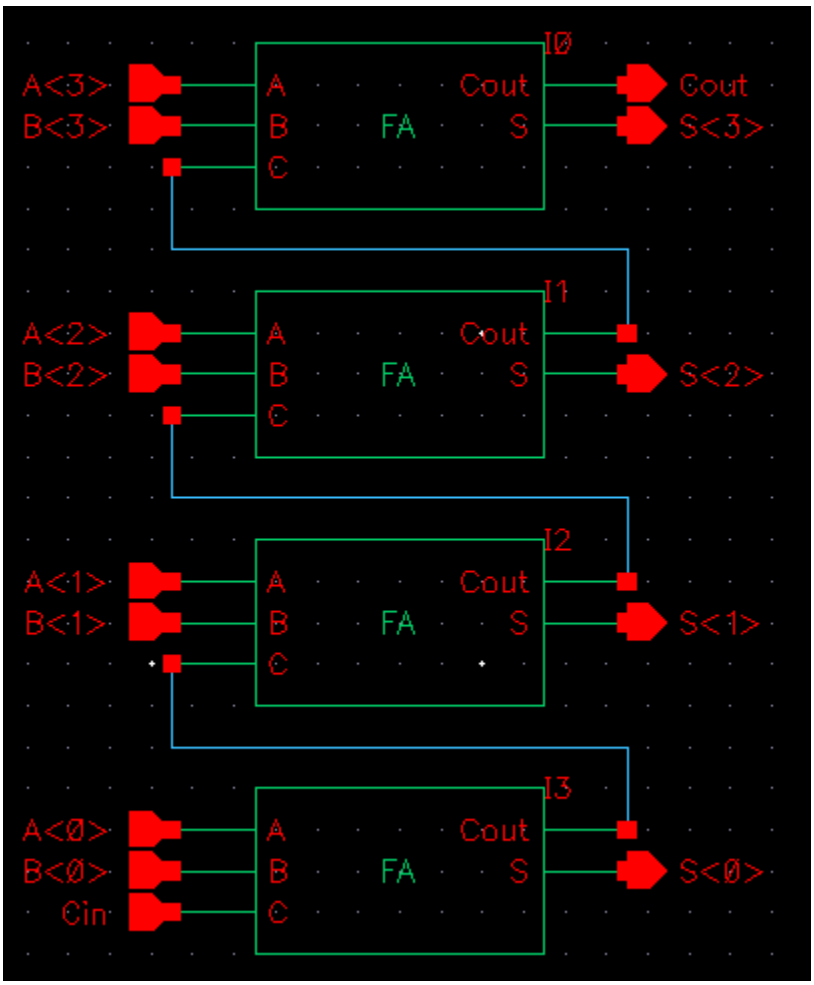

vdd!
gnd!
A<0>
B<0>
A<1>
B<1>
A<2>
B<2>
A<3>
B<3>
TRANSOUT
OUT
BP
INV1OUT

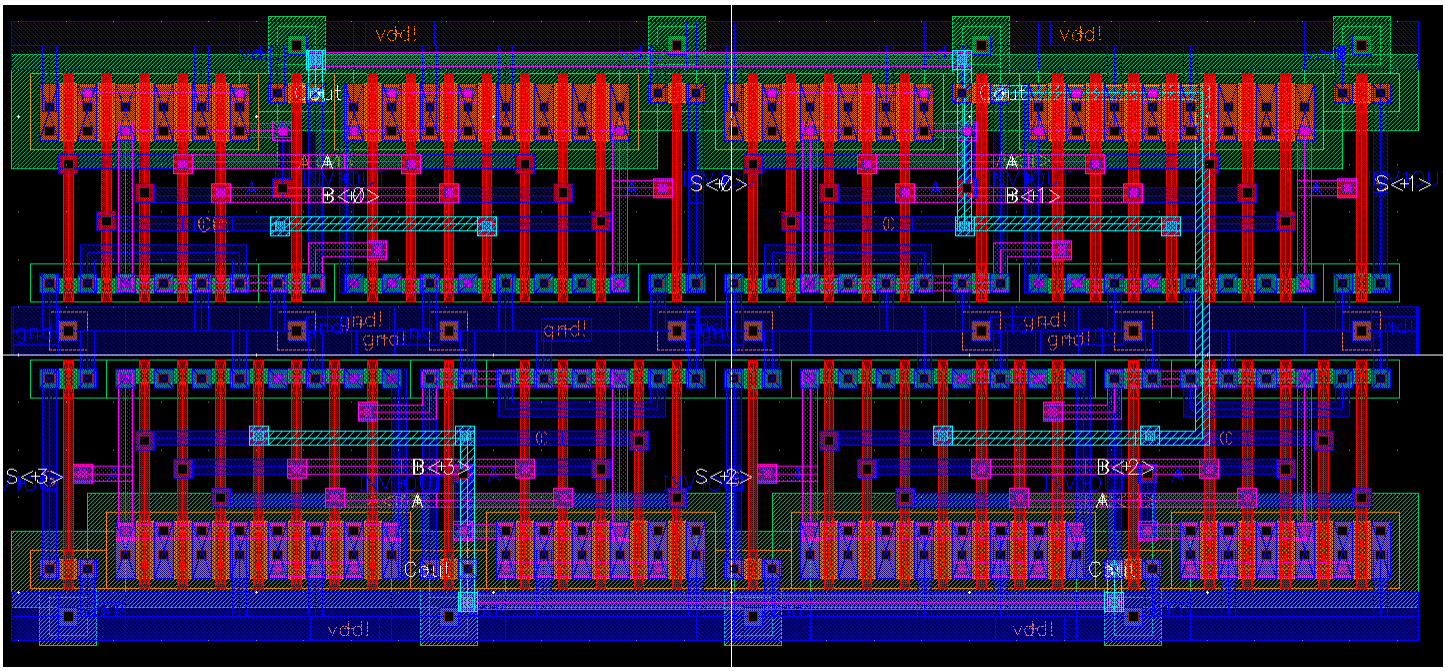
Mux


vdd
gnd
X1
B
TRANS
TRANSOUT
I1
S
A
INV1
INV1OUT
F
X2
B
TRANS
TRANSOUT
I2


vdd!
vdd!
vdd!
A
INV1OUT
B
B
TRANSOUT
TRANSOUT
gnd!
gnd!
gnd!

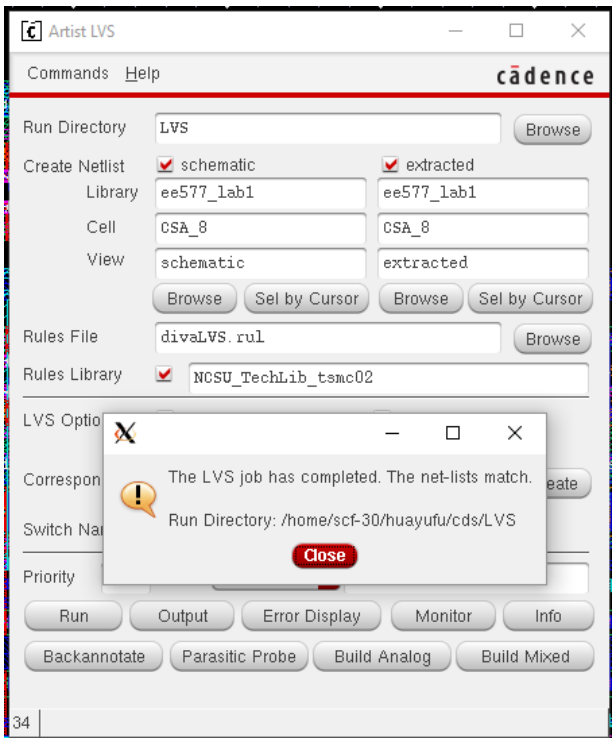
4-bit adder





7. Total area=58.4*24=1401.6 um^2

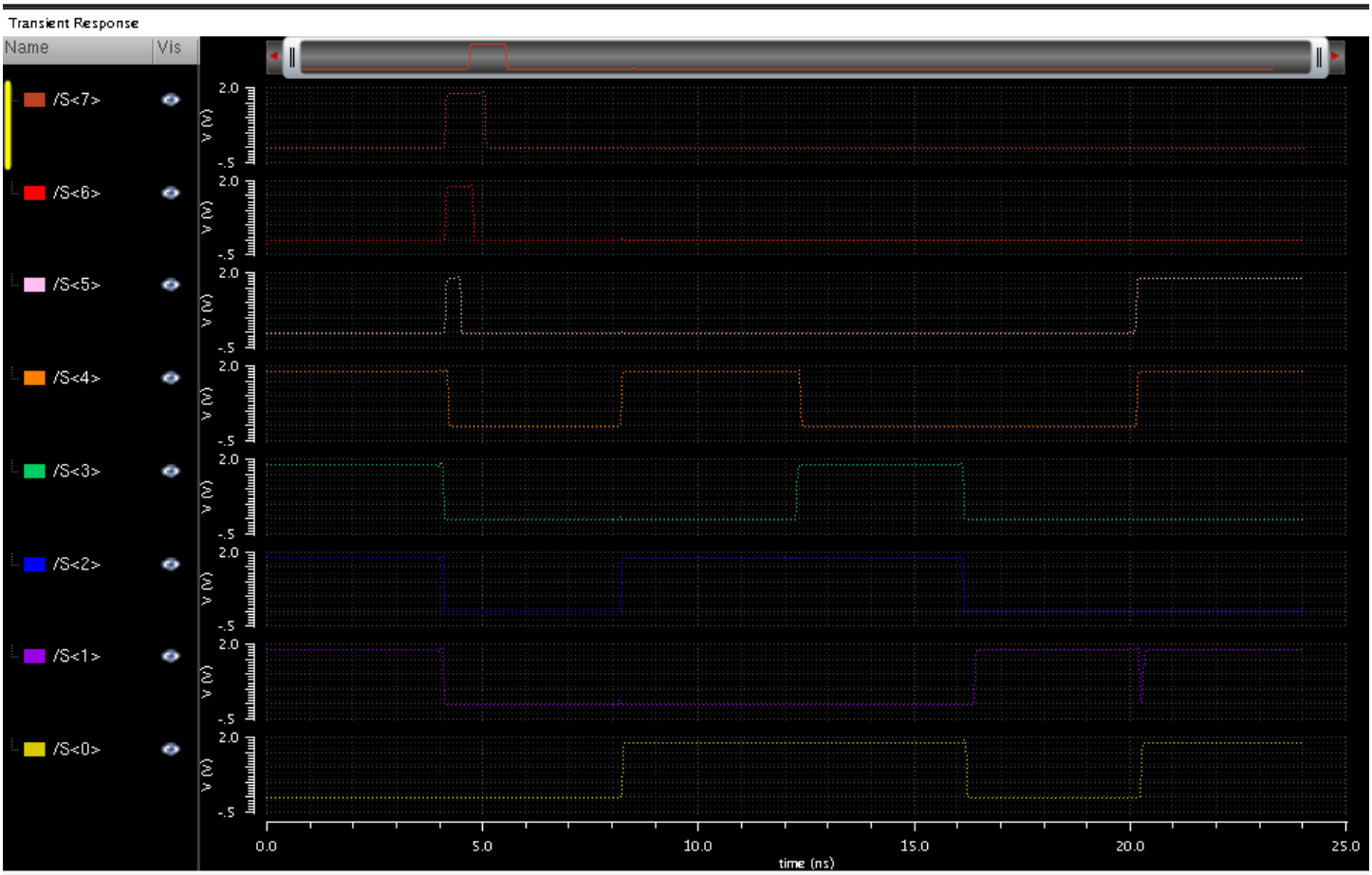
8. LVS



9. Functional test waveforms and results on the layoutof8-bit Carry-skip adder for any six random inputs.

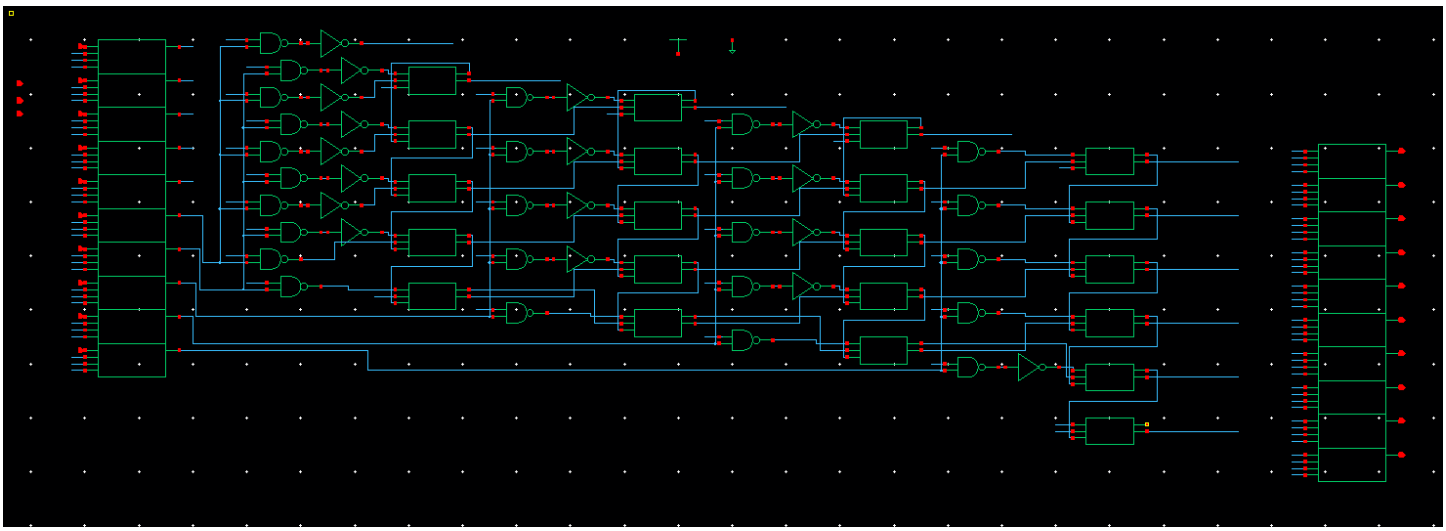
```
radix   4       4       4       4
io      i       i       i       i
vname   A<[7:4]>        A<[3:0]>        B<[7:4]>        B<[3:0]>
slope 0.01
vih 1.8
tunit ns
0       0       F       0       F
4       F       F       0       1
8       0       A       0       B
12      0       C       0       1
16      0       1       0       1
20      1       2       2       1
```

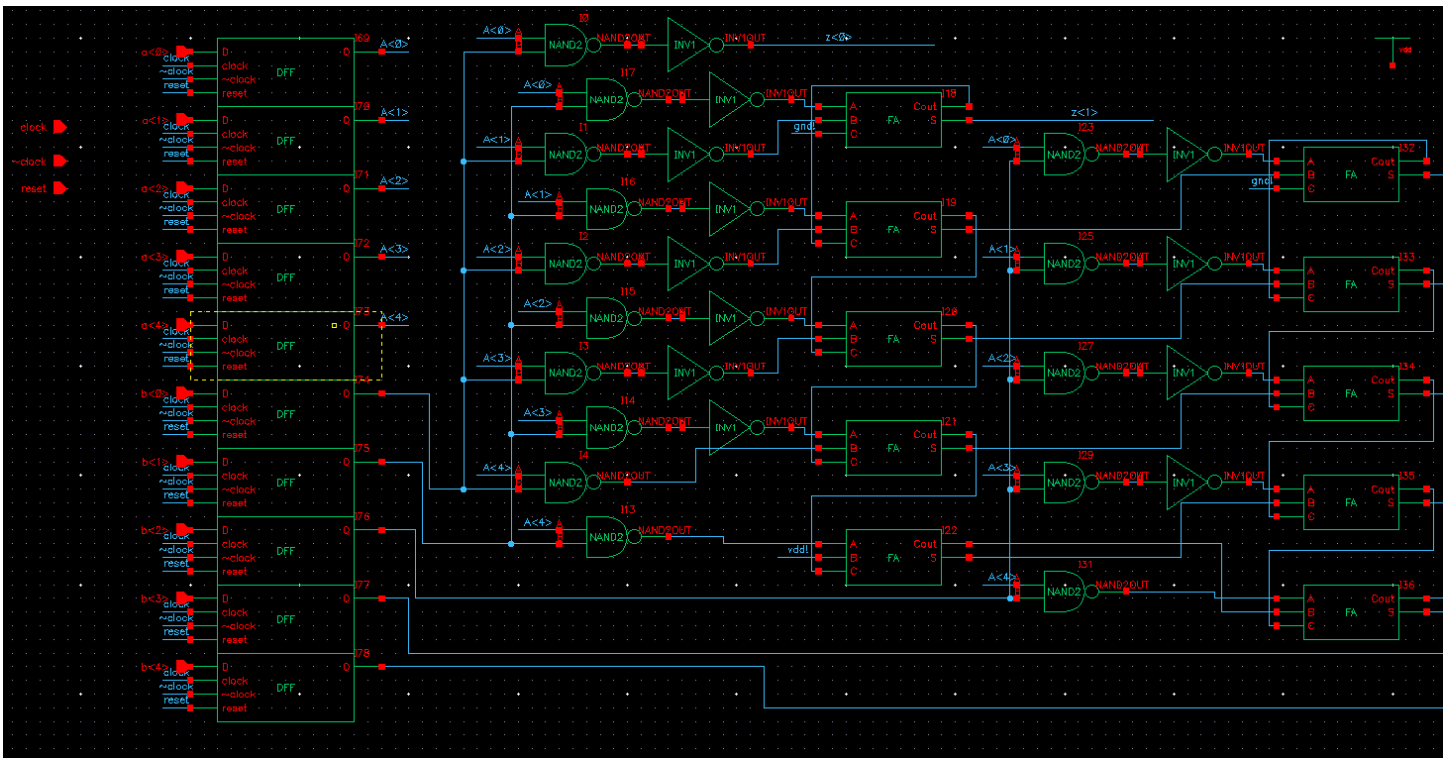
A	B	expected S	actual S
1111	1111	11110	11110
11111111	1	0	0
1010	1011	10101	10101
1100	1	1101	1101
1	1	10	10
10010	100001	110011	110011

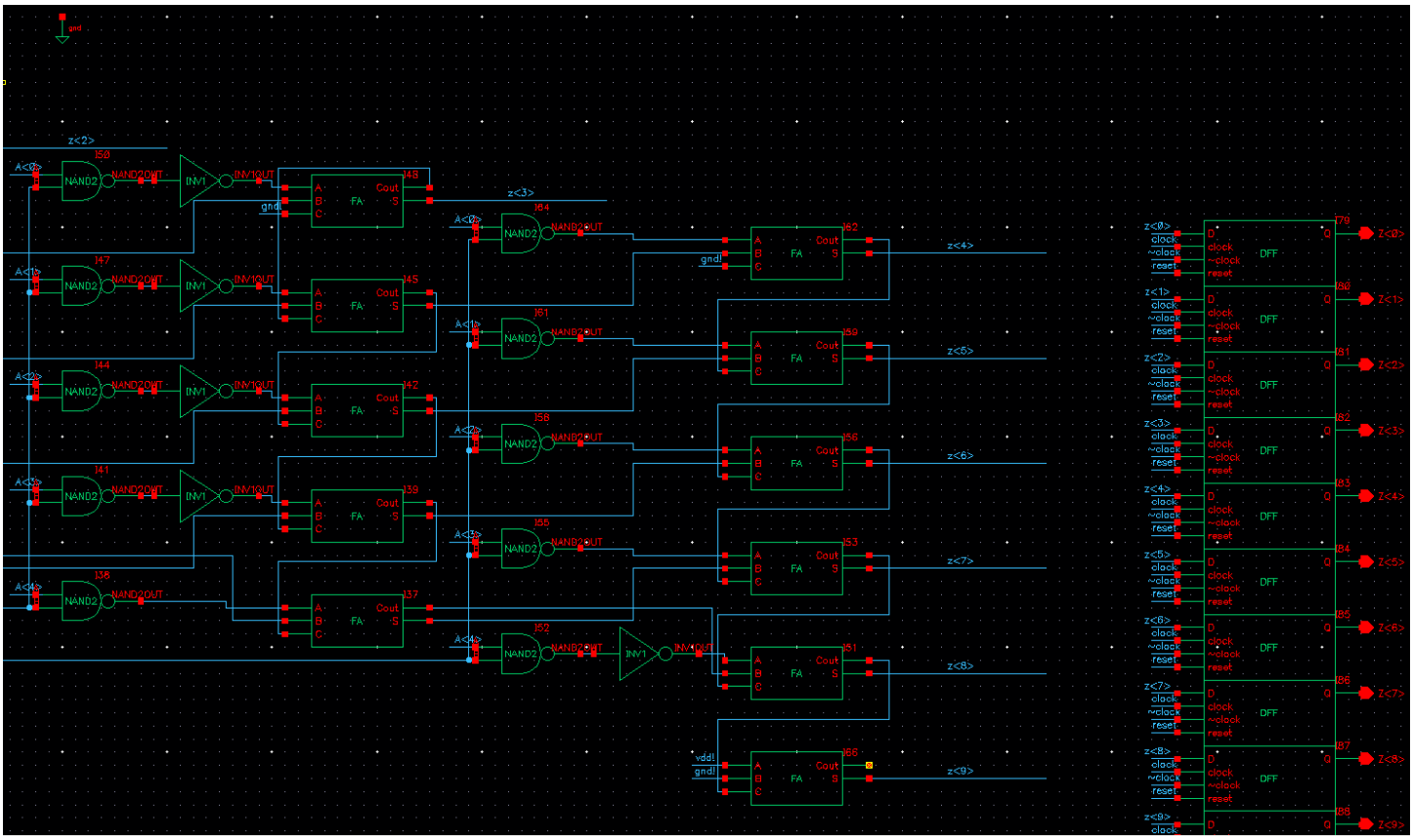

Transient Response
Name
Vis
/S<7>
/S<6>
/S<5>
/S<4>
/S<3>
/S<2>
/S<1>
/S<0>
2.0
V (V)
-.5
0.0
5.0
10.0
15.0
20.0
25.0
time (ns)

2’s Complement Multiplier

10. Schematic and layout for2’s Complement Multiplier.

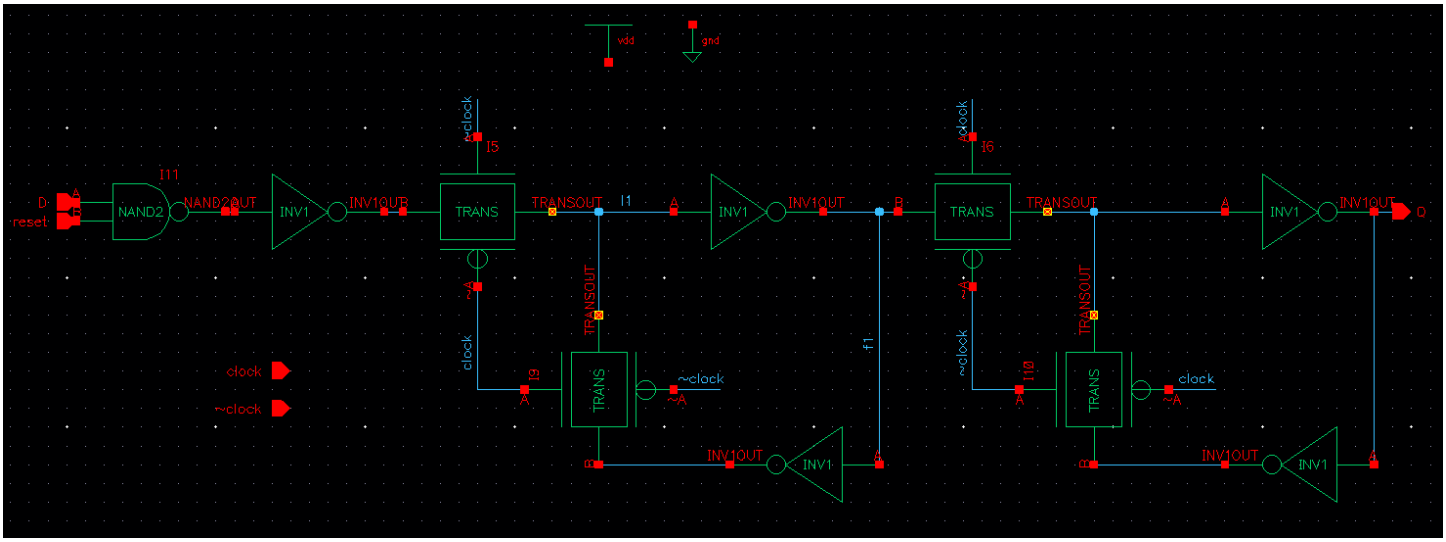


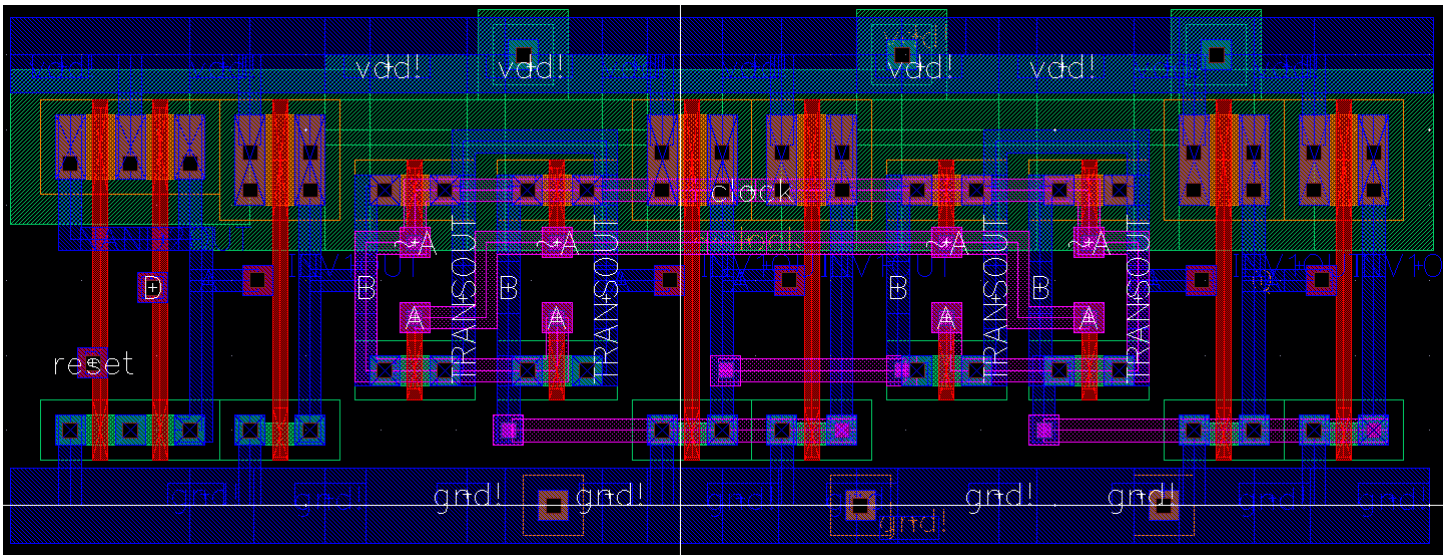




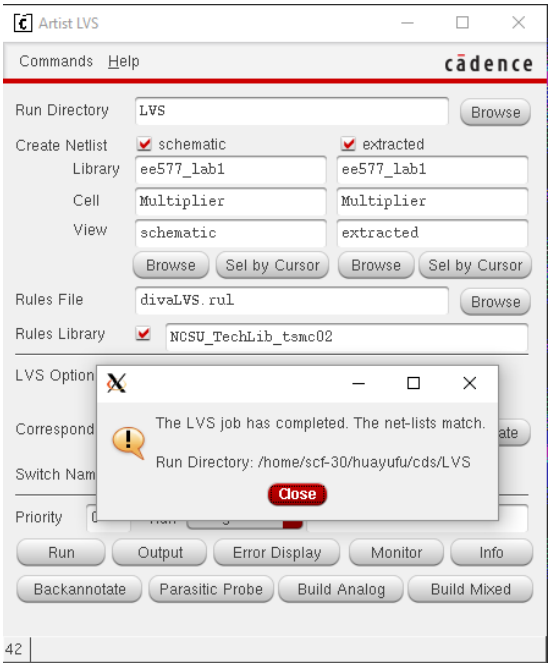
Total area=133*42=5586 um^2

DFF


vdd
gnd
NAND2
INV1
TRANS
TRANSOUT
INV1OUT
clock
~clock
reset
Q

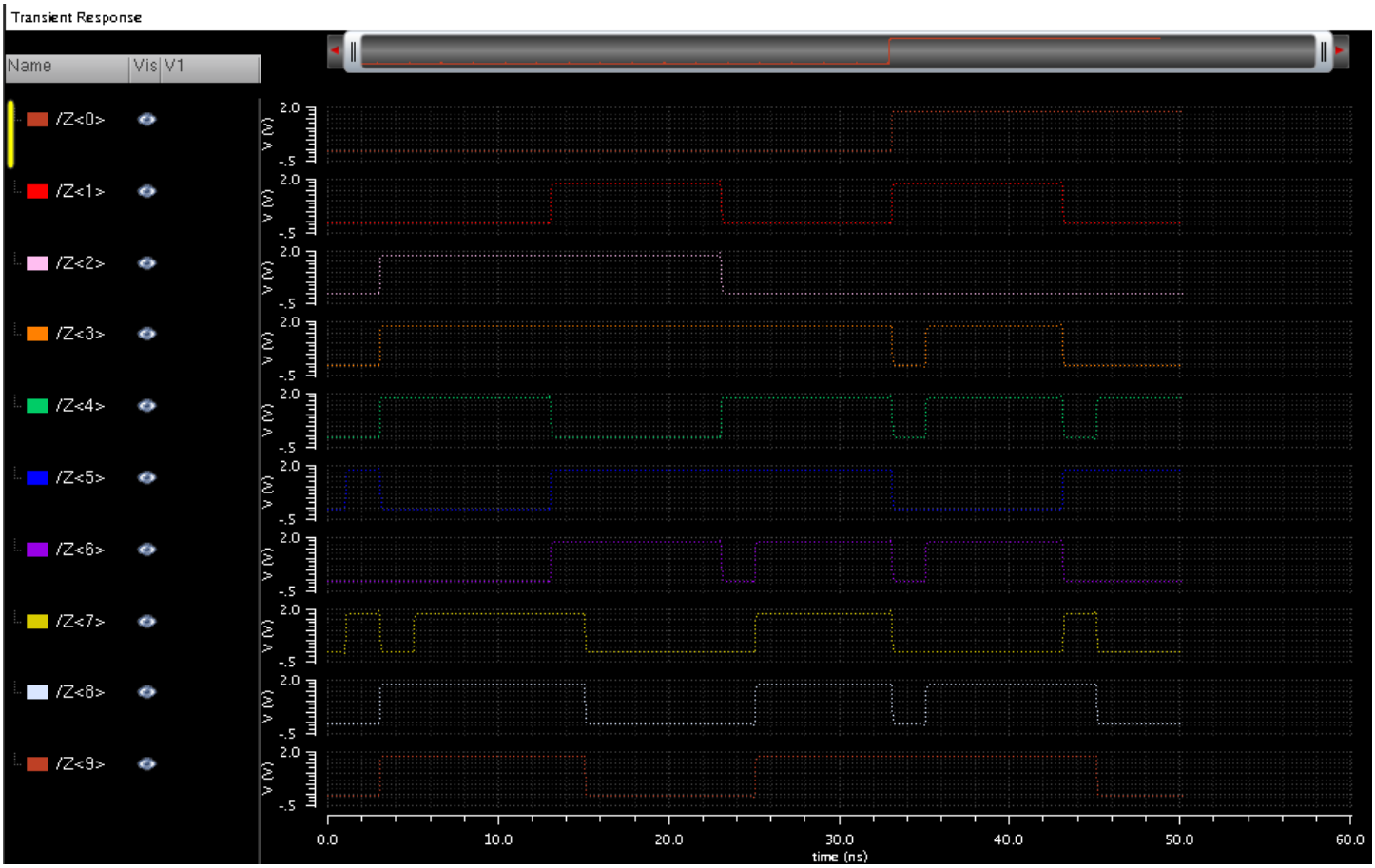

vdd!
gnd!
clock
reset
TRANSOUT

11. LVS


Artist LVS
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
ee577_lab1
Cell
Multiplier
View
schematic
extracted
Sel by Cursor
Rules File
divaLVS.rul
Rules Library
NCSU_TechLib_tsmc02
The LVS job has completed. The net-lists match.
Run Directory: /home/scf-30/huayufu/cds/LVS
Close
Priority
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed

Functional Test using Perlor Python

12. Functional test waveforms and results on the layout of 2's Complement Multiplier for the 5 test



op1	op2	result	op1	op2	restut
10	-10	-100	0b01010	0b10110	1110011100
10	11	110	0b01010	0b01011	0,001,101,110
1	-8	-8	0b00001	0b11000	1111111000
-11	15	-165	0b10101	0b01111	1101011011
-7	-7	49	0b11001	0b11001	0,000,110,001