# EE 477 Laboratory #2
# Part 1

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## Cell Sizes:

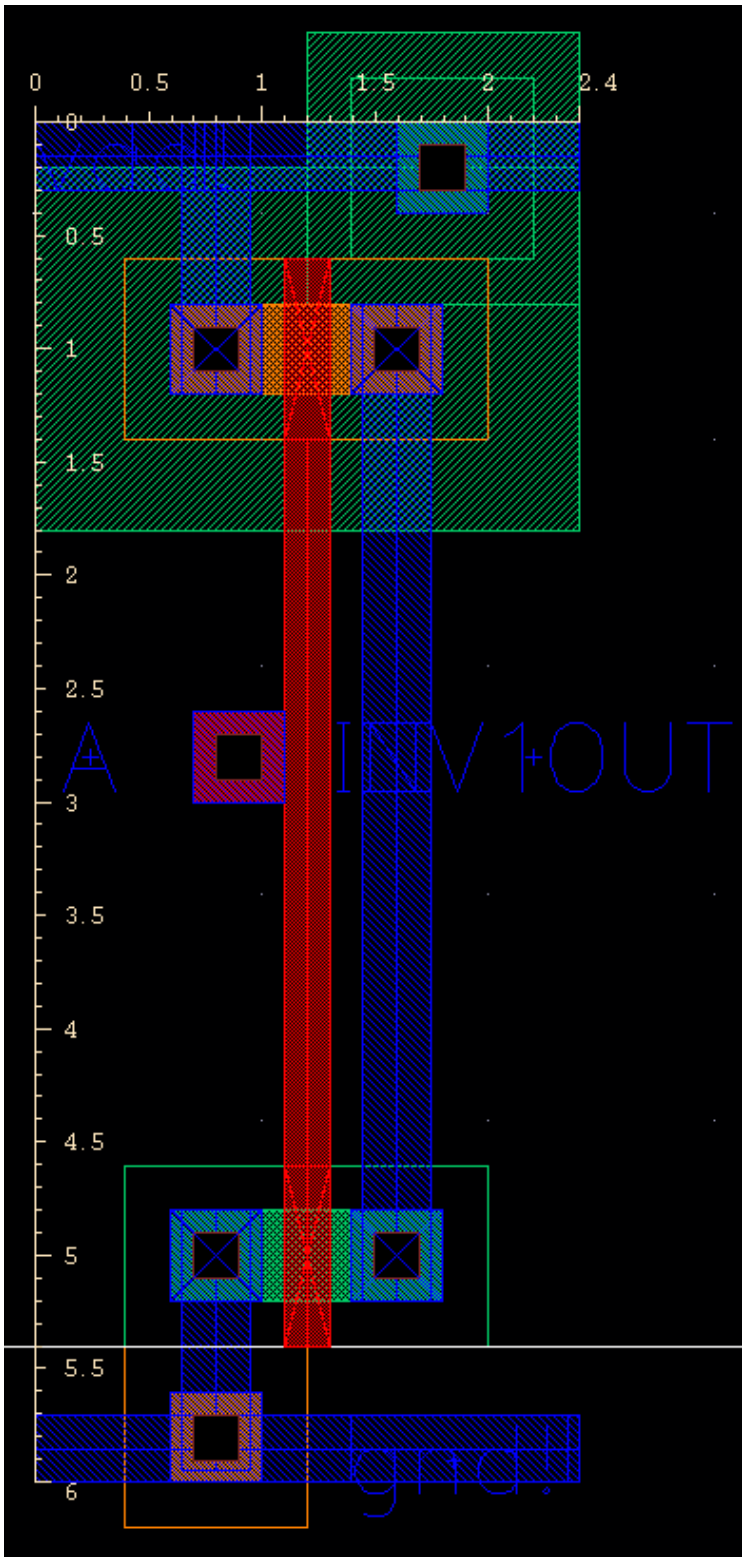
| Name | Height | Width |
|---|---|---|
| Inverter #1 | 6 | 2.4 |
| 2-input NAND | 6 | 3.2 |

# Table of Contents

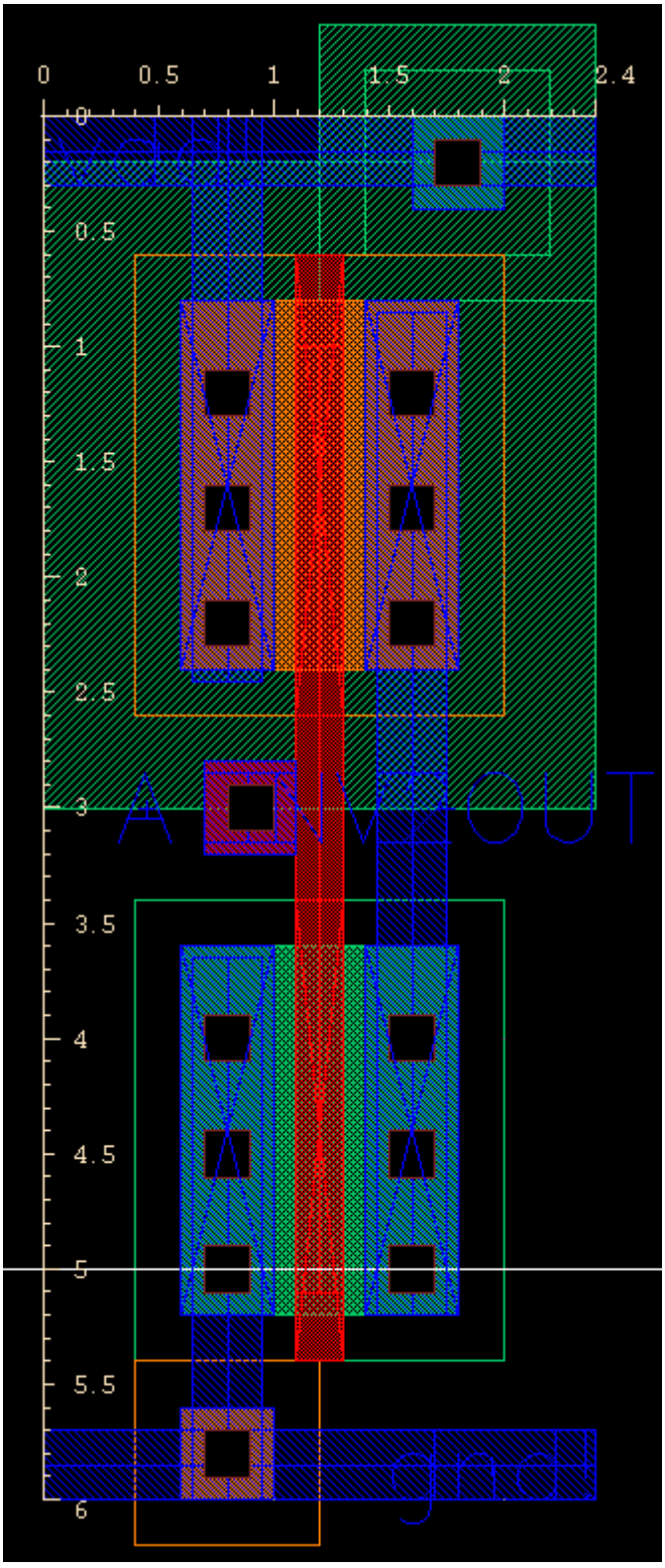
1. List of All Cell Simulated:

| Name | Height | Width |
|---|---|---|
| Inverter #1 | 6 | 2.4 |
| Inverter #2 | 6 | 2.4 |
| Inverter #3 | 6 | 2.4 |
| Transmission Gate | 6 | 2.4 |
| 2-input NAND | 6 | 3.2 |
| 3-input NAND | 6 | 4 |
| Compound Gate | 6 | 8.8 |

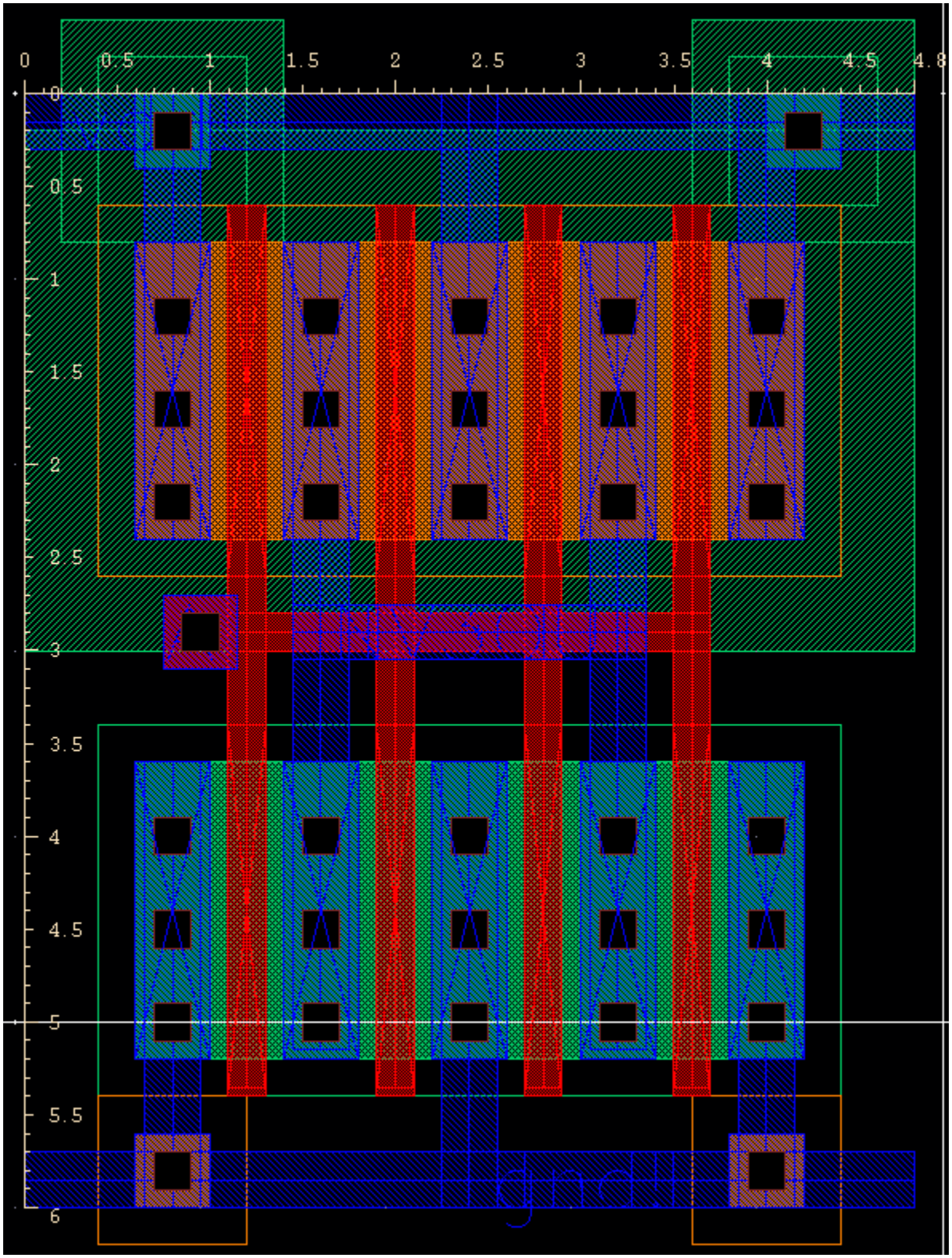
2. Cell layout images:
   A. Inverter #1



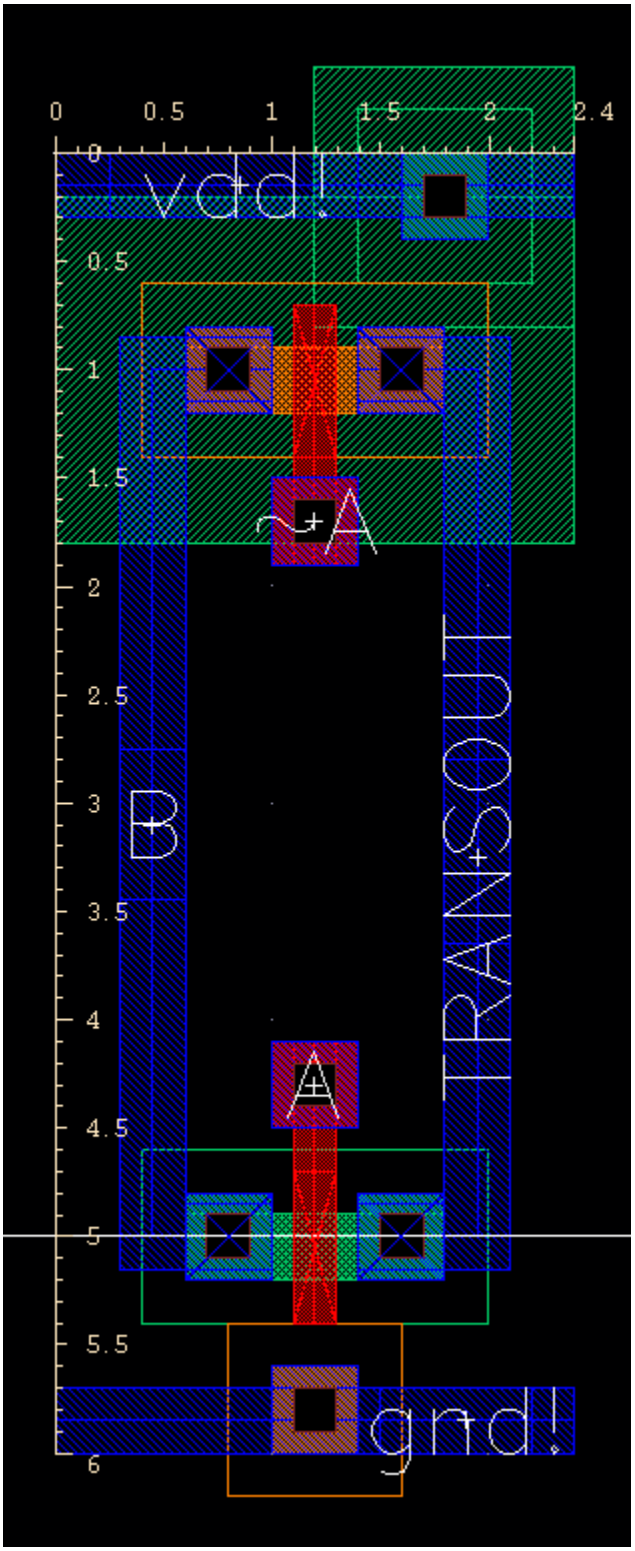
B. Inverter #2



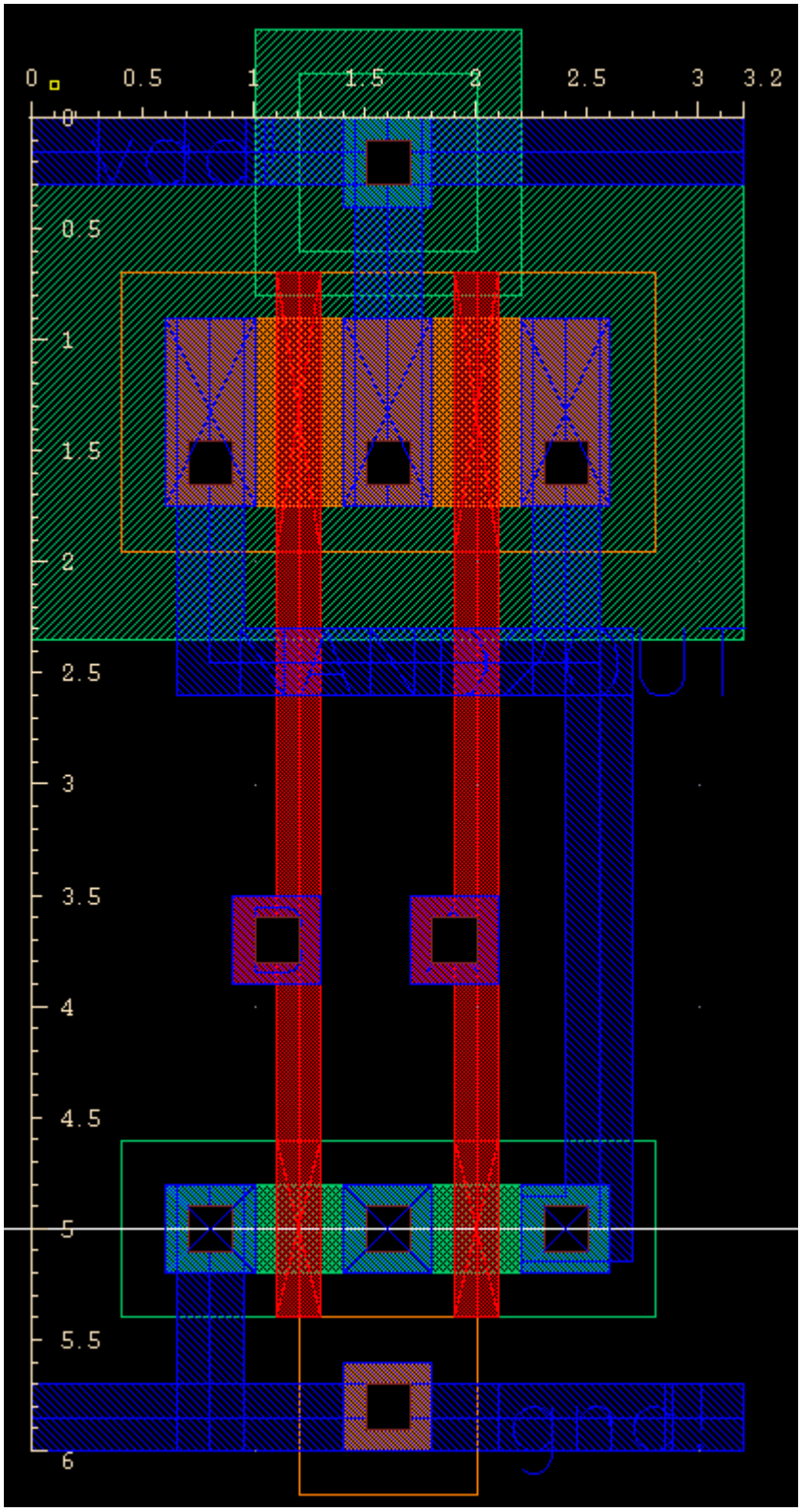
C. Inverter #3



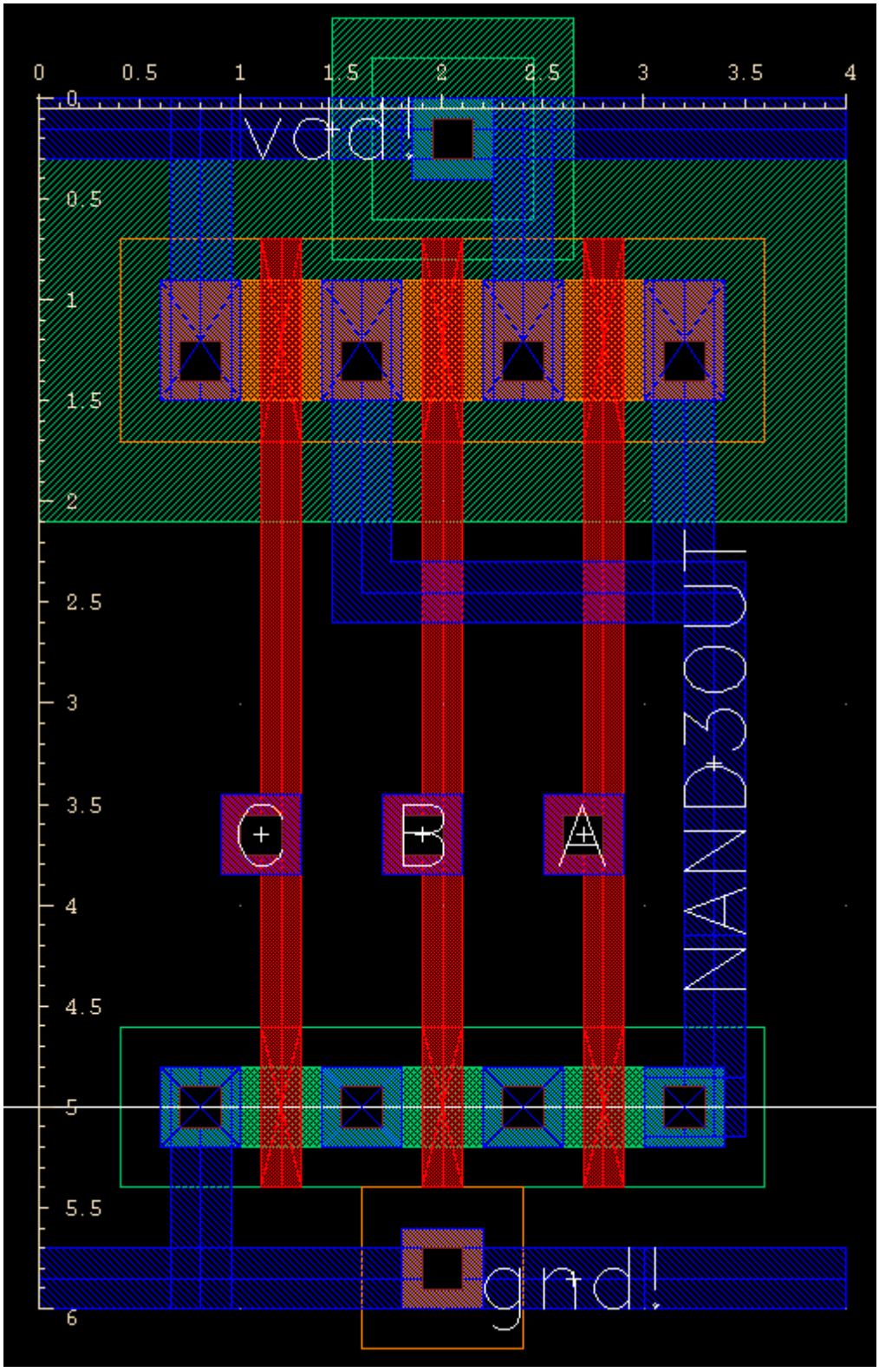
D. Transmission Gate



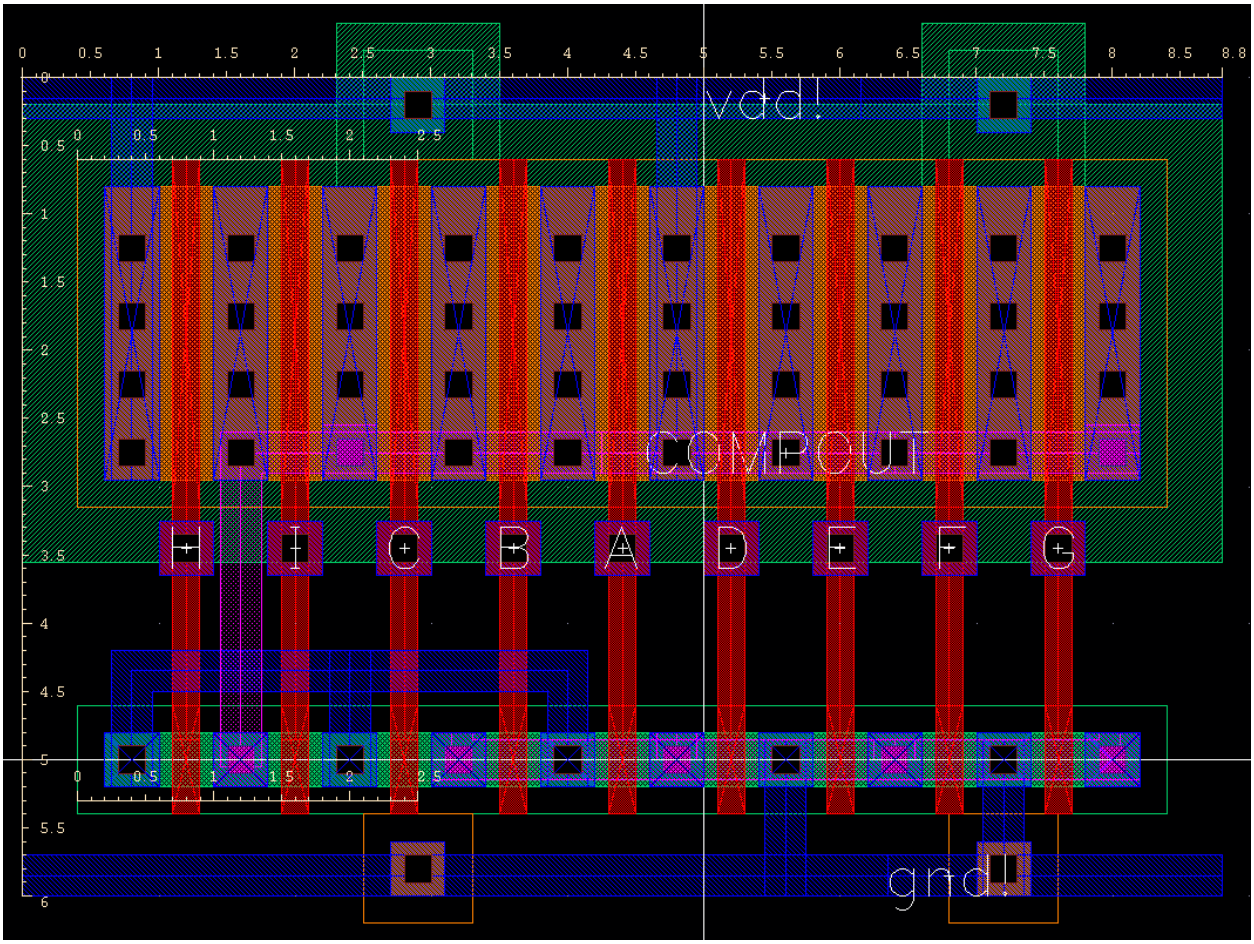
E. 2-input NAND



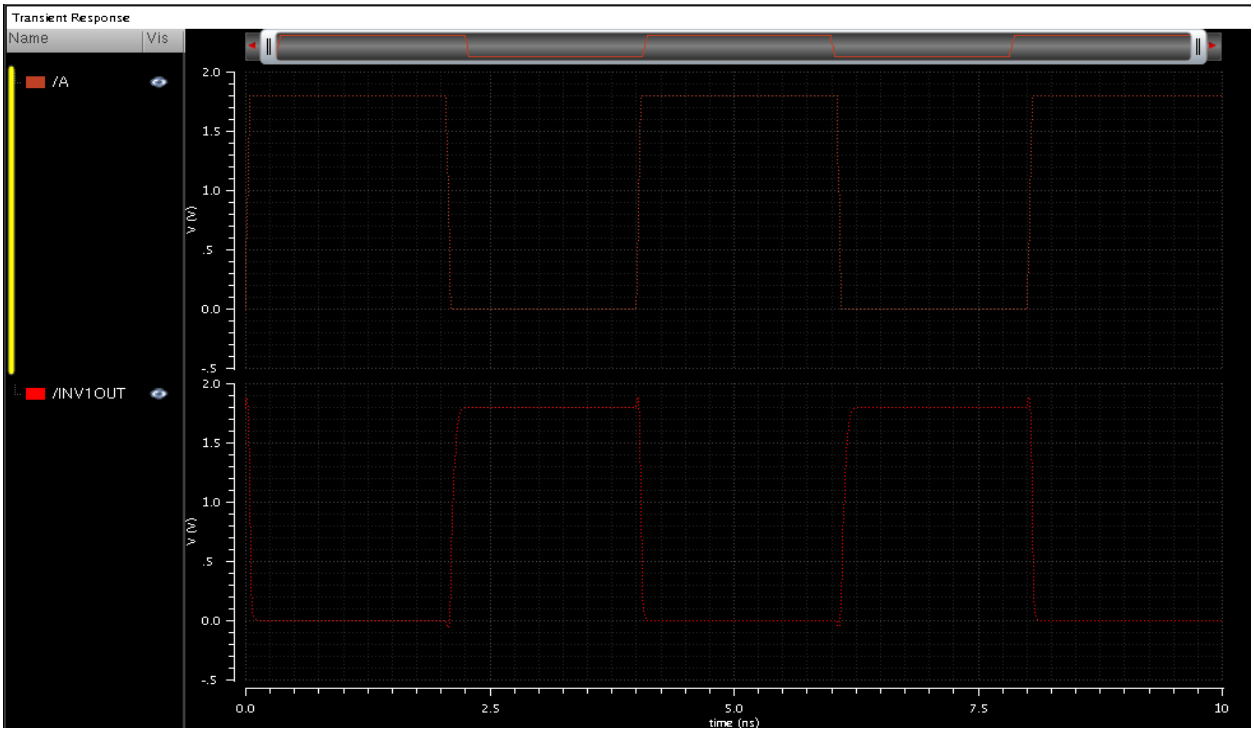
F. 3-input NAND



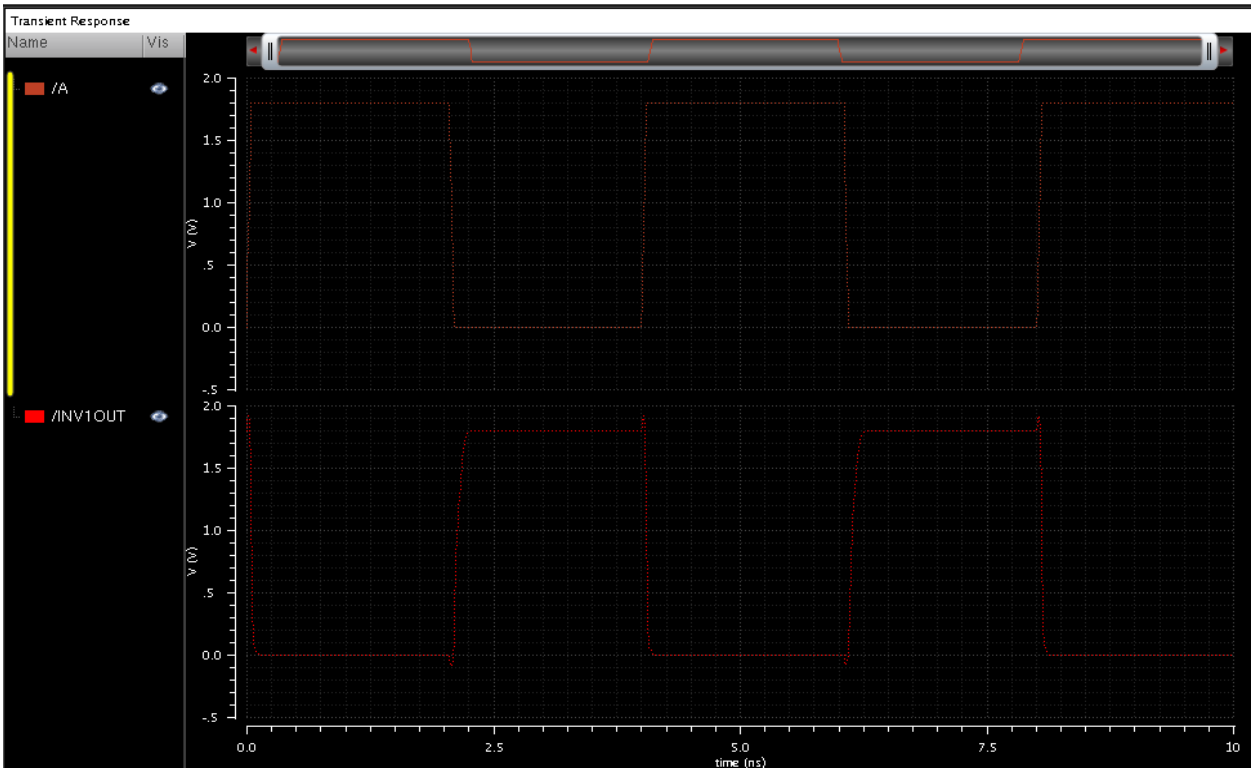
G. Compound Gate



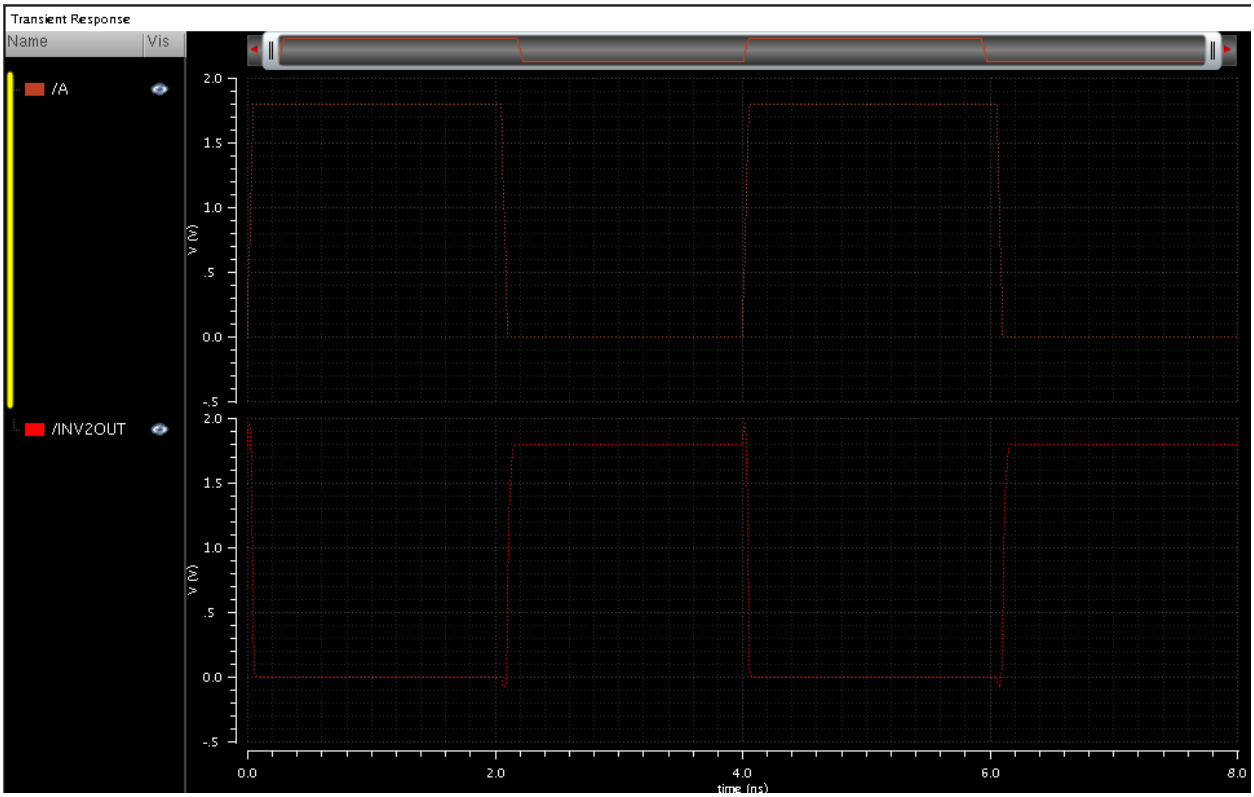
3. The SPECTRE simulations:
   A. Inverter #1
      1. T=27 Celsius



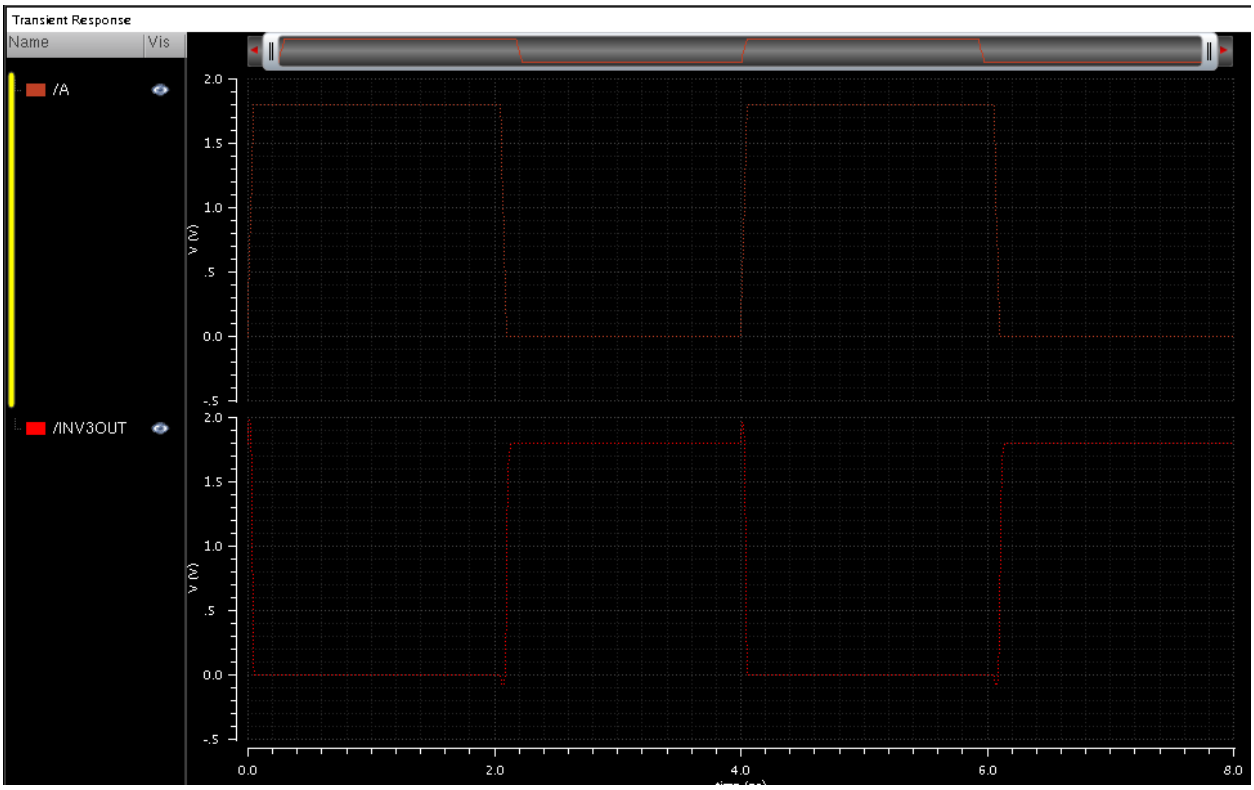

      2. T=100 Celsius



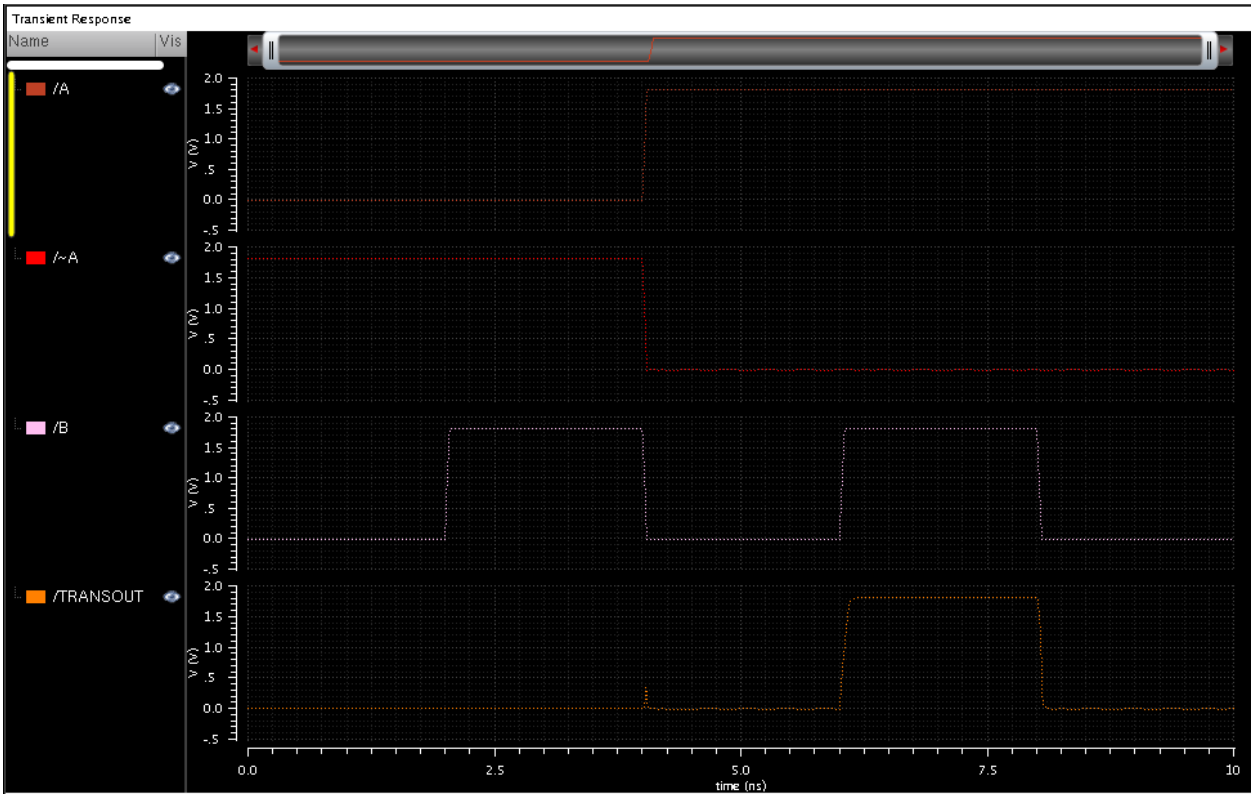
B. Inverter #2



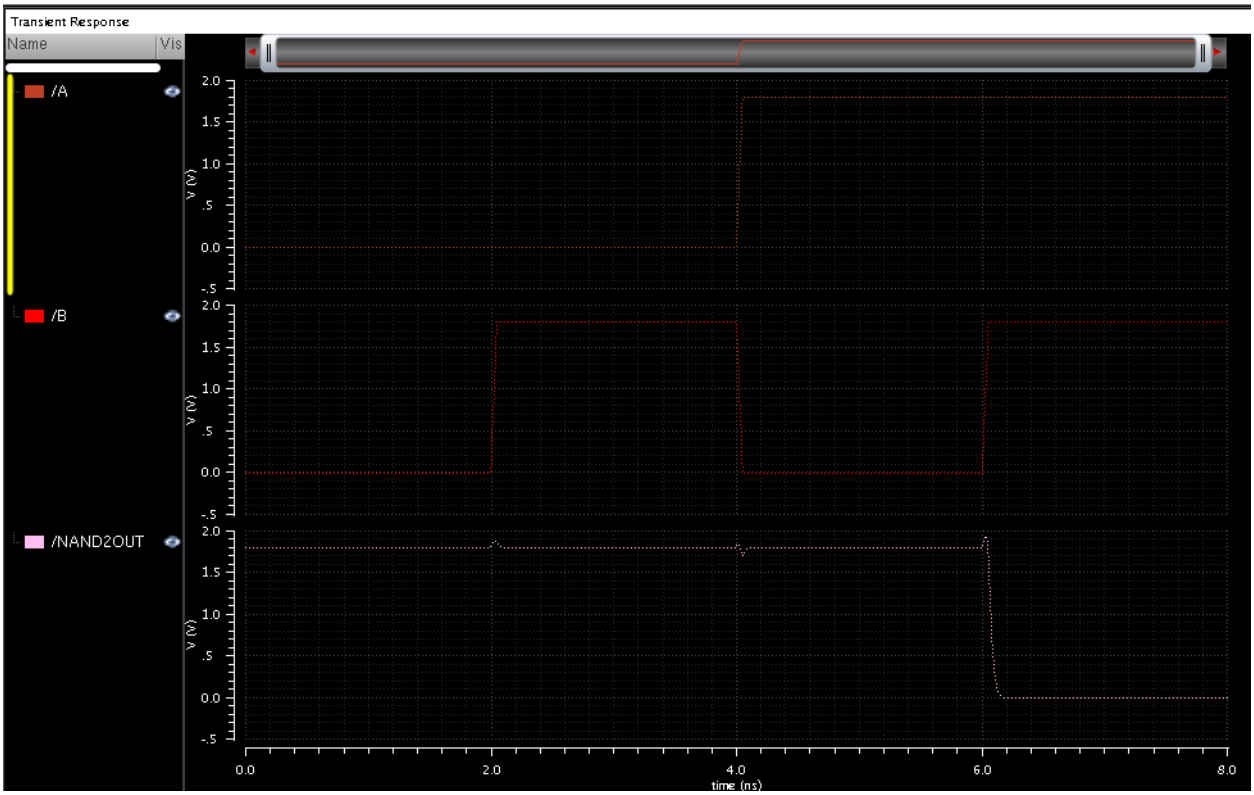

C. Inverter #3



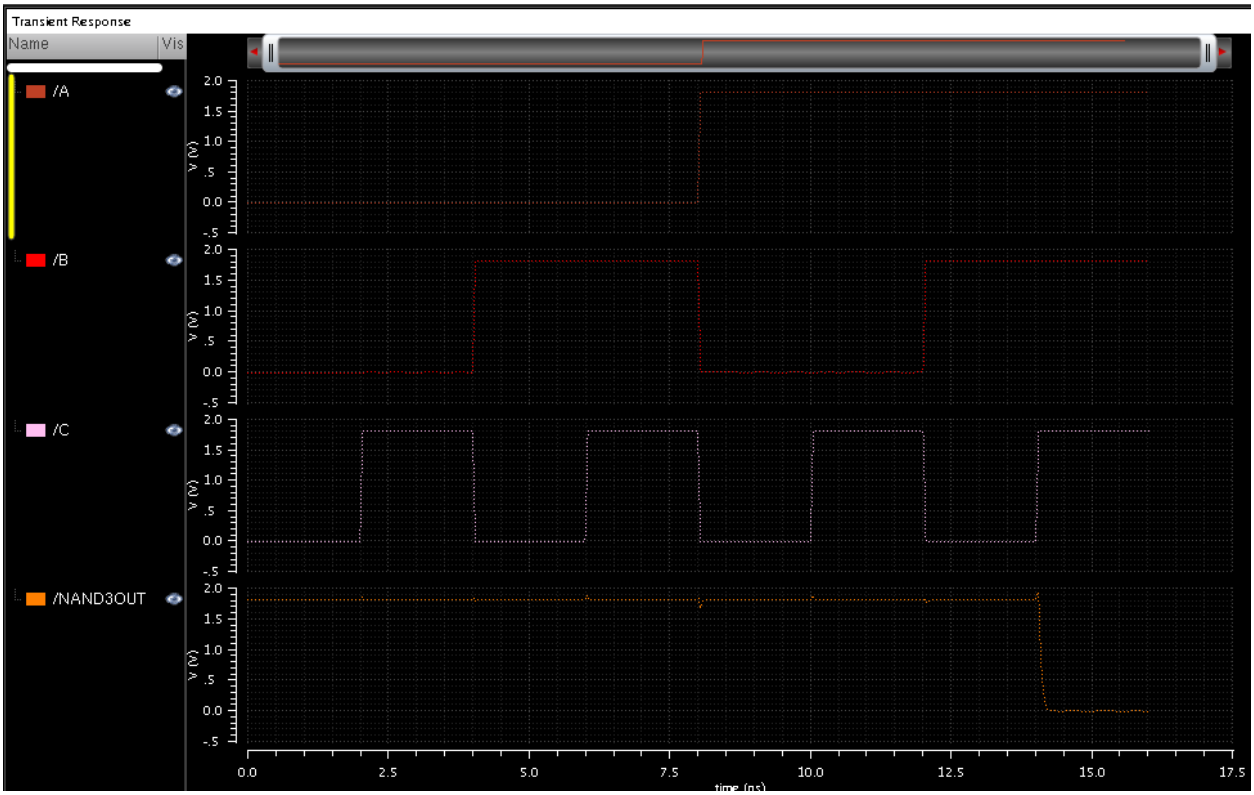
D. Transmission Gate




E. 2-input NAND

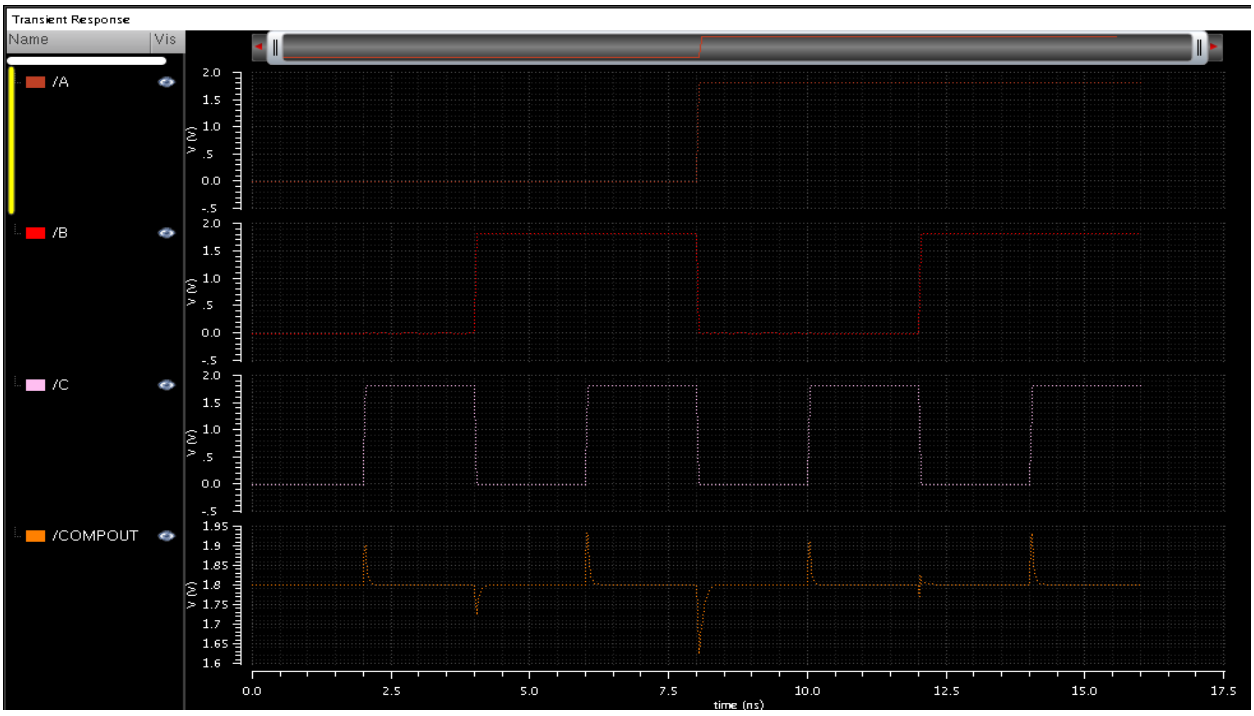


F. 3-input NAND

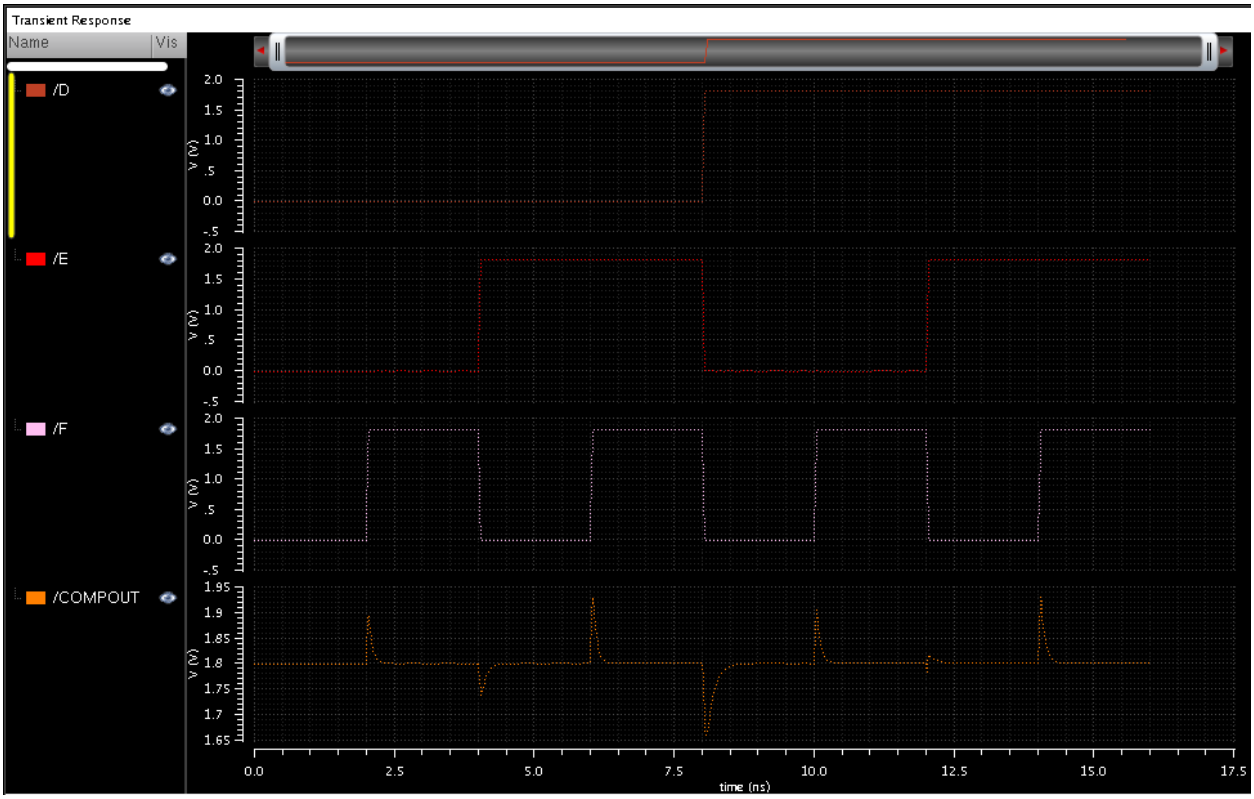



G. Compound Gate

1. all combinations of A, B, C from 000 to 111, counting up in binary 000, 001, 010, etc. , while holding DEF amd GHI to 000.



2. hold ABC=010 and GHI to 000, and then change DEF from 000 to 111




4. comparison of the inverter #1 at the different temperatures

| Temperature | Rise time | Fall time |
|---|---|---|
| 27 Celsius | 7.23E-11 | 2.61E-11 |
| 100 Celsius | 9.00E-11 | 2.90E-11 |

As the temperature increases the rise time and fall time of the inverter #1 both increases. And the ratio of rise and fall time increases. In conclusion, higher temperature will reduce the performance of inverter.

5. discussion of cell rise and fall times and a comparison to the simulation results for Lab 1

| Name | Schematic(LAB1) | | | Layout(LAB2) | | | Percentage Difference | | |
|---|---|---|---|---|---|---|---|---|---|
| | Rise time | Fall time | R/F ratio | Rise time | Fall time | R/F ratio | Rise time | Fall time | R/F ratio |
| Inverter #1 | 7.16E-11 | 2.56E-11 | 280% | 7.23E-11 | 2.61E-11 | 277% | -1% | -2% | 1% |
| Inverter #2 | 3.95E-11 | 1.93E-11 | 205% | 3.94E-11 | 1.87E-11 | 211% | 0% | 3% | -3% |
| Inverter #3 | 2.91E-11 | 1.69E-11 | 172% | 2.36E-11 | 1.48E-11 | 159% | 23% | 14% | 8% |
| Transmission Gate | 7.40E-11 | 3.70E-11 | 200% | 8.34E-11 | 3.89E-11 | 214% | -11% | -5% | -7% |
| 2-input NAND | 6.28E-11 | 5.81E-11 | 108% | 6.23E-11 | 6.10E-11 | 102% | 1% | -5% | 6% |
| 3-input NAND | 9.70E-11 | 9.04E-11 | 107% | 9.04E-11 | 9.57E-11 | 95% | 7% | -5% | 13% |
| Compound Gate | 6.60E-10 | 5.60E-10 | 118% | 5.36E-10 | 4.78E-10 | 112% | 23% | 17% | 5% |

The chart above shows the comparison of the rise and fall times between schematic and layout.

For inverter #1 and #2, the percentage difference is small, since I used single NMOS and single PMOS to form the inverter.

For inverter #3, the percentage difference is large, since I used multiple small NMOS and PMOS, not the signal large transistors. The parasitic capacitance between the single large transistor and multiple small transistor might be different. And the resistance between the single large transistor and multiple small transistor might be different.

For Transmission Gate, the percentage difference is also large. The reason is there is ntap and ptap in layout design, and I connected them to the vdd and ground. If I disconnect the vdd and gnd the behavior is similar to the schematic simulation. And the rise time is 43.81E-12 s, the fall time is 38.7E-12 s.

For NANDs and Compound Gate, the Rise/Fall ratio is closer to 1 compared with the schematic simulation, and all of them falls within the required region of rise and fall time. Therefore, the overall performance of layout simulation is better than the schematic simulation.

In general, rise time will decrease in the layout simulation compared with schematic simulation. And as the rise time falls the fall time also falls. If we have the rise time larger than the fall time in the schematic simulation, the performance will be better in layout simulation, which means the fall time decrease is smaller than rise decrease.