EE552 Homework 5 (QDI + Proteus)

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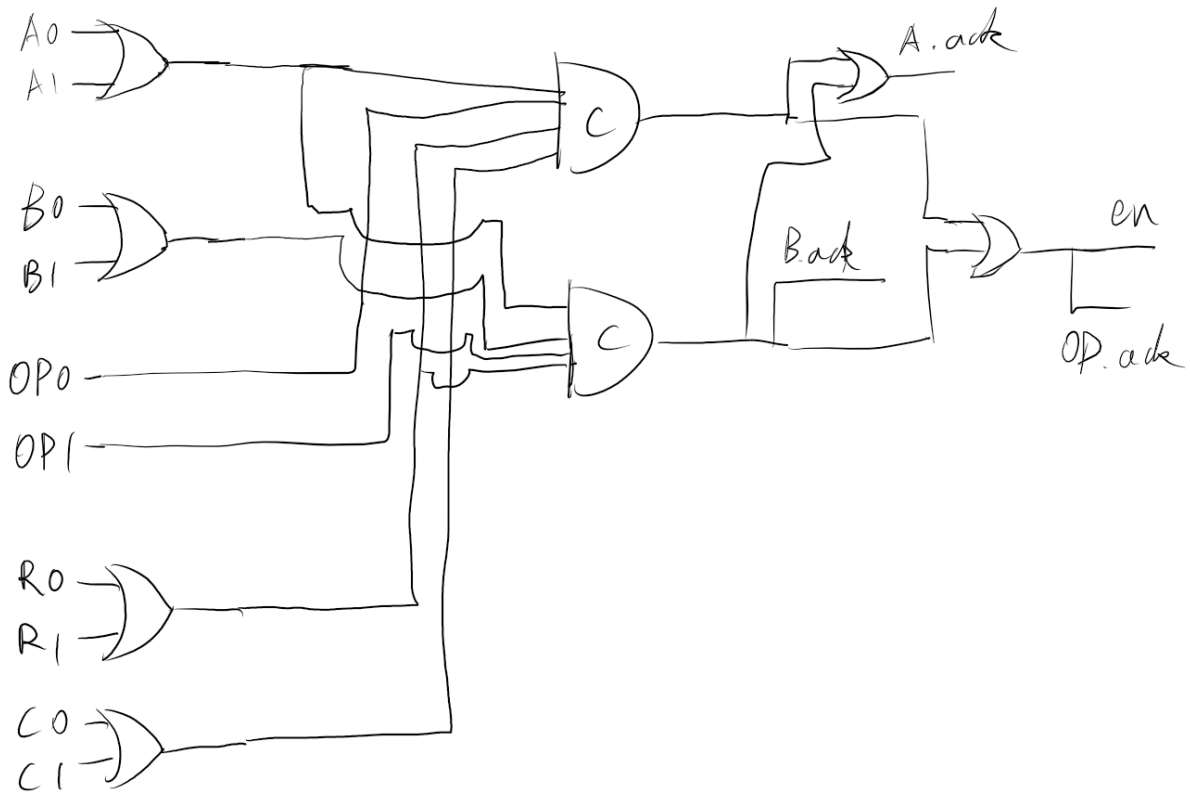
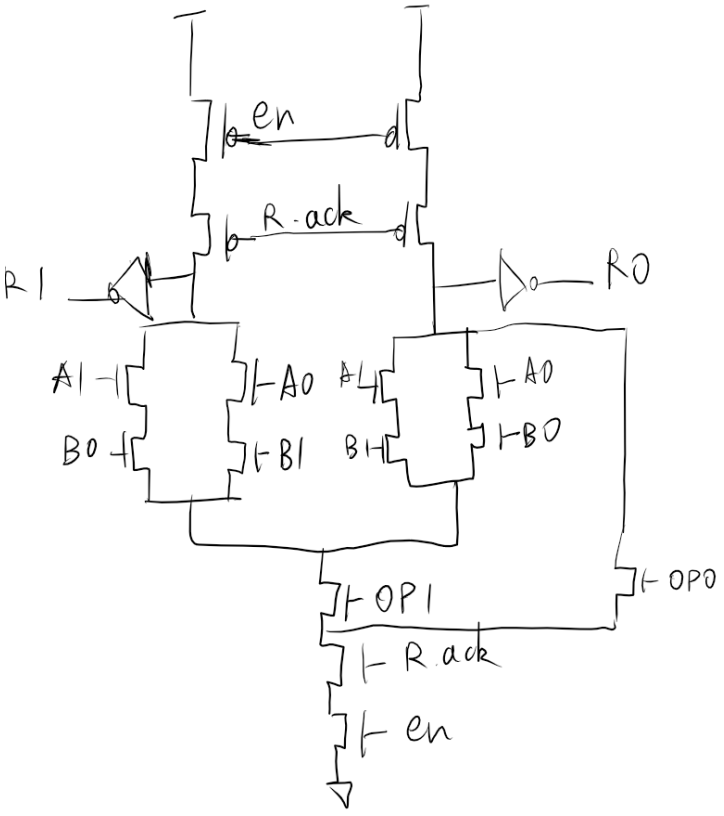
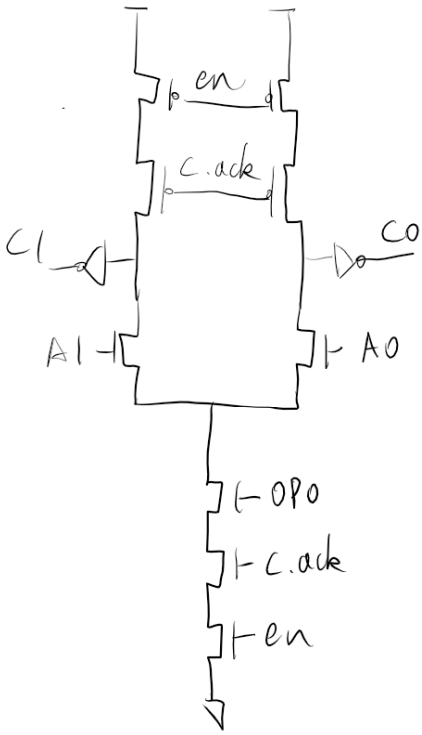
Part One

1. QDI circuit design







Part Two

2. Proteus Auto Pilot!

i. Execute command:
--config=[] (same as include)
--task=[rc,clockfree,encounter] (comma separated tasklist, or shortcuts [all|syn|spr])

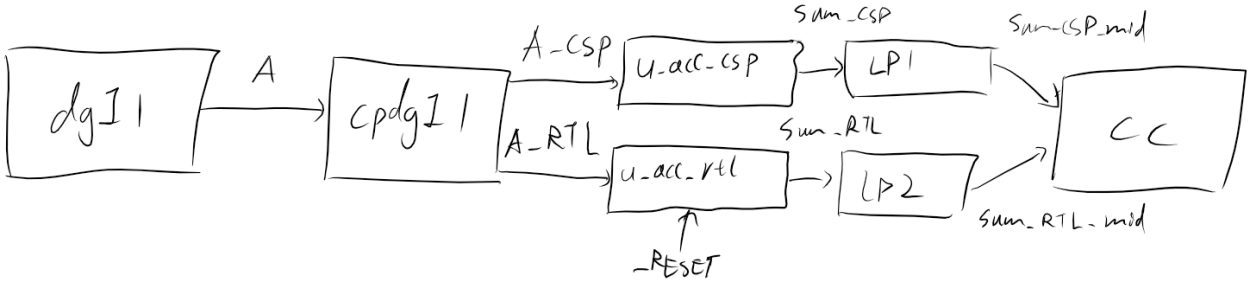
ii. What is the width of input and output channels?
Width is 16

iii. What is the channel coding (e1of2/e1of4/single rail)?
e1of2

iv. What is the difference between acc_csp.sv and acc_csp_gold.sv?
One is use the proteus design one is use SystemVerilogCSP

v.

vi. What is the type of channels used in this testbench?
e1ofN_M



vii. Which parameter controls the width of the channel (M or N)?
M

viii. Which command line executes rc? What is the input file name synthesized by rc? What is the output file of the rc and where is it located?

a. `time proteus-a --include=${design}.config --sv=1 --task=rc --force=1`
b. acc-csp.sv
c. acc.qdi.rc.out located at acc.qdi

ix. Which command line executes svc2rtl? What is the output file name of svc2rtl?
`time svc2rtl ${design}_csp.sv ${design}.rtl.sv > & /dev/null`
`Output file name acc.rtl.sv`

x.

xi. What are the major steps of Proteus synthesis?

a. `Check Syntax of The Input File Using vlog`
b. `Run svc2rtl`
c. `Format Verilog Output`
d. `Run RC`
e. `Run clockfree`
f. `Run encounter`
g. `Generate cosim wrapper`
h. `Read total number of gates in RC results`

xii. How many Send and Receives are used in the top-level module in acc.rtl.sv?
1 send 1 receive

xiii. When RC synthesizes the top-level in acc.rtl.sv module, it connects Vdd to the enable of all Send and Receive modules. Explain why?
Make send and receive open, more accurate RC synthesizes

xiv. Open rc.log file and determine the number of logic gates and tok_bufs.
64 logic gates, 16 token buffers

xv. Open the ClockFree report file and determine the number of added slack-matching buffers.
81

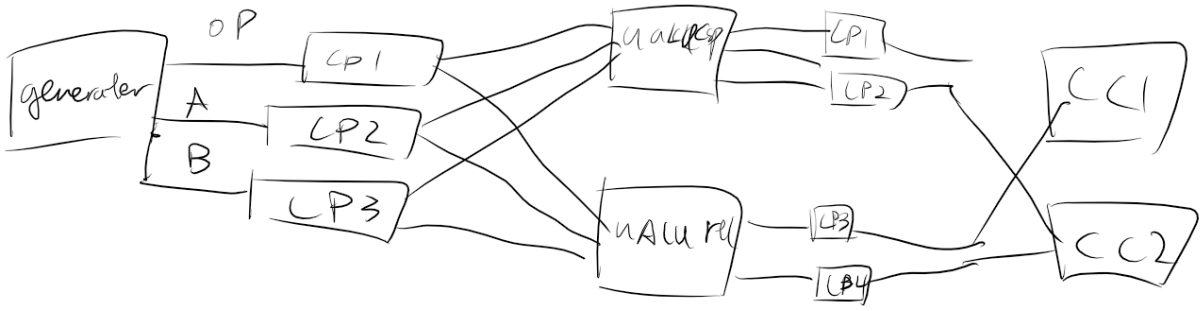
xvi. Open the output of rc, How many input and output ports does the top-level module have? How many SEND and RECEIVE gates are instantiated in this file?
`16 input 16 output`
`16 send 16 receive`

xvii. Explain the concept of cosim testbench. Which files do implement the cosim testbench. How many input and output ports does acc_cosim_wrapper module has?
Run.do file implement
`1 input 0 output`

3. Special ALU Design

i. How many Send and Receives are used in the top-level module in ALU.rtl.sv? Draw the block diagram of the top-level module as if the channels where 4-bit wide.

9 send 8 receive



ii. What logic function do you expect to be connected to the enable signals of the Receive modules connected to A, B and OP and Send modules connected to Y and Z.

VDD

iii. Open rc.log file and determine the number of logic gates and tok_bufs. What is the total area of your design reported by rc.

iv. Open the ClockFree log file and determine the number of added slack-matching buffers.

v. What is the cycle time of your design in post synthesis simulation?

4ns

Golden file works. But Proteus not success