EE552 Homework 6 (dual clock FIFO)

Huayu Fu
4745159848
4/6/2017

Objective

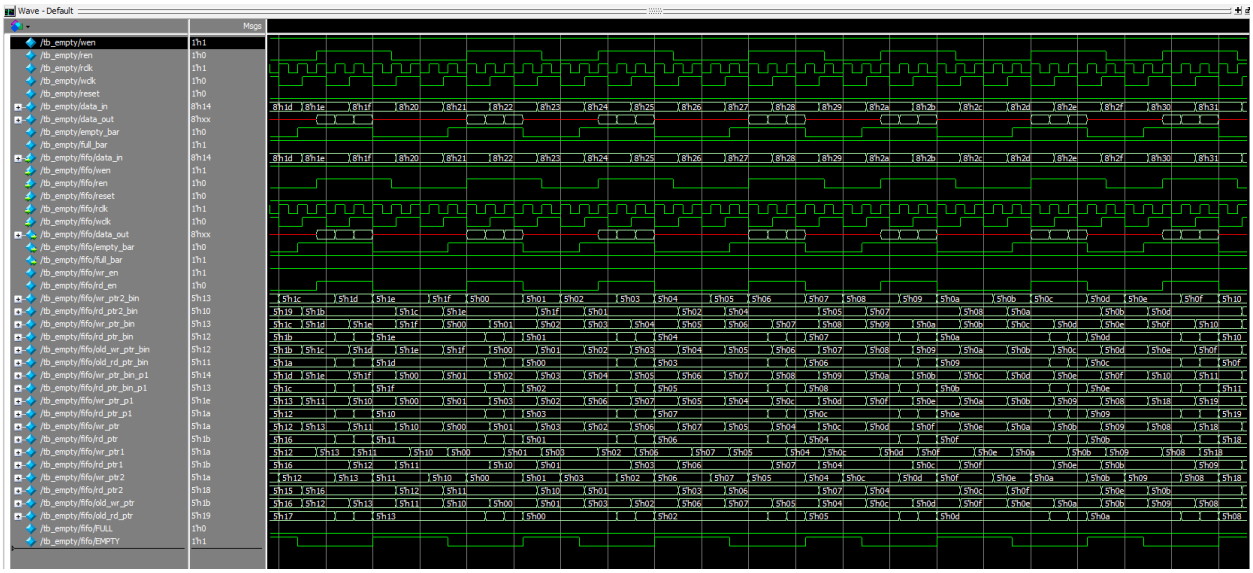
To design a dual clock FIFO with following features:

1) Use two Flip Flop synchronizer for rd_ptr and wr_ptr
2) Use gray code counter to implement the write/read pointer.
3) A dual_clk_FIFO 32 location 8 bit wide.

Simulations

cases:

1. 500Mhz for the reader side and 200Mhz for the writer side.



2. 100Mhz for the reader side and 400MHz for the writer side