EE577B Lab3 Report

Huayu Fu

10/3/2017

FIFO

a. timing slack

```
Point                                   Incr       Path
-------------------------------------------------------------
clock wclk (rise edge)                  0.00       0.00
clock network delay (ideal)             0.00       0.00
input external delay                    1.00       1.00 f
reset (in)                              0.00       1.00 f
U776/Y (INVX1)                          0.13       1.13 r
U698/Y (AND2X1)                         0.03       1.15 r
U699/Y (INVX1)                          0.05       1.20 f
U654/Y (AND2X1)                         0.06       1.26 f
U560/Y (AND2X1)                         0.05       1.31 f
U561/Y (INVX1)                          0.00       1.31 r
U352/Y (OAI21X1)                        0.01       1.32 f
rd_ptr_reg[0]/D (DFFPOSX1)              0.00       1.32 f
data arrival time                                  1.32
clock rclk (rise edge)                  2.10       2.10
clock network delay (ideal)             0.00       2.10
rd_ptr_reg[0]/CLK (DFFPOSX1)            0.00       2.10 r
library setup time                      -0.06      2.04
data required time                                 2.04
-------------------------------------------------------------
data required time                                 2.04
data arrival time                                  -1.32
-------------------------------------------------------------
slack (MET)                                        0.73
Startpoint: get (input port clocked by wclk)
Endpoint: data_out[0]
          (output port clocked by wclk)
Path Group: wclk
Path Type: max
Point                                   Incr       Path
-------------------------------------------------------------
clock wclk (rise edge)                  0.00       0.00
clock network delay (ideal)             0.00       0.00
input external delay                    1.00       1.00 r
get (in)                                0.00       1.00 r
U913/Y (AND2X2)                         0.07       1.07 r
U744/Y (AND2X1)                         0.03       1.10 r
data_out[0] (out)                       0.00       1.10 r
data arrival time                                  1.10

clock wclk (rise edge)                  2.10       2.10
clock network delay (ideal)             0.00       2.10
output external delay                   -1.00      1.10
data required time                                 1.10
```

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data required time 1.10

data arrival time -1.10

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slack (MET) 0.00

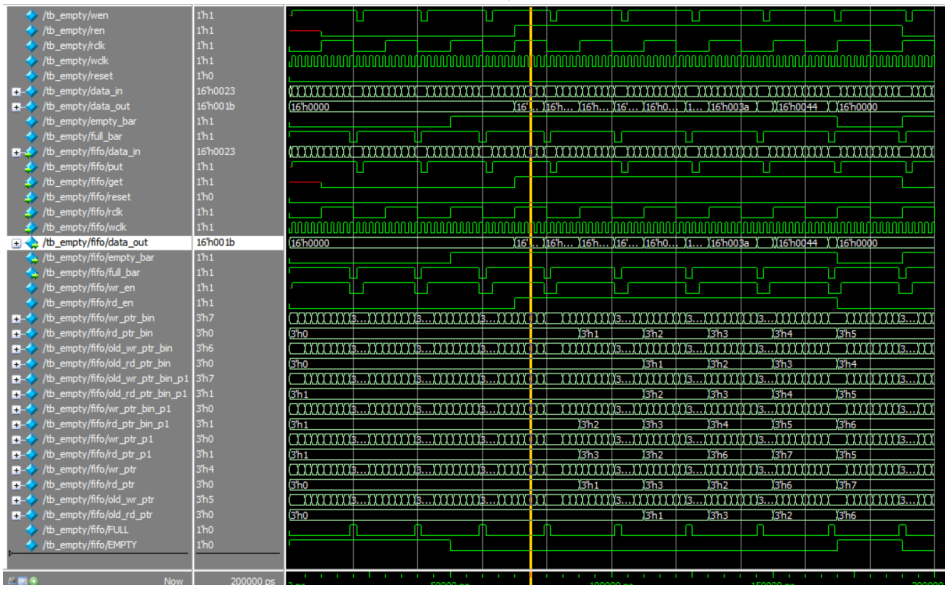
b. area

```
****************************************
Report : area
Design : FIFO_2clk
Version: F-2011.09-SP2
Date   : Tue Oct  3 22:27:33 2017
****************************************
Library(s) Used:
   gscl45nm (File: /home/scf-22/ee577/NCSU45PDK/FreePDK45/osu_soc/lib/files/gscl45nm.db)
Number of ports:                23
Number of nets:                916
Number of cells:               869
Number of combinational cells:          703
Number of sequential cells:             160
Number of macros:                       0
Number of buf/inv:                      214
Number of references:                   22

Combinational area:      1901.134270
Noncombinational area:   1276.495972
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:         3177.630241
Total area:              undefined
```

c. The waveform shows when the clock speed difference is more than the fifo size, unexpected situation would occure: which is after the fifo is full, it still write.



LIFO

a. slack

```
Startpoint: X (input port clocked by clk)
Endpoint: Y[1] (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                   Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                   0.00       0.00
clock network delay (ideal)             0.00       0.00
input external delay                    1.00       1.00 r
X (in)                                  0.00       1.00 r
U20/Y (INVX1)                           0.02       1.02 f
U10/Y (AOI22X1)                         0.03       1.05 r
U17/Y (BUFX2)                           0.04       1.08 r
U9/Y (OAI21X1)                          0.01       1.09 f
Y[1] (out)                              0.00       1.09 f
data arrival time                                  1.09

clock clk (rise edge)                   2.10       2.10
clock network delay (ideal)             0.00       2.10
output external delay                  -1.00       1.10
data required time                                 1.10
-----------------------------------------------------------
data required time                                 1.10
data arrival time                                 -1.09
-----------------------------------------------------------
slack (MET)                                        0.01
```

b. area

```
****************************************
Report : area
Design : fsm
Version: F-2011.09-SP2
Date   : Sat Sep 23 03:58:39 2017
****************************************
Library(s) Used:
    gscl45nm (File: /home/scf-22/ee577/NCSU45PDK/FreePDK45/osu_soc/lib/files/gscl45nm.db)
Number of ports:                  5
Number of nets:                  19
Number of cells:                 16
Number of combinational cells:           14
Number of sequential cells:               2
Number of macros:                         0
Number of buf/inv:                        7
Number of references:                     9
```

Combinational area: 32.381699
Noncombinational area: 15.956200
Net Interconnect area: undefined (No wire load specified)

Total cell area: 48.337899
Total area: undefined

TCAM

a. Timing

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : TCAM
Version: F-2011.09-SP2
Date   : Tue Oct  3 20:07:25 2017
****************************************

Operating Conditions: typical   Library: gscl45nm
Wire Load Model Mode: top

  Startpoint: DIN[13] (input port clocked by clk)
  Endpoint: j_reg[1] (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                   Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   0.00       0.00
  clock network delay (ideal)             0.00       0.00
  input external delay                    1.00       1.00 r
  DIN[13] (in)                            0.00       1.00 r
  U1918/Y (AND2X1)                        0.04       1.04 r
  U1919/Y (INVX1)                         0.03       1.07 f
  U293/Y (XOR2X1)                         0.04       1.11 r
  U290/Y (NAND3X1)                        0.02       1.13 f
  U1757/Y (BUFX2)                         0.03       1.16 f
  U285/Y (NOR3X1)                         0.05       1.21 r
  U2254/Y (AND2X1)                        0.04       1.25 r
  U1228/Y (AND2X1)                        0.06       1.30 r
  U130/Y (NAND3X1)                        0.03       1.33 f
  U1571/Y (BUFX2)                         0.03       1.36 f
  U129/Y (AOI22X1)                        0.02       1.39 r
  U1349/Y (BUFX2)                         0.04       1.42 r
  U128/Y (OAI21X1)                        0.01       1.44 f
  U127/Y (NAND3X1)                        0.03       1.47 r
```

U2017/Y (BUFX2)	0.05	1.51	r
U2248/Y (INVX1)	0.04	1.55	f
U120/Y (NOR3X1)	0.05	1.60	r
U119/Y (AOI21X1)	0.02	1.62	f
U1827/Y (BUFX2)	0.04	1.65	f
U117/Y (NAND3X1)	0.03	1.69	r
U1367/Y (BUFX2)	0.03	1.72	r
U116/Y (OAI21X1)	0.01	1.73	f
U2269/Y (INVX1)	0.01	1.74	r
U2208/Y (AND2X1)	0.03	1.77	r
U2209/Y (INVX1)	0.02	1.79	f
U109/Y (NAND3X1)	0.03	1.83	r
U2207/Y (BUFX2)	0.06	1.89	r
U1516/Y (AND2X1)	0.03	1.92	r
U1517/Y (INVX1)	0.02	1.93	f
U107/Y (OAI21X1)	0.03	1.97	r
U1537/Y (AND2X1)	0.04	2.01	r
U1538/Y (INVX1)	0.02	2.03	f
U103/Y (NAND3X1)	0.03	2.06	r
U1368/Y (BUFX2)	0.03	2.10	r
U102/Y (OAI21X1)	0.01	2.11	f
U2266/Y (INVX1)	0.01	2.12	r
U2011/Y (AND2X1)	0.03	2.15	r
U2012/Y (INVX1)	0.02	2.17	f
U95/Y (NAND3X1)	0.03	2.20	r
U2010/Y (BUFX2)	0.05	2.25	r
U1520/Y (AND2X1)	0.03	2.27	r
U1521/Y (INVX1)	0.02	2.29	f
U93/Y (OAI21X1)	0.03	2.33	r
U1561/Y (AND2X1)	0.04	2.36	r
U1562/Y (INVX1)	0.02	2.38	f
U88/Y (NAND3X1)	0.03	2.42	r
U1369/Y (BUFX2)	0.03	2.45	r
U87/Y (OAI21X1)	0.01	2.46	f
U2270/Y (INVX1)	0.01	2.47	r
U2212/Y (AND2X1)	0.03	2.50	r
U2213/Y (INVX1)	0.02	2.52	f
U80/Y (NAND3X1)	0.03	2.56	r
U2211/Y (BUFX2)	0.06	2.62	r
U1522/Y (AND2X1)	0.03	2.65	r
U1523/Y (INVX1)	0.02	2.67	f
U78/Y (OAI21X1)	0.03	2.70	r
U1539/Y (AND2X1)	0.04	2.74	r
U1540/Y (INVX1)	0.02	2.76	f
U73/Y (NAND3X1)	0.03	2.79	r
U1370/Y (BUFX2)	0.03	2.83	r
U72/Y (OAI21X1)	0.01	2.84	f
U2264/Y (INVX1)	0.01	2.85	r

U2024/Y (AND2X1)	0.03	2.88 r
U2025/Y (INVX1)	0.02	2.90 f
U65/Y (NAND3X1)	0.03	2.93 r
U2023/Y (BUFX2)	0.05	2.98 r
U1526/Y (AND2X1)	0.03	3.01 r
U1527/Y (INVX1)	0.02	3.03 f
U63/Y (OAI21X1)	0.03	3.07 r
U1563/Y (AND2X1)	0.04	3.10 r
U1564/Y (INVX1)	0.02	3.12 f
U58/Y (NAND3X1)	0.03	3.15 r
U1371/Y (BUFX2)	0.03	3.19 r
U57/Y (OAI21X1)	0.01	3.20 f
U2271/Y (INVX1)	0.01	3.21 r
U2205/Y (AND2X1)	0.03	3.24 r
U2206/Y (INVX1)	0.02	3.26 f
U50/Y (NAND3X1)	0.03	3.29 r
U2204/Y (BUFX2)	0.05	3.35 r
U2232/Y (INVX1)	0.03	3.38 f
U41/Y (AOI22X1)	0.05	3.43 r
U1231/Y (BUFX2)	0.03	3.46 r
U2268/Y (INVX1)	0.02	3.48 f
U1541/Y (AND2X1)	0.03	3.51 f
U1542/Y (INVX1)	0.00	3.51 r
U37/Y (NAND3X1)	0.02	3.53 f
U1556/Y (BUFX2)	0.03	3.56 f
U35/Y (NAND3X1)	0.03	3.59 r
U1290/Y (BUFX2)	0.03	3.62 r
U2253/Y (INVX1)	0.02	3.64 f
U1935/Y (OR2X1)	0.05	3.69 f
U1936/Y (INVX1)	0.01	3.70 r
U32/Y (NAND3X1)	0.01	3.71 f
U1826/Y (BUFX2)	0.04	3.75 f
U30/Y (NOR3X1)	0.04	3.79 r
U29/Y (OAI21X1)	0.03	3.81 f
U2109/Y (AND2X1)	0.04	3.85 f
U2110/Y (INVX1)	0.04	3.90 r
U1230/Y (OR2X1)	0.06	3.96 r
U17/Y (AOI21X1)	0.02	3.98 f
U1530/Y (BUFX2)	0.03	4.01 f
U16/Y (AOI21X1)	0.01	4.02 r
U1291/Y (BUFX2)	0.03	4.06 r
U2274/Y (INVX1)	0.01	4.07 f
j_reg[1]/D (DFFPOSX1)	0.00	4.07 f
data arrival time	4.07	
clock clk (rise edge)	5.00	5.00
clock network delay (ideal)	0.00	5.00
j_reg[1]/CLK (DFFPOSX1)	0.00	5.00 r

```
  library setup time                -0.06      4.94
  data required time                           4.94
  ---------------------------------------------------------
  data required time                           4.94
  data arrival time                           -4.07
  ---------------------------------------------------------
  slack (MET)                                  0.87
```

b. Area

```
****************************************
Report : area
Design : TCAM
Version: F-2011.09-SP2
Date   : Tue Oct  3 20:07:25 2017
****************************************
Library(s) Used:
   gscl45nm (File: /home/scf-22/ee577/NCSU45PDK/FreePDK45/osu_soc/lib/files/gscl45nm.db)
Number of ports:                  24
Number of nets:                 2124
Number of cells:                1923
Number of combinational cells:          1735
Number of sequential cells:              188
Number of macros:                  0
Number of buf/inv:                858
Number of references:              14
Combinational area:      3909.268898
Noncombinational area:    1924.599339
Net Interconnect area:      undefined  (No wire load specified)
Total cell area:         5833.868237
Total area:              undefined
```