# EE 477 Laboratory #2
# Part 1

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11/12/2016

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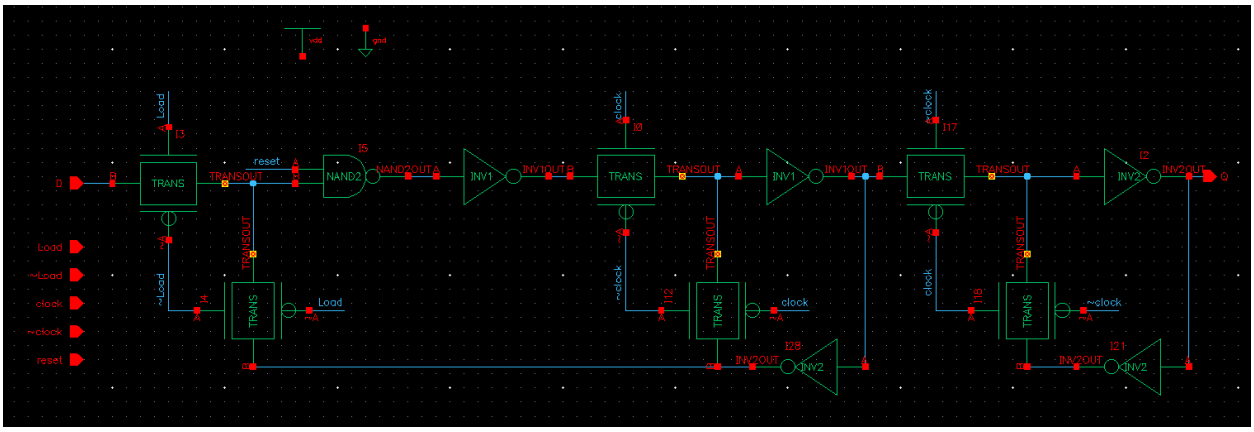
1. Description of the flip-flop

    As required, the flip flop is negative edge triggered, therefore, the first latch load data D when clock is HIGH, recirculate data when clock is LOW; and the second latch load data when the clock is LOW, recirculate data when clock is HIGH.

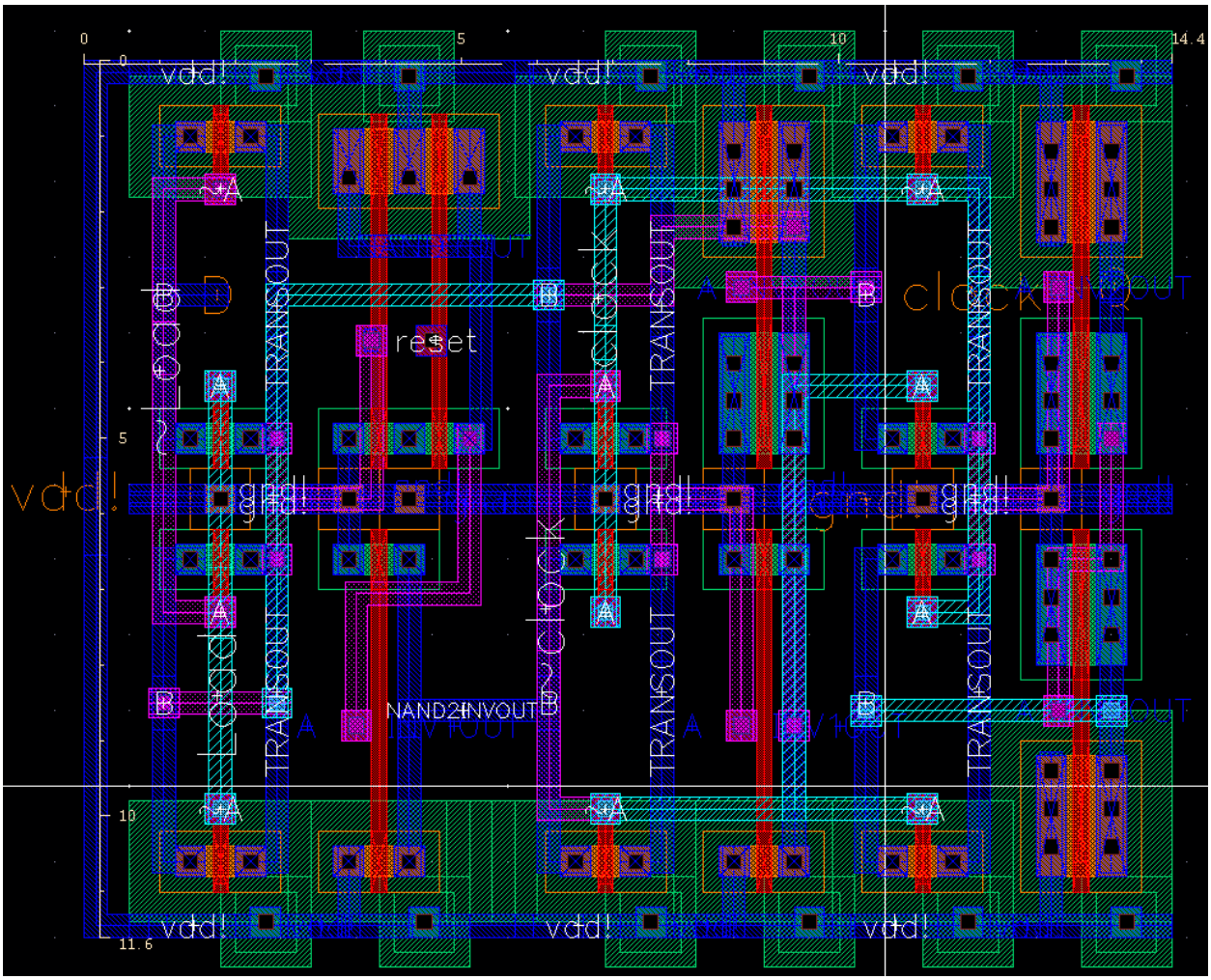
    To enable the synchronously reset, reset must be placed before clocked mux in latch1. I have a 2 input NAND connected to the data D and reset as input, and output to the input of an inverter, then drive the output of inverter to the input clocked mux in latch1. And the reset is active LOW.

    For the load function, I placed a mux at the begging of data D input. When Load is HIGH, the output of mux is the Data D; when Load is LOE, the output is the feedback of latch1. And the load has lower priority than reset.

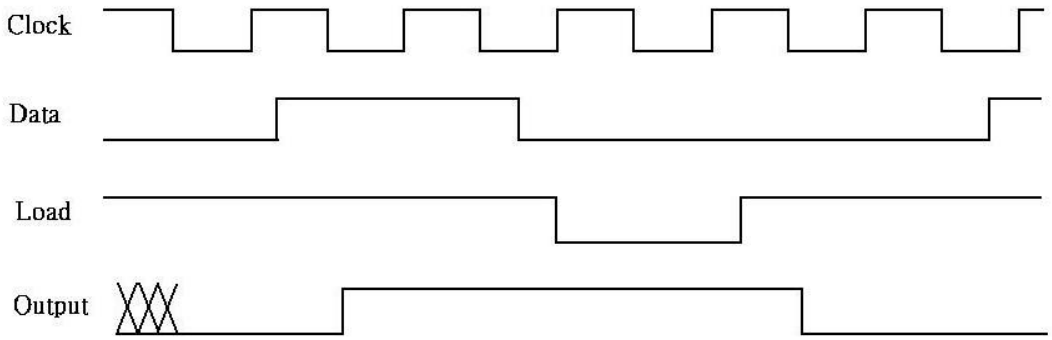
2. Gate level circuit diagram.



3. Flip-Flop layout.

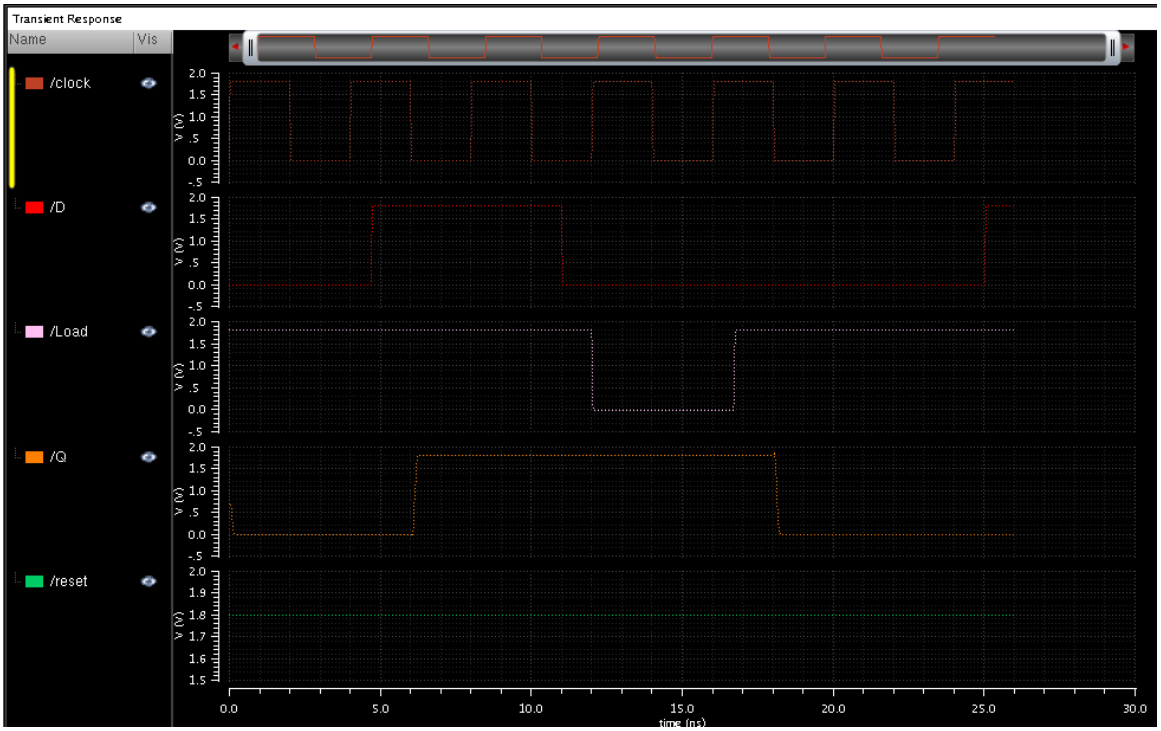


4. Description of all the simulation experiments
   A. The test with the given waveform.

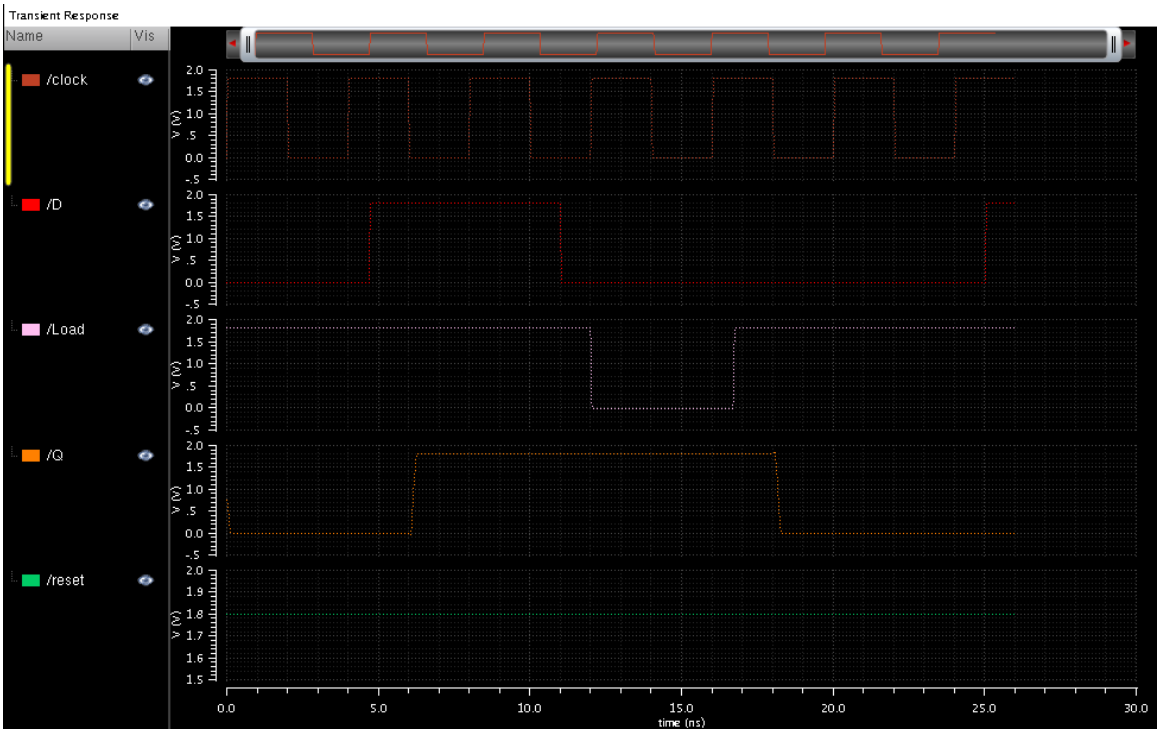



   B. Reset test:
      Start with the clock HIGH, D HIGH and Load HIGH and then lower the clock. And reset is enabled. The correct result would be the Q does not change as the D changes, the output is constant 0 V.
   C. Load test:
      Start with Load HIGH, data D HIGH, reset disabled, and then drive Load to LOW, after load to low drive D to LOW, then drive Load to high. If the circuit is correct, Q will not change when Load is LOW.
   D. Find the minimal clock period:
      Have a fixed sequence of input and adjust clock speed, by using the bisection method. Until the clock speed reaches the smallest clock with correct output, which means the output changes is less than 2 clock cycle after the input changes, we can find the minimal clock speed.
   E. Measure the setup time:
      Enable the load, disable the reset. And start with D LOW, drive D to HIGH at the time of half clock period before the clock falling edge. Then start the “bisection method”, if the output Q correct, cut the time in half, if not correct, choose the mid-point of the time between recent success try and recent failed try. After get the time for Q from LOW to HIGH, then test if the time period works for D form HIGH to LOW, if output Q correct, the time we get is the setup time.

5. Waveforms
    A. Given Waveform
        a. Schematic Simulation

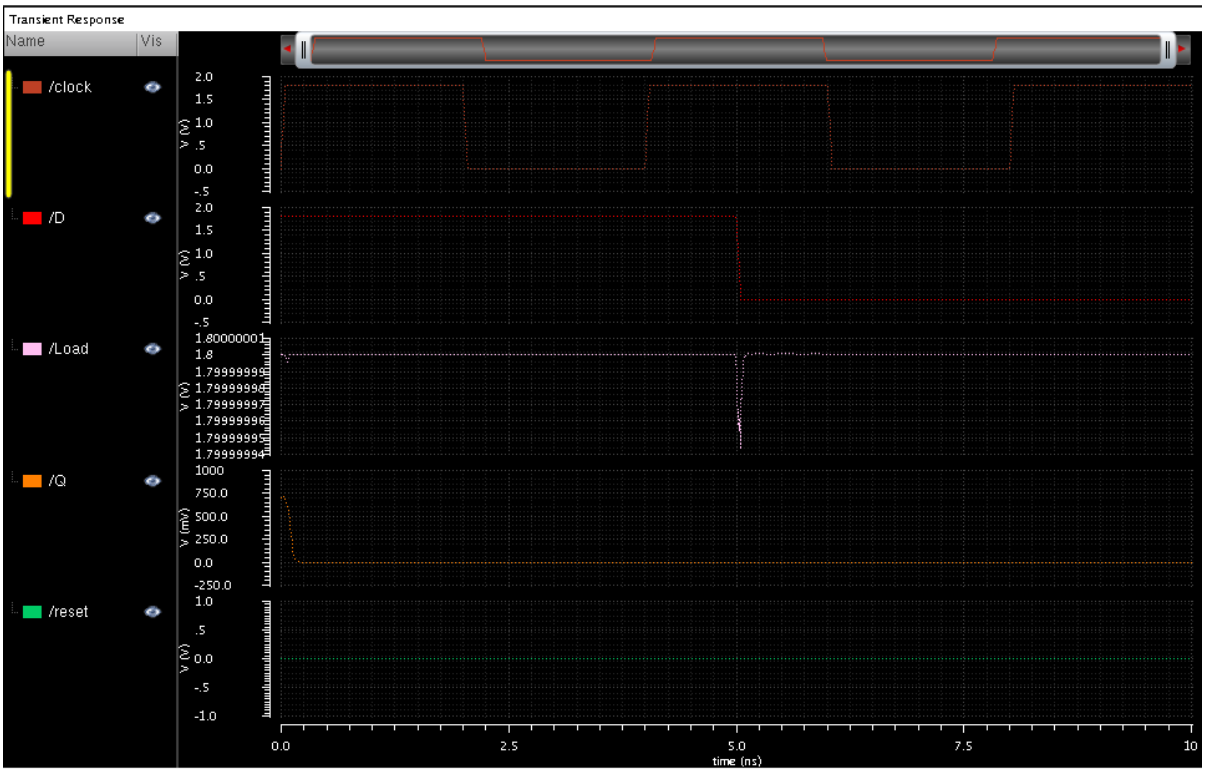



        b. Layout Simulation

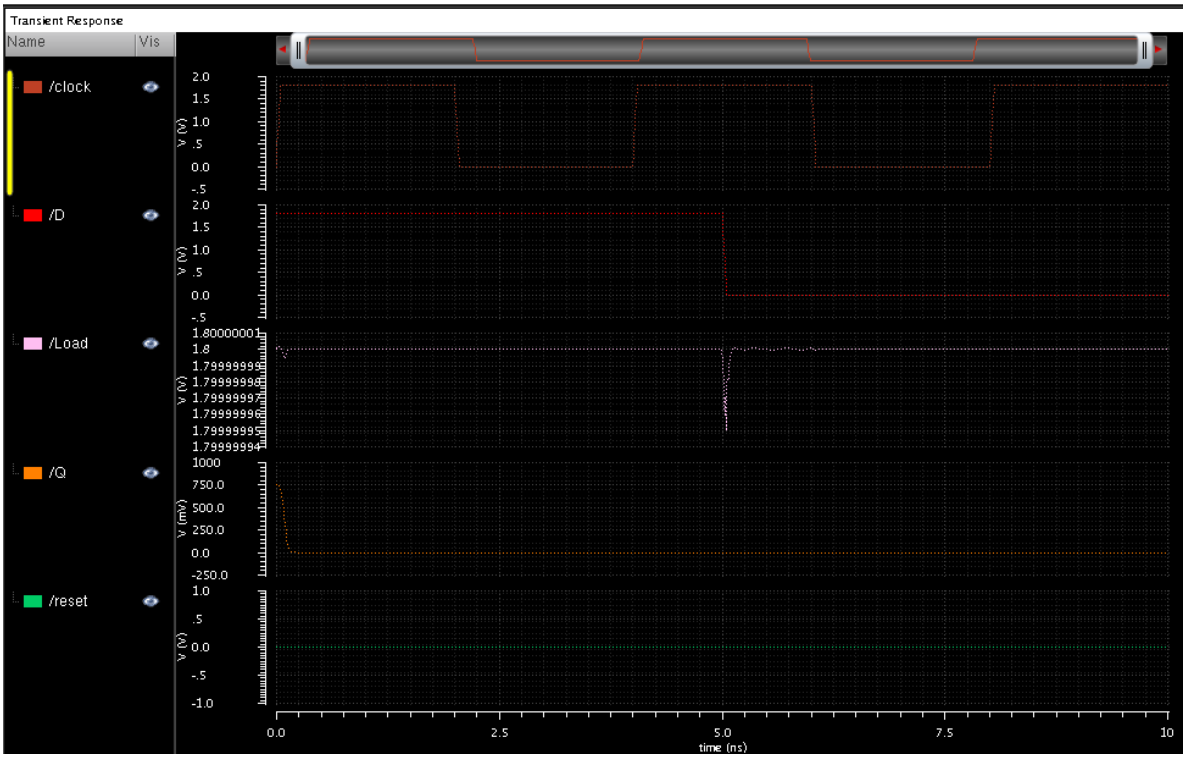


B. Reset test

a. Schematic Simulation

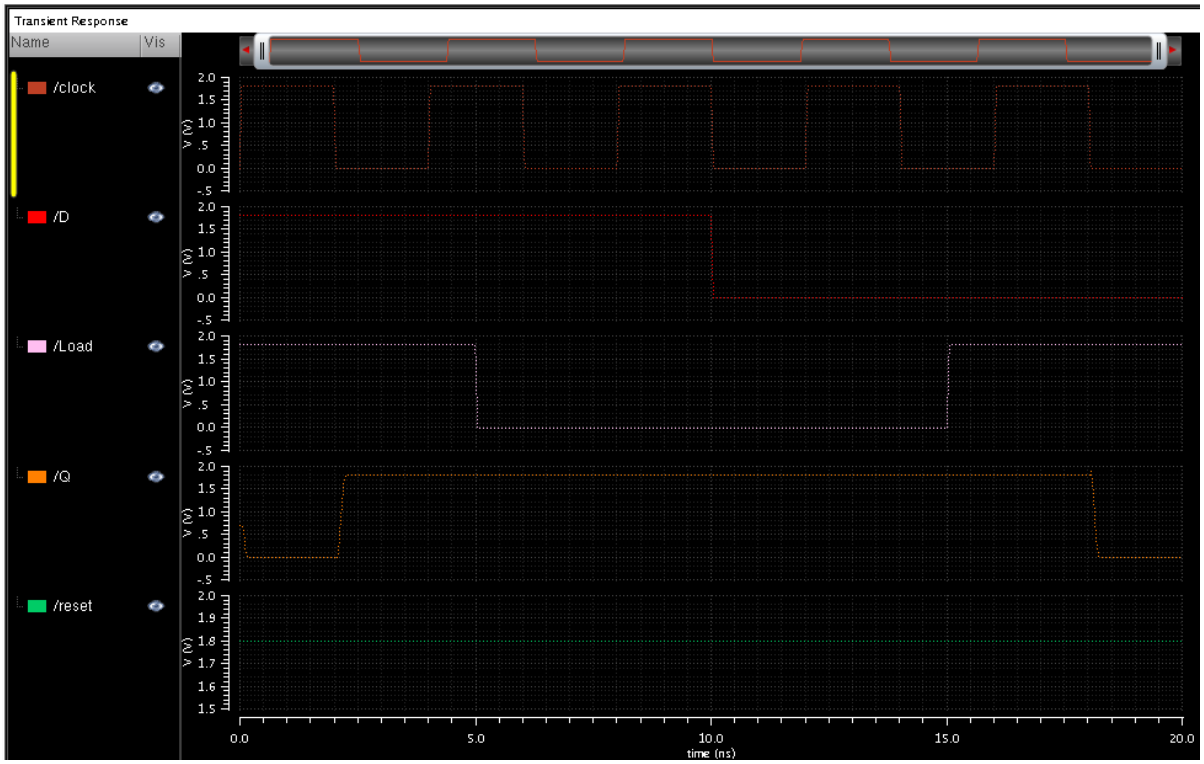



b. Layout Simulation

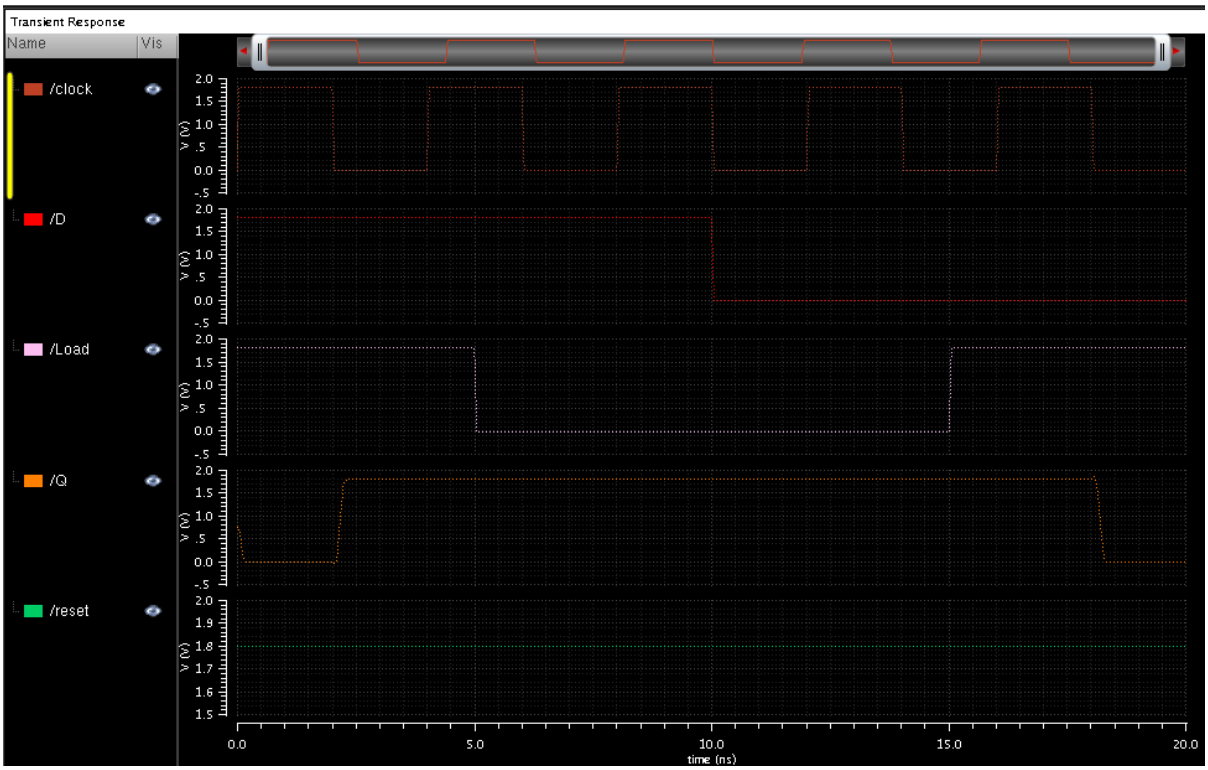


C. Load test

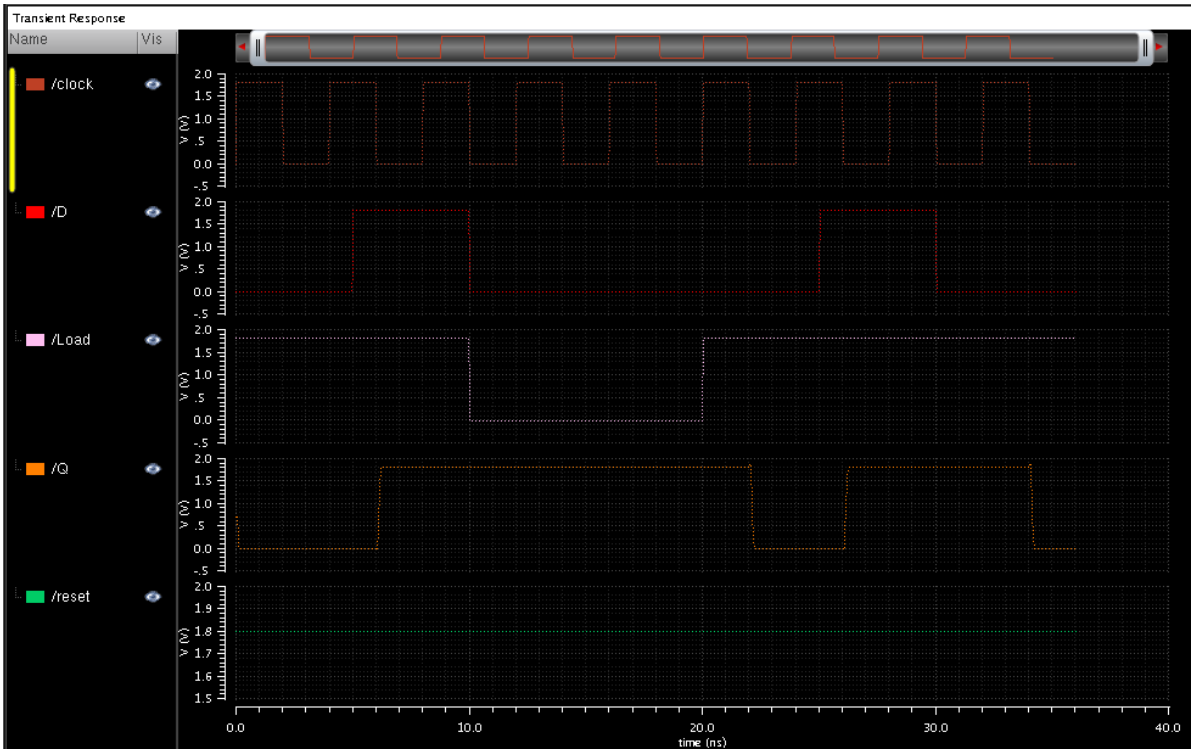
a. Schematic Simulation



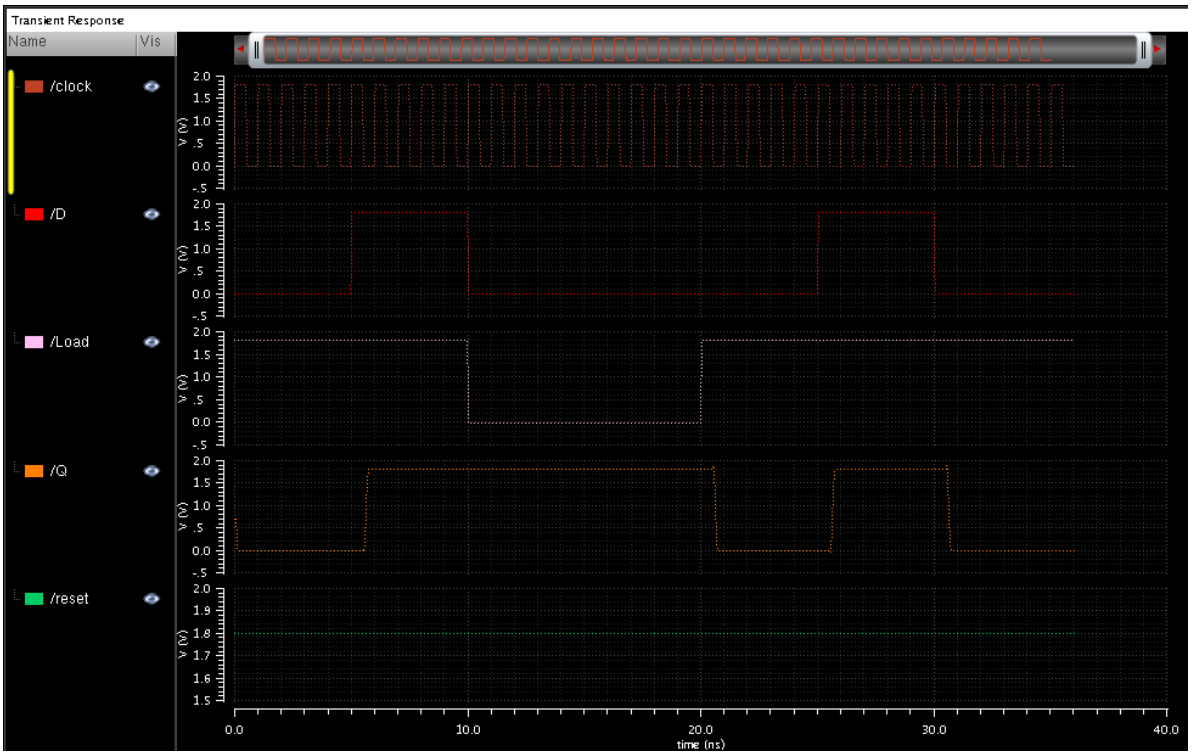

b. Layout Simulation



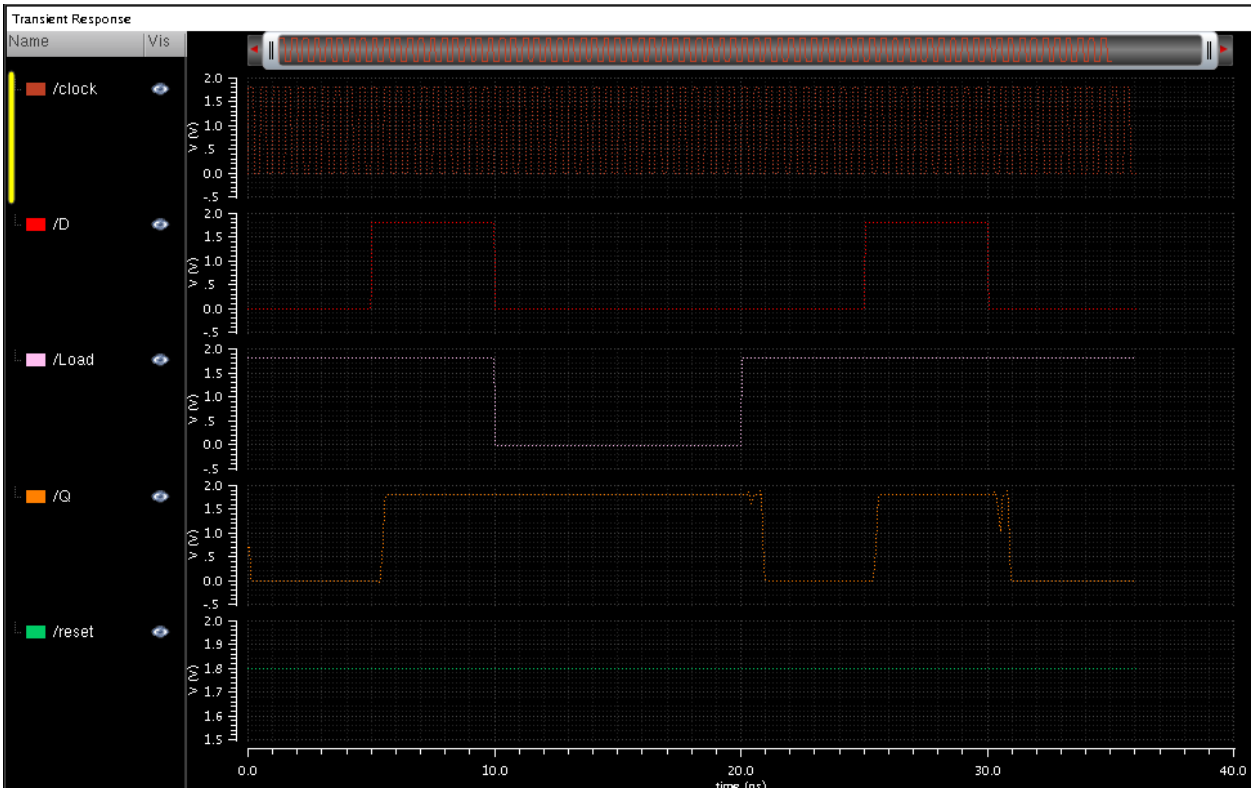
D. Minimum Clock
   a. Schematic Simulation
      1. 4n: success



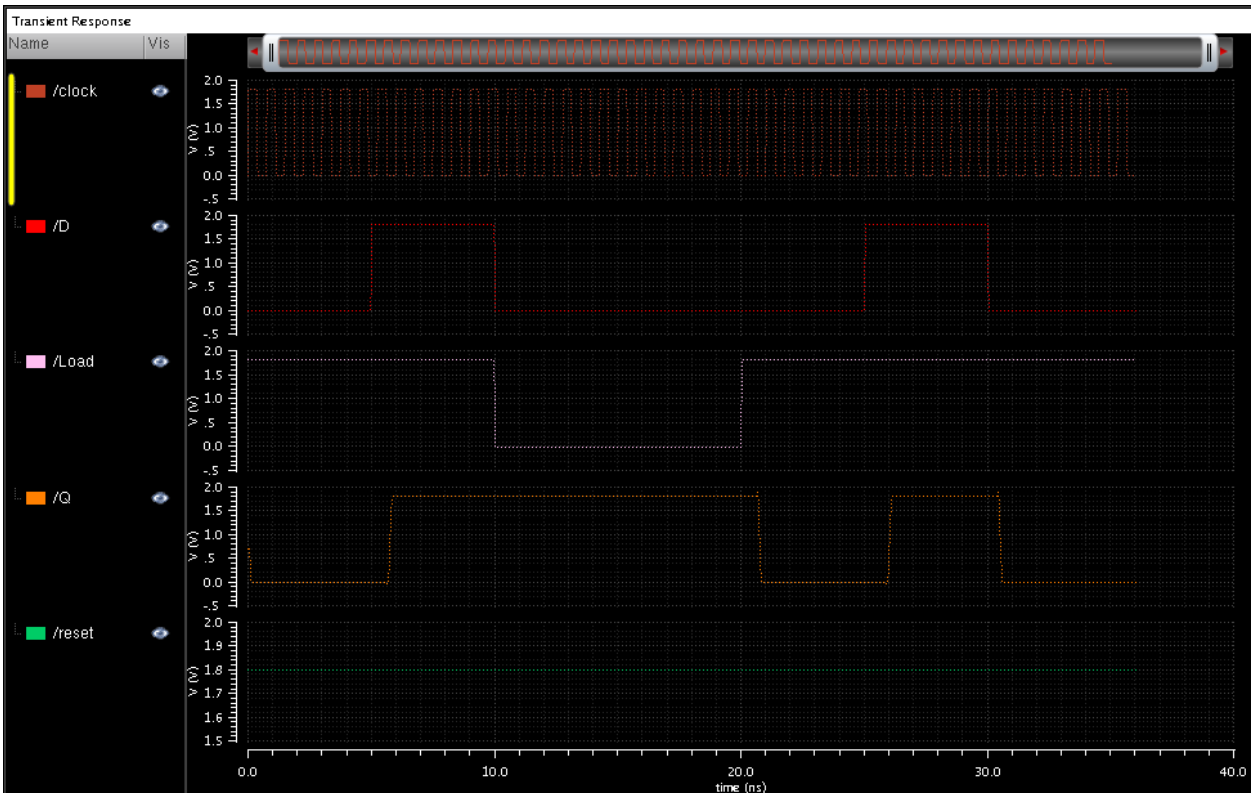

      2. 1ns: success



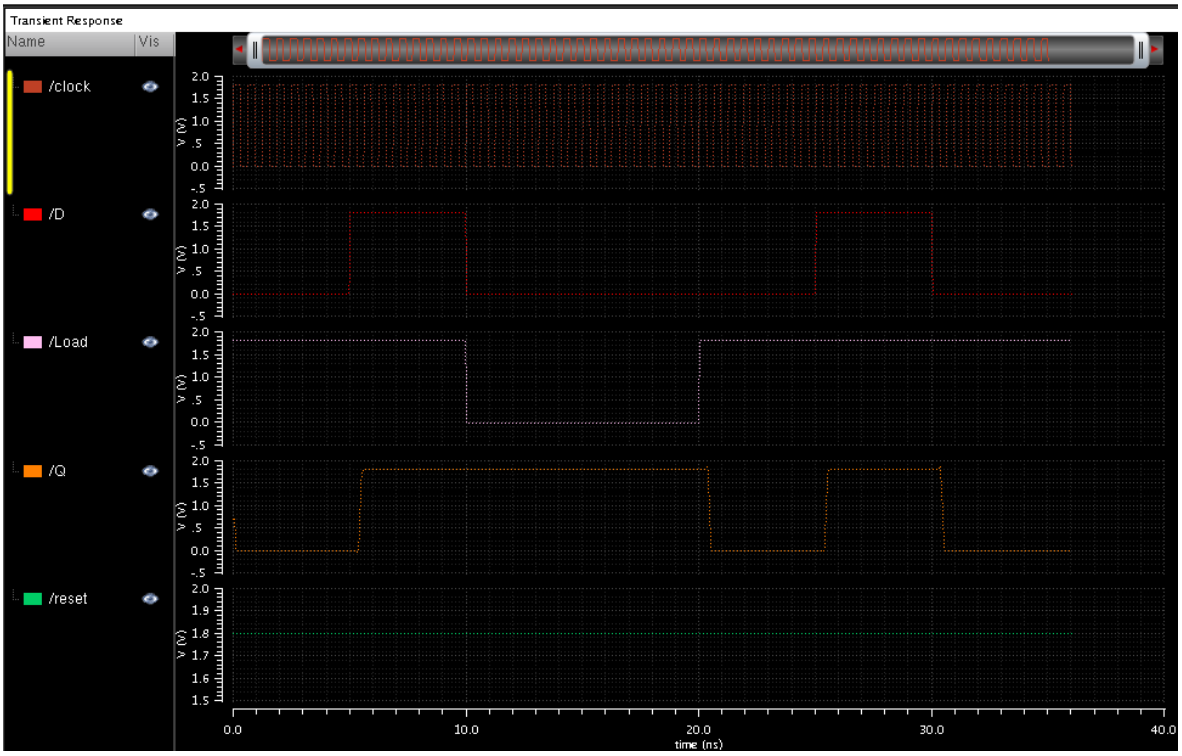
3. 0.5n: failed, used 2 clock to fall.



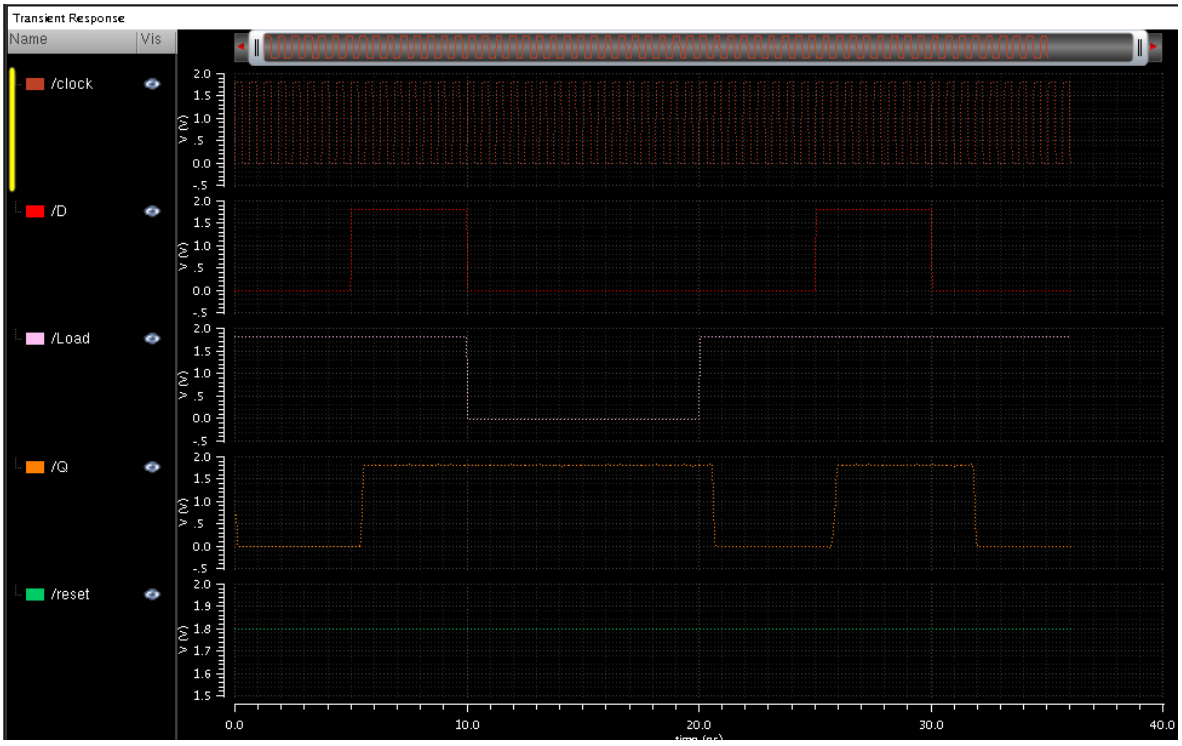

4. 0.75n: success



5. 0.625n: success



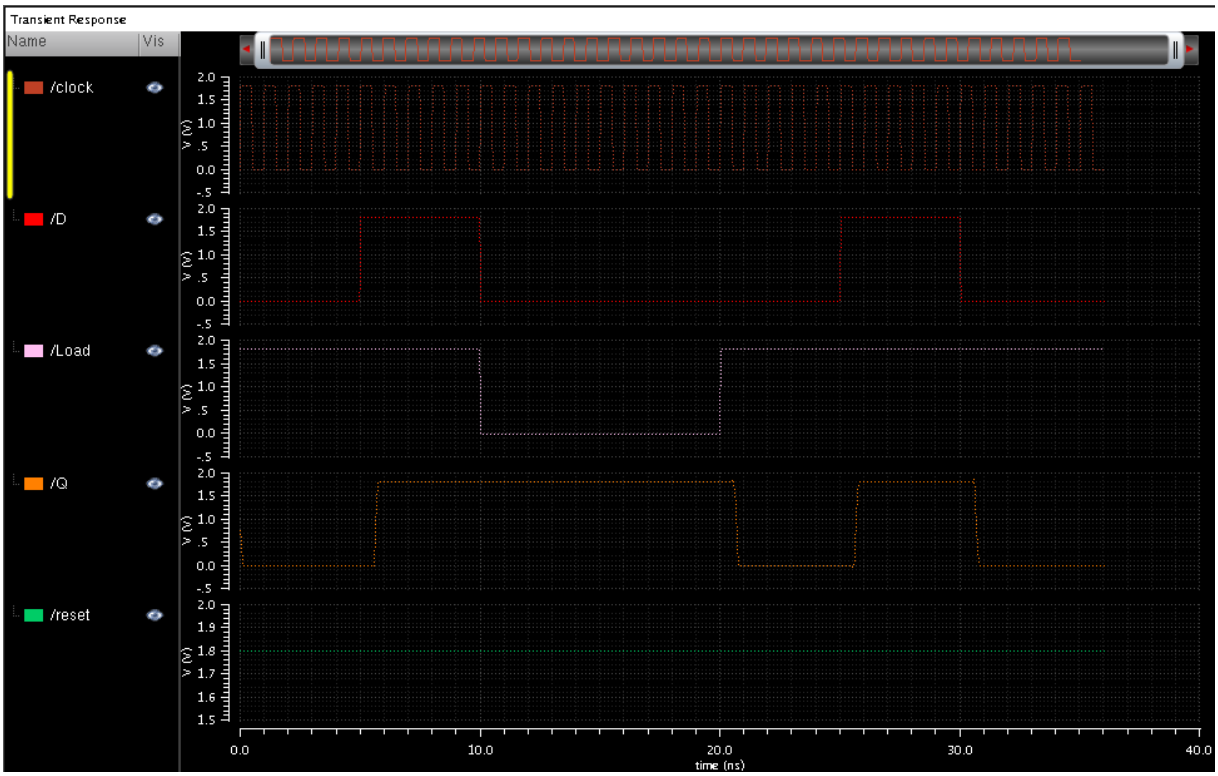

6. 0.5625n: failed, used more than 2 clock to fall.



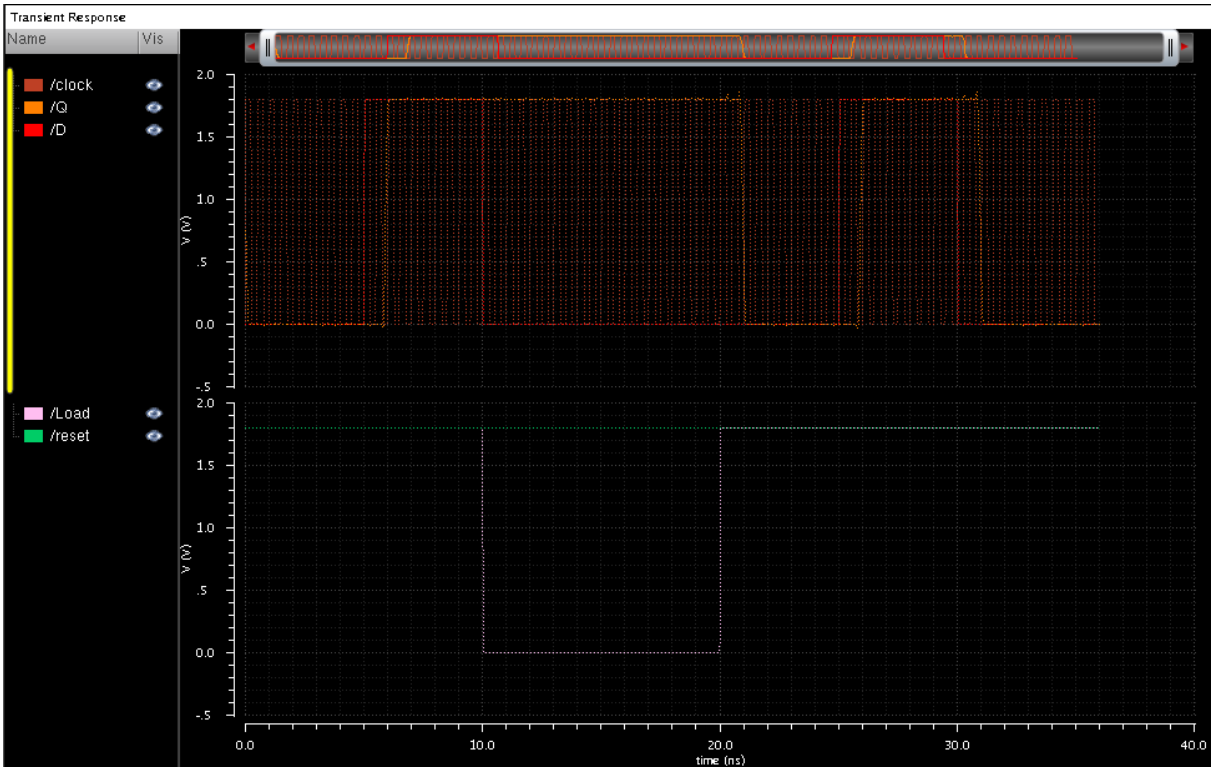

Therefore, the minimal clock speed from layout simulation is 0.625ns.

b. Layout simulation.

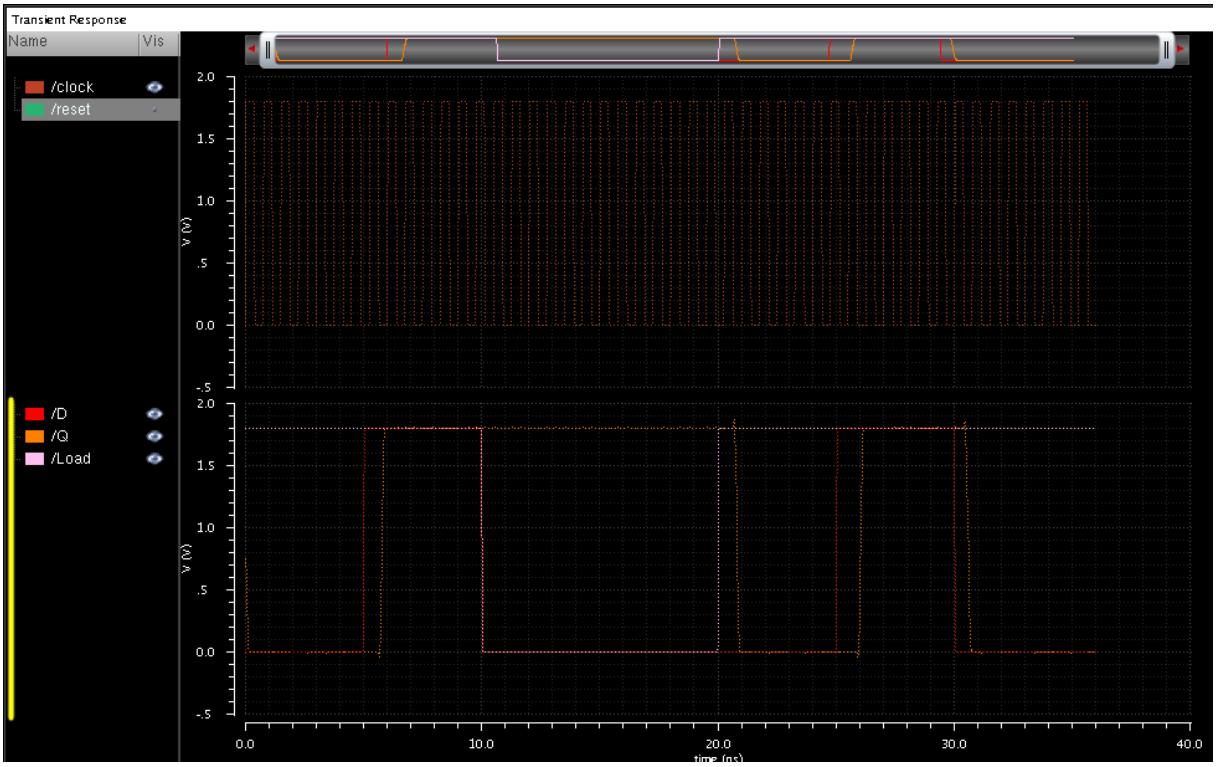
1. 1n: success



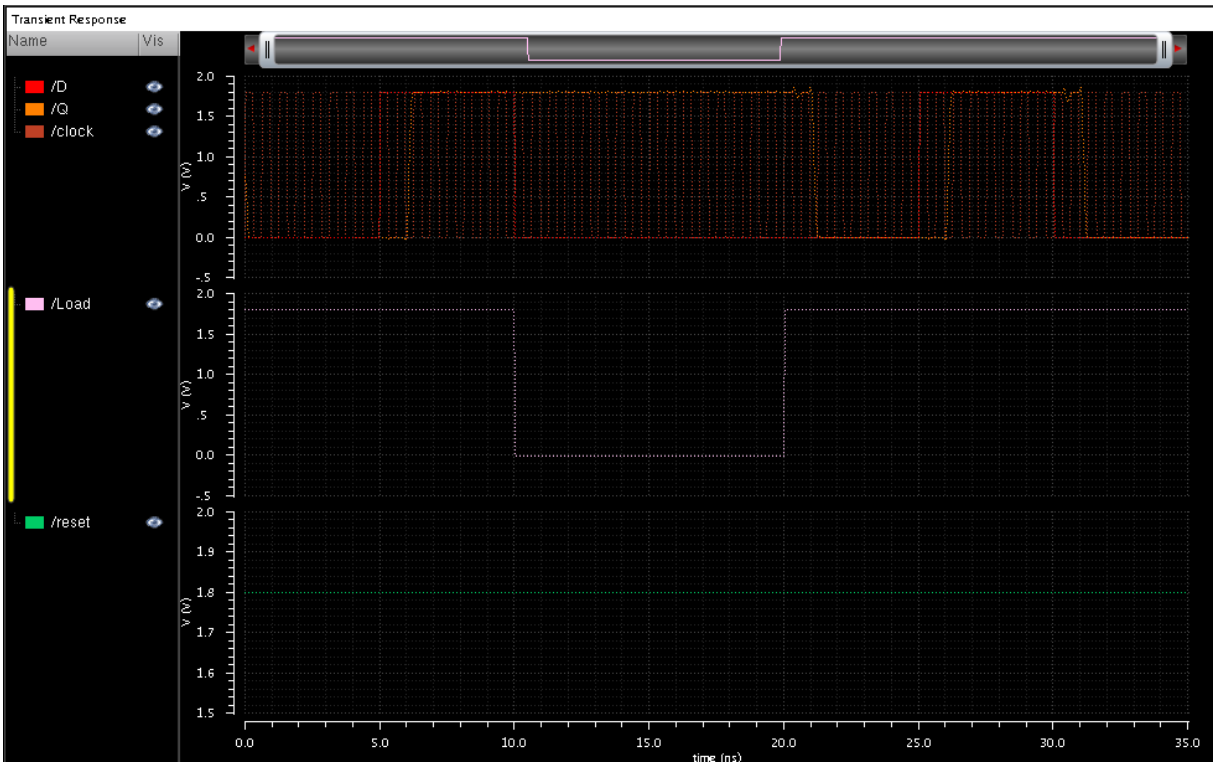

2. 0.5n: failed, 2 clock to fall.



3. 0.75n: success.




4. 0.625n: failed. More than 2 clock to rise and fall.

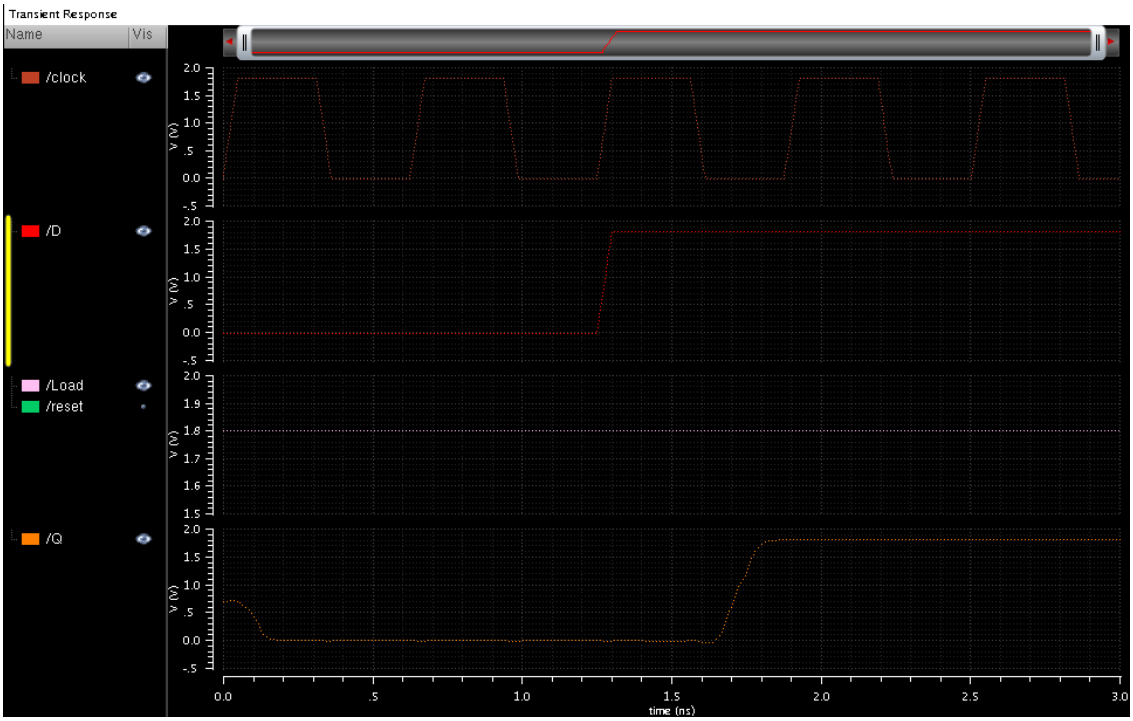



Therefore, the minimal clock speed from layout simulation is 0.75ns.

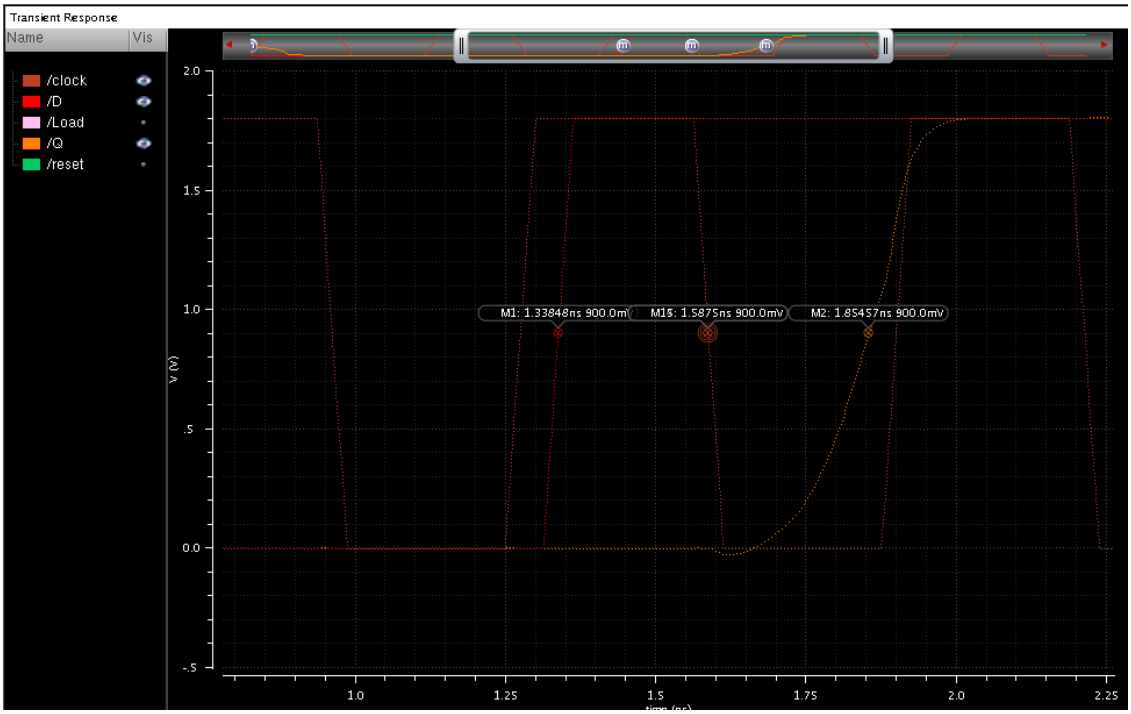
E. Setup time measurement

a. Schematic

1. Schematic Simulation for the first try, with the clock speed of 0.625ns

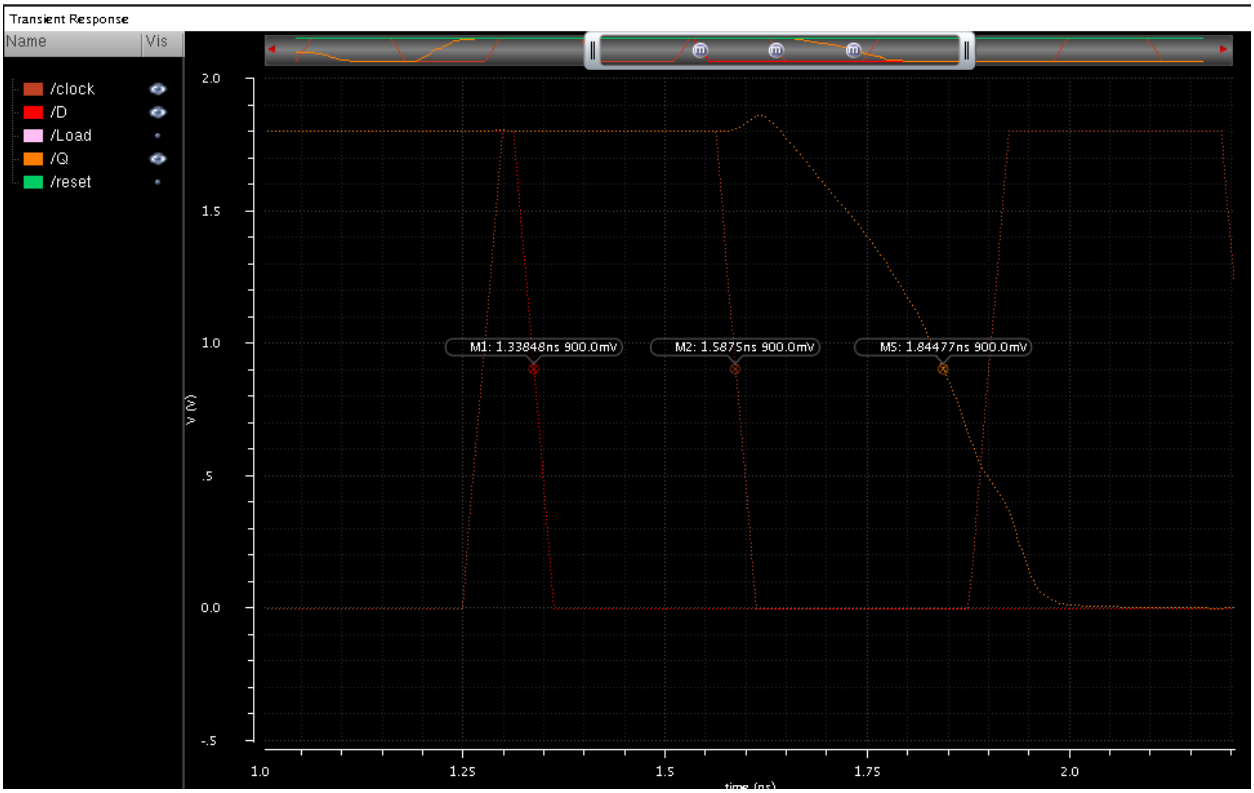



2. Founded minimal setup time for rising.




Setup time= 1.5875-1.33848=0.24902 ns; Vin to Vout time=1.85157-1.33848=0.51309ns

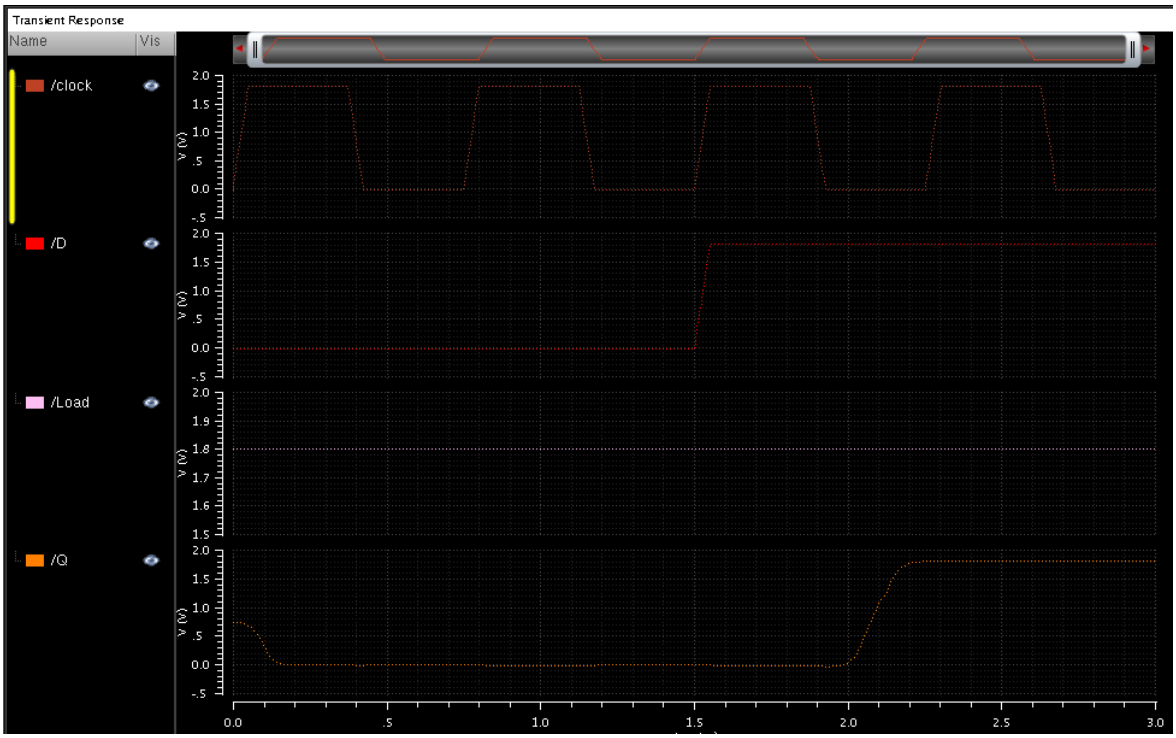
3. Redo the simulation for falling with same setup time.



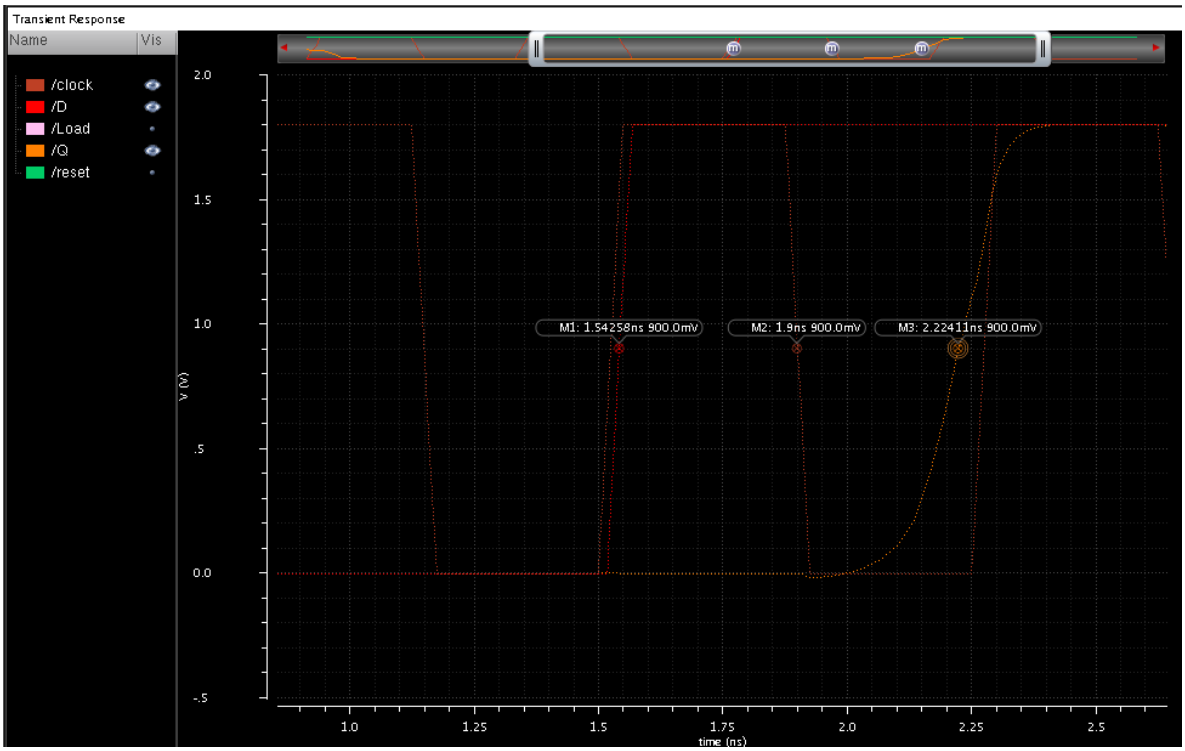

Since 1.84477<1.85157, Vin to Vout time for the schematic design is 0.51309ns.

b. layout

1. Layout simulation for the first try

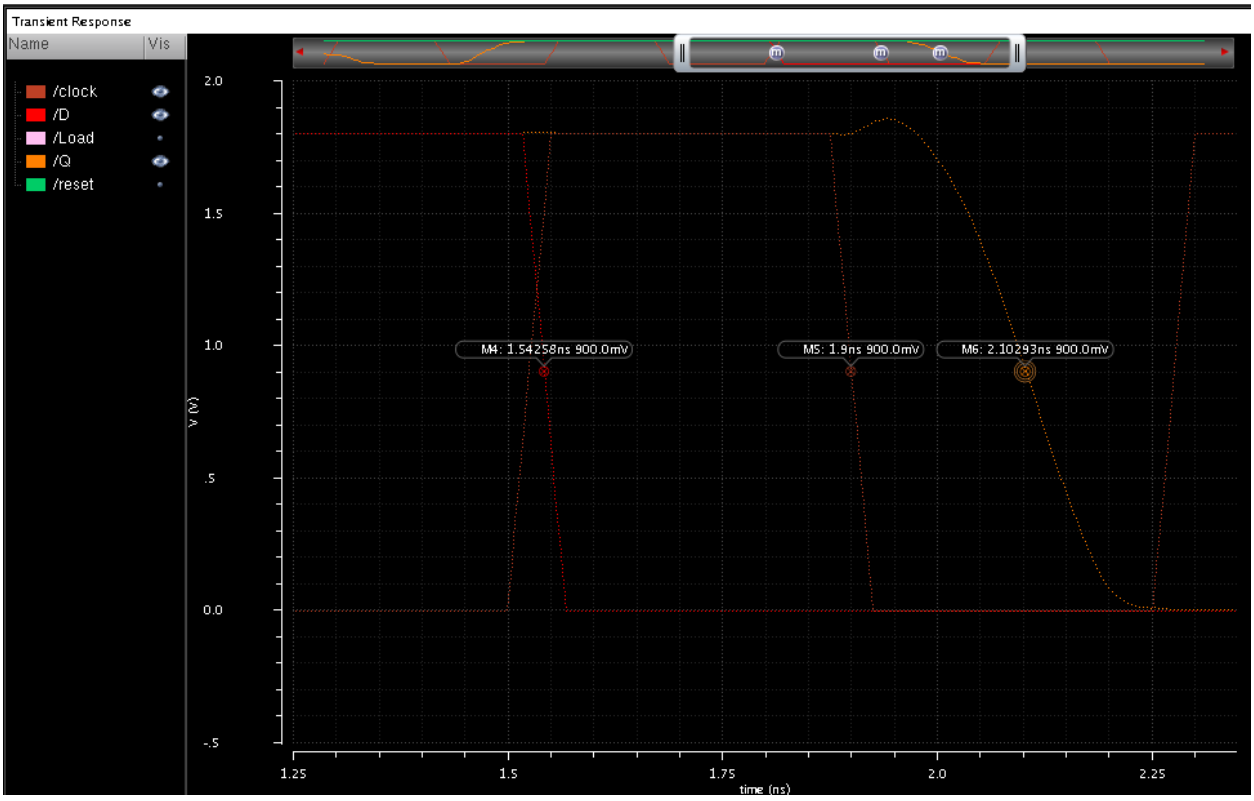



2. Founded minimal setup time for rising.




Setup time = 1.9-1.54258=0.35742ns Vin to Vout time= 2.22411-1.54258=0.68153ns

3. Redo the simulation for the falling with the same setup time




Since 2.10293<2.22411, the Vin to Vout time for the layout design is 0.68153ns

6. Values from simulation

The approach to get the setup time for schematic.

| rise point of D | difference | setup time | Correctness |
|---|---|---|---|
| 1.25 | 0.3125 | 0.3125 | Yes |
| 1.40625 | 0.15625 | 0.15625 | No |
| 1.328125 | 0.078125 | 0.234375 | No |
| 1.2890625 | 0.0390625 | 0.2734375 | Yes |
| 1.30859375 | 0.01953125 | 0.25390625 | Yes |
| 1.318359375 | 0.009765625 | 0.244140625 | No |
| 1.3134765625 | 0.004882813 | 0.249023438 | Yes |

The approach to get the setup time for layout.

| rise point of D | difference | setup time | Correctness |
|---|---|---|---|
| 1.5 | 0.375 | 0.375 | Yes |
| 1.6875 | 0.1875 | 0.1875 | No |
| 1.59375 | 0.09375 | 0.28125 | No |
| 1.546875 | 0.046875 | 0.328125 | No |
| 1.5234375 | 0.0234375 | 0.3515625 | No |
| 1.51171875 | 0.01171875 | 0.36328125 | Yes |
| 1.517578125 | 0.005859375 | 0.357421875 | Yes |
| 1.520507813 | 0.002929688 | 0.354492188 | No |

The result:

| Design | Minimum Clock | Setup time | Vin to Vout time |
|---|---|---|---|
| Layout | 0.625ns | 0.249ns | 0.51309 |
| Schematic | 0.75ns | 0.354ns | 0.68153 |