EE 477 Laboratory #3

Huayu Fu
4745159848
huayufu@usc.edu

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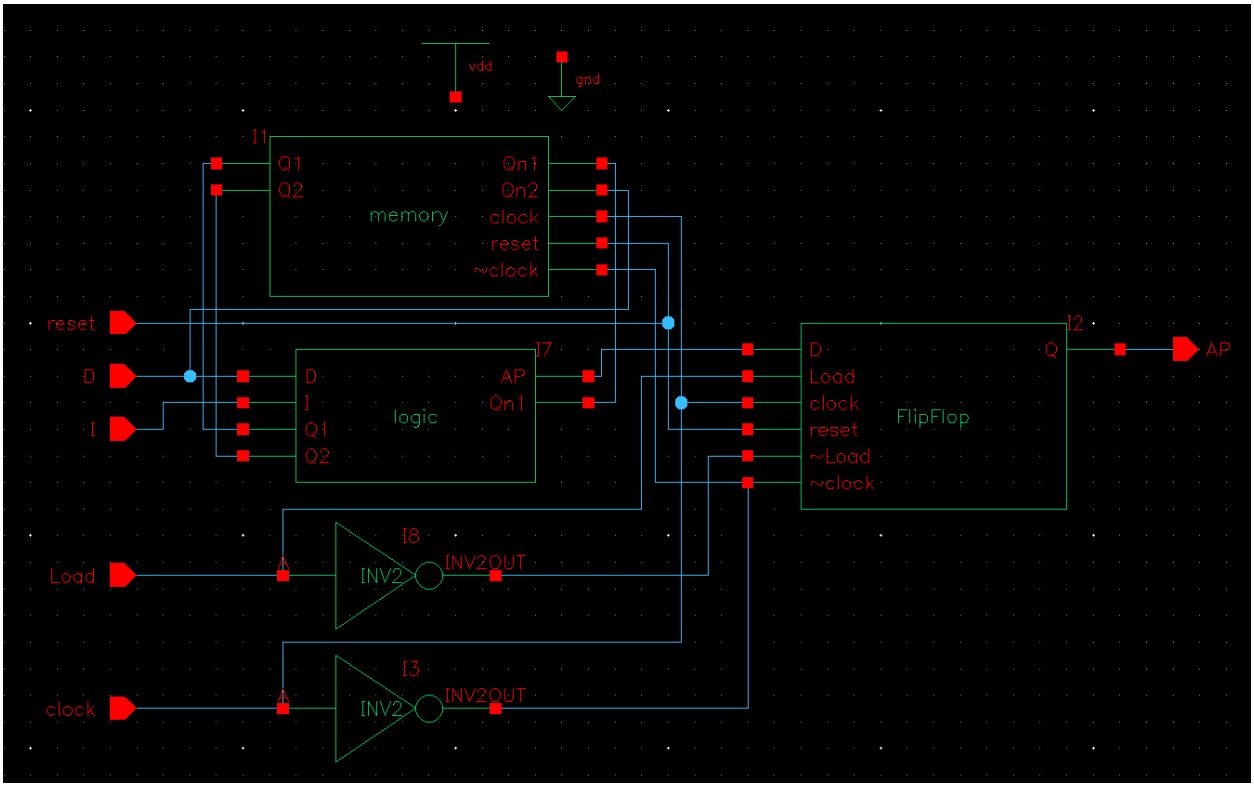
AREA-DELAY product = 22.4*27*1.15=695.52

Table of Contents

1. Description of the neuron

   The graph below is the gate level circuit diagram for the neuron design.



It consists the logic block, flip-flop block, memory block, and 2 inverter2 to invert the Load and clock signal for ~Load and ~clock signal.

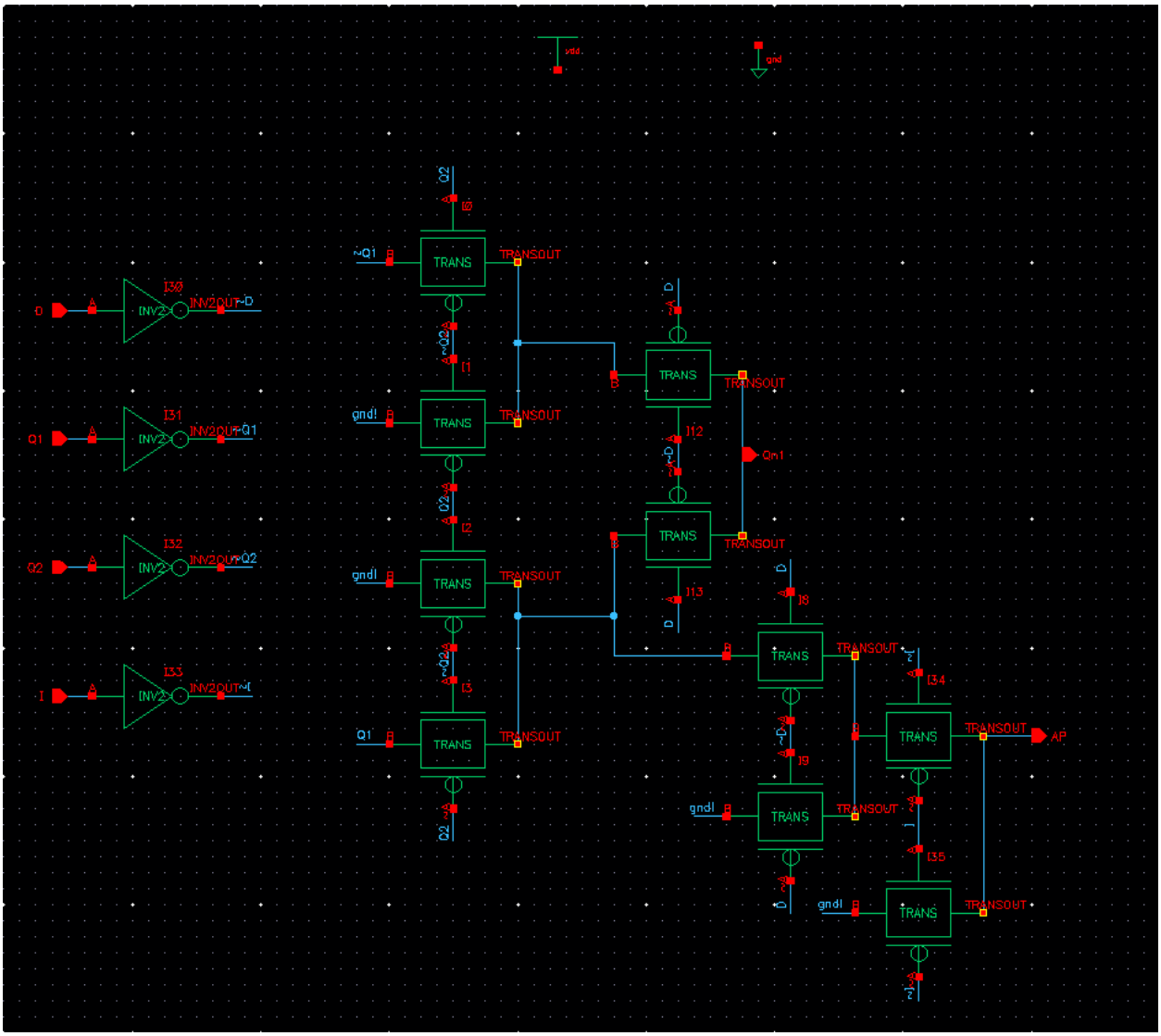
Logic block will take the input data D, I and current state Q1 Q2 to calculate the next state and weather it is the time to fire.

Memory block will store the next state and output the current state based on the clock change with the synchronized reset.

Flip flop will take the output from logic block from the port AP. If Load is high and reset is not asserted, the actual AP will come out at the falling edge of clock.

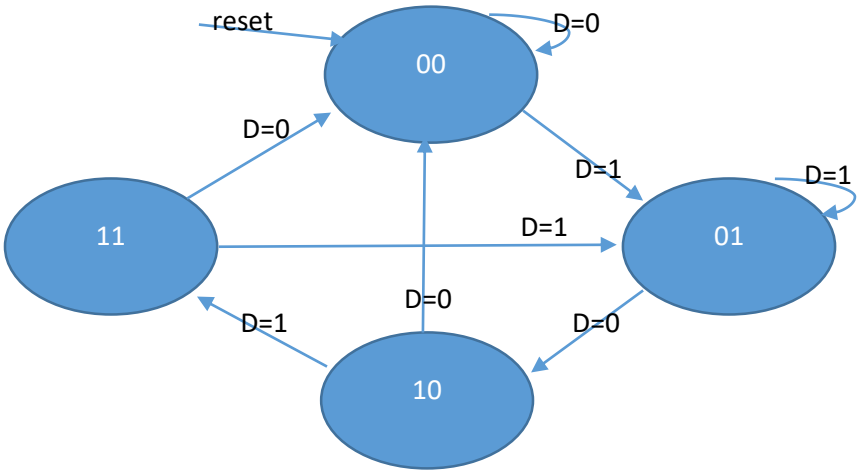
A. The logic block:

a. Schematic of logic block.



b. The state machine:

I designed the state machine for the logic, it has 4 states. The initial state (00), wait for 1 state (01), wait for 0 state (10) and wait for the last 1 state (11).



Then I draw the K-map to minimize the logic and got:

Qn1=~D*~Q1*Q2+D*Q1*~Q2

Qn2=D

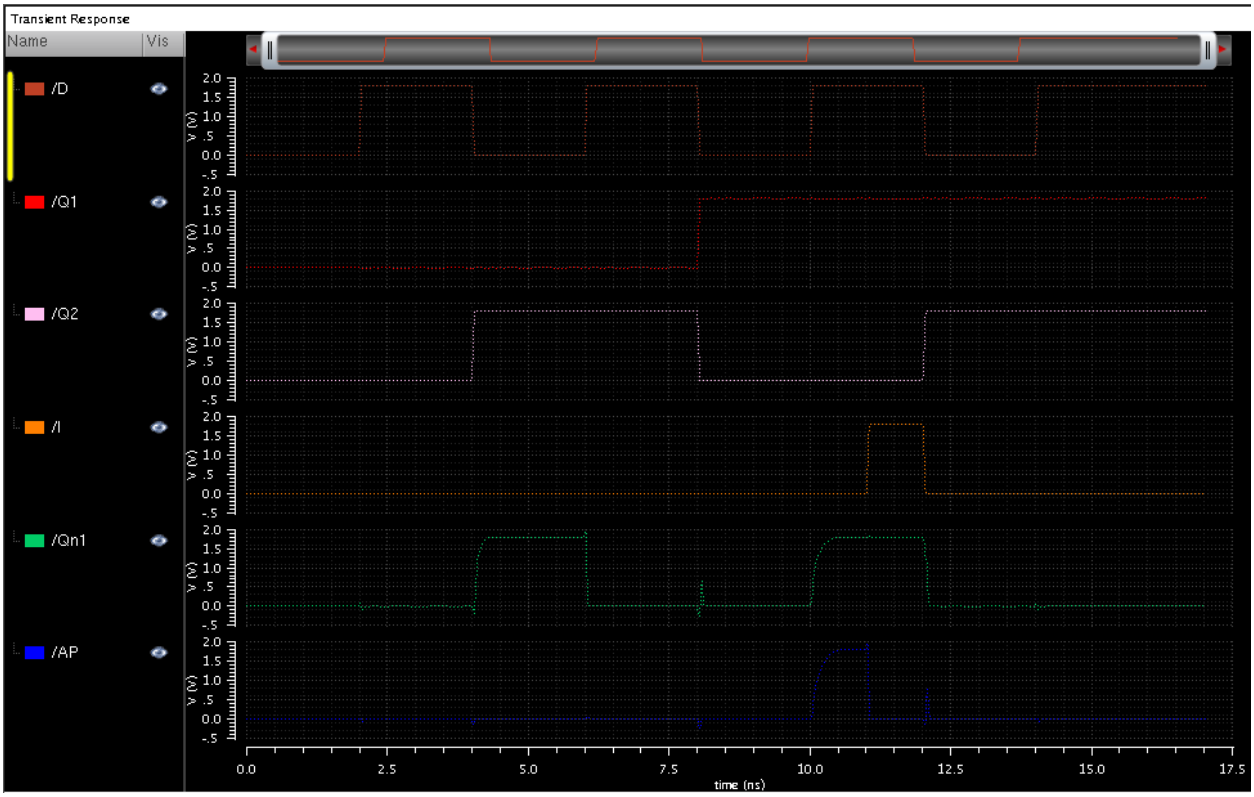
AP=D*Q1*~Q2*I

Then I converted it in to transmission gate design as the schematic shows.

c. choice of the inverter at the input:

After the logic design, I come up the two ideas of how to invert the input, the first one is to have a inverter1 to invert the input and two inverter2 to delay the input. And the second one is to have inverter2 to invert the input. After the simulation, the idea two performs better and saves spaces.

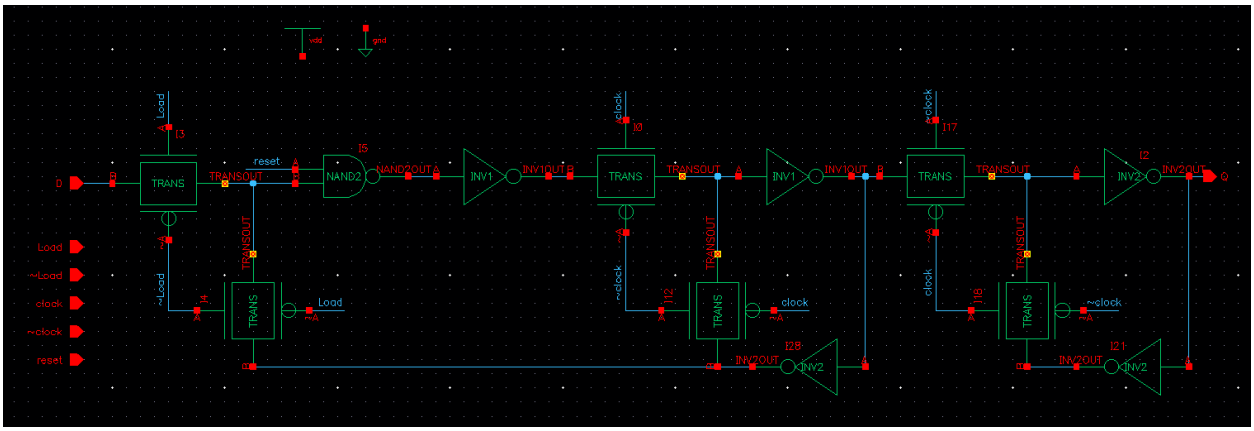
d. Simulations:



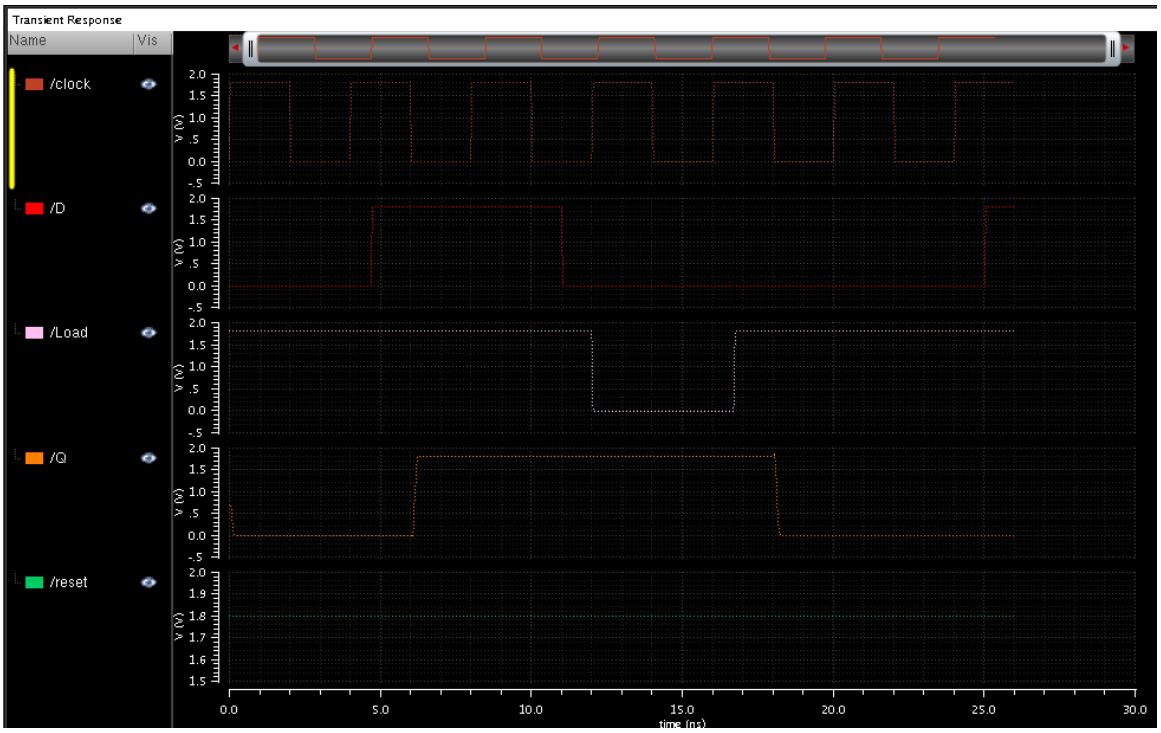
B. The flip-flop block

a. Schematic of flip-flop block:

The flip-flop block is the same as the block designed in lab2. It consists transmission gate nand2 gate, inverter 1 and inverter 2. It will load at the falling edge of clock with synchronized reset and load. And reset have higher priority.

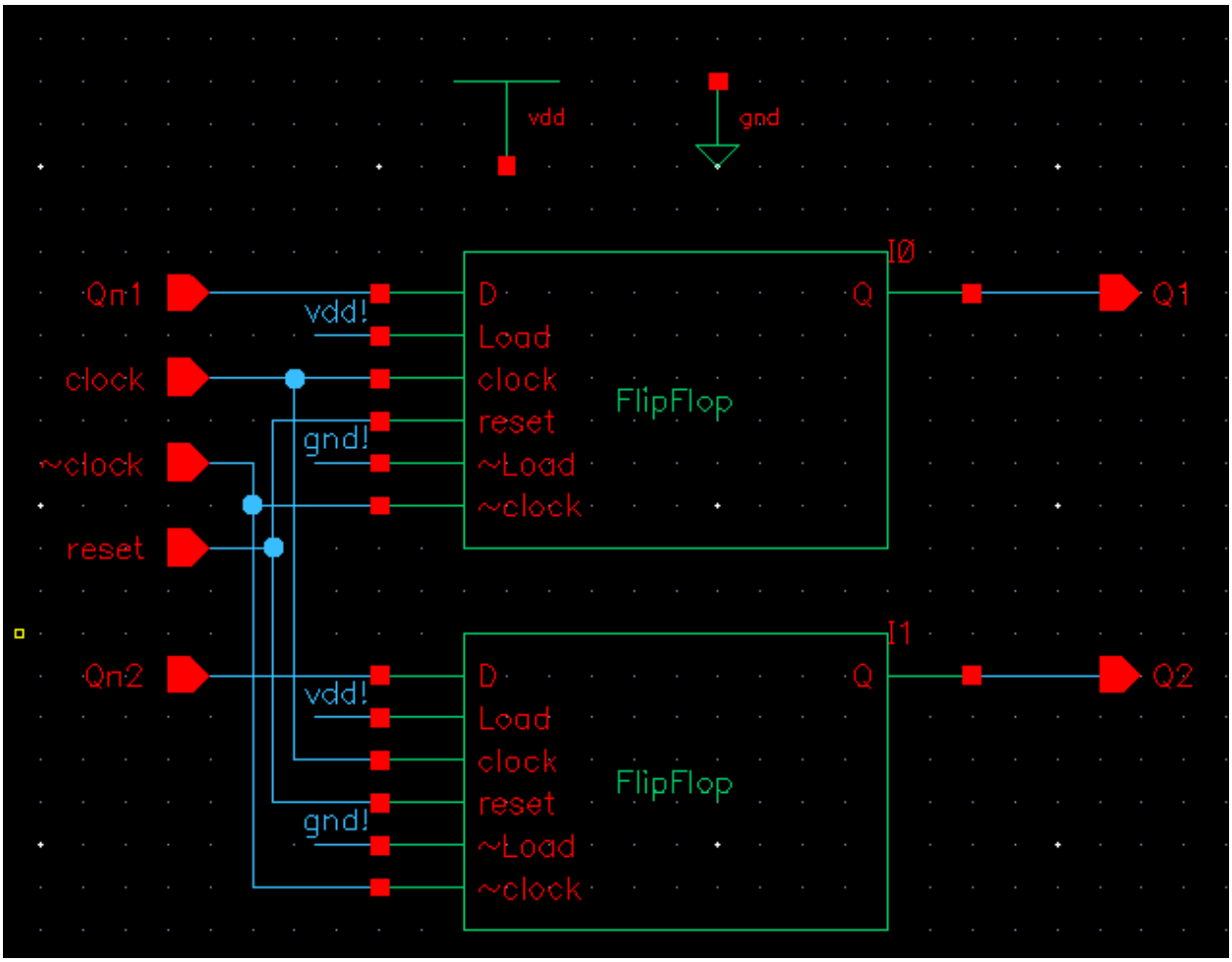


b. Simulations:



C. The memory block

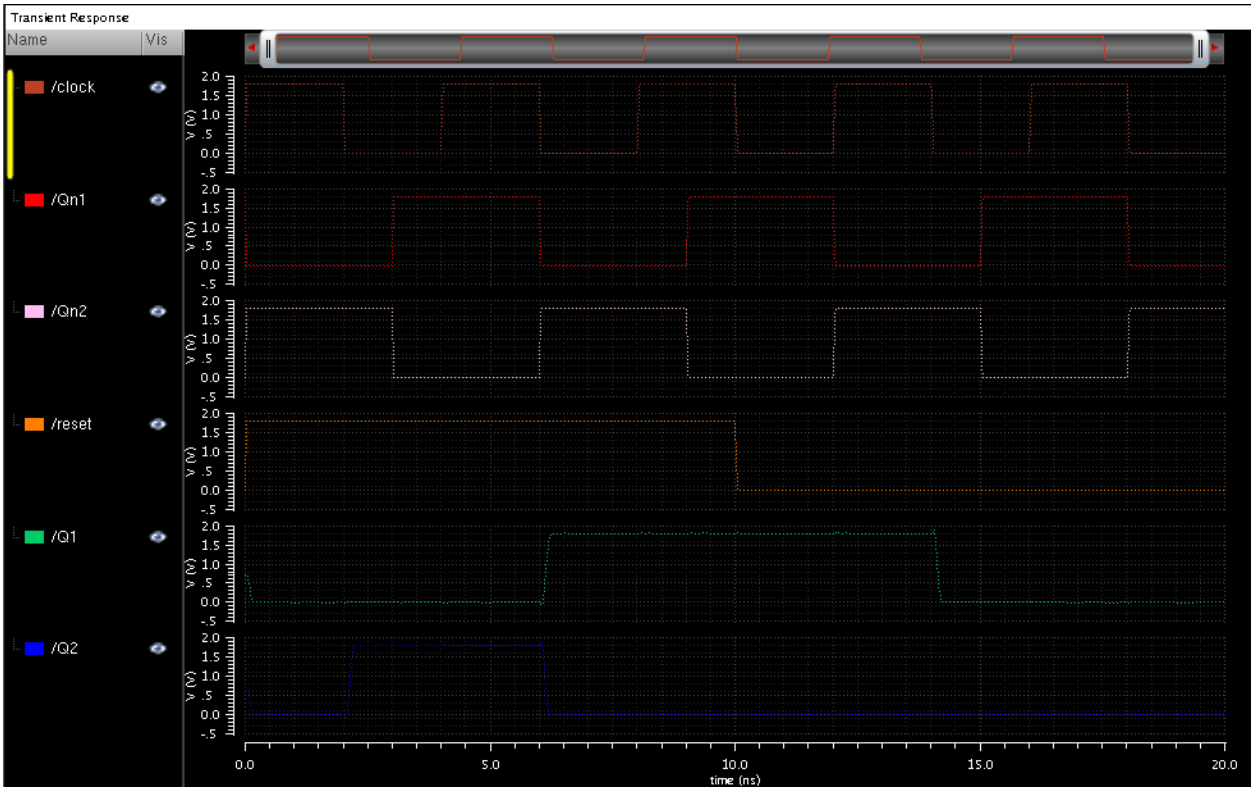
a. Schematic of memory block:



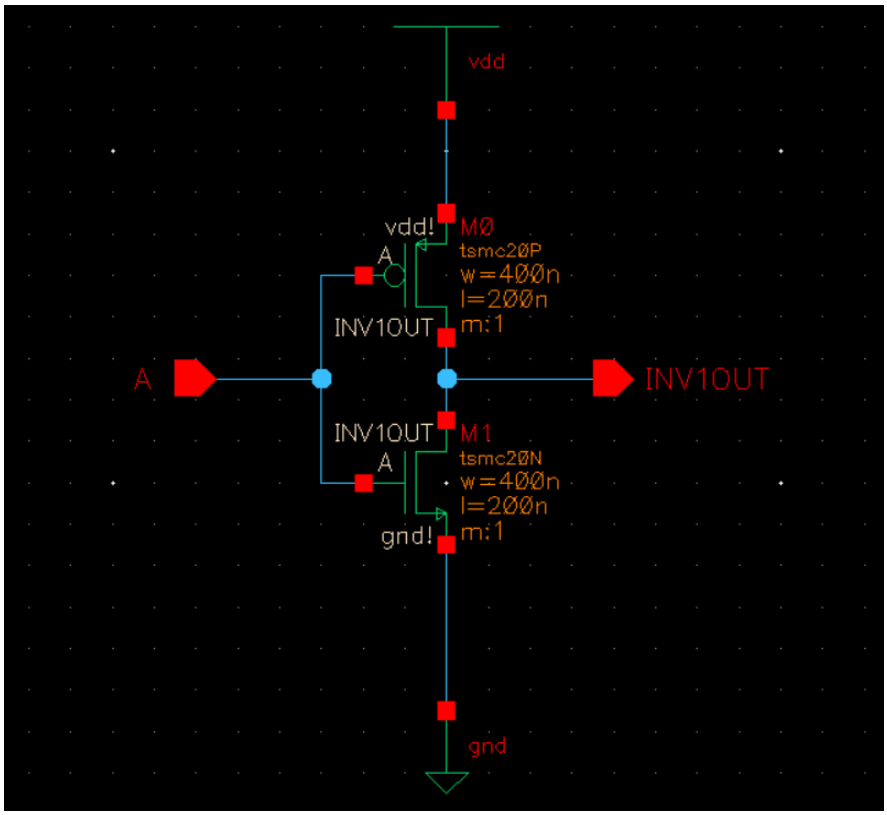
b. The design:

I used two flip flop to construct the memory and it have the function of active low reset and will load 2 inputs at the falling edge of clock. And I also connected the unused input load to vdd and ~load to gnd. The input is connected to the output of the next state logic.

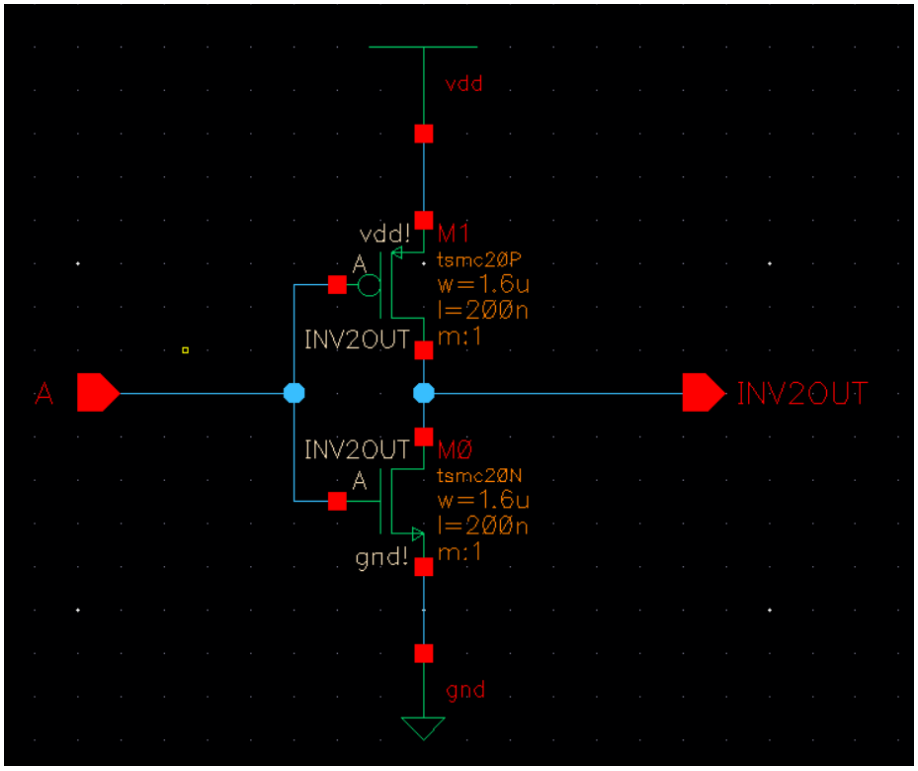
c. Simulations:



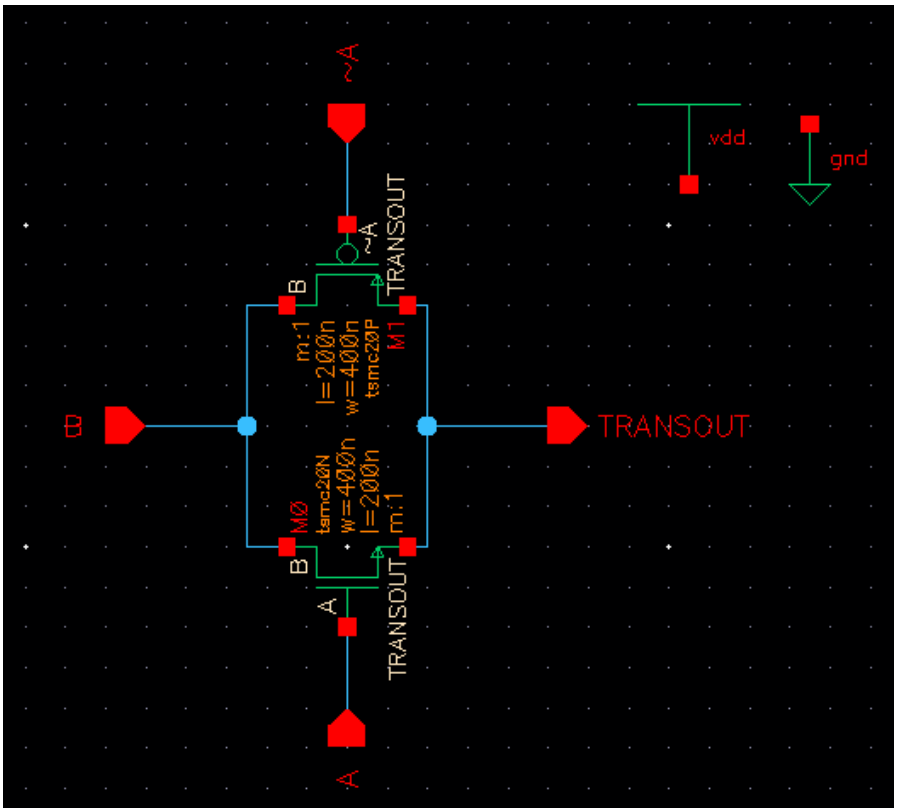
D. Transistor level diagram for the module used in the neuron.
   a. INV1



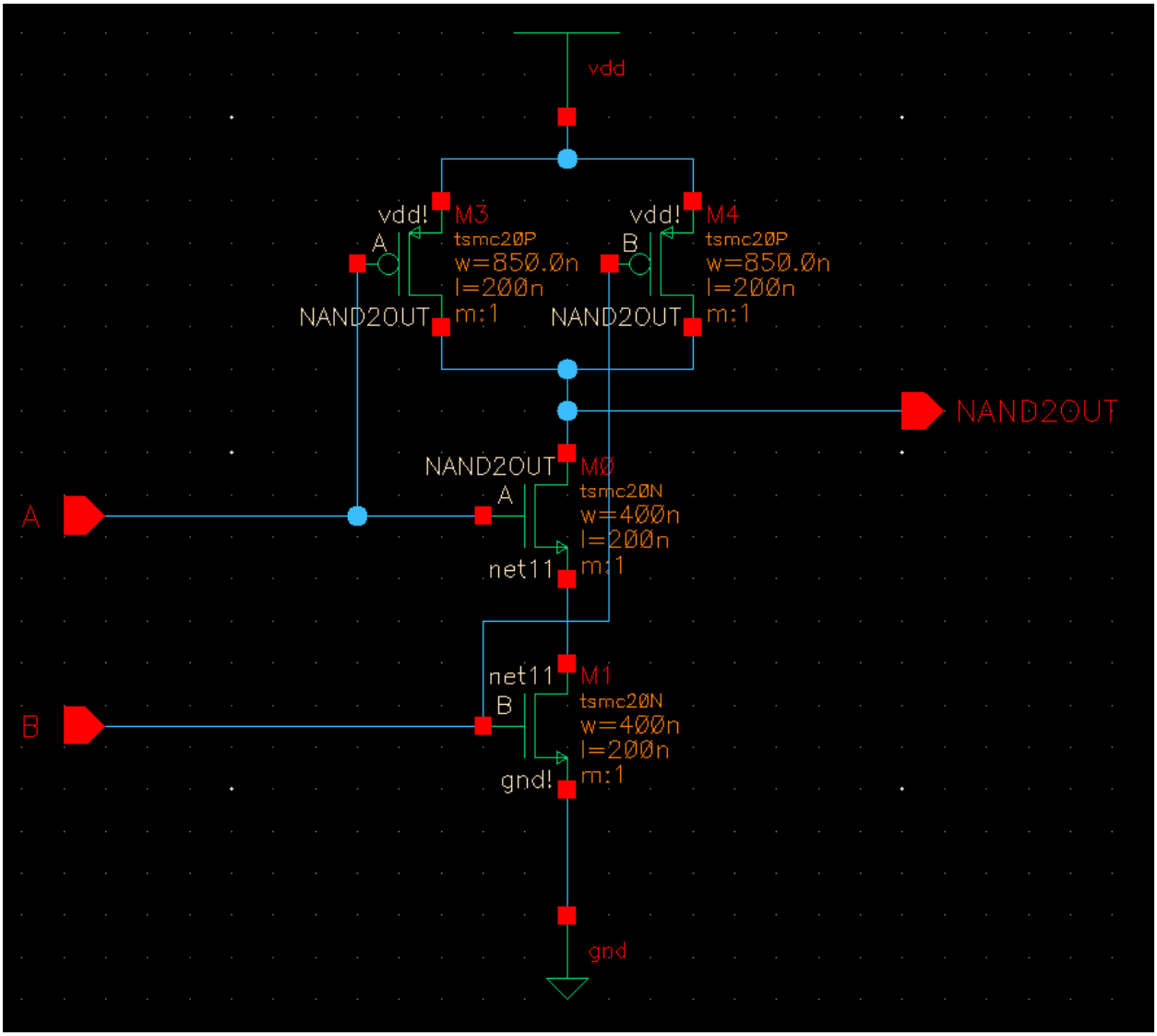
b. INV2



c. TRANS



d. 2-input NAND



E. The schematic simulation of neuron:

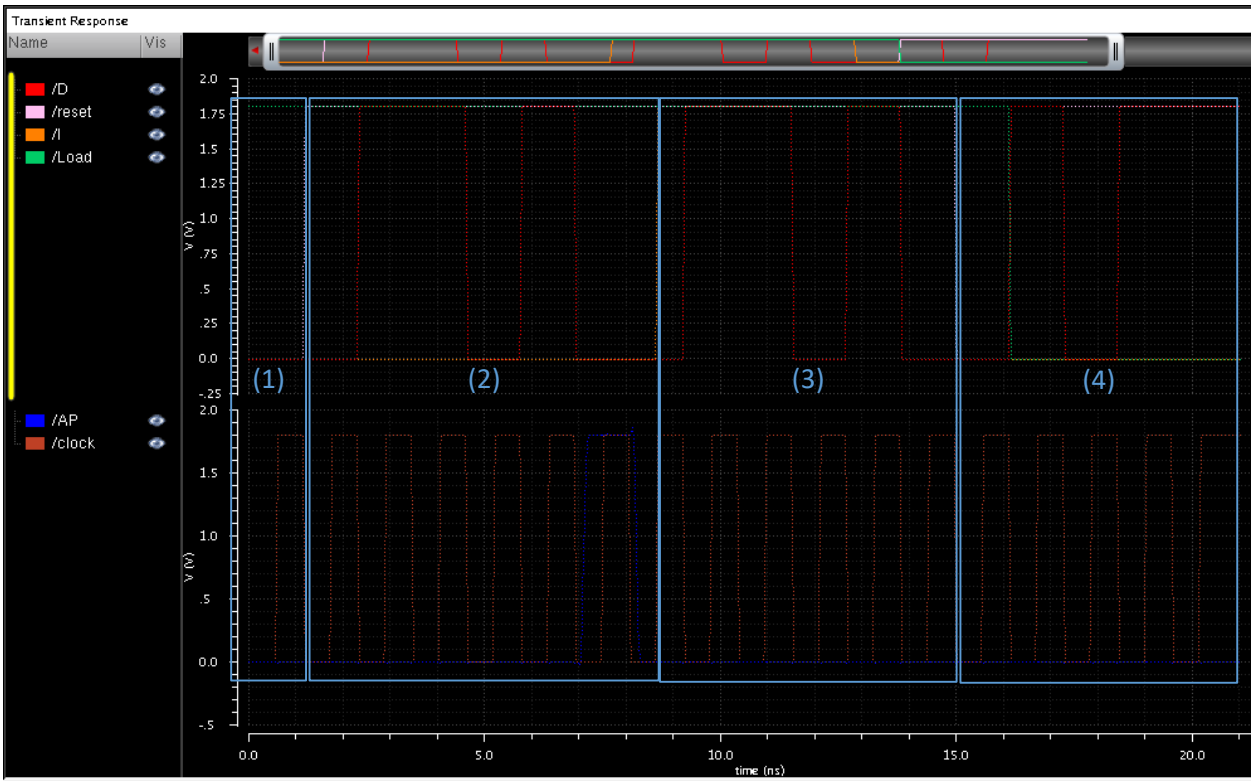
a. The test case from lab:

(1) Set load to 1 and keep it high. Reset neuron flip flop.

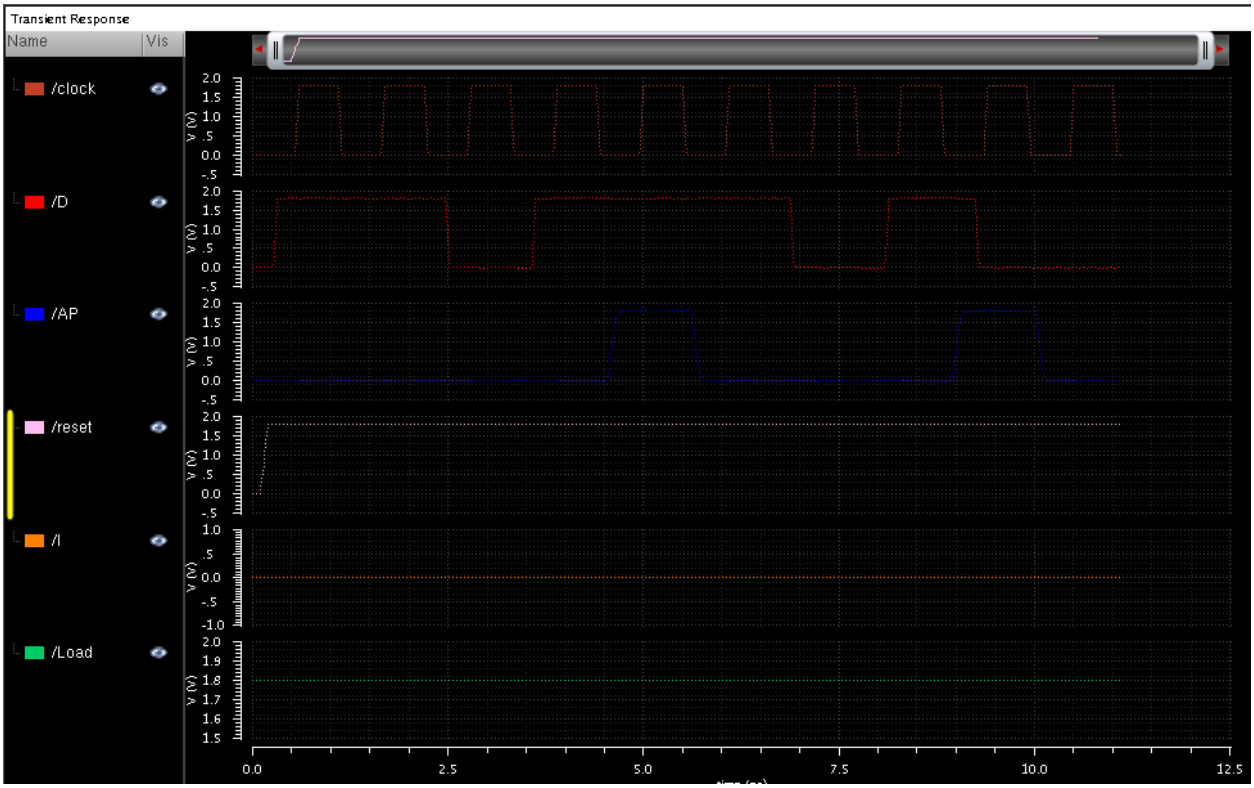
(2) Set load to 1 and keep it high, while keeping I = 0. Then test your neuron by sequencing through D=0 to D=1 to D = 1 to D = 0 to D = 1 to D = 0. (2 different values).

(3) Set I = 1 (inhibition), leave load =1 and sequence through the same inputs. The output AP should be low.

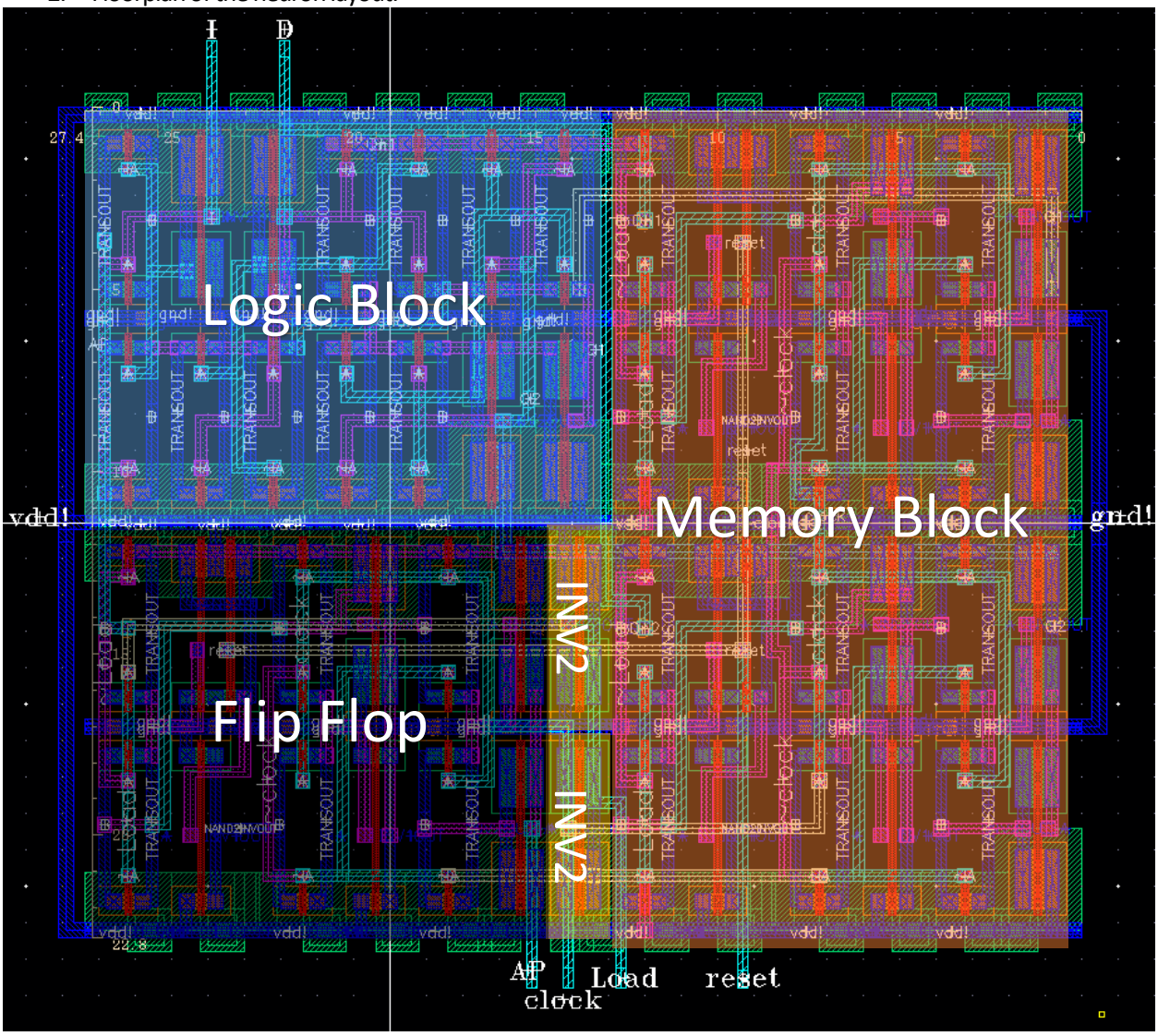
(4) Reset the neuron flip flop. Now set load to 0 (zero). Set the data input D to 1, and I = 0, then on the next clocks 0 then 1 with I = 0. The flip-flop output should remain zero.



b. Given test case:



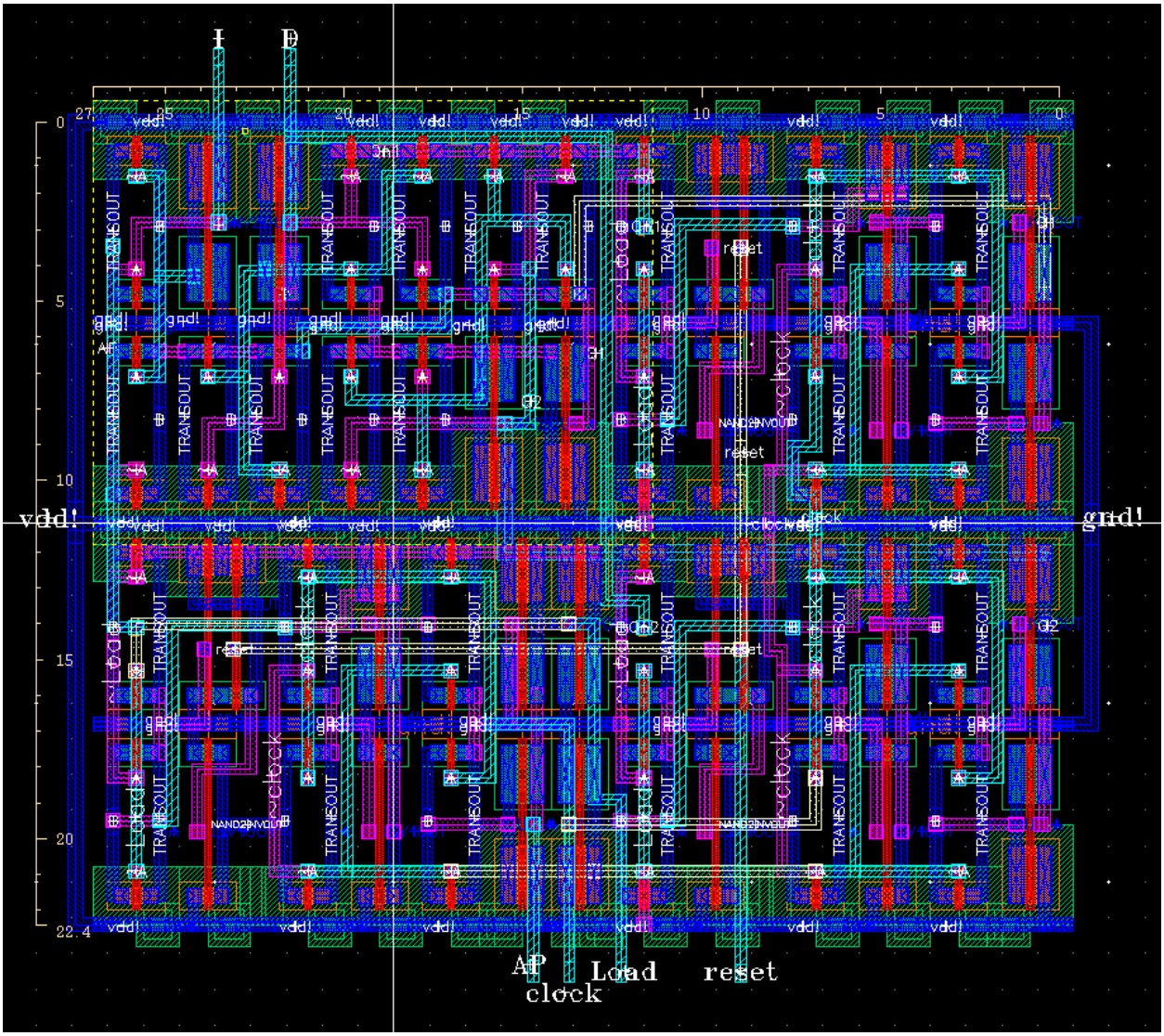
2. Floorplan of the neuron layout:



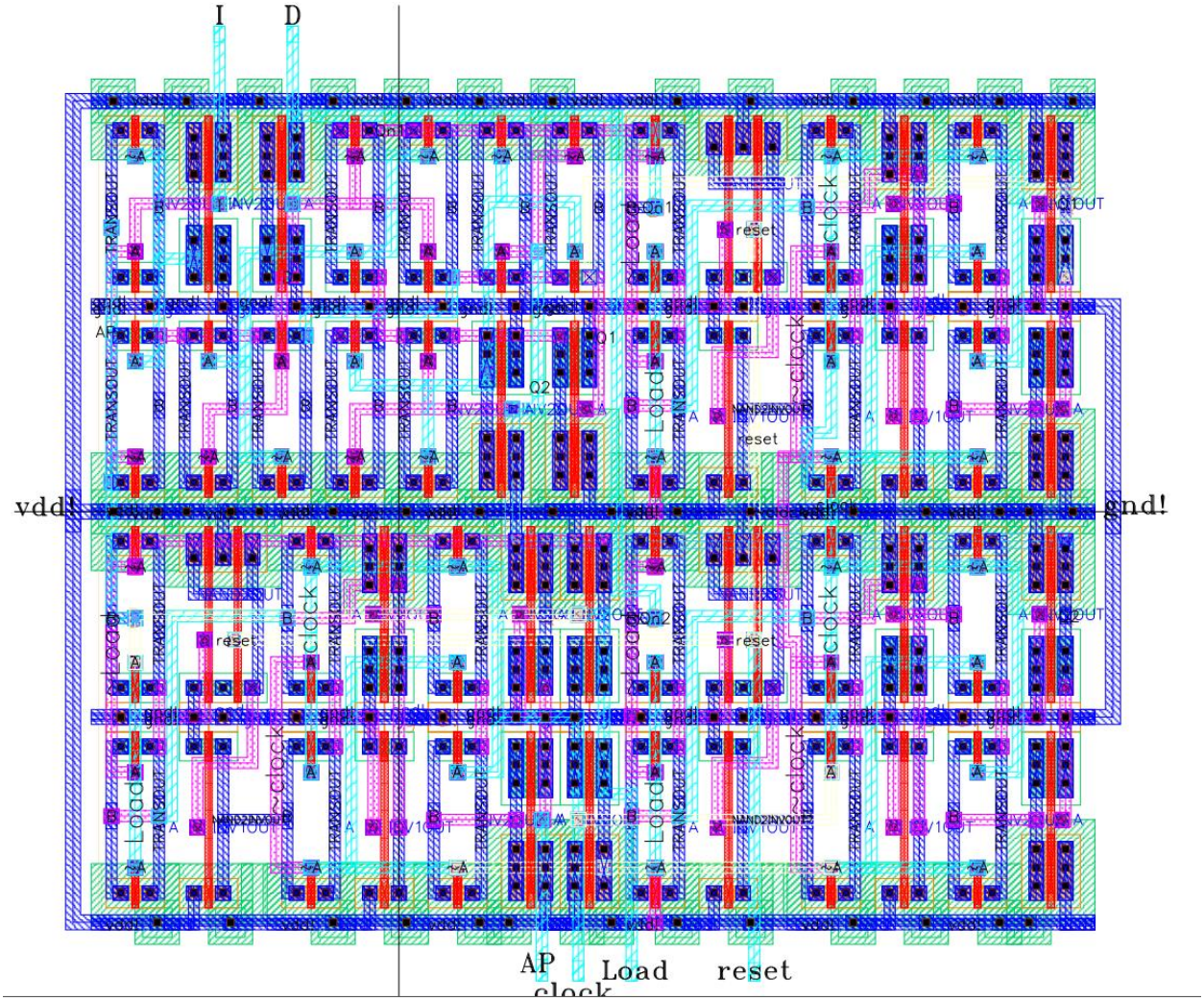
3. Neuron layout image and neuron layout simulation & description

For the layout, I put each function in to a block and combined 3 blocks (logic, memory and flip-flop) and 2 inverter2 in to one big block, with the size of 22.4 by 27. I tried to share the vdd and gnd, minimize the distance between the block next to each other. Due to the time constrain, I did not resize the modules.

A. Layout image



B. Layout print out:



C. Simulations:

a. The simulation one is in following sequence:

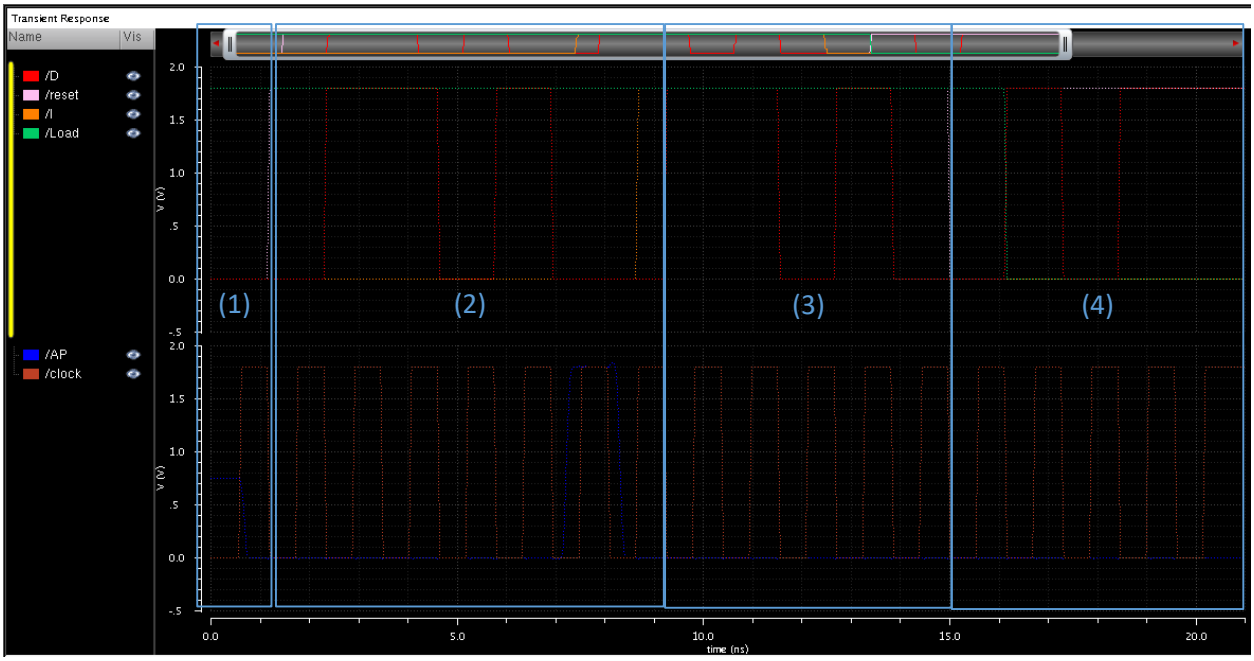
(1) Set load to 1 and keep it high. Reset neuron flip flop.

(2) Set load to 1 and keep it high, while keeping I = 0. Then test your neuron by sequencing through D=0 to D=1 to D = 1 to D = 0 to D = 1 to D = 0. (2 different values).

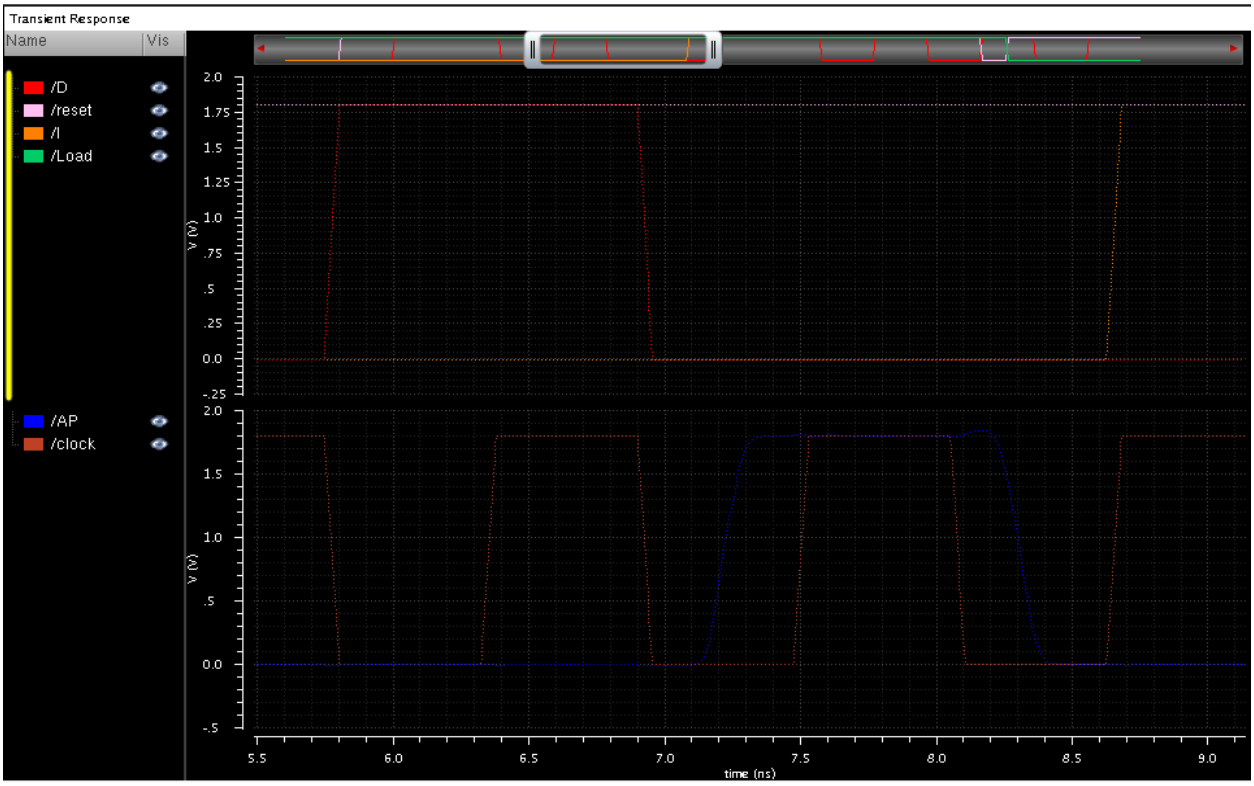
(3) Set I = 1 (inhibition), leave load =1 and sequence through the same inputs. The output AP should be low.

(4) Reset the neuron flip flop. Now set load to 0 (zero). Set the data input D to 1, and I = 0, then on the next clocks 0 then 1 with I = 0. The flip-flop output should remain zero.

And the minimal clock period I found is 1.15ns



b. Zoom in for the minimal clock



c. The given waveform at clock period =1.15ns: