EE 477 Laboratory #1

Logic Gate Design/Layout and Simulation Experiments with Combinational Cells

10/29/2016

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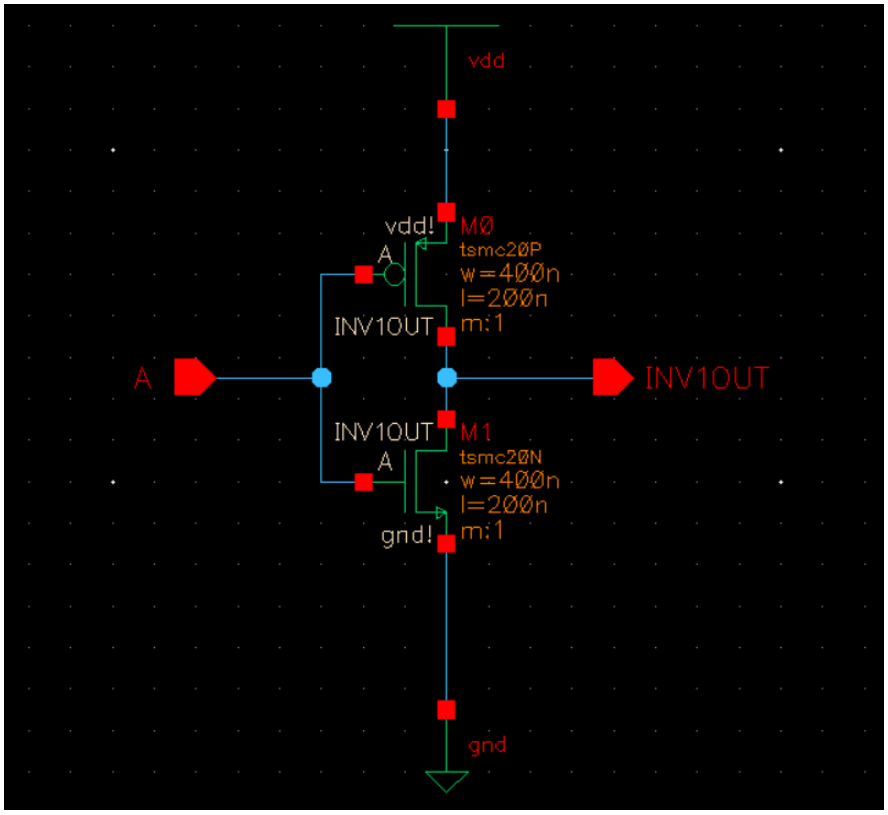
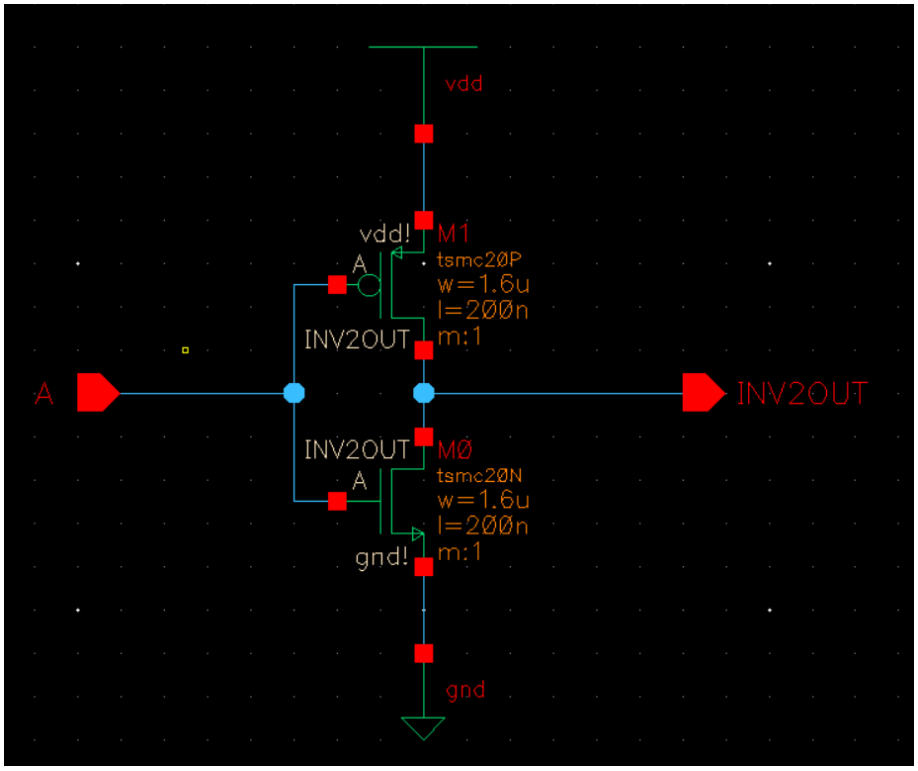
1. Transistor schematics of gates taken from Cadence

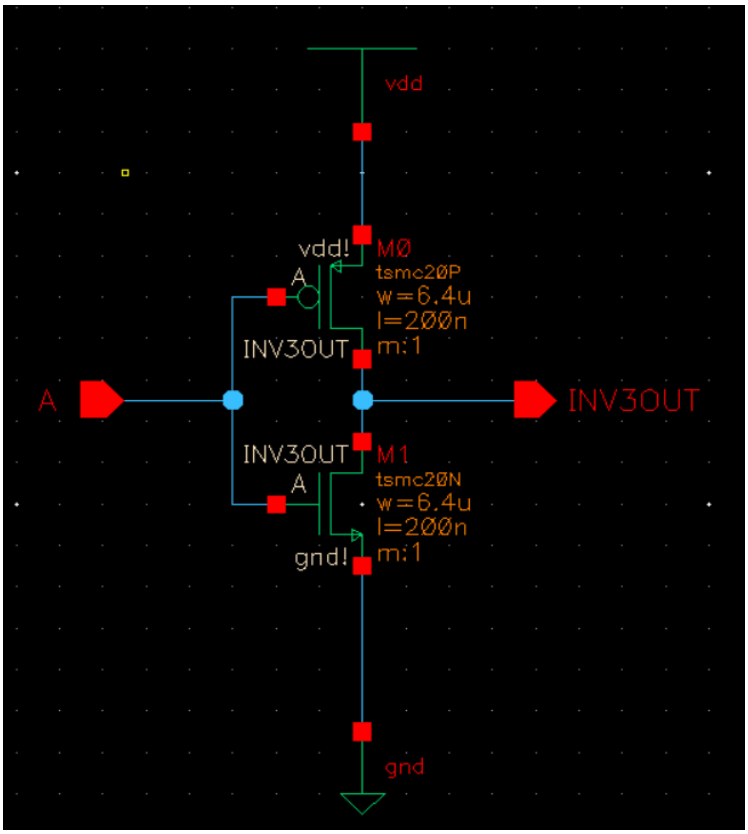
A. Inverter 1



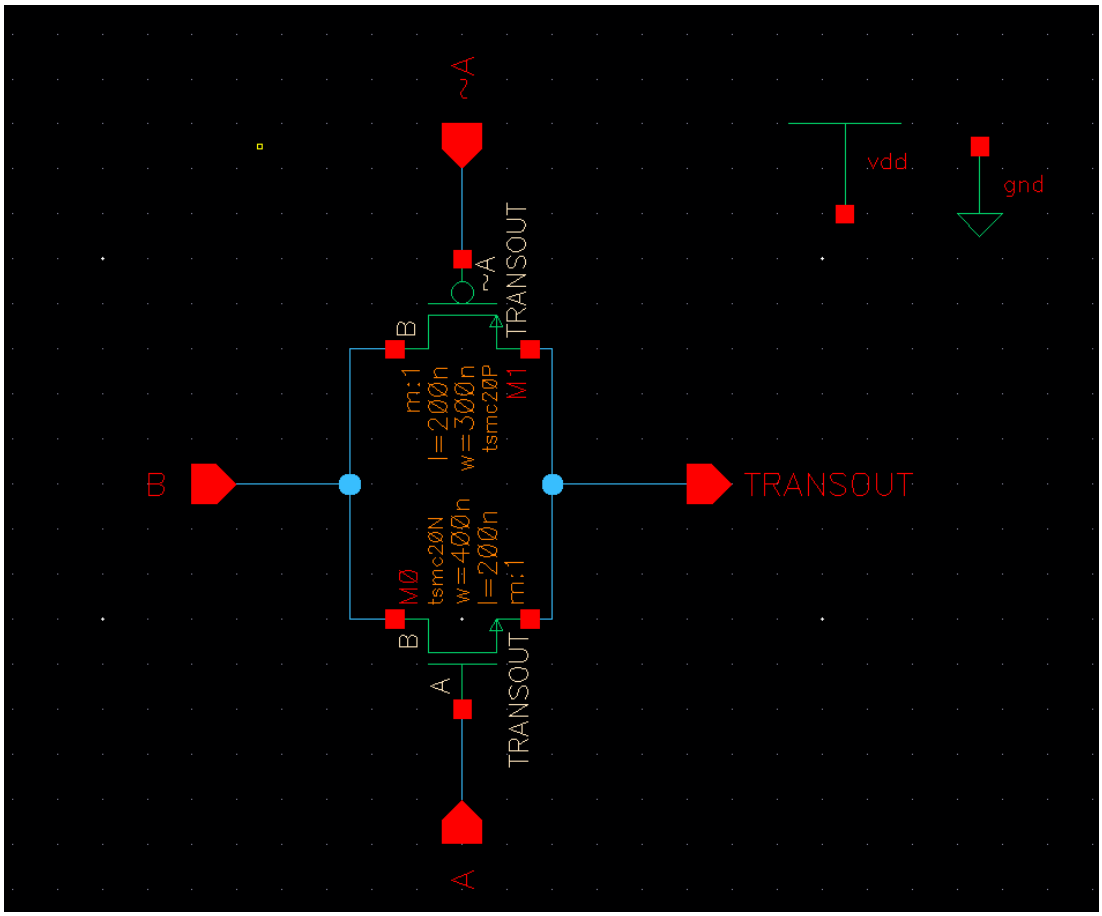
B. Inverter 2



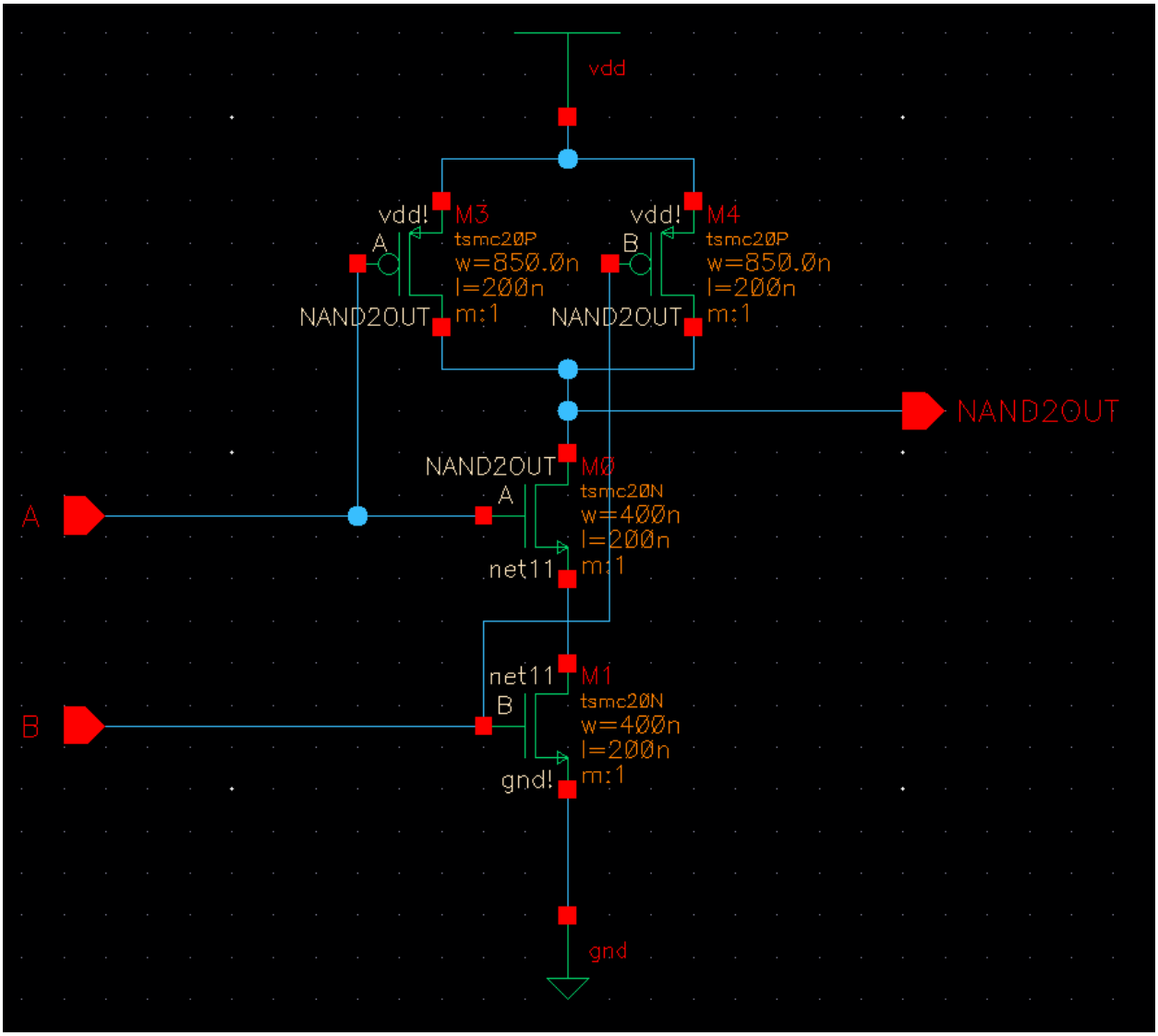
C. Inverter 3



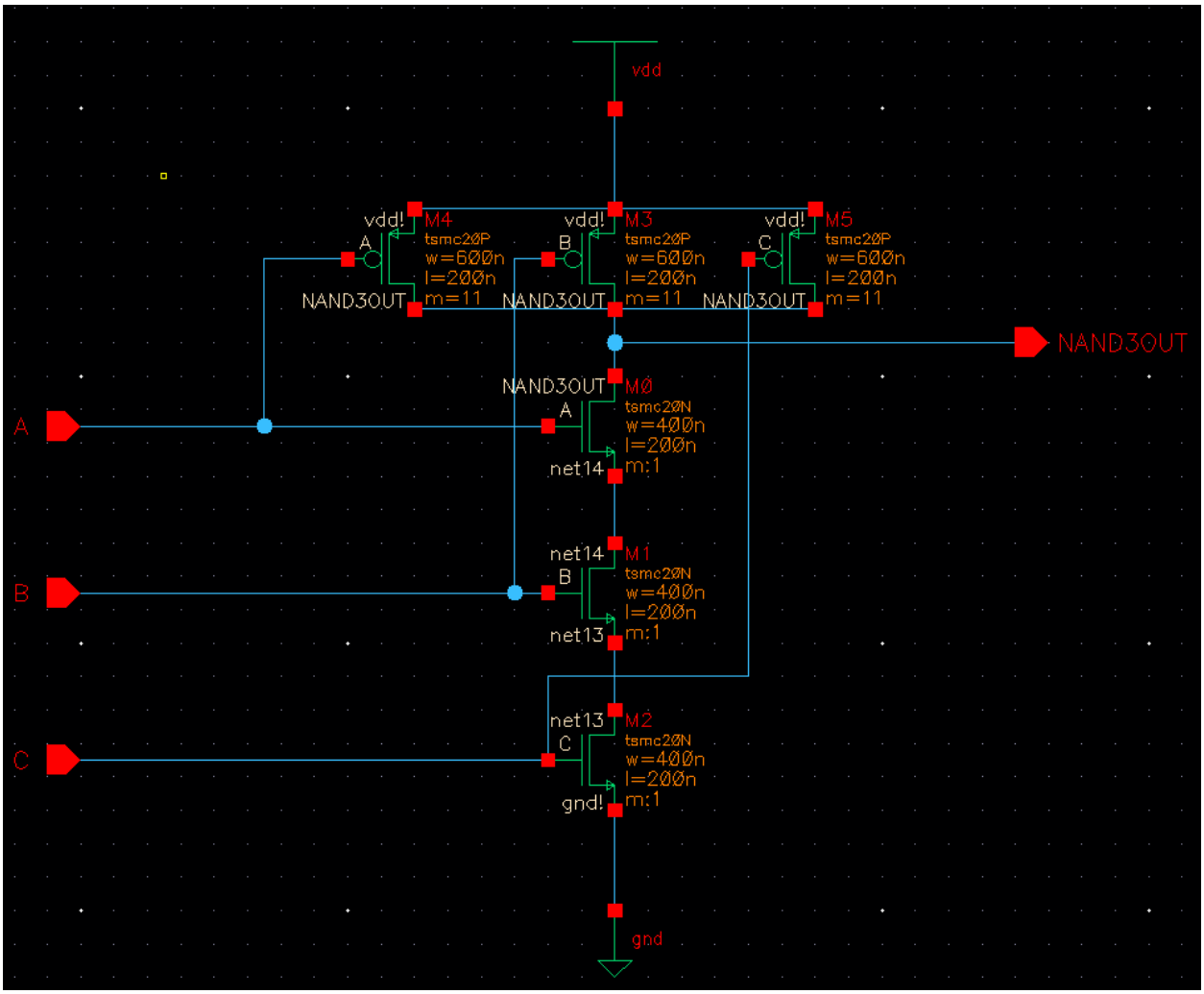
D. Transmission Gate



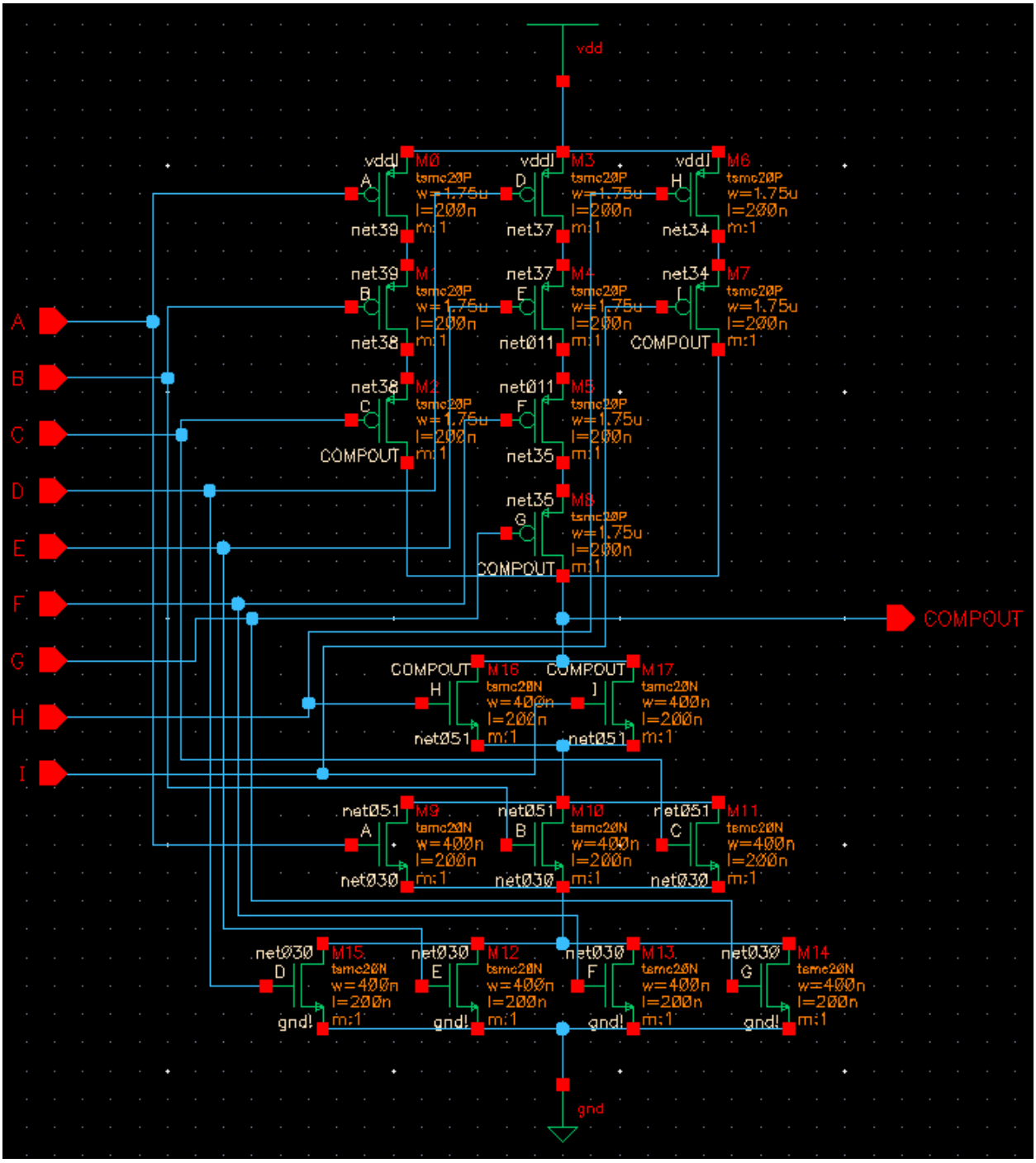
E. 2-input NAND



F. 3-input NAND



G. Compound Gate COMPOUT = NOT {[A+B+C] *[D+E+F+G]* [H+I]}



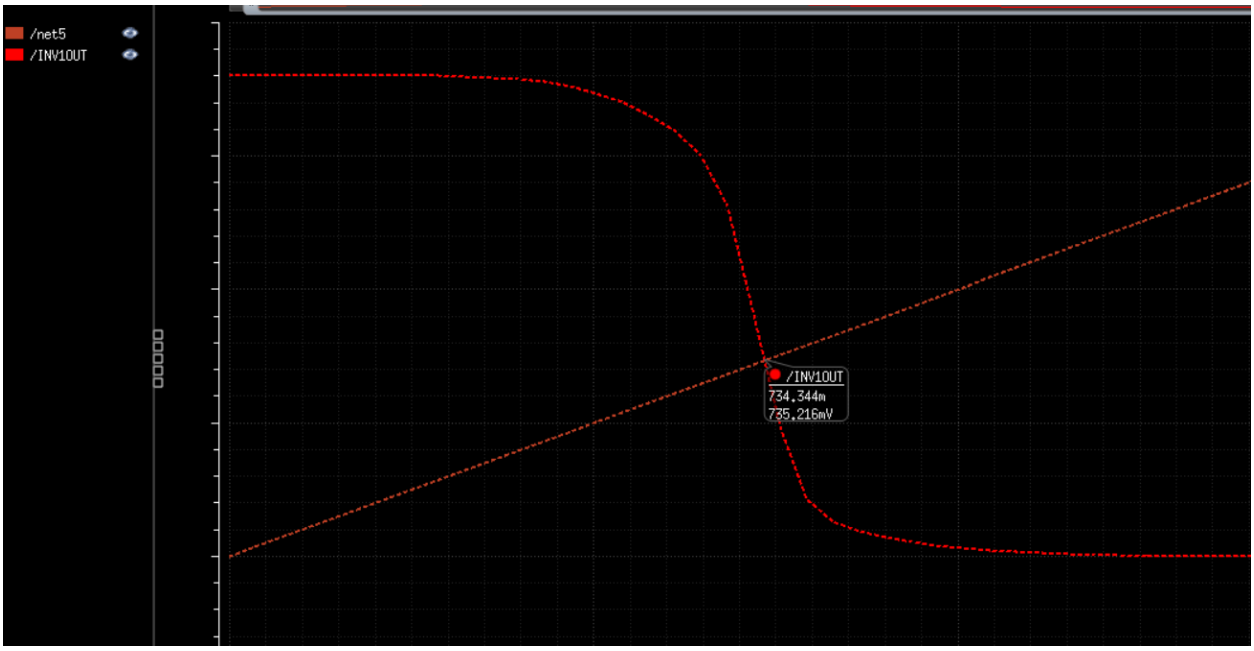
2. Discussion and explanation of how you sized transistors, and the beta ratio you found, including measured rise and fall times.

A. INV1 is sized according to the lab instruction, unit size. W=400nm, L=200nm.

B. INV2 is sized according to the lab instruction, 4 times wide as INV1. W=1.6um, L=1.6um.

C. INV3 is sized according to the lab instruction, 4 times wide as INV2. W=6.4um, L=6.4um.

Beta Ratio is calculated based on the DC analysis of INV3. The point when input equals output, is a sure point for both transistor in saturation region and the beta ratio is calculated based on the following reading and equation.



K=βn/βk=(Vgsp-Vtp)^2/(Vgsn-Vtn)^2=(0.734-1.8+0.4215645)^2/(0.734-0.3796589)^2=3.30

D. Transmission gate is sized according to the lab instruction, unit size. W=400nm, L=200nm.

E. 2-input NAND

For 2 input NAND gate, the calculated Wp is 6.5 λ

In a worst case scenario, 2RCHN = RCHP

$\frac{2Ln}{\beta_n Wn}=\frac{Lp}{\beta_p Wp}$

$W_p = \frac{\beta n * W_n}{\beta_p * 2}$=3.3*4$\lambda$/2=6.5$\lambda$=650nm

However, the simulated result of raise time and fall time does not meet our excortication of +-10%.

After manipulating the value of Wp. I found the minimal width of Wp falls into the excepted range is 850nm.

Wp	Raise time	Fall time	Ratio
6.5λ	7.25E-11	5.279E-11	1.373366168
7λ	6.968E-11	5.409E-11	1.288223331
7.5λ	6.711E-11	5.536E-11	1.21224711
8λ	6.483E-11	5.675E-11	1.142378855
8.5λ	6.278E-11	5.814E-11	1.079807362

Therefore, Wp=850nm Lp=200nm Wn=400nm Ln=200nm

F. 3-input NAND

For 3 input NAND gate, the calculated Wp is 4.5 λ

In a worst case scenario, 3RCHN = RCHP

3RCHN = RCHP

$\frac{3Ln}{\beta_n Wn}=\frac{Lp}{\beta_p Wp}$

$W_p = \frac{\beta n * W_n}{\beta_p * 3}$=3.3*4$\lambda$/3=4.5$\lambda$

However, the simulated result of raise time and fall time does not meet our excortication of +-10%.

After manipulating the value of Wp. I found the minimal width of Wp falls into the excepted range is 600nm.

Wp	Raise time	Fall time	Ratio
4.5λ	1.148E-10	8.241E-11	1.393034826
5λ	1.078E-10	8.51E-11	1.266745006
5.5λ	1.024E-10	8.779E-11	1.166419866
6λ	9.696E-11	9.444E-11	1.026683609

Therefore, Wp=600nm Lp=200nm Wn=400nm Ln=200nm

G. Compound Gate

For 3 input NAND gate, the calculated Wp is 21.5 λ

In a worst case scenario, 3RCHN = 4RCHP

$\frac{3Ln}{\beta_n Wn}=\frac{4Lp}{\beta_p Wp}$

$W_p = \frac{\beta n * W_n \ \ *4}{\beta_p * 3}$=3.3*4$\lambda * 4$/3=17.5$\lambda$

However, the simulated result of raise time and fall time does not meet our excortication of +-20%.

After manipulating the value of Wp. I found the minimal width of Wp falls into the excepted range is 2.15um.

Wp	Raise time	Fall time	Ratio
17.5λ	686	474	1.447257384
20λ	669.3	528.6	1.266174801
20.5λ	666.2	539.1	1.235763309
21λ	663.2	550.4	1.20494186
21.5λ	660.4	560.3	1.178654292
22λ	657.7	572	1.149825175

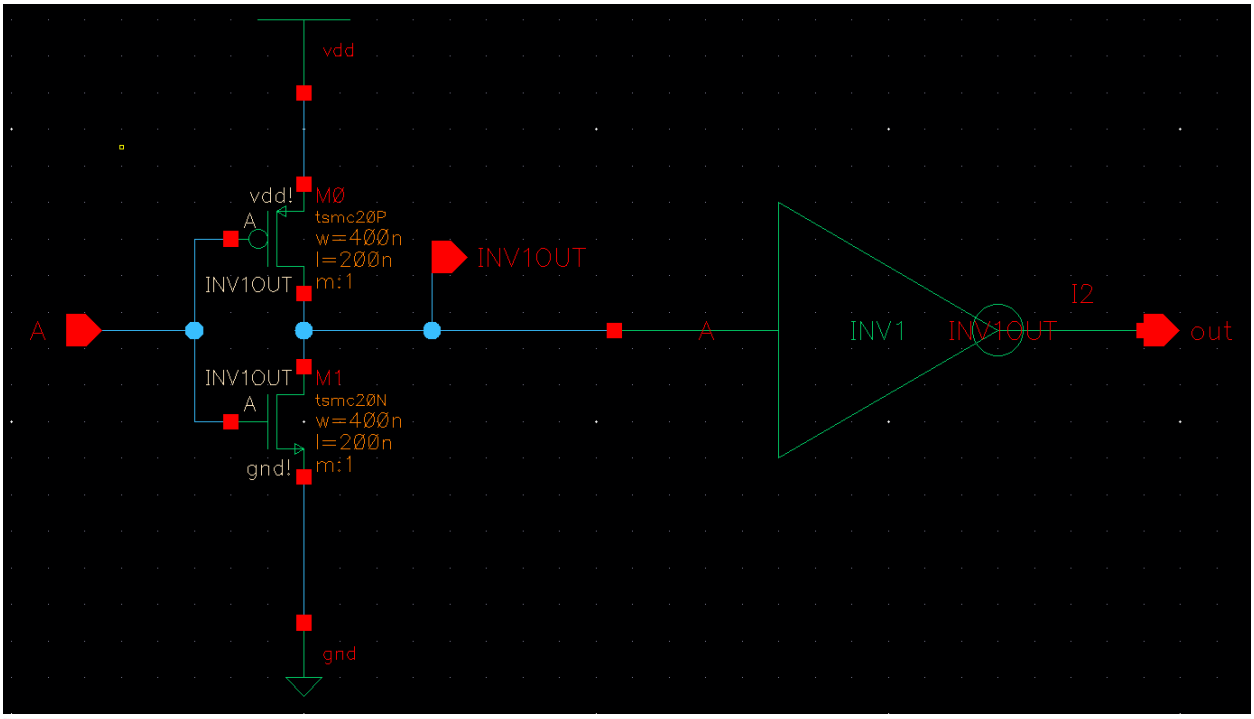
Therefore, Wp=2.15um Lp=200nm Wn=400nm Ln=200nm

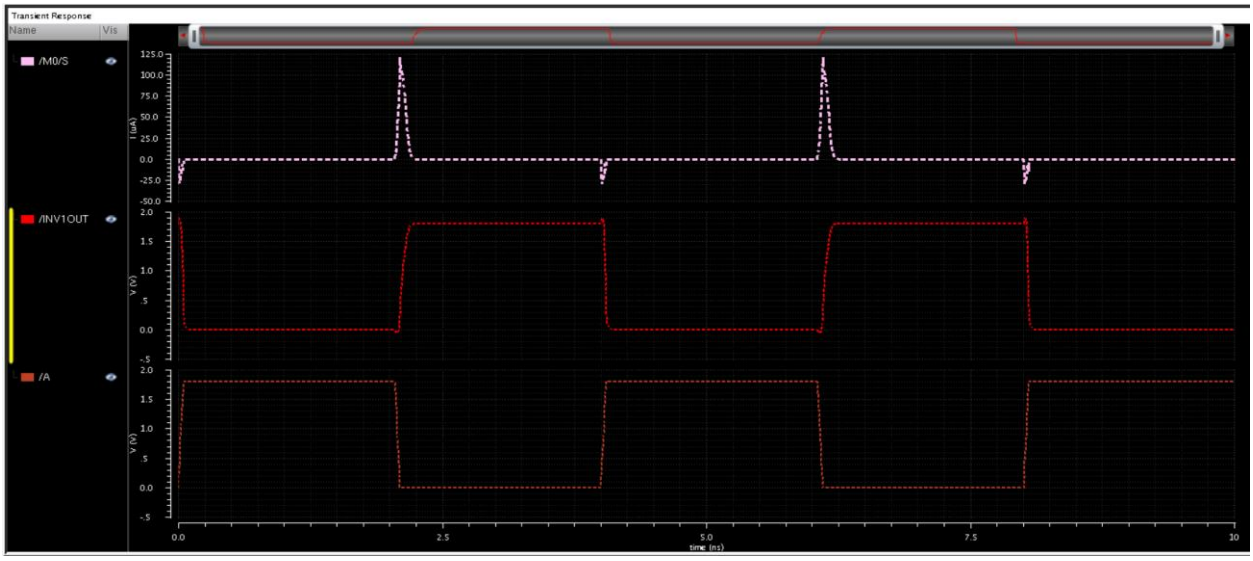
3. Description of your design methodology.

In order to use all the block in the later design, the block with the exactly same height are preferred. I chose the height of 6.5um as the global height. This height is good for all the different layouts in this lab even for the complicated compound gate. VDD and GND are placed horizontally so that they can be easily lined up. VDD is on the top and GND is on the bottom. Ntap is placed on the upper right corner and Ptap is placed on lower left side of layout. It will benefit the combining of blocks. VDD and GND can be shared without conflict.

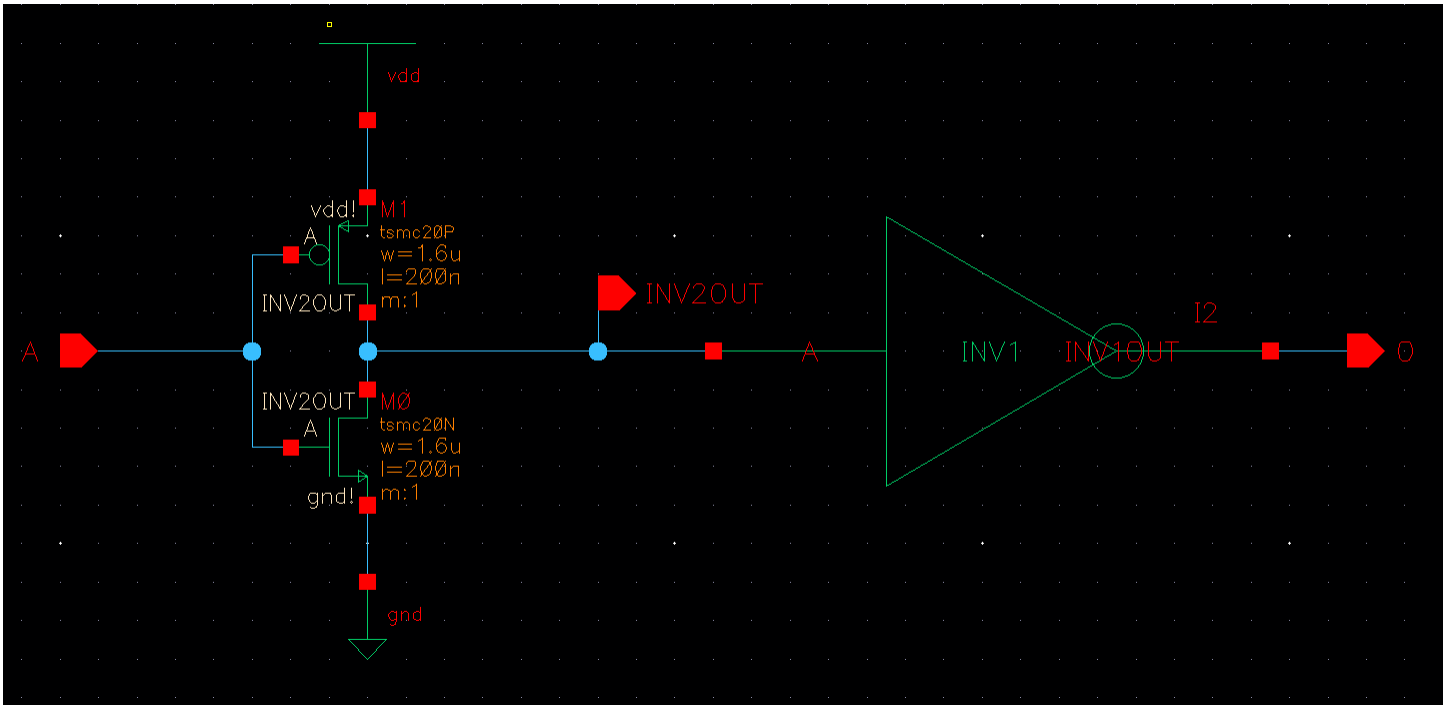
4. SPECTRE input and output waveforms for each gate schematic simulation in the form of images showing the waveforms.

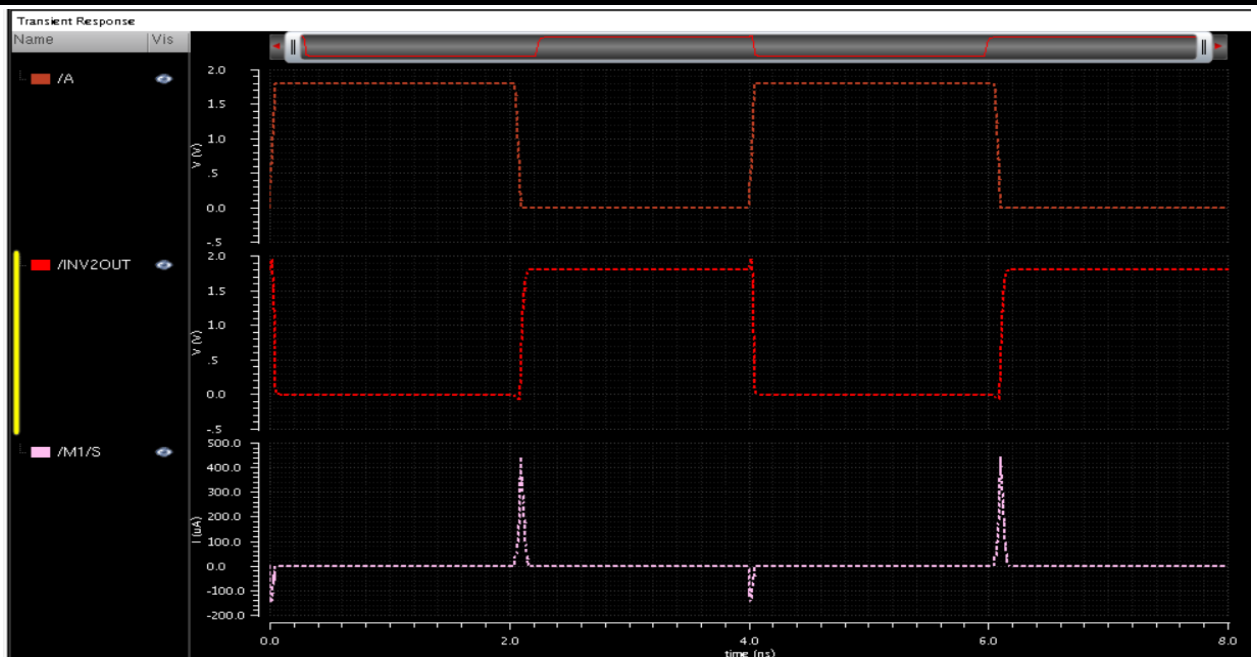
A. INV1



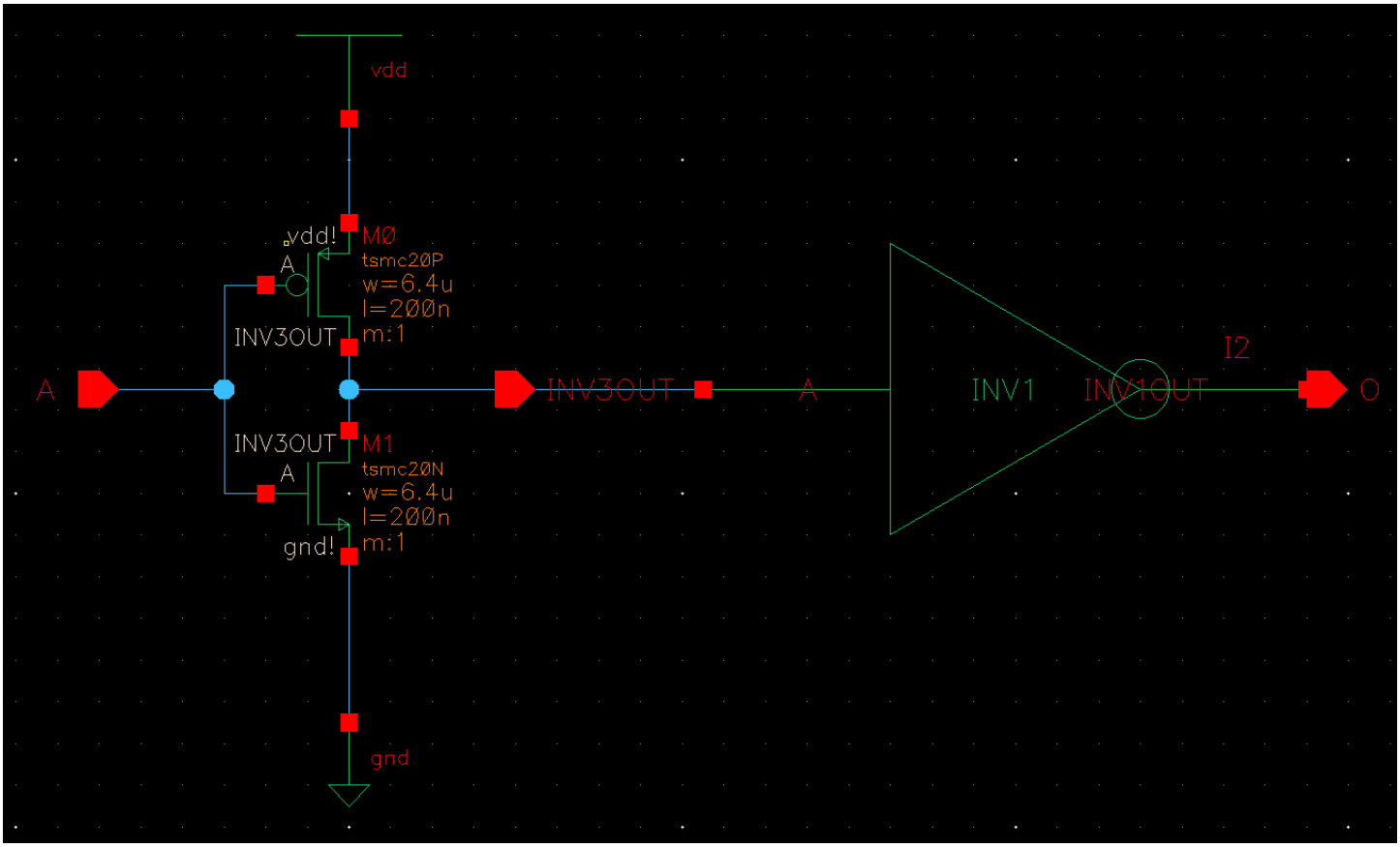


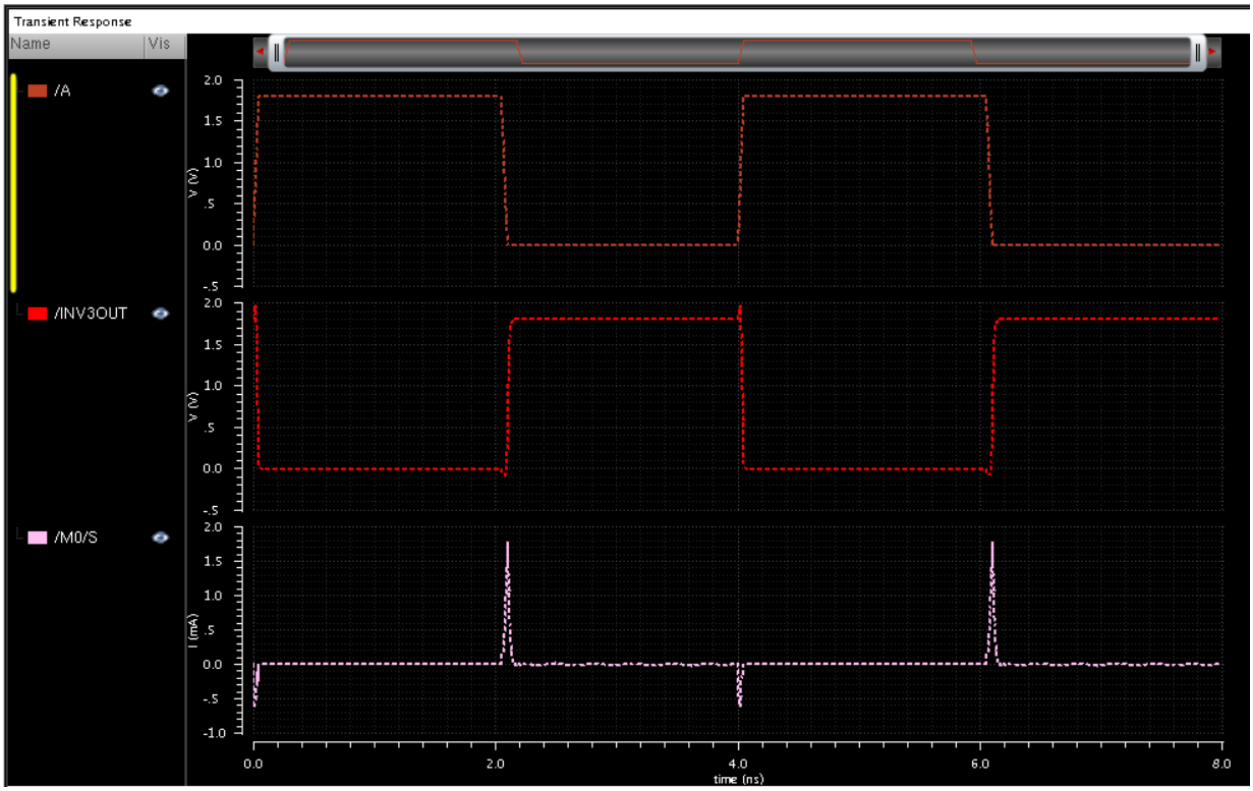
B. INV2


vdd
vdd!
M1
tsmc20P
w=1.6u
l=200n
m:1
A
INV2OUT
INV2OUT
A
INV1
INV1OUT
I2
O
A
INV2OUT
MØ
tsmc20N
w=1.6u
l=200n
m:1
gnd!
gnd

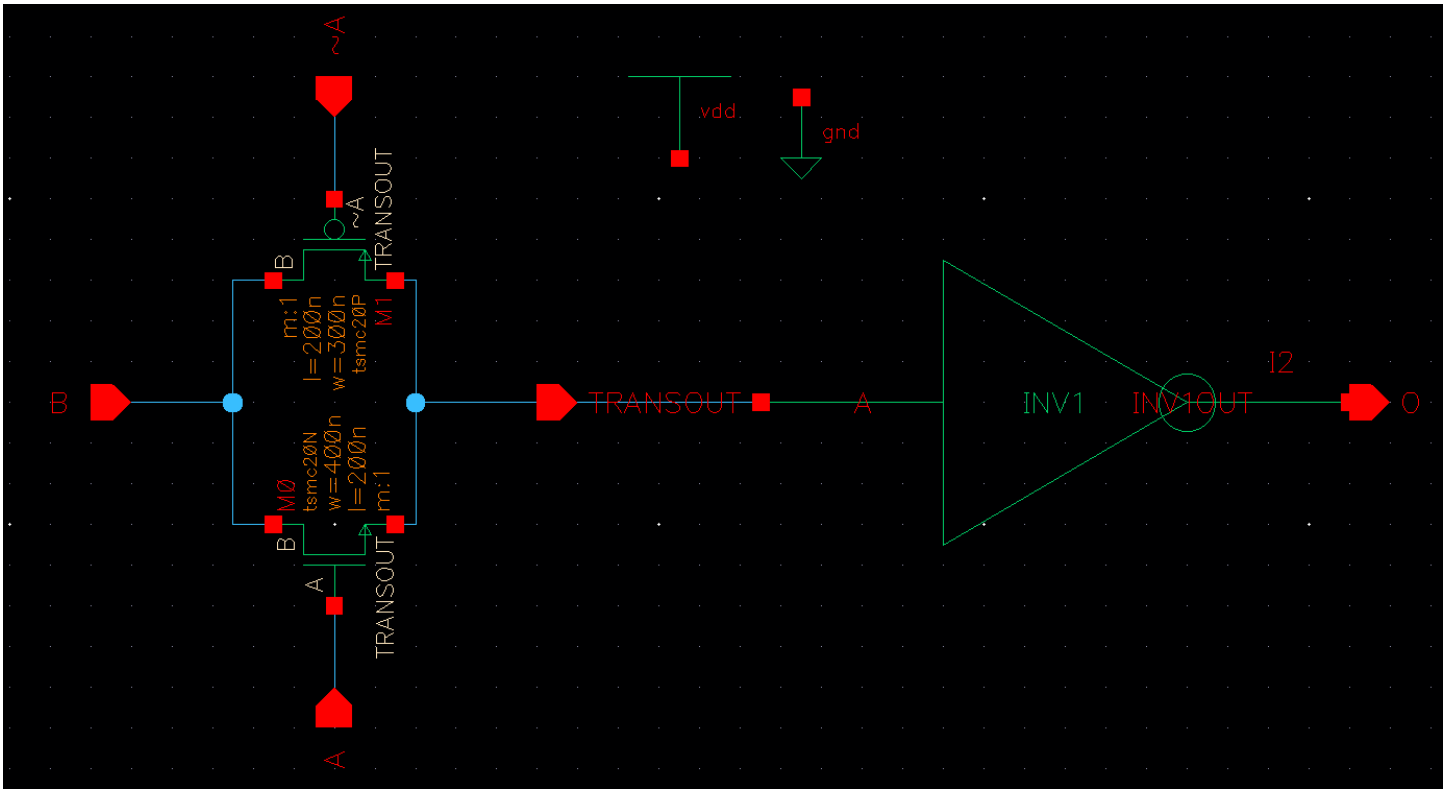

Transient Response
Name
Vis
/A
/INV2OUT
/M1/S
V (V)
I (uA)
time (ns)
0.0
2.0
4.0
6.0
8.0

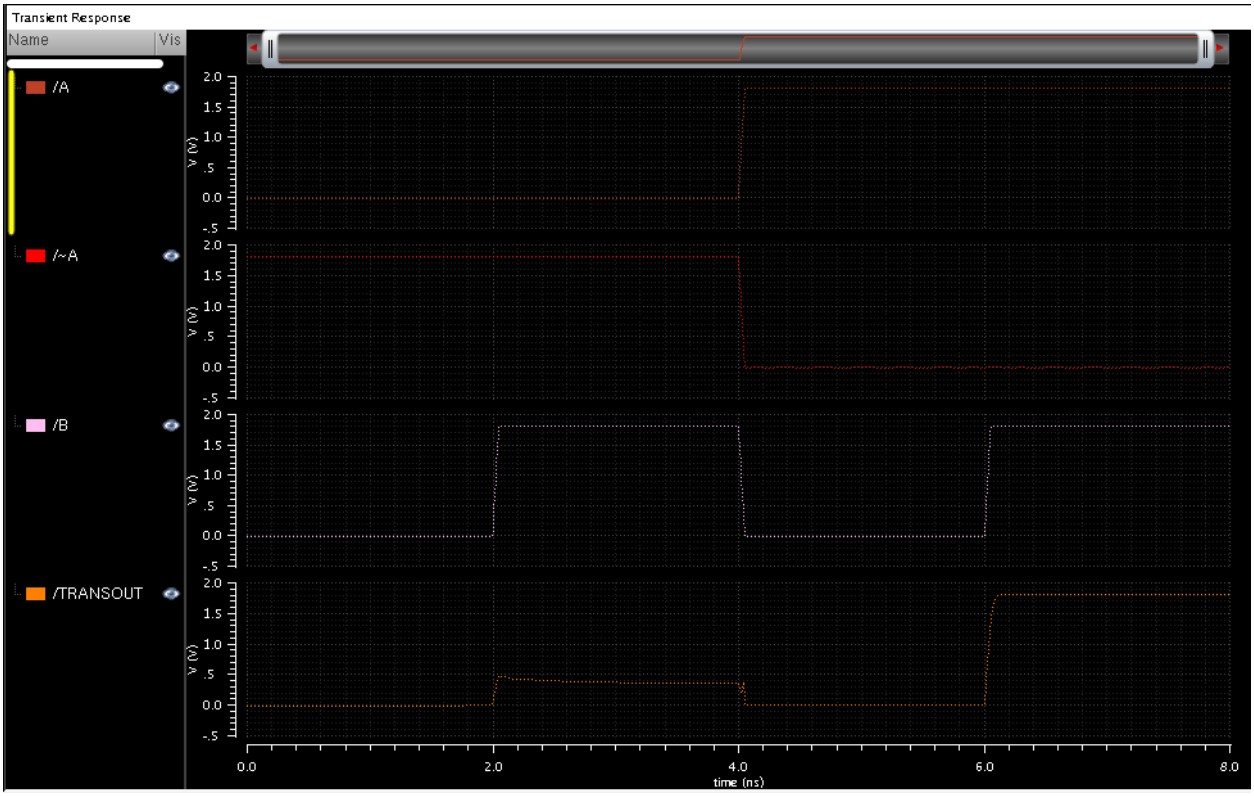
C.INV3


vdd
vdd!
M0
A
tsmc20P
w=6.4u
l=200n
INV3OUT
m:1
A
INV3OUT
INV3OUT
M1
A
tsmc20N
w=6.4u
l=200n
gnd!
m:1
gnd
INV3OUT
A
INV1
INV1OUT
I2
O

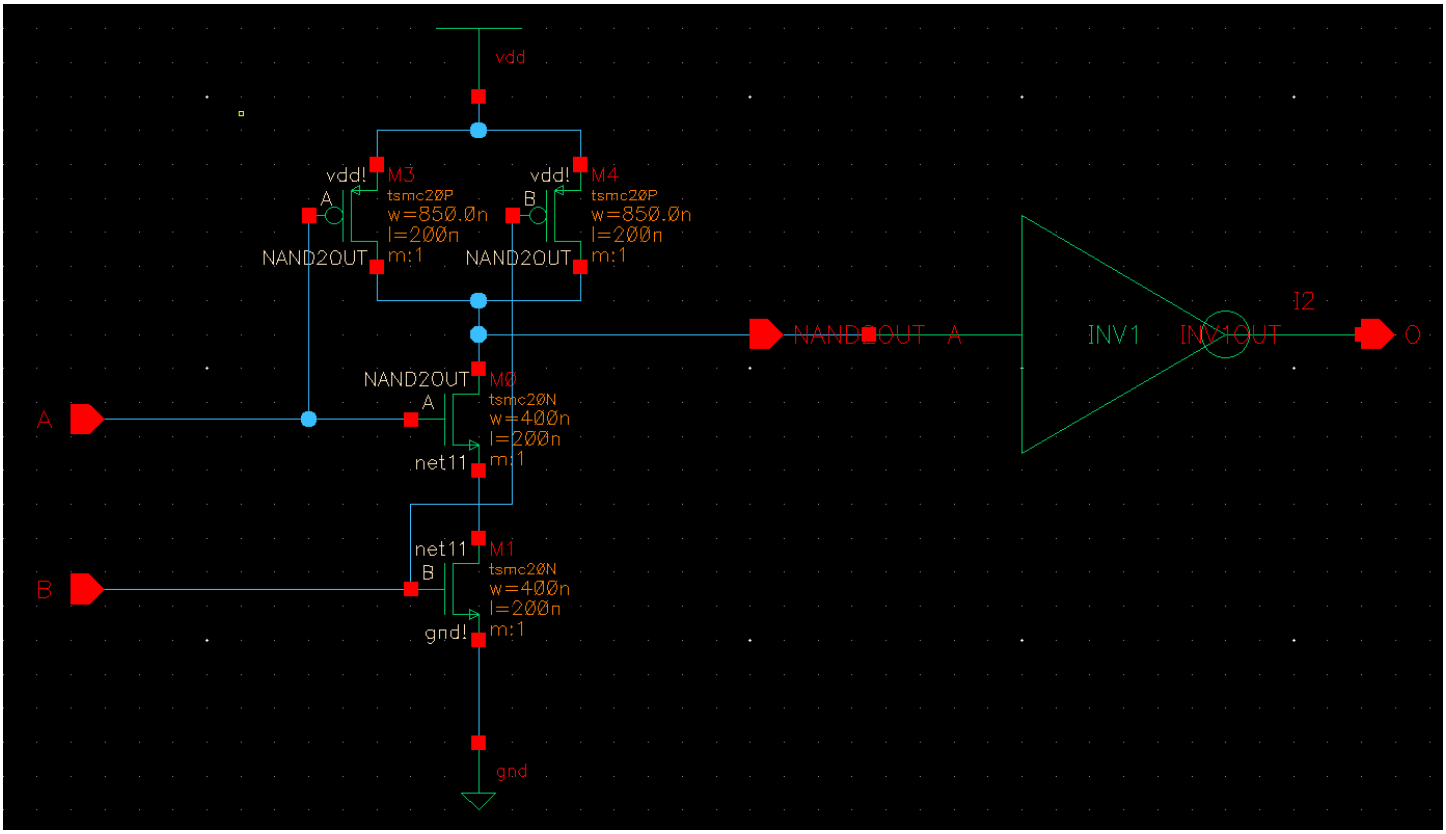

Transient Response
Name
Vis
/A
/INV3OUT
/M0/S
V (V)
I (mA)
time (ns)
0.0
2.0
4.0
6.0
8.0

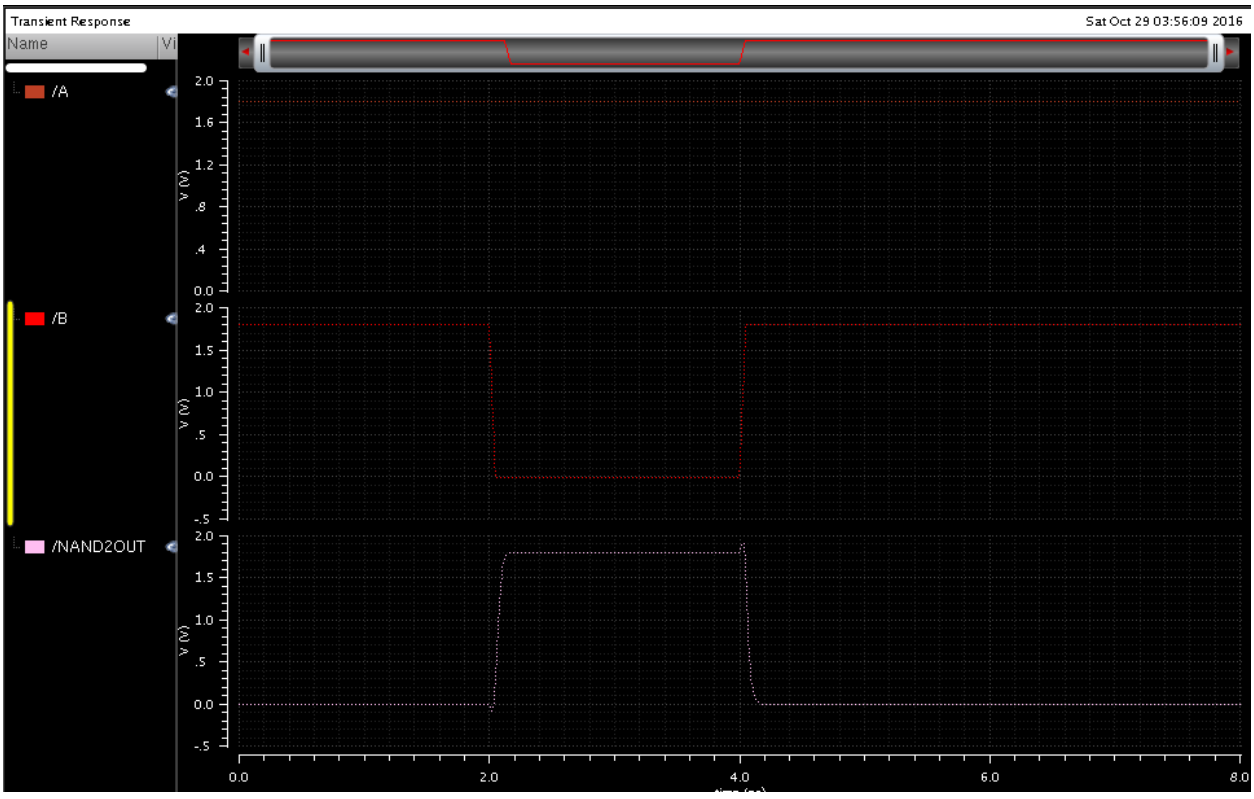
D. Transmission Gate



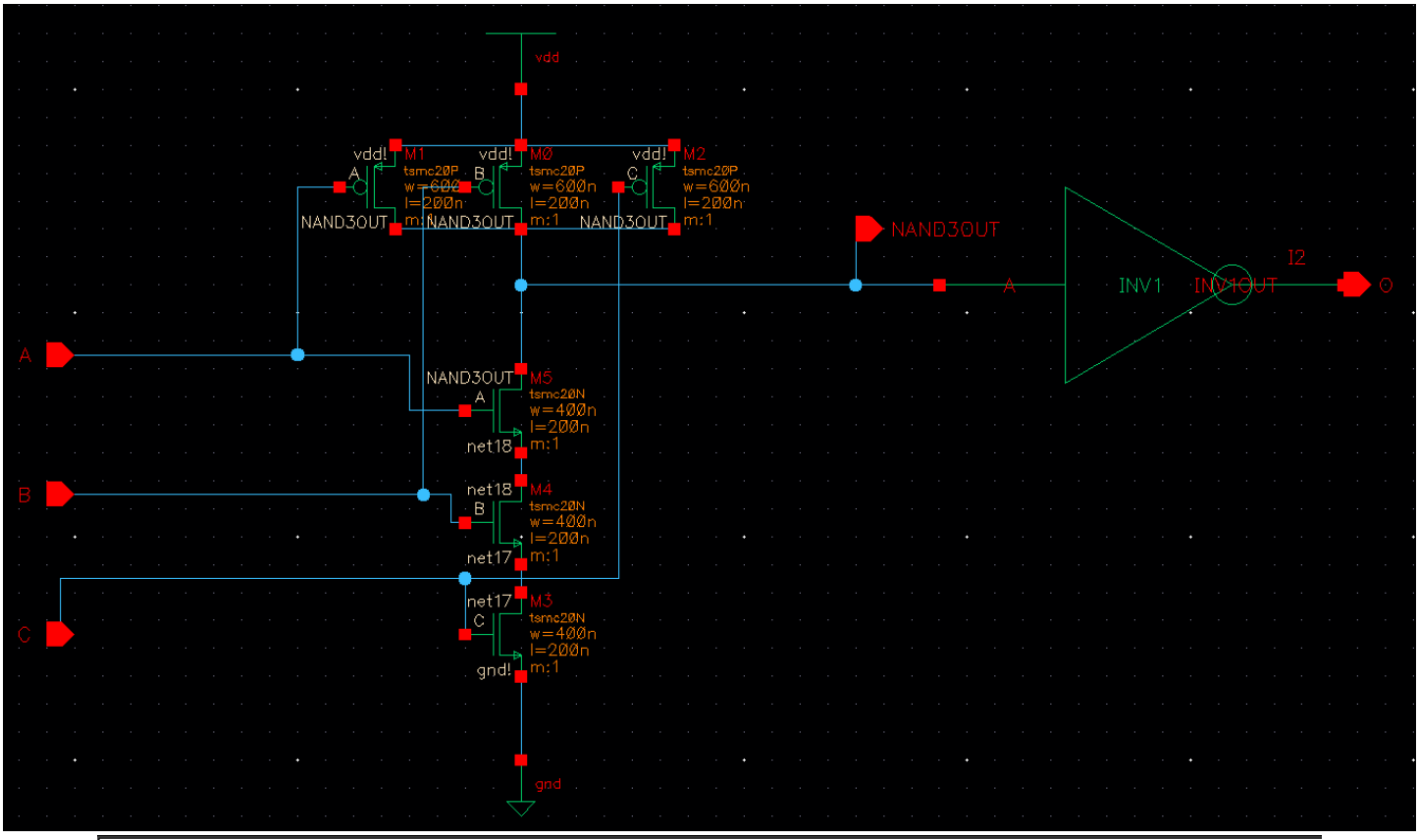


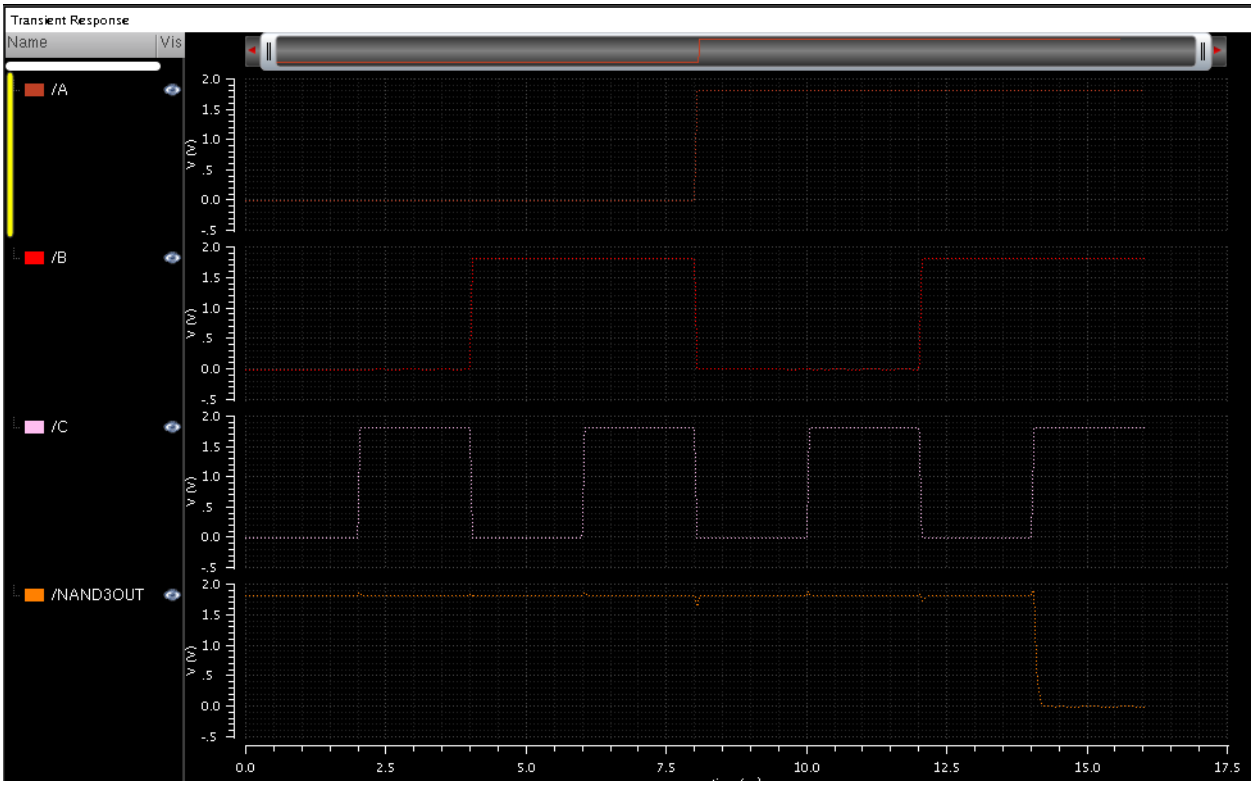
E. 2-input NAND



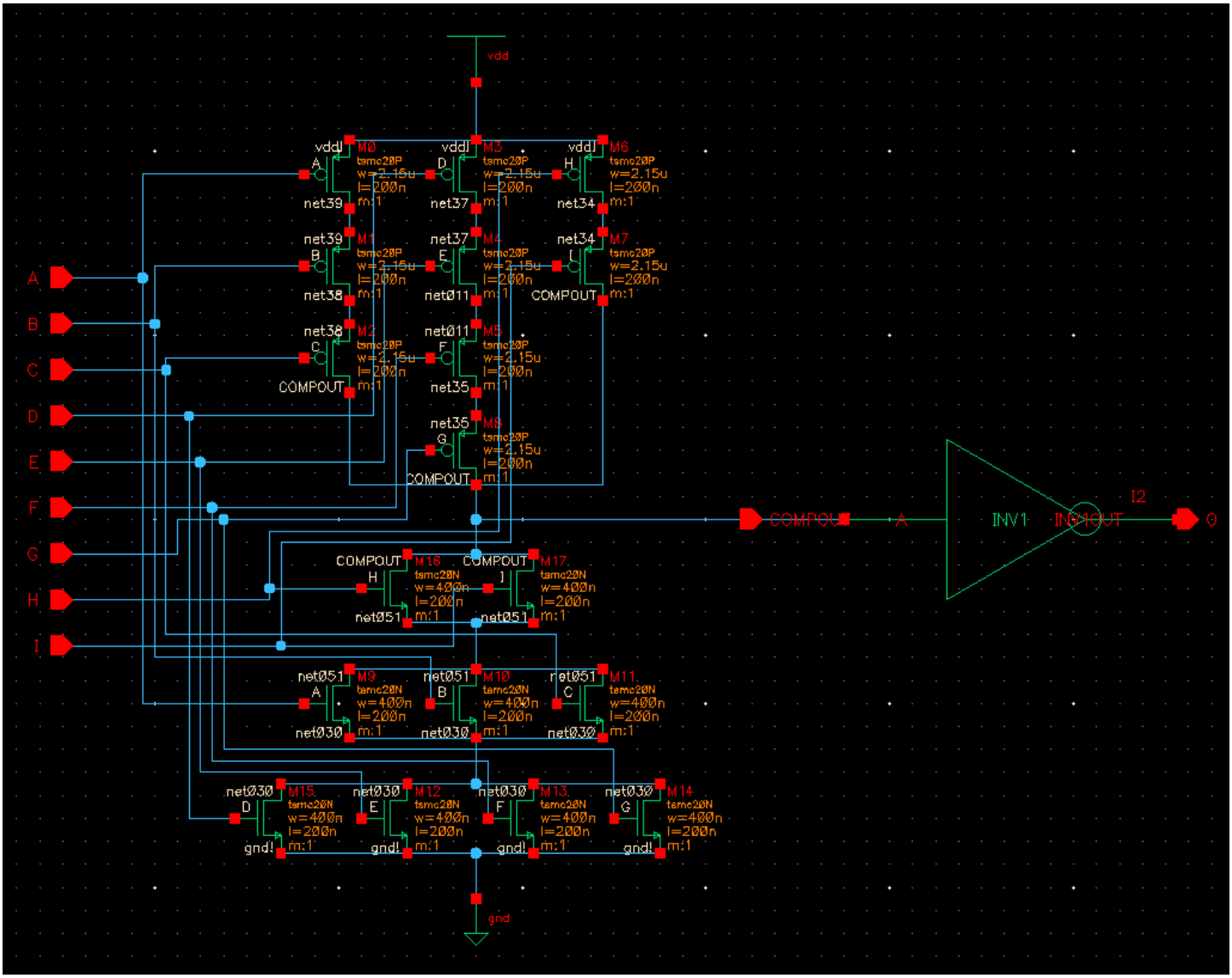


F. 3-input NAND

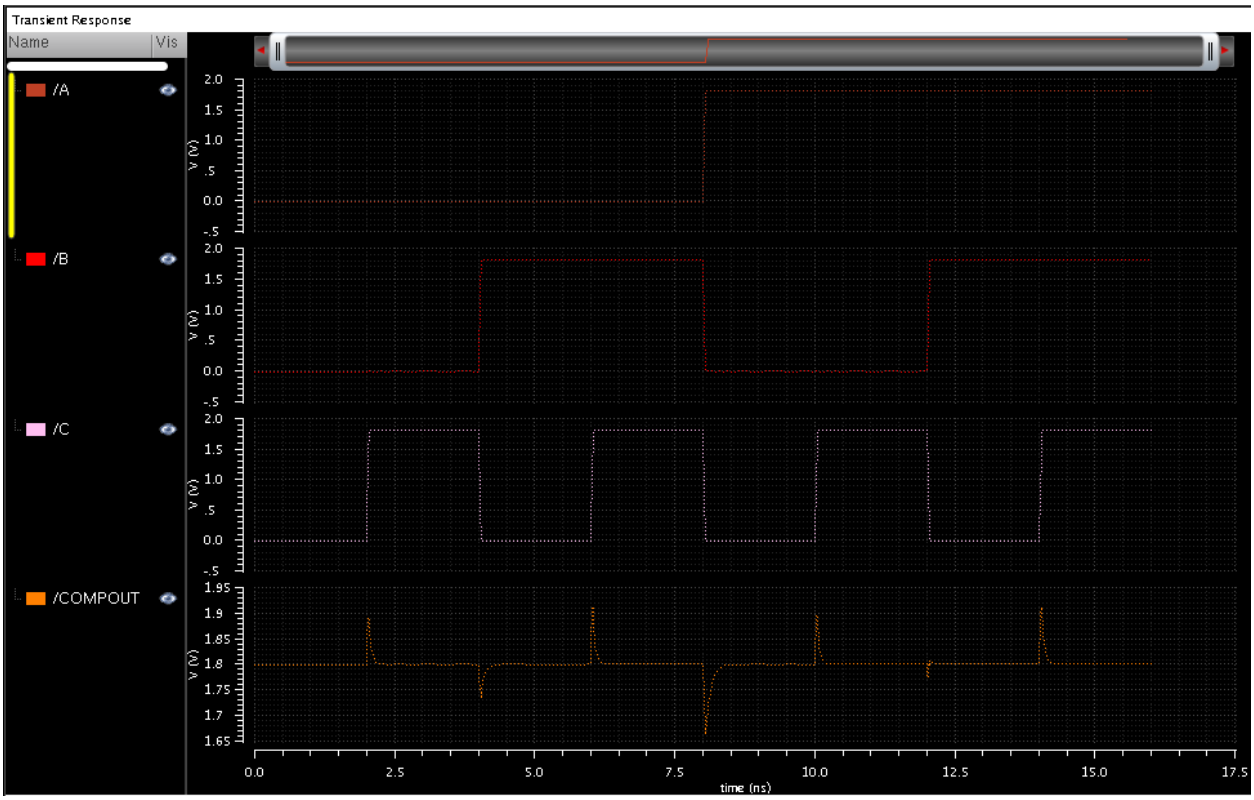




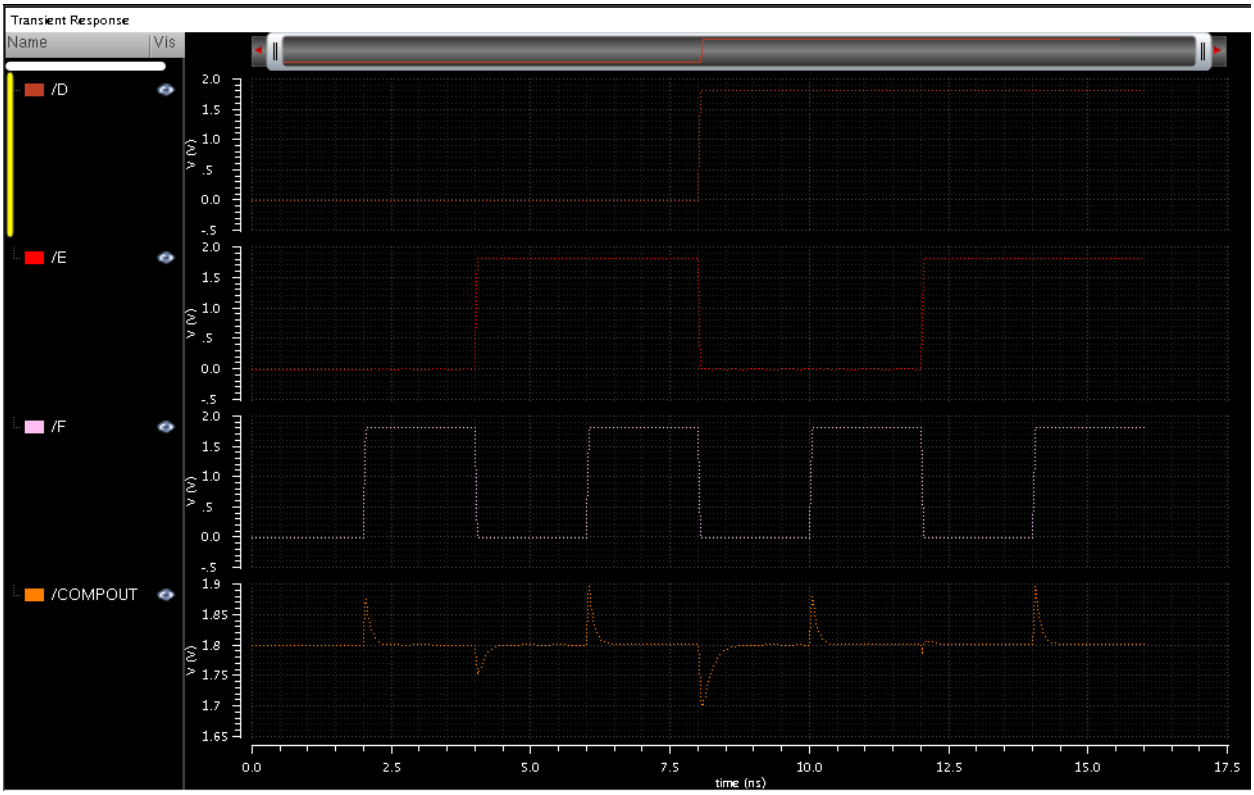
G. Compound Gate



1. all combinations of A, B, C from 000 to 111, counting up in binary 000, 001, 010, etc. , while holding DEF amd GHI to 000.

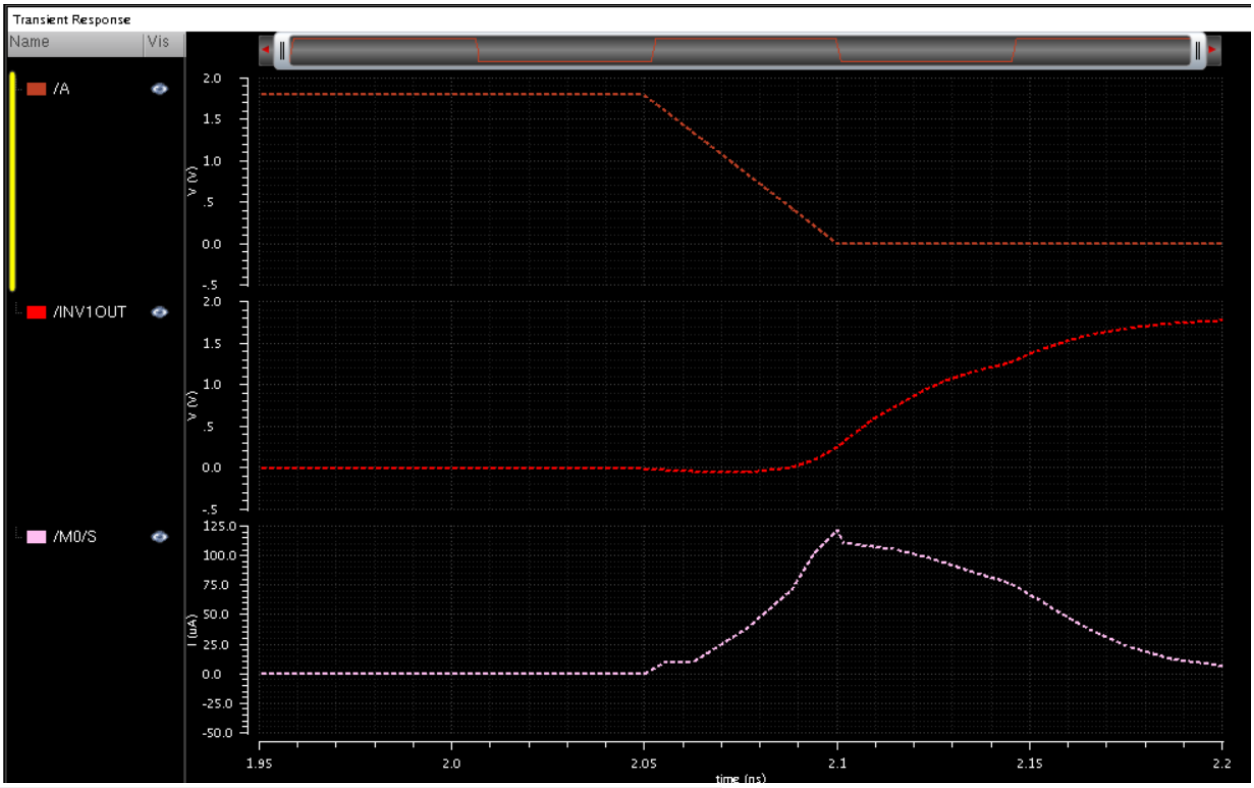


2. hold ABC=010 and GHI to 000, and then change DEF from 000 to 111



5. Results of the power computations.

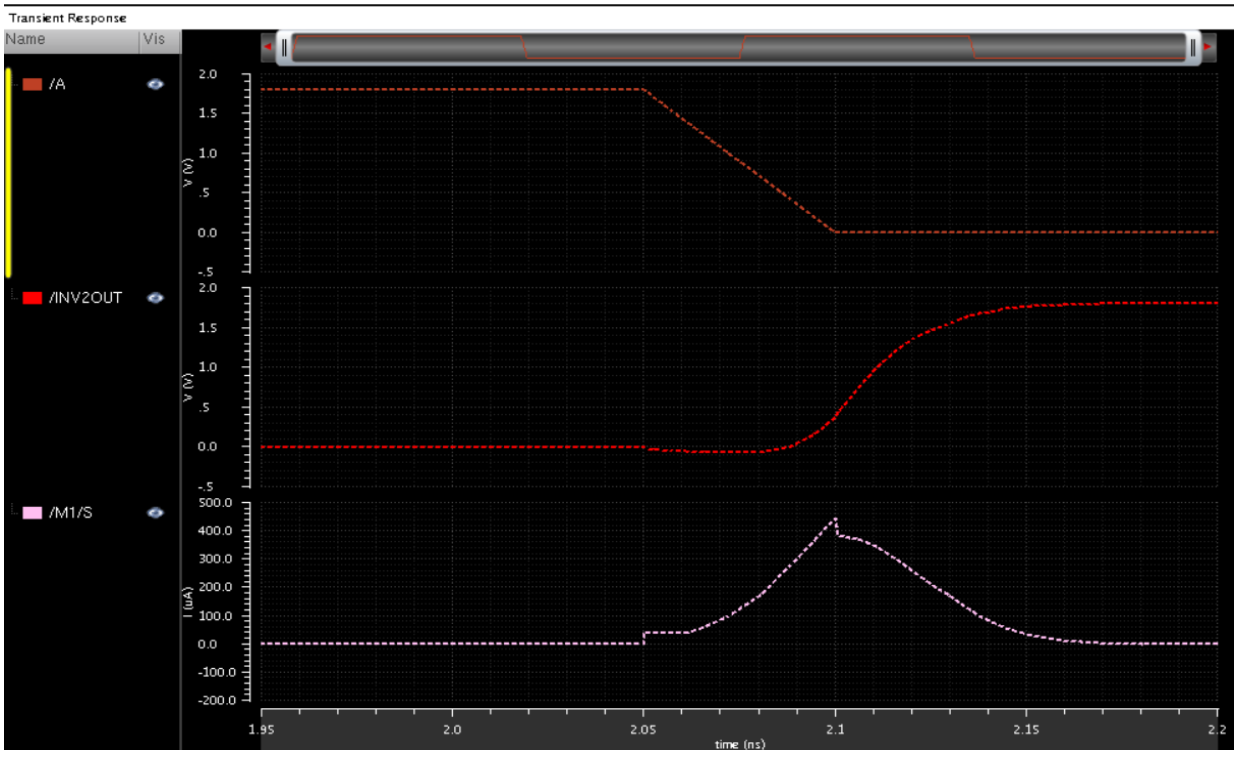
INV1



33.51E-6
average(clip(i("/M0/S" ?result "tran") 1.95E-9 2.2E-9))

The Average current flowing (the period form 0.1ns before the input falls to 0.1ns after the input become low) is 33.51*10^{-6} A, and Vdd is equal to 1.8V. The average power is 33.51*10^{-6} A*1.8V=6.032*10^{-5}W

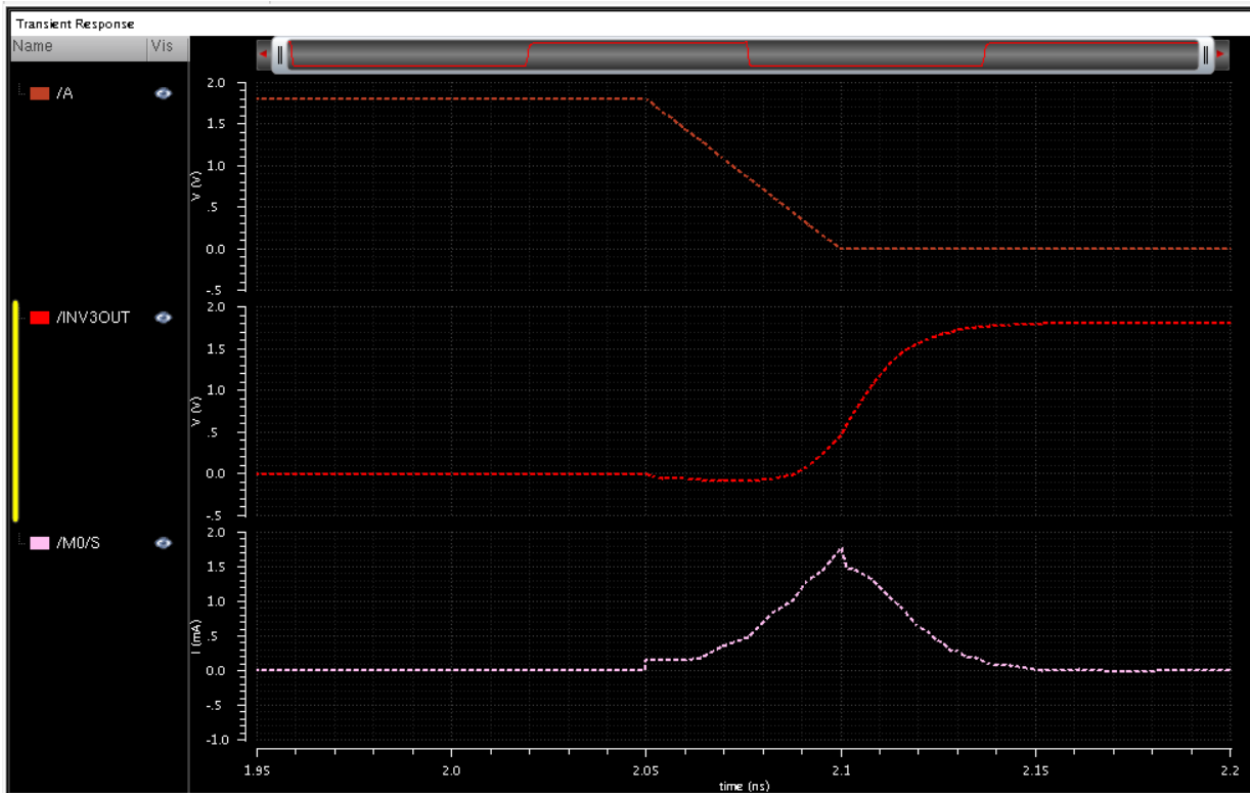
INV2



```
77.27E-6
average(clip(i("/M1/S" ?result "tran") 1.95E-9 2.2E-9))
```

The Average current flowing (the period form 0.1ns before the input falls to 0.1ns after the input become low) is 77.27*10^{-6} A, and Vdd is equal to 1.8V. The average power is 77.27 *10^{-6} A*1.8V=1.391*10^{-4}W

INV3

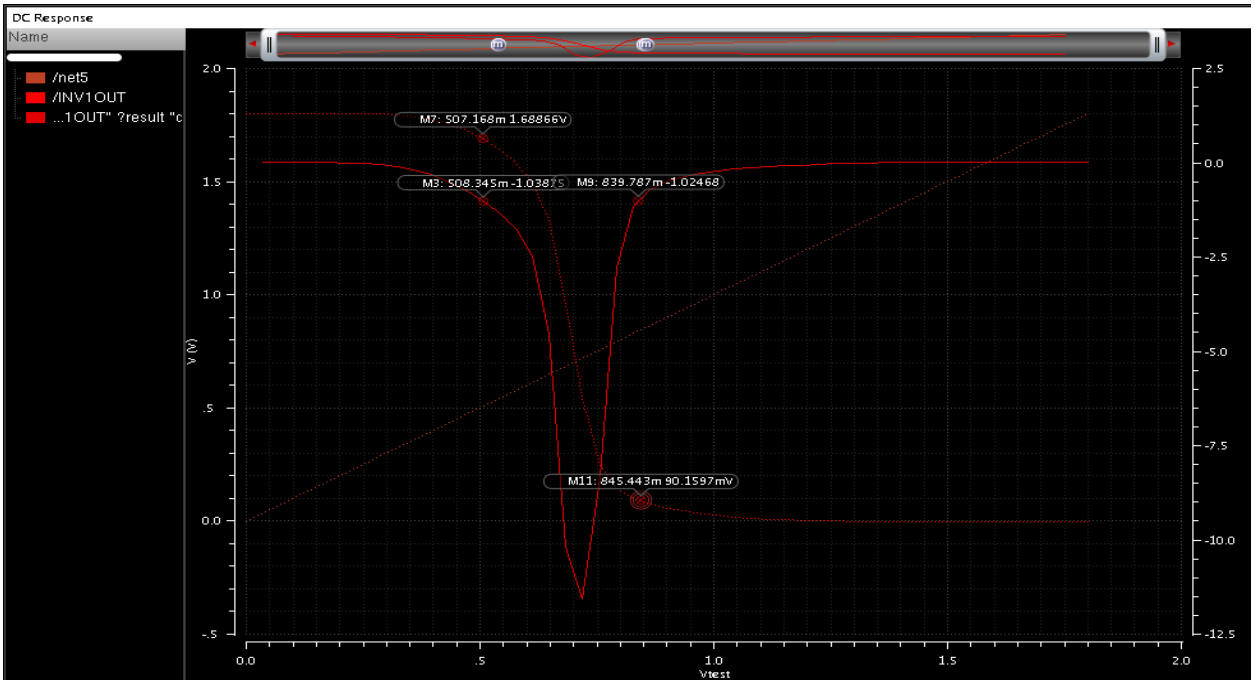



```
251.4E-6
average(clip(i("/M0/S" ?result "tran") 1.95E-9 2.2E-9))
```

The Average current flowing (the period form 0.1ns before the input falls to 0.1ns after the input become low) is 251.4*10^{-6} A, and Vdd is equal to 1.8V. The average power is 251.4*10^{-6} A*1.8V=4.525*10^{-4}W

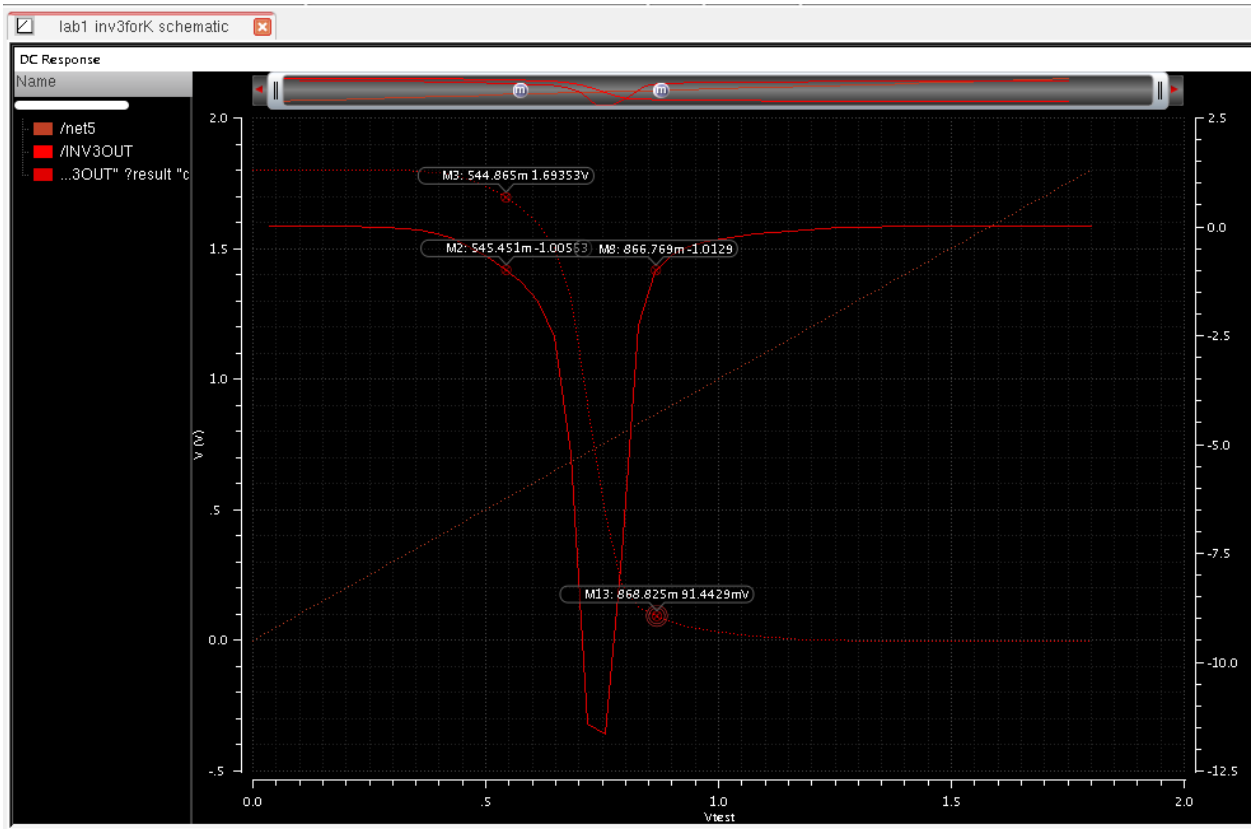
6. Results of the noise margin computations

Inv1



As shown above the VIH=1.689V VIL=0.09016. So that the low noise margin can be calculated.
NML= VIL Max – VOL Max= 0.09016-0= 0.09016V NMH= VOH Min– VIH Min= 1.8-1.689= 0.111V

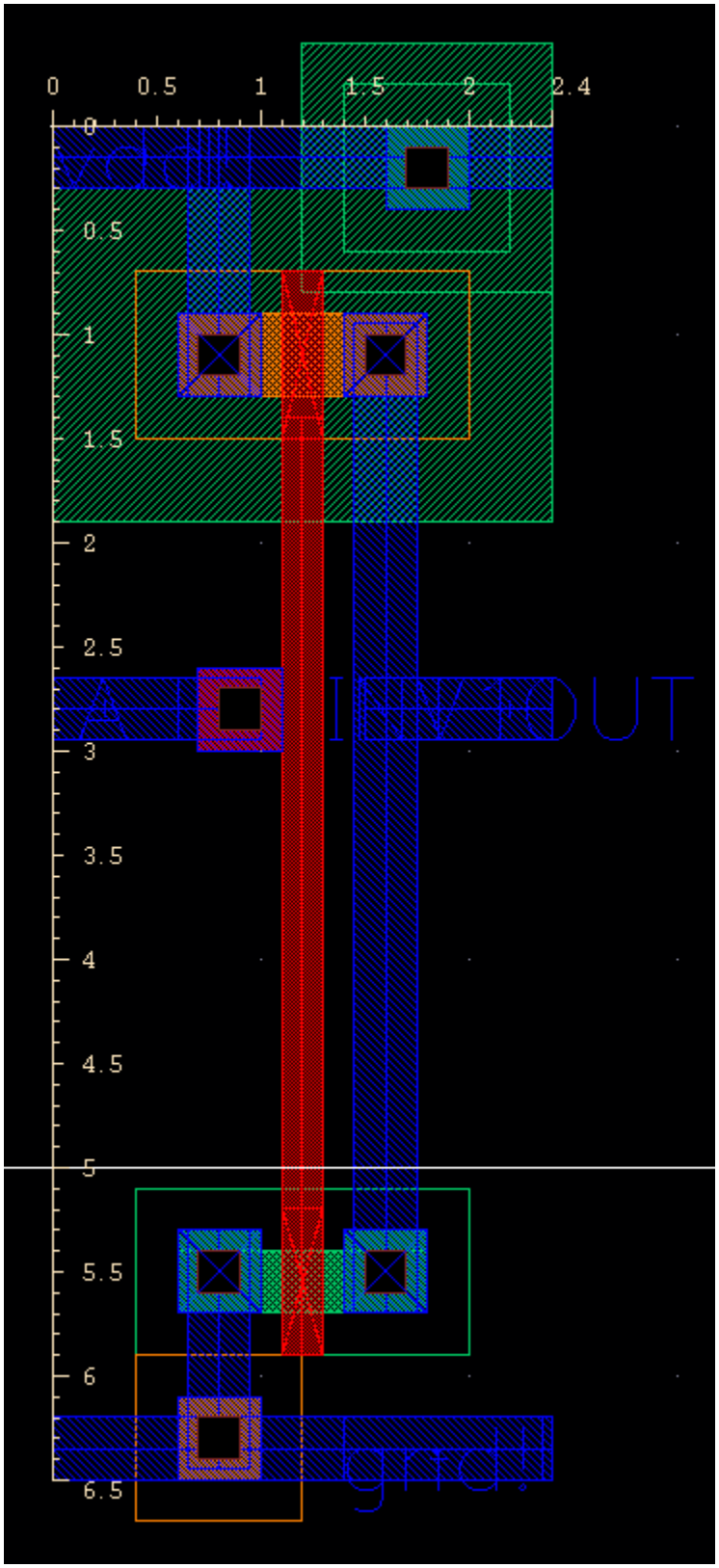
Inv3



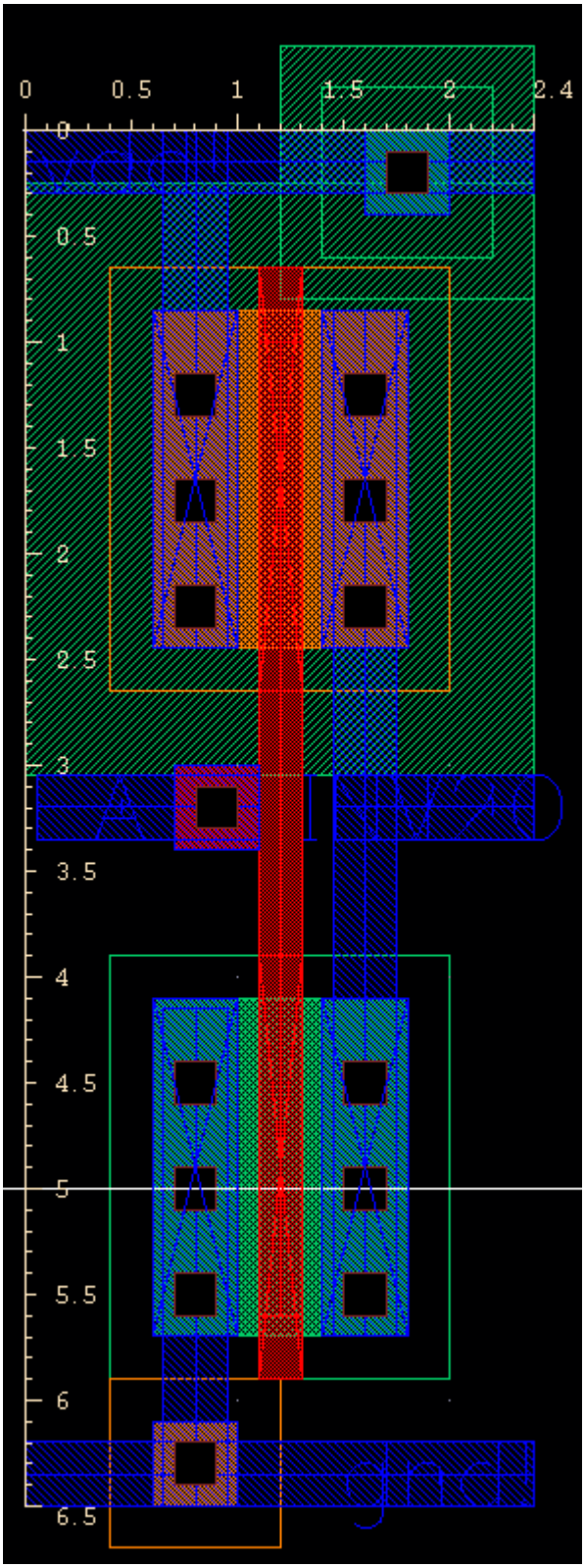
As shown above the VIH=1.694V VIL=0.09144. So that the low noise margin can be calculated.
NML= VIL Max – VOL Max= 0.09144-0= 0.09144 NMH= VOH Min– VIH Min= 1.8-1.694= 0.116V

7. Layouts of gates, captured as images

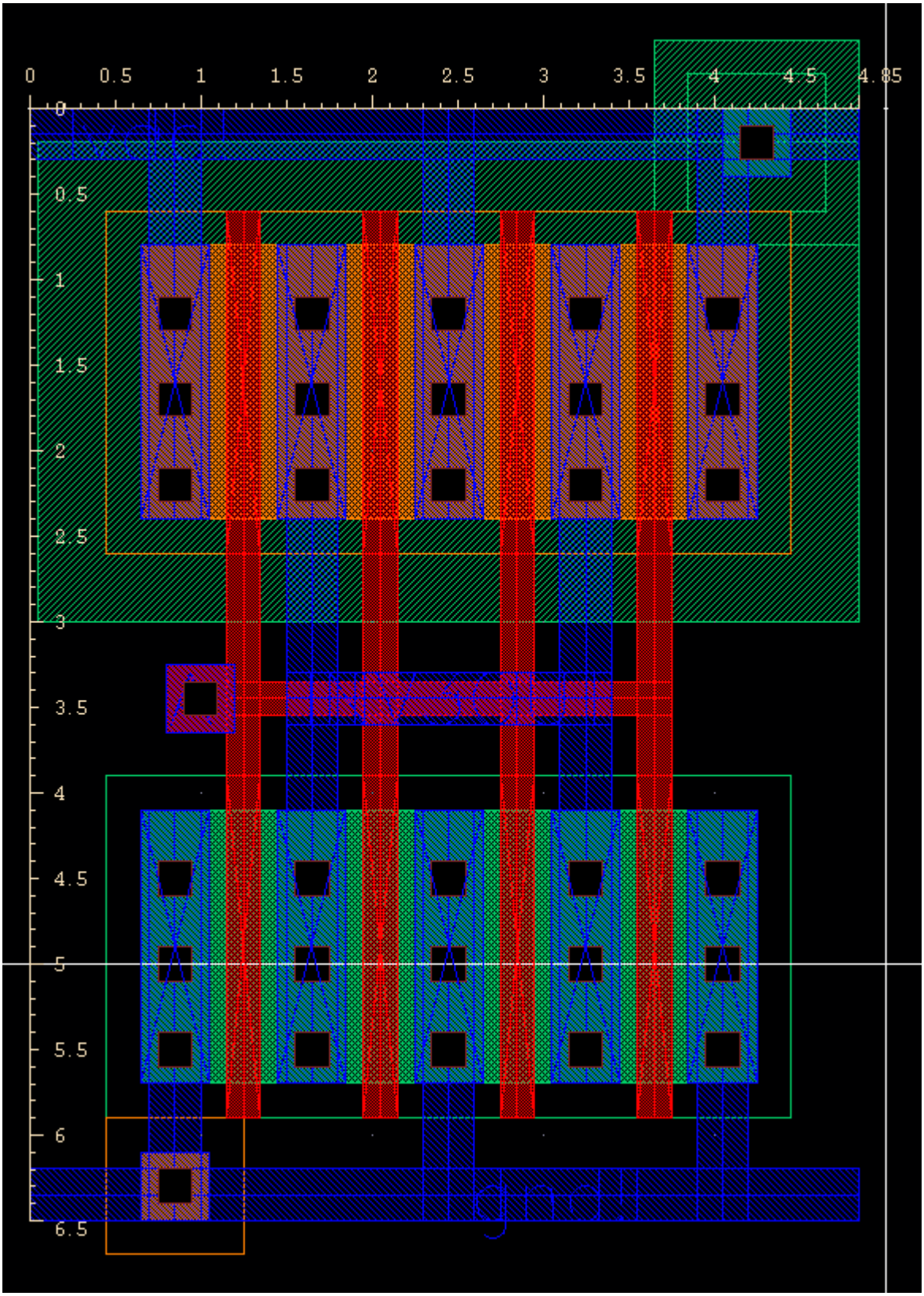
A. INV1



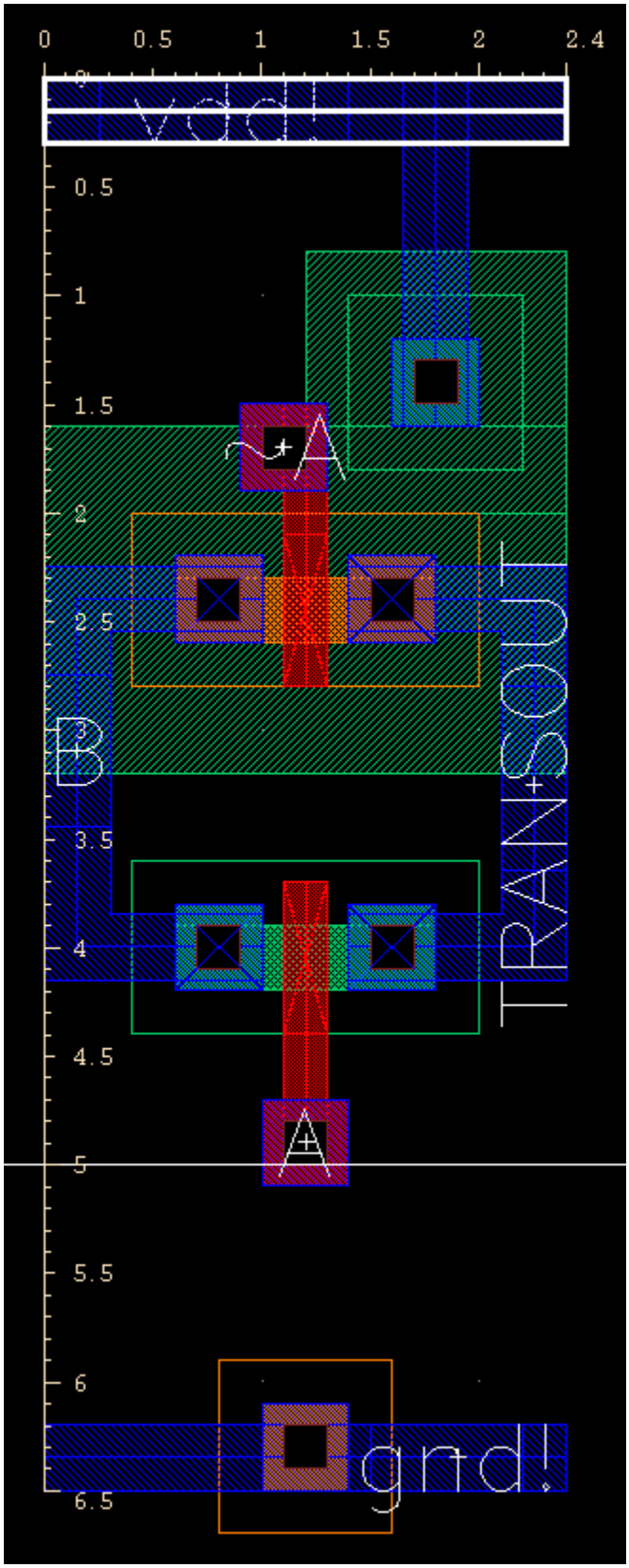
B. Inverter 2



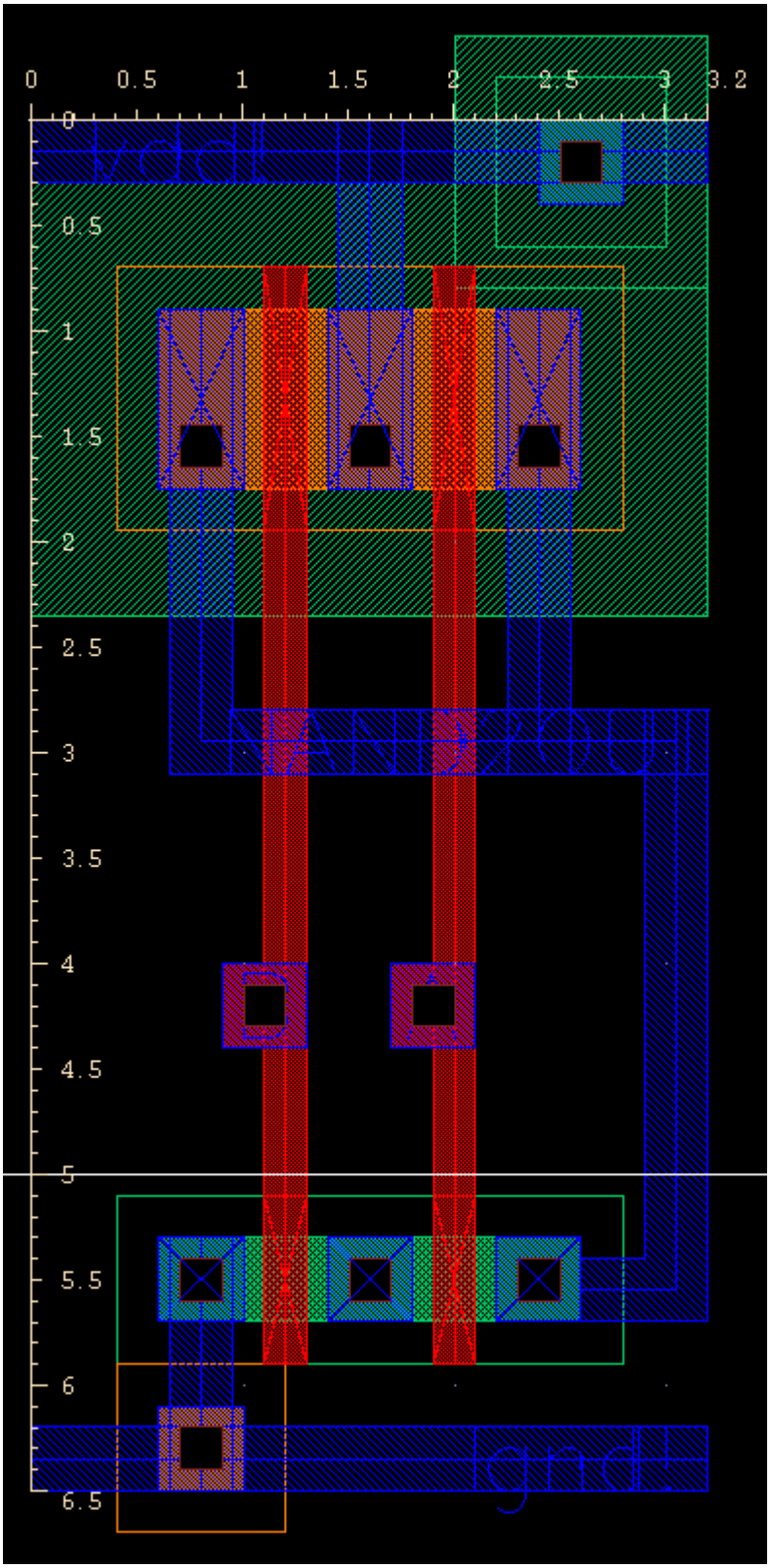
C. Inverter 3



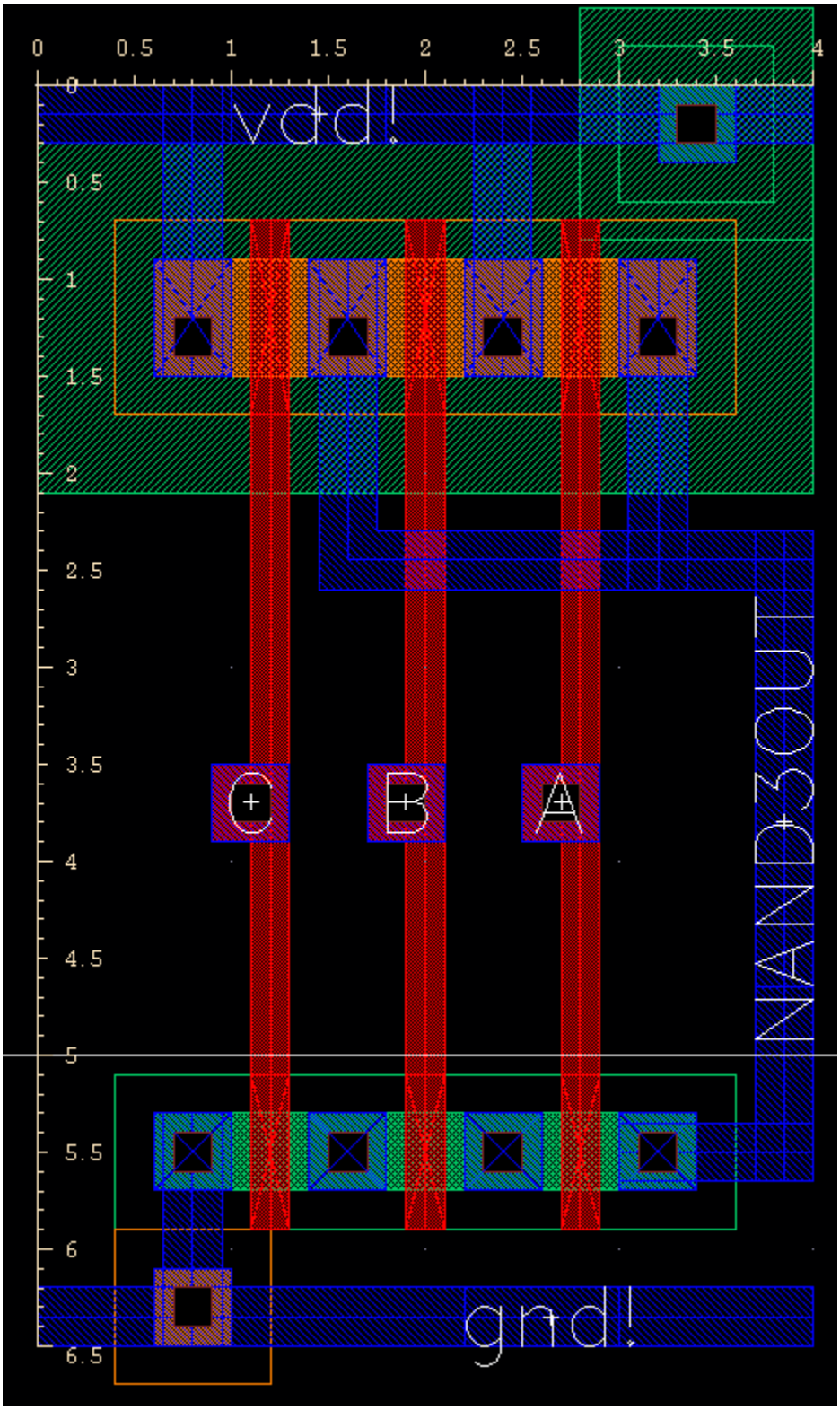
D. Transmission Gate



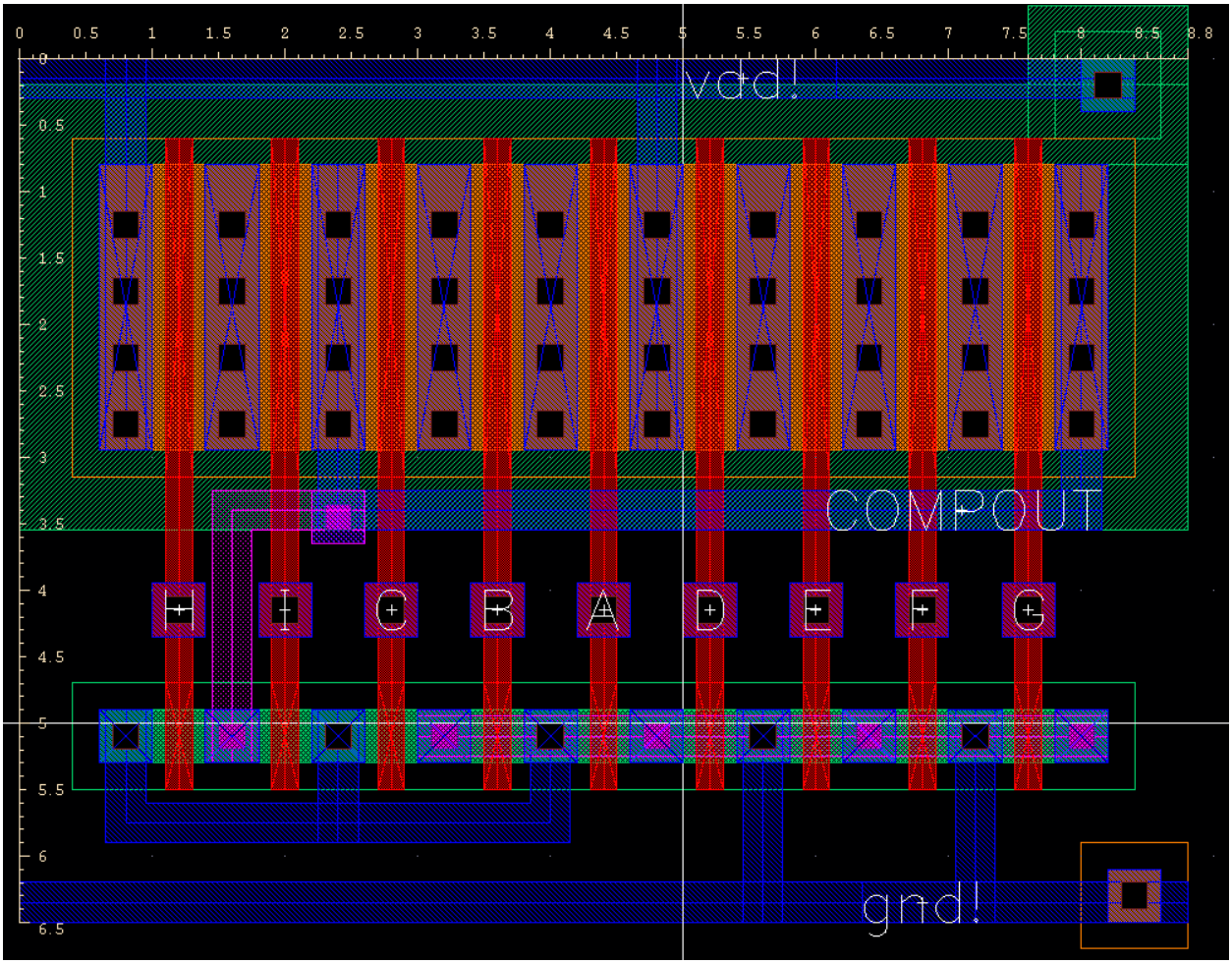
E. 2-input NAND



F. 3-input NAND



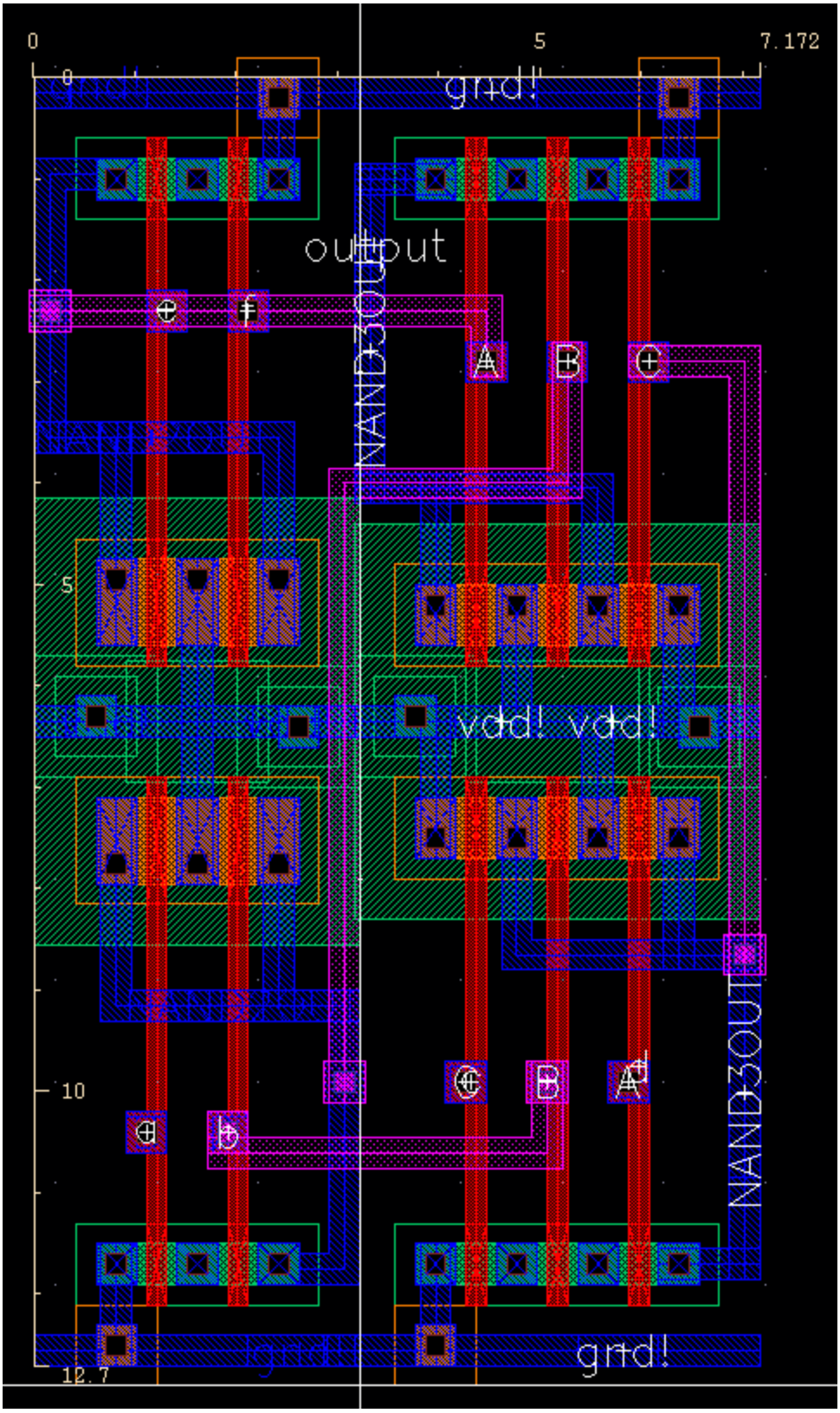
G. Compound Gate COMPOUT = NOT {[A+B+C] *[D+E+F+G]* [H+I]}



8. Table of cell sizes

Name	Height(m)	Width(m)	Area(m)
INV1	6.5E-06	2.4E-06	1.56E-11
INV2	6.5E-06	2.4E-06	1.56E-11
INV3	6.5E-06	4.9E-06	3.153E-11
TRANS	6.5E-06	2.4E-06	1.56E-11
NAND2	6.5E-06	3.2E-06	2.08E-11
NAND3	6.5E-06	4E-06	2.6E-11
COMP	6.5E-06	8.8E-06	5.72E-11

9. Layout of the logic block, captured as an image.



10. Conclusions

This lab is time consuming and provided a good practice in VLSI design.

For the compound gate sizing, I initially draw the schematic in the order of ABC DEFG HI for the nmos form COMPOUT to GND, however, it is not easy to make the number of capacitors to charge and to discharge equal for the worst case. I moved the DEFG to the bottom directly connected to the ground. And I got the worst case raise fall time by first discharging all capacitors (make ADH=111 others = 0) then charge the circuit through DEFG (make AH=11 others =0), which is worst case rise, then discharge all through ADH (make ADH=111 others = 0), which is worst case fall. 4RCHP=3RCHN

When trying to figure out Euler path, I noticed that I have to make ABC nmos in the middle in order to go over all the transistors once.