EE552 HW8

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2.Sequencer Design

a. i.

-h: show the help information

-eqn file generate logic description in EQN format

-cg generate complex gates

-gc generate generalized C elements

-tm[n] technology mapping (n is the depth of search)

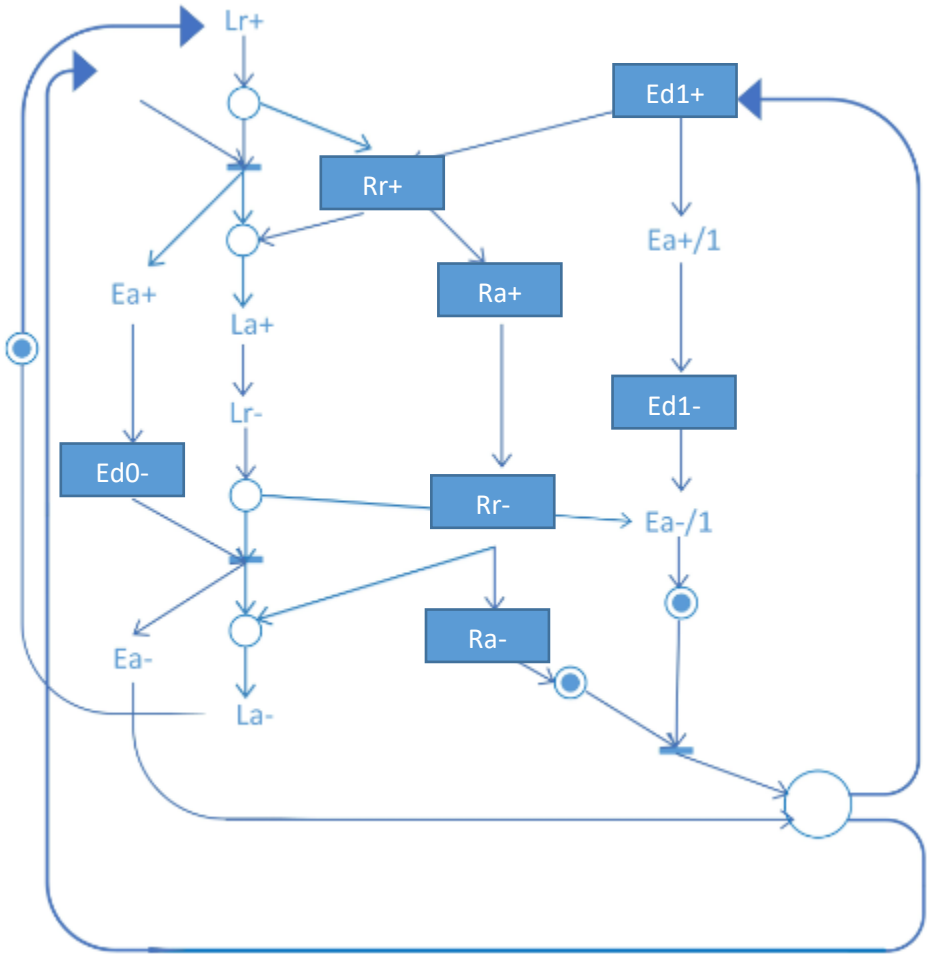
ii. draw_astg $1.g -bw -o $1.ps is to draw .g file into the .ps file and to display the .ps file.

b. because two states have conflicts.

c. S3, S6 and S10

3. SEND1of1 Design

a.



b. Circle means a place. A circle with dot inside means a place with token

4.Performance Analysis of Marked Graphs

a. a1>=a3+4-t

a2>=a4+2-t

a3>=a1+3

a3>=a2+5

a4>=a1+2

a4>=a2+3

a4>=a2+3

a1+a2+a3+a4>=a1+a2+a3+a4+4+2+5+3-2t

t>=7

b. Arrival time: A1 = 2, A2 = 0, A3 = 5, A4 = 4. Cycle time = 7

5.Slack-Matching

a. arrival times of TBs: TB0:16 TB1:16 TB2:18 TB3:18 TB4:20 TB5:20 TB6:22 TB7:22

arrival times of FAs: FA0:0 FA1:2 FA3:4 FA4:6

b. A0=A1=A2=A3=B0=B1=B2=B3=15

arrival times of TBs: all equals 15

arrival times of FAs: FA0:0 FA1:2 FA3:4 FA4:6

Total number of buffer=8