Howard Fu

817 W 30TH ST, LOS ANGELES, CA 90007 | (302) 563-6256 | huayufu@usc.edu | http://huayufu.xyz

SUMMARY

Master's Student in Computer Engineering will graduate in May 2018, specializing in ***Digital Design*** and ***Computer Architecture*** with added emphasis on ***Object Oriented Programming*** and ***Embedded Systems***, and insight on *Engineering Leadership*.

EDUCATION

University of Southern California, Los Angeles, CA GPA: 3.61 May 2018

Master of Science, Computer Engineering, Digital VLSI and Computer Architecture

University of Delaware, Newark, DE GPA: 3.5 May 2016

Bachelor of Electrical Engineering, Minor in Computer Science

SKILLS

Programming: VHDL, Verilog, C/C++, Python, Perl, Tcl, Assembly

Digital Design: SRAM design, FSM design, Logic Effort, Power Optimization, RTL design, Handshake Protocol, ASIC/FPGA Design Flow, Static Timing Analysis

System and Tools: Linux/Unix, Git, Xilinx ISE, Cadence Virtuoso, Design Compiler, IC Compiler II, ModelSim, HSPICE

EXPERIENCES

Technical Intern, ***R&D, ECO team, Synopsys*** [C++, Tcl, IC Compiler II, gdb, Perforce, EDA] May - August 2017

- Proposed an algorithmic and memory efficiency base layer density aware model for eco/spare cell placement to reduce the turnaround time by avoiding base layer density violations in earlier stage at backend design flow
- Implemented the model in the main branch of *IC Compiler II* on remote *Unix server* with *version control tools* and *gdb* in *C++,* tested the model with the Tcl test scripts, successfully demonstrated the correctness of the model
- Created high efficiency and high accuracy place-able region locating service with the visualization on *ICC II GUI*

Project Leader, *General-Purpose 16-bit CPU Full-customize Design Project* [Python, Cadence Virtuoso] March- April 2017

- Designed a 5-stage pipelined CPU, featuring 512-bit SRAM and 16-byte register file, supports add/sub, multiply, and/or, SFL/SFR, and store/load instructions
- Programmed frontend and backend python code for instruction decoding and golden result generation
- Conducted *layout drawing*, performed *Power & Delay optimization* and employed *power gating* and *dynamic logic* techniques, and achieved 3.5ns clock period and 9.3 mW power consumption in performance

Digital Neuron VLSI Design Contest [Cadence Virtuoso] October- December 2016

- Designed a special-purpose digital circuit that mimics a neuron; performed *logic* and *timing verification*
- Won ***third place*** in Design Contest with the area-delay product of 695 (average 7000)

PROJECTS

Operating System Course Project [C, Multi-Threading, Linux, gdb] March- May 2017

- Created multi-threaded program using C and POSIX API, emulated the process of token bucket with the statistical summary, with the concern of mutual exclusive and deadlock.
- Implemented a Linux similar operating system, Weenix in C programming language. Completed a UNIX-like multi-threaded/ processed kernel with Virt*ual File-System(VFS)* layer and a *Virtual Memory (VM)* layer in a team of 4

Asynchronous Design of Tree-structured Network-on-Chip (NoC) with FEC [Verilog, SystemVerilog, modelsim] March 2017

- Designed a NoC with router, arbiter, merge and hamming code module; Synthesized into gate cells with *PCHB* templates

Dual-clock Asynchronous FIFO [Verilog, ModelSim, CDC (clock domain crossing)] February 2017

- Designed Dual-clock FIFO with pointer synchronizer, featuring gray code converter to reduce metastability

Music Visualizer Embedded System (SoC) Design [Xilinx IDE, FPGA, EDK, SDK, VHDL, C, Python] February- May 2016

- Designed a Music Visualizer with VGA output prototyped on Spartan-6 FPGA board
- Created *VHDL* peripherals for fetching audio input, programmed audio processing and visualization algorithm running in ARM-based IP-core in *FPGA* board, and programmed controller to control Visualizer through *UART* port
- Empowered the *FPGA* board to output smooth patterns to VGA port, with two different display modes