

OSノード0

(1) ICRへの
書き込み

コア0

LAPIC

ICR

OSノード1

(3) 割り込み処理の開始

コア1

LAPIC

(2) IPIの送信

The diagram illustrates the process of Inter-Processor Interrupt (IPI) transmission between two OS nodes, OSノード0 and OSノード1, which are separated by a vertical dashed line. OSノード0 contains コア0 (Core 0), which includes a LAPIC (Local APIC) and an ICR (Interrupt Command Register). An arrow labeled (1) ICRへの書き込み (Writing to ICR) points from the OSノード0 box to the ICR box. OSノード1 contains コア1 (Core 1), which includes a LAPIC. An arrow labeled (2) IPIの送信 (IPI transmission) originates from the LAPIC in コア0 and points to the LAPIC in コア1. Finally, an arrow labeled (3) 割り込み処理の開始 (Start of interrupt processing) points from the LAPIC in コア1 to the OSノード1 box.