

OSノード0

(1) ICRへの
書き込み

コア0

LAPIC

ICR

OSノード1

(3) 割り込み処理の開始

コア1

LAPIC

(2) IPIの送信

The diagram illustrates the process of sending an Inter-Processor Interrupt (IPI) from OS Node 0 to OS Node 1. A vertical dashed line separates the two nodes. On the left, OS Node 0 contains Core 0, which has a Local APIC (LAPIC) containing an Interrupt Command Register (ICR). An arrow labeled '(1) ICRへの書き込み' points to the ICR. A horizontal arrow labeled '(2) IPIの送信' originates from the ICR and points to the LAPIC of Core 1 in OS Node 1. An arrow labeled '(3) 割り込み処理の開始' points from the LAPIC of Core 1 to OS Node 1.