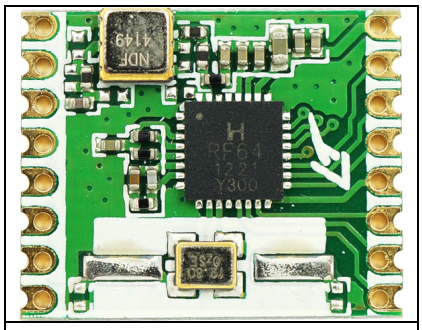
RFM64 ISM TRANSCEIVER MODULE V1.2

General Description

The RFM64 is a low cost transceiver module operating in the 433MHz frequency bands. The RFM64 is optimized for very low power consumption (3mA in receiver mode). It incorporates a baseband modem with data rates up to 150 kb/s. Data handling features include a sixty-four byte FIFO, packet handling, automatic CRC generation and data whitening. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American(FCC part15.247 and 15.249) regulatory standards.

In order to better use RFM64 modules, this specification also involves a large number of the parameters and functions of its core chip RF64's, including those IC pins which are not leaded out. All of these can help customers gain a better understanding of the performance of RFM64 modules, and enhance the application skills.



RFM64

Features

- Low Rx power consumption: 3mA
- Low Tx power consumption: 25 mA @ +10 dBm
- Good reception sensitivity: down to -104 dBm at 25 kb/s in FSK, -110 dBm at 2kb/s in OOK
- Programmable RF output power: up to +12 dBm in 8 steps
- Packet handling feature with data whitening and automatic CRC generation
- RSSI (Received Signal Strength Indicator)
- Bit rates up to 150 kb/s, NRZ coding
- On-module frequency synthesizer
- FSK and OOK modulation
- Incoming sync word recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
- Module size:19.7X16mm
- Optimized Circuit Configuration for Low-cost applications

Applications

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control
- Remote Wireless Control
- Active RFID PHY

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Acronyms

BOM	Bill Of Materials
BR	Bit Rate
BW	Bandwidth
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU
CP	Charge Pump
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesis
DLL	Dynamically Linked Library
ERP	Equivalent Radiated Power
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
Fdev	Frequency Deviation
FIFO	First In First Out
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
ID	IDentificator
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
NZIF	Near Zero Intermediate Frequency
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
POR	Power On Reset
RBW	Resolution BandWidth
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SR	Shift Register
Stby	Standby
Tx	Transmitter
uC	Microcontroller
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator
XOR	eXclusive OR

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This product datasheet contains a detailed description of the RFM64 performance and functionality.

1. General Description

The RFM64 is a s FSK and OOK transceiver module capable of operation in the 433MHz license free ISM frequency bands. It complies with both the relevant European and North American standards, EN 300-220 V2.1.1 (June 2006 release) and FCC Part 15 (10-1-2006 edition). A unique feature of this circuit is its extremely low current consumption in receiver mode of only 3mA (typ).

1.1. Simplified Block Diagram

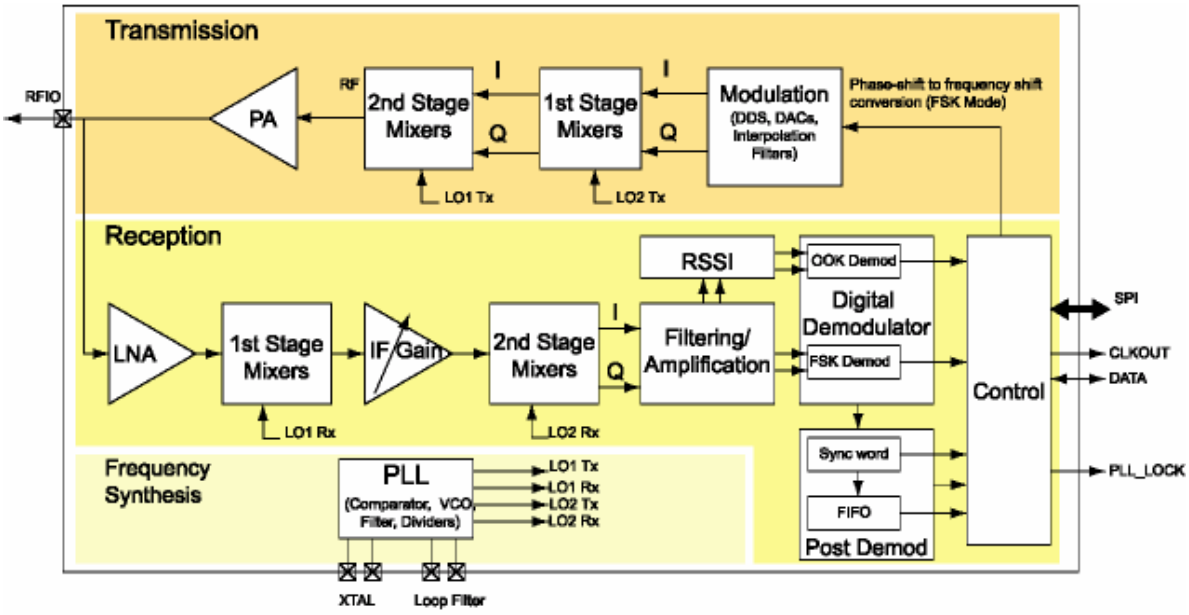

Figure 1: RFM64 Simplified Block Diagram

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1.2. Pin Diagram

The following diagram shows the pins arrangement of the package, top view.

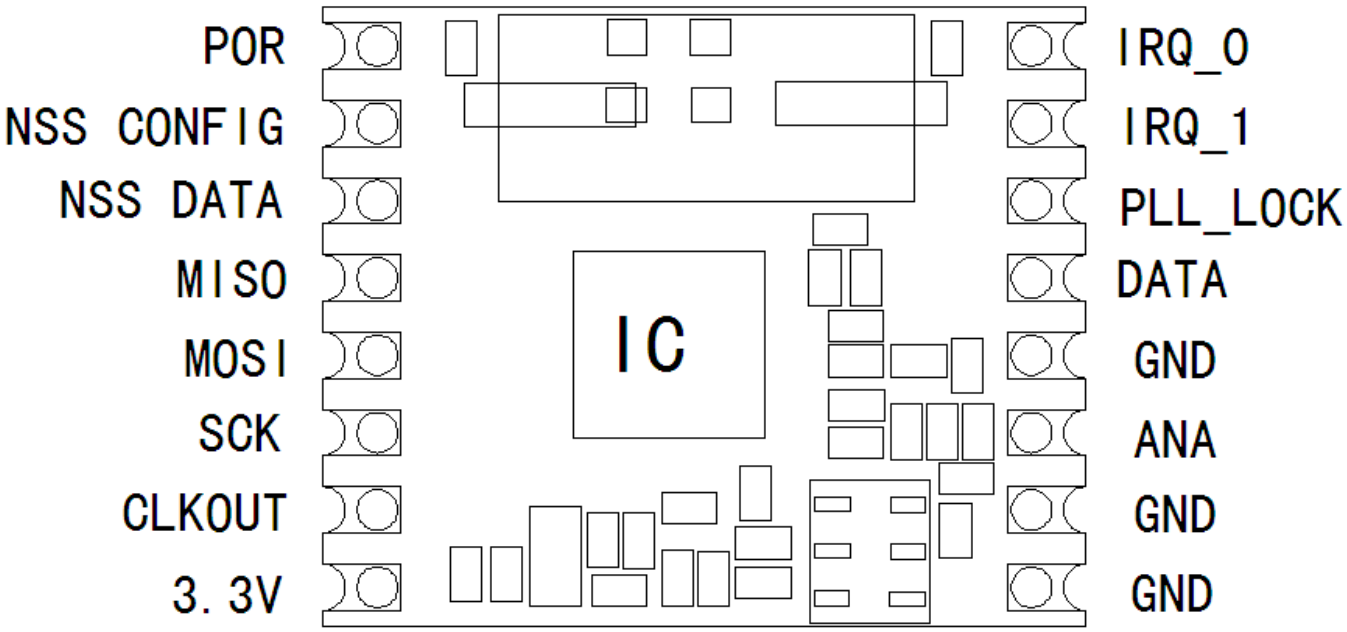

Figure 2: RFM64 Pin Diagram

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1.3. Pin Description

Table 2: RFM64 Pinouts

Number	Name	Type	Description
1	POR	I/O	POR. Do not connect if unused
2	NSS_CONFIG	I	SPI CONFIG enable
3	NSS_DATA	I	SPI DATA enable
4	MISO	O	SPI data output
5	MOSI	I	SPI data input
6	SCK	I	SPI clock input
7	CLKOUT	O	Clock output
8	3.3V	I	Supply voltage
9	GND	I	Exposed ground pad
10	GND	I	Exposed ground pad
11	ANA	I/O	RF input/output
12	GND	I	Exposed ground pad
13	DATA	I/O	NRZ data input and output (Continuous mode)
14	PLL_LOCK	O	PLL lock detection output
15	IRQ_1	O	Interrupt output
16	IRQ_0	O	Interrupt output

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2. Electrical Characteristics

2.1. ESD Notice

The RFM64 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model).
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins. It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply voltage	-0.3	3.7	V
Tmr	Storage temperature	-55	125	°C
Pmr	Input level	-	0	dBm

2.3. Operating Range

Table 4: Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply Voltage	2.1	3.6	V
Trop	Temperature	-40	+85	°C
ML	Input Level	-	0	dBm

2.4. Module Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, unless otherwise specified.

2.4.1. Power Consumption

Table 5: Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.1	2	µA
IDDST	Supply current in standby mode, CLKOUT disabled	Crystal oscillator running	-	65	85	µA
IDDFS	Supply current in FS mode	Frequency synthesizer running	-	1.3	1.7	mA
IDDR	Supply current in receiver mode		-	3.0	3.5	mA
IDDT	Supply current in transmitter mode	Output power = +10 dBm Output power = 1dBm(1)	- -	25 16	30 21	mA mA

(1) Guaranteed by design and characterization

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2.4.2. Frequency Synthesis

Table 6: Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Frequency ranges	433MHz module	432		436	MHz
BR_F	Bit rate (FSK)	NRZ	0.78	-	150	Kb/s
BR_O	Bit rate (OOK)	NRZ	0.78	-	32	Kb/s
FDA	Frequency deviation (FSK)		33	50	200	kHz
XTAL	Crystal oscillator frequency	For All Module		12.8		MHz
FSTEP	Frequency synthesizer step	Variable, depending on the frequency.	-	2	-	kHz
TS_OSC	Oscillator wake-up time	From Sleep mode(1)	-	1.5	5	ms
TS_FS	Frequency synthesizer wake-up time at most 10 kHz away from the target	From Stby mode	-	500	800	µs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step	-	180	-	µs
		1 MHz step	-	200	-	µs
		5 MHz step	-	250	-	µs
		7 MHz step	-	260	-	µs
		12 MHz step	-	290	-	µs
		20 MHz step	-	320	-	µs
		27 MHz step	-	340	-	µs

(1) Guaranteed by design and characterization

2.4.3. Transmitter

Table 7: Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFOP	RF output power, programmable with 8 steps of typ. 3dB	Maximum power setting	-	+12	-	dBm
		Minimum power setting	-	-8	-	dBm
PN	Phase noise	Measured with a 600 kHz offset, at the transmitter output.	-	-112	-	dBc/Hz
SPT	Transmitted spurious	At any offset between 200 kHz and 600 kHz, unmodulated carrier, Fdev = 50 kHz.	-	-	-47	dBc
TS_TR(1)	Transmitter wake-up time	From FS to Tx ready.	-	120	500	µs
TS_TR2(1)	Transmitter wake-up time	From Stby to Tx ready.	-	600	900	µs

(1) Guaranteed by design and characterization

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2.4.4. Receiver

On the following table, fc and fo describe the bandwidth of the active channel filters as described in section 3.4.4.2. All sensitivities are measured receiving a PN15 sequence, for a BER of 0.1.%

Table 8: Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Sensitivity (FSK)	434 MHz, BR=25 kb/s, Fdev =50 kHz, fc=100 kHz	-	-104	-	dBm
			-	-	-	
			-	-	-	
			-	-	-	
RFS_O	Sensitivity (OOK)	434 MHz, 2kb/s NRZ fc-fo=50 kHz, fo=50 kHz	-	-110	-	dBm
			-	-	-	
			-	-	-	
			-	-	-	
CCR	Co-channel rejection	Modulation as wanted signal	-	-12	-	dBc
ACR	Adjacent channel rejection	Offset = 300 kHz	-	-	-	dB
		Offset = 600 kHz	-	42	-	dB
		Offset = 1.2 MHz	-	53	-	dB
BI	Blocking immunity	Offset = 1 MHz, unmodulated	-	53	-	dBc
		Offset = 2 MHz, unmodulated, no SAW	-	-	-	
		Offset = 10 MHz, unmodulated, no SAW	-	-	-	
RXBW_F(1,2)	Receiver bandwidth in FSK mode	Single side BW Polyphase Off	50	-	250	kHz
RXBW_O(1,2)	Receiver bandwidth in OOK mode	Single side BW Polyphase On	50	-	400	kHz
IIP3	Input 3rd order intercept point	Interferers at 1MHz and 1.950 MHz offset	-	-28	-	dBm
TS_RE(1)	Receiver wake-up time	From FS to Rx ready	-	280	500	µs
TS_RE2(1)	Receiver wake-up time	From Stby to Rx ready	-	600	900	µs
TS_RE_HOP	Receiver hop time from Rx ready to Rx ready with a frequency hop	200 kHz step	-	400	-	µs
		1MHz step	-	400	-	µs
		5MHz step	-	460	-	µs
		7MHz step	-	480	-	µs
		12MHz step	-	520	-	µs
		20MHz step	-	550	-	µs
		27MHz step	-	600	-	µs
TS_RSSI	RSSI sampling time	From Rx ready	-	-	1/Fdev	s
DR_RSSI	RSSI dynamic Range	Ranging from sensitivity	-	70	-	dB

(1) Information from design and characterization
(2) This reflects the whole receiver bandwidth, as described in sections 3.4.4.1 and 3.4.4.2

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2.4.5. Digital Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, unless otherwise specified.

Table 9: Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Digital input level high		0.8*VDD	-	-	V
VIL	Digital input level low		-	-	0.2*VDD	V
VOH	Digital output level high	Imax=1mA	0.9*VDD	-	-	V
VOL	Digital output level low	Imax=-1mA	-	-	0.1*VDD	V
SCK_CONFIG	SPI Config. clock frequency		-	-	6	MHz
SCK_DATA	SPI data clock frequency		-	-	1	MHz
T_DATA	DATA hold and setup time		2	-	-	µs
T_MOSI_C	MOSI setup time for SPI Config.		250	-	-	ns
T_MOSI_D	MOSI setup time for SPI Data.		312	-	-	ns
T_NSSC_L	NSS_CONFIG low to SCK rising edge. SCK falling edge to NSS_CONFIG high.		500	-	-	ns
T_NSSD_L	NSS_DATA low to SCK rising edge. SCK falling edge to NSS_DATA high.		625	-	-	ns
T_NSSC_H	NSS_CONFIG rising to falling edge.		500	-	-	ns
T_NSSD_H	NSS_DATA rising to falling edge.		625	-	-	ns

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3. Architecture Description

This section describes in depth the architecture of this ultra low-power transceiver:

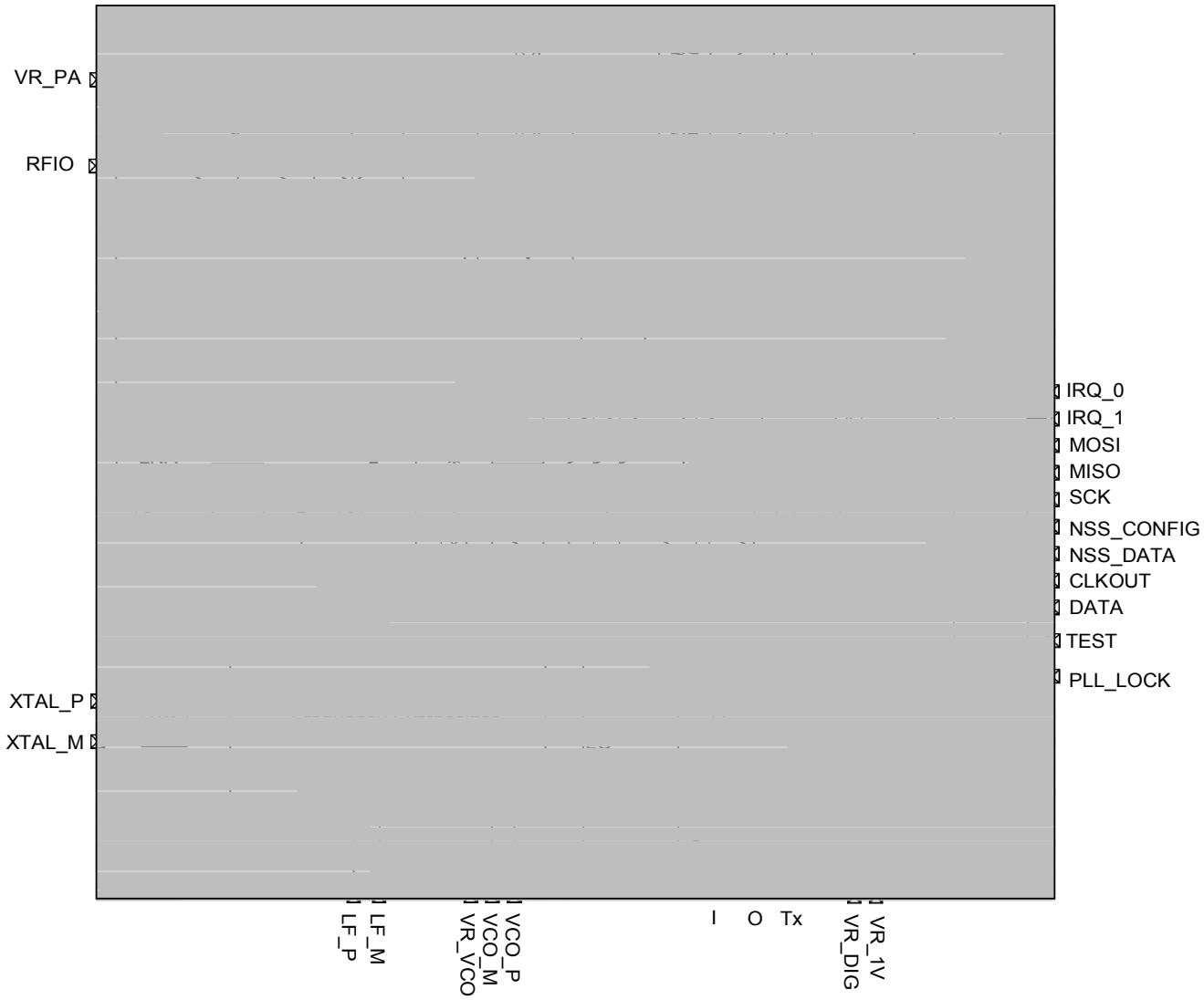

Figure 3: RFM64 Detailed Block Diagram

3.1. Power Supply Strategy

To provide stable sensitivity and linearity characteristics over a wide supply range, the RFM64 is internally regulated. This internal regulated power supply structure is described below:

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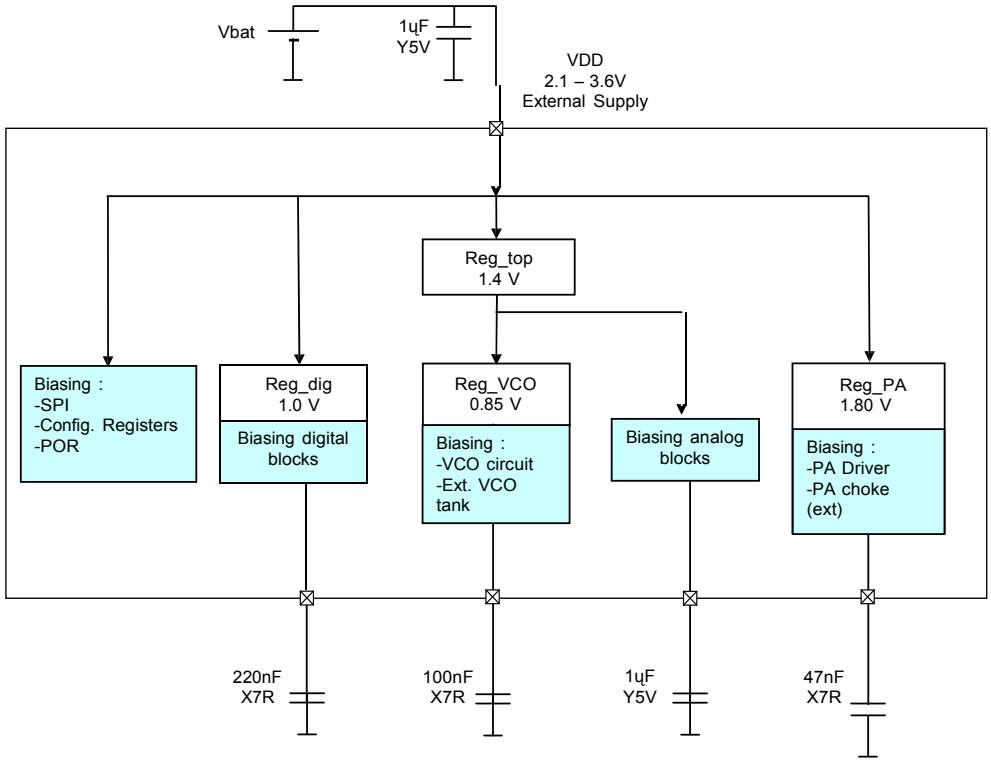

Figure 4: Power Supply Breakdown

To ensure correct operation of the regulator circuit, the decoupling capacitor connection shown in Figure 4 is required. These decoupling components are recommended for any design.

3.2. Frequency Synthesis Description

The frequency synthesizer of the RFM64 is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit.

3.2.1. Reference Oscillator

The RFM64 embeds a crystal oscillator, which provides the reference frequency for the PLL. The recommended crystal specification is given in section 7.1.

3.2.2. CLKOUT Output

The reference frequency, or a sub-multiple of it, can be provided on CLKOUT by activating the bit OSCParam_Clkout_on. The division ratio is programmed through bits OSCParam_Clkout_freq. The two applications of the CLKOUT output are:

- To provide a clock output for a companion uC, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the RFM64, ensure that the CLKOUT signal is disabled when unused.

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3.2.3. PLL Architecture

The crystal oscillator (XO) forms the reference oscillator of an Integer-N Phase Locked Loop (PLL), whose operation is discussed in the following section. Figure 5 shows a block schematic of the RFM64 PLL. Here the crystal reference frequency and the software controlled dividers R, P and S determine the output frequency of the PLL.

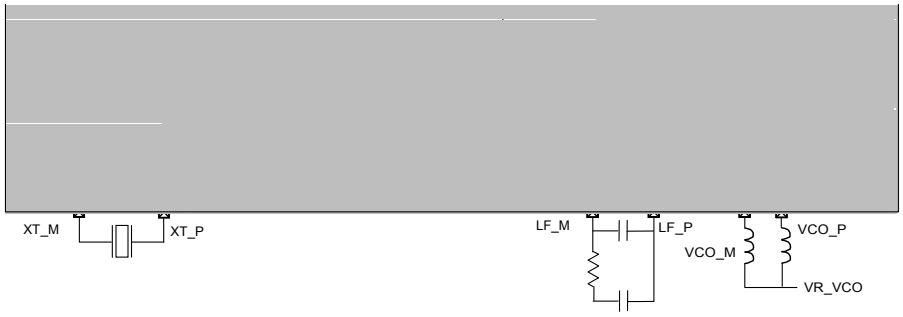

Figure 5: Frequency Synthesizer Description

The VCO tank inductors are connected on an external differential input. Similarly, the loop filter is also located externally. However, there is an internal 8pF capacitance at VCO input that should be subtracted from the desired loop filter capacitance.

The output signal of the VCO is used as the input to the local oscillator (LO) generator stage, illustrated in Figure 6. The VCO frequency is subdivided and used in a series of up (down) conversions for transmission (reception).

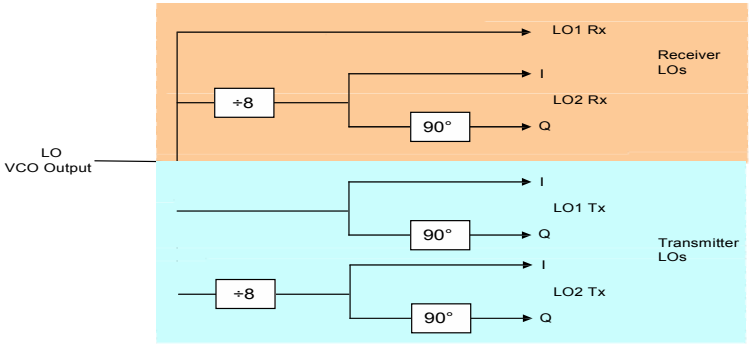

Figure 6: LO Generator

3.2.4. PLL Tradeoffs

With an integer-N PLL architecture, the following criterion must be met to ensure correct operation:

- The comparison frequency, Fcomp, of the Phase Frequency Detector (PFD) input must remain higher than six times the PLL bandwidth (PLLBW) to guarantee loop stability and to reject harmonics of the comparison frequency Fcomp. This is expressed in the inequality:

$$PLLBW \leqslant \frac{Fcomp}{6}$$

- However the PLLBW has to be sufficiently high to allow adequate PLL lock times
- Because the divider ration R determines Fcomp, it should be set close to 119, leading to Fcomp≈100 kHz which will ensure suitable PLL stability and speed.

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With the recommended of the reference design of section 7.5.3, the PLL prototype is the following:

- 64 ≤ R ≤ 169
- S < P+1
- LLBW = 15 kHz nominal
- Startup times and reference frequency spurs as specified.

3.2.5. Voltage Controlled Oscillator

The integrated VCO requires only two external tank circuit inductors. As the input is differential, the two inductors should have the same nominal value. The performance of these components is important for both the phase noise and the power consumption of the PLL. It is recommended that a pair of high Q factor inductors is selected. These should be mounted orthogonally to other inductors (in particular the PA choke) to reduce spurious coupling between the PA and VCO. In addition, such measures may reduce radiated pulling effects and undesirable transient behavior, thus minimizing spectral occupancy. Note that ensuring a symmetrical layout of the VCO inductors will further improve PLL spectral purity.

For best performance wound type inductors, with tight tolerance, should be used as described in section 7.5.3.

3.2.5.1. SW Settings of the VCO

To guarantee the optimum operation of the VCO over the RF64's frequency and temperature ranges, the following settings should be programmed into the RFM64:

Target channel (MHz)	300-330	320-350	350-390	390-430	430-470	470-510
Freq_band	000	001	010	011	100	101

Table 10: MCParam_Freq_band Setting

3.2.5.2. Trimming the VCO Tank by Hardware and Software

To ensure that the frequency band of operation may be accurately addressed by the R, P and S dividers of the synthesizer, it is necessary to ensure that the VCO is correctly centered. Note that for the reference design (see section 7.5) no centering is necessary. However, any deviation from the reference design may require the optimization procedure, outlined below, to be implemented. This procedure is simplified thanks to the built-in VCO trimming feature which is controlled over the SPI interface. This tuning does not require any RF test equipment, and can be achieved by simply measuring Vtune, the voltage between pins LFM and LFP.

The VCO is centered if the voltage is within the range:

$$100 \leqslant Vtune(mV) \leqslant 200$$

Note that this measurement should be conducted when in transmit mode at the center frequency of the desired band (for example ~315 MHz in the 300-330 MHz band), with the appropriate MCParam_Freq_band setting.

If this inequality is not satisfied then adjust the MCParam_VCO_trim bits from 00 whilst monitoring Vtune. This allows the VCO voltage to be trimmed in + 60 mV increments. Should the desired voltage range be inaccessible, the voltage may be adjusted further by changing the tank circuit inductance value. Note that an increase in inductance will result in an increase Vtune.

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Note for mass production: The VCO capacitance is piece to piece dependant. As such, the optimization proposed above should be verified on several prototypes, to ensure that the population is centered on 150 mV.

3.2.6. PLL Loop Filter

To adequately reject spurious components arising from the comparison frequency Fcomp, an external 2nd order loop filter is employed.

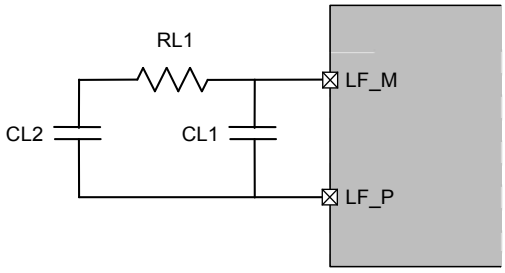

Figure 7: Loop Filter

Following the recommendations made in section 3.2.4, the loop filter proposed in the reference design's bill of material on section 7.5.3 should be used. The loop filter settings are frequency band independent and are hence relevant to all implementations of the RFM64.

3.2.7. PLL Lock Detection Indicator

The RFM64 also features a PLL lock detect indicator. This is useful for optimizing power consumption, by adjusting the synthesizer wake up time (TS_FS), since the PLL startup time is lower than specified under nominal conditions. The lock status can be read on bit IRQParam_PLL_lock, and must be cleared by writing a "1" to this same register. In addition, the lock status can be reflected in pin PLL_LOCK, by setting the bit IRQParam_Enable_lock_detect.

3.2.8. Frequency Calculation

As shown in Figure 5 the PLL structure comprises three different dividers, R, P and S, which set the output frequency through the LO. A second set of dividers is also available to allow rapid switching between a pair of frequencies: R1/P1/S1 and R2/P2/S2. These six dividers are programmed by six bytes of the register MCParam from addresses 6 to 11.

3.2.8.1. FSK Mode

The following formula gives the relationship between the local oscillator, and R, P and S values, when using FSK modulation.

$$Frf, fsk = \frac{9}{8} Flo$$

$$Frf, fsk = \frac{9}{8} \frac{Fxtal}{R+1} \left[75(P+1) + S\right]$$

3.2.8.2. OOK Mode

Due to the manner in which the baseband OOK symbols are generated, the signal is always offset by the FSK frequency deviation (Fdev - as programmed in MCParam_Freq_dev). Hence, the center of the transmitted OOK signal is:

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$$Frf,ook,tx = \frac{9}{8}Flo - Fdev$$

$$Frf,ook,tx = \frac{9}{8}\frac{Fxtal}{R+1}\left[75(P+1)+S\right] - Fdev$$

Consequently, in receive mode, due to the low intermediate frequency (Low-IF) architecture of the RFM64 the frequency should be configured so as to ensure the correct low-IF receiver baseband center frequency, IF2.

$$Frf,ook,rx = \frac{9}{8}Flo - IF2$$

$$Frf,ook,rx = \frac{9}{8}\frac{Fxtal}{R+1}\left[75(P+1)+S\right] - IF2$$

Note that from Section 3.4.4, it is recommended that IF2 be set to 100 kHz.

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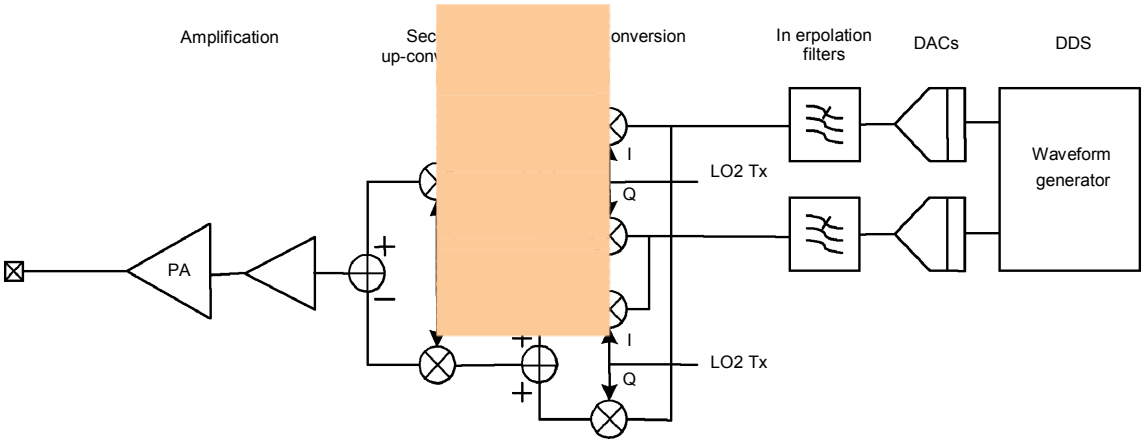

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