FUJITSU

FUJITSU-MONAKA®

PMU Events

1.0, 31 October 2024

Revision History

Change Date	Edition	Description of Change
10/31/2024	1.0	First-Release

Introduction

The FUJITSU-MONAKA processor (called MONAKA, below) is a super scalar processor of the out-of-order execution type. The MONAKA is designed to realize a carbon-neutral society by reducing energy consumption by more than 40% in next-generation data centers and complies with the ARMv9-A architecture profile and the Scalable Vector Extension (SVE2) for ARMv9-A. MONAKA consists of 4 core dies, 4 SRAM dies and 1 IO die per socket. Each core die contains 36 processor cores, each SRAM die contains 34 cache banks, each IO die contains a DDR5 memory controller and a PCI-Express Gen6/CXL3.0 root complex. The core die and the SRAM die constitute four pairs each and are connected by 3D mounting.

Events

ARMv9 Common Events

0x0000, SW_INCR

This event counts on writes to the PMSWINC register.

0x0001, L1I_CACHE_REFILL

This event counts operations that cause a refill of the L1I cache.
See L1I_CACHE_REFILL of ARMv9 Reference Manual for more information.

0x0002, L1I_TLB_REFILL

This event counts operations that cause a TLB refill of the L1I TLB.
See L1I_TLB_REFILL of ARMv9 Reference Manual for more information.

0x0003, L1D_CACHE_REFILL

This event counts operations that cause a refill of the L1D cache.
See L1D_CACHE_REFILL of ARMv9 Reference Manual for more information.

0x0004, L1D_CACHE

This event counts operations that cause a cache access to the L1D cache.
See L1D_CACHE of ARMv9 Reference Manual for more information.

0x0005, L1D_TLB_REFILL

This event counts operations that cause a TLB refill of the L1D TLB.
See L1D_TLB_REFILL of ARMv9 Reference Manual for more information.

0x0008, INST_RETIRED

This event counts every architecturally executed instruction.

0x0009, EXC_TAKEN

This event counts each exception taken.

0x000a, EXC_RETURN

This event counts each executed exception return instruction.

0x000b, CID_WRITE_RETIRED

This event counts every write to CONTEXTIDR.

0x0010, BR_MIS_PRED

This event counts each correction to the predicted program flow that occurs because of a misprediction from, or no prediction from, the branch prediction resources and that relates to instructions that the branch prediction resources are capable of predicting.

0x0011, CPU_CYCLES

This event counts every cycle.

0x0012, BR_PRED

This event counts every branch or other change in the program flow that the branch prediction resources are capable of predicting.

0x0013, MEM_ACCESS

This event counts architecturally executed memory-reading instructions and memory-writing instructions, as defined by the LDST_SPEC events.

0x0014, L1I_CACHE

This event counts operations that cause a cache access to the L1I cache.
See L1I_CACHE of ARMv9 Reference Manual for more information.

0x0015, L1D_CACHE_WB

This event counts every write-back of data from the L1D cache.
See L1D_CACHE_WB of ARMv9 Reference Manual for more information.

0x0016, L2D_CACHE

This event counts operations that cause a cache access to the L2 cache.
See L2D_CACHE of ARMv9 Reference Manual for more information.

0x0017, L2D_CACHE_REFILL

This event counts operations that cause a refill of the L2 cache.
See L2D_CACHE_REFILL of ARMv9 Reference Manual for more information.

0x0018, L2D_CACHE_WB

This event counts every write-back of data from the L2 cache caused by L2 replace, non-temporal-store and DC ZVA.

0x001b, INST_SPEC

This event counts every architecturally executed instruction.

0x0021, BR_RETIRED

This event counts architecturally executed branch instruction.

0x0022, BR_MIS_PRED_RETIRED

This event counts architecturally executed branch instruction which was mispredicted.

0x0023, STALL_FRONTEND

This event counts every cycle counted by the CPU_CYCLES event on that no operation was issued because there are no operations available to issue for this PE from the frontend.

0x0024, STALL_BACKEND

This event counts every cycle counted by the CPU_CYCLES event on that no operation was issued because the backend is unable to accept any operations.

0x0025, L1D_TLB

This event counts operations that cause a TLB access to the L1D TLB.
See L1D_TLB of ARMv9 Reference Manual for more information.

0x0026, L1I_TLB

This event counts operations that cause a TLB access to the L1I TLB.
See L1I_TLB of ARMv9 Reference Manual for more information.

0x002b, L3D_CACHE

This event counts operations that cause a cache access to the L3 cache, as defined by the sum of L2D_CACHE_REFILL_L3D_CACHE and L2D_CACHE_WB_VICTIM_CLEAN events.

0x002d, L2D_TLB_REFILL

This event counts operations that cause a TLB refill of the L2D TLB.
See L2D_TLB_REFILL of ARMv9 Reference Manual for more information.

0x002e, L2I_TLB_REFILL

This event counts operations that cause a TLB refill of the L2I TLB.
See L2I_TLB_REFILL of ARMv9 Reference Manual for more information.

0x002f, L2D_TLB

This event counts operations that cause a TLB access to the L2D TLB.
See L2D_TLB of ARMv9 Reference Manual for more information.

0x0030, L2I_TLB

This event counts operations that cause a TLB access to the L2I TLB.
See L2I_TLB of ARMv9 Reference Manual for more information.

0x0034, DTLB_WALK

This event counts data TLB access with at least one translation table walk.

0x0035, ITLB_WALK

This event counts instruction TLB access with at least one translation table walk.

0x0036, LL_CACHE_RD

This event counts access counted by L3D_CACHE that is a Memory-read operation, as defined by the L2D_CACHE_REFILL_L3D_CACHE events.

0x0037, LL_CACHE_MISS_RD

This event counts access counted by L3D_CACHE that is not completed by the L3D cache, and a Memory-read operation, as defined by the L2D_CACHE_REFILL_L3D_MISS events.

0x0039, L1D_CACHE_LMISS_RD

This event counts operations that cause a refill of the L1D cache that incurs additional latency.

0x003a, OP_RETIRED

This event counts every architecturally executed micro-operation.

0x003b, OP_SPEC

This event counts every speculatively executed micro-operation.

0x003c, STALL

This event counts every cycle that no instruction was dispatched from decode unit.

0x003d, STALL_SLOT_BACKEND

This event counts every cycle that no instruction was dispatched from decode unit due to the backend.

0x003e, STALL_SLOT_FRONTEND

This event counts every cycle that no instruction was dispatched from decode unit due to the frontend.

0x003f, STALL_SLOT

This event counts every cycle that no instruction or operation Slot was dispatched from decode unit.

0x0040, L1D_CACHE_RD

This event counts L1D CACHE caused by read access.

0x0041, L1D_CACHE_WR

This event counts L1D CACHE caused by write access.

0x0042, L1D_CACHE_REFILL_RD

This event counts L1D_CACHE_REFILL caused by read access.

0x0043, L1D_CACHE_REFILL_WR

This event counts L1D_CACHE_REFILL caused by write access.

0x0050, L2D_CACHE_RD

This event counts L2D CACHE caused by read access.

0x0051, L2D_CACHE_WR

This event counts L2D CACHE caused by write access.

0x0052, L2D_CACHE_REFILL_RD

This event counts L2D CACHE_REFILL caused by read access.

0x0053, L2D_CACHE_REFILL_WR

This event counts L2D CACHE_REFILL caused by write access.

0x0056, L2D_CACHE_WB_VICTIM

This event counts every write-back of data from the L2 cache caused by L2 replace.

0x0066, MEM_ACCESS_RD

This event counts architecturally executed memory-reading instructions, as defined by the LD_SPEC events.

0x006c, LDREX_SPEC

This event counts architecturally executed load-exclusive instructions.

0x006f, STREX_SPEC

This event counts architecturally executed store-exclusive instructions.

0x0070, LD_SPEC

This event counts architecturally executed memory-reading instructions, as defined by the LD_RETIRED event.

0x0071, ST_SPEC

This event counts architecturally executed memory-writing instructions, as defined by the ST_RETIRED event. This event counts DCZVA as a store operation.

0x0072, LDST_SPEC

This event counts architecturally executed memory-reading instructions and memory-writing instructions, as defined by the LD_RETIRED and ST_RETIRED events.

0x0073, DP_SPEC

This event counts architecturally executed integer data-processing instructions.
See DP_SPEC of ARMv9 Reference Manual for more information.

0x0074, ASE_SPEC

This event counts architecturally executed Advanced SIMD data-processing instructions.

0x0075, VFP_SPEC

This event counts architecturally executed floating-point data-processing instructions.

0x0076, PC_WRITE_SPEC

This event counts only software changes of the PC that defined by the instruction architecturally executed, condition code check pass, software change of the PC event.

0x0077, CRYPTO_SPEC

This event counts architecturally executed cryptographic instructions, except PMULL and VMULL.

0x0078, BR_IMMED_SPEC

This event counts architecturally executed immediate branch instructions.

0x0079, BR_RETURN_SPEC

This event counts architecturally executed procedure return operations that defined by the BR_RETURN_RETIRED event.

0x007a, BR_INDIRECT_SPEC

This event counts architecturally executed indirect branch instructions that includes software change of the PC other than exception-generating instructions and immediate branch instructions.

0x007c, ISB_SPEC

This event counts architecturally executed Instruction Synchronization Barrier instructions.

0x007d, DSB_SPEC

This event counts architecturally executed Data Synchronization Barrier instructions.

0x007e, DMB_SPEC

This event counts architecturally executed Data Memory Barrier instructions, excluding the implied barrier operations of load/store operations with release consistency semantics.

0x007f, CSDB_SPEC

This event counts speculatively executed control speculation barrier instructions.

0x0081, EXC_UNDEF

This event counts only other synchronous exceptions that are taken locally.

0x0082, EXC_SVC

This event counts only Supervisor Call exceptions that are taken locally.

0x0083, EXC_PABORT

This event counts only Instruction Abort exceptions that are taken locally.

0x0084, EXC_DABORT

This event counts only Data Abort or SError interrupt exceptions that are taken locally.

0x0086, EXC_IRQ

This event counts only IRQ exceptions that are taken locally, including Virtual IRQ exceptions.

0x0087, EXC_FIQ

This event counts only FIQ exceptions that are taken locally, including Virtual FIQ exceptions.

0x0088, EXC_SMC

This event counts only Secure Monitor Call exceptions.
The counter does not increment on SMC instructions trapped as a Hyp Trap exception.

0x008a, EXC_HVC

This event counts for both Hypervisor Call exceptions taken locally in the hypervisor and those taken as an exception from Non-secure EL1.

0x00a0, L3D_CACHE_RD

This event counts access counted by L3D_CACHE that is a Memory-read operation, as defined by the L2D_CACHE_REFILL_L3D_CACHE events.

0x4004, CNT_CYCLES

This event counts the constant frequency cycles counter increments at a constant frequency equal to the rate of increment of the System counter.

0x4005, STALL_BACKEND_MEM

This event counts every cycle that no instruction was dispatched from decode unit due to memory stall.

0x4006, L1I_CACHE_LMISS

This event counts operations that cause a refill of the L1I cache that incurs additional latency.

0x4009, L2D_CACHE_LMISS_RD

This event counts operations that cause a refill of the L2D cache that incurs additional latency.

0x400b, L3D_CACHE_LMISS_RD

This event counts access counted by L3D_CACHE that is not completed by the L3D cache, and a Memory-read operation, as defined by the L2D_CACHE_REFILL_L3D_MISS events.

0x400c, TRB_WRAP

This event counts the event generated each time the current write pointer is wrapped to the base pointer.

0x400d, PMU_OVFS

This event counts the event generated each time one of the condition occurs described in Arm Architecture Reference Manual for A-profile architecture. This event is only for output to the trace unit.

0x400e, TRB_TRIG

This event counts the event generated when a Trace Buffer Extension Trigger Event occurs.

0x400f, PMU_HOVFS

This event counts the event generated each time an event is counted by an event counter <n> and all of the condition occur described in Arm Architecture Reference Manual for A-profile architecture. This event is only for output to the trace unit.

0x4010, TRCEXTOUT0

This event counts the event generated each time an event is signaled by the trace unit external event 0.

0x4018, CTI_TRIGOUT4

This event counts the event generated each time an event is signaled on CTI output trigger 4.

0x8000, SIMD_INST_RETIRED

This event counts architecturally executed SIMD instructions, excluding the Advanced SIMD scalar instructions and the instructions listed in Non-SIMD SVE instructions section of ARMv9 Reference Manual.

0x8002, SVE_INST_RETIRED

This event counts architecturally executed SVE instructions, including the instructions listed in Non-SIMD SVE instructions section of ARMv9 Reference Manual.

0x8005, ASE_INST_SPEC

This event counts architecturally executed Advanced SIMD operations.

0x8006, SVE_INST_SPEC

This event counts architecturally executed SVE instructions, including the instructions listed in Non-SIMD SVE instructions section of ARMv9 Reference Manual.

0x8007, ASE_SVE_INST_SPEC

This event counts architecturally executed Advanced SIMD and SVE operations.

0x8008, UOP_SPEC

This event counts all architecturally executed micro-operations.

0x800e, SVE_MATH_SPEC

This event counts architecturally executed math function operations due to the SVE FTSMUL, FTMAD, FTSSEL, and FEXPA instructions.

0x8010, FP_SPEC

This event counts architecturally executed operations due to scalar, Advanced SIMD, and SVE instructions listed in Floating-point instructions section of ARMv9 Reference Manual.

0x8011, ASE_FP_SPEC

This event counts architecturally executed Advanced SIMD floating-point operation.

0x8012, SVE_FP_SPEC

This event counts architecturally executed SVE floating-point operation.

0x8013, ASE_SVE_FP_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point operations.

0x8014, FP_HP_SPEC

This event counts architecturally executed half-precision floating-point operation.

0x8015, ASE_FP_HP_SPEC

This event counts architecturally executed Advanced SIMD half-precision floating-point operation.

0x8016, SVE_FP_HP_SPEC

This event counts architecturally executed SVE half-precision floating-point operation.

0x8017, ASE_SVE_FP_HP_SPEC

This event counts architecturally executed Advanced SIMD and SVE half-precision floating-point operations.

0x8018, FP_SP_SPEC

This event counts architecturally executed single-precision floating-point operation.

0x8019, ASE_FP_SP_SPEC

This event counts architecturally executed Advanced SIMD single-precision floating-point operation.

0x801a, SVE_FP_SP_SPEC

This event counts architecturally executed SVE single-precision floating-point operation.

0x801b, ASE_SVE_FP_SP_SPEC

This event counts architecturally executed Advanced SIMD and SVE single-precision floating-point operations.

0x801c, FP_DP_SPEC

This event counts architecturally executed double-precision floating-point operation.

0x801d, ASE_FP_DP_SPEC

This event counts architecturally executed Advanced SIMD double-precision floating-point operation.

0x801e, SVE_FP_DP_SPEC

This event counts architecturally executed SVE double-precision floating-point operation.

0x801f, ASE_SVE_FP_DP_SPEC

This event counts architecturally executed Advanced SIMD and SVE double-precision floating-point operations.

0x8020, FP_DIV_SPEC

This event counts architecturally executed floating-point divide operation.

0x8021, ASE_FP_DIV_SPEC

This event counts architecturally executed Advanced SIMD floating-point divide operation.

0x8022, SVE_FP_DIV_SPEC

This event counts architecturally executed SVE floating-point divide operation.

0x8023, ASE_SVE_FP_DIV_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point divide operations.

0x8024, FP_SQRT_SPEC

This event counts architecturally executed floating-point square root operation.

0x8025, ASE_FP_SQRT_SPEC

This event counts architecturally executed Advanced SIMD floating-point square root operation.

0x8026, SVE_FP_SQRT_SPEC

This event counts architecturally executed SVE floating-point square root operation.

0x8027, ASE_SVE_FP_SQRT_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point square root operations.

0x8028, FP_FMA_SPEC

This event counts architecturally executed floating-point fused multiply-add and multiply-subtract operations.

0x8029, ASE_FP_FMA_SPEC

This event counts architecturally executed Advanced SIMD floating-point FMA operation.

0x802a, SVE_FP_FMA_SPEC

This event counts architecturally executed SVE floating-point FMA operation.

0x802b, ASE_SVE_FP_FMA_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point FMA operations.

0x802c, FP_MUL_SPEC

This event counts architecturally executed floating-point multiply operations.

0x802d, ASE_FP_MUL_SPEC

This event counts architecturally executed Advanced SIMD floating-point multiply operation.

0x802e, SVE_FP_MUL_SPEC

This event counts architecturally executed SVE floating-point multiply operation.

0x802f, ASE_SVE_FP_MUL_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point multiply operations.

0x8030, FP_ADDSUB_SPEC

This event counts architecturally executed floating-point add or subtract operations.

0x8031, ASE_FP_ADDSUB_SPEC

This event counts architecturally executed Advanced SIMD floating-point add or subtract operation.

0x8032, SVE_FP_ADDSUB_SPEC

This event counts architecturally executed SVE floating-point add or subtract operation.

0x8033, ASE_SVE_FP_ADDSUB_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point add or subtract operations.

0x8034, FP_RECPE_SPEC

This event counts architecturally executed floating-point reciprocal estimate operations due to the Advanced SIMD scalar, Advanced SIMD vector, and SVE FRECPE and FRSQRTE instructions.

0x8035, ASE_FP_RECPE_SPEC

This event counts architecturally executed Advanced SIMD floating-point reciprocal estimate operations.

0x8036, SVE_FP_RECPE_SPEC

This event counts architecturally executed SVE floating-point reciprocal estimate operations.

0x8037, ASE_SVE_FP_RECPE_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point reciprocal estimate operations.

0x8038, FP_CVT_SPEC

This event counts architecturally executed floating-point convert operations due to the scalar, Advanced SIMD, and SVE floating-point conversion instructions listed in Floating-point conversions section of ARMv9 Reference Manual.

0x8039, ASE_FP_CVT_SPEC

This event counts architecturally executed Advanced SIMD floating-point convert operation.

0x803a, SVE_FP_CVT_SPEC

This event counts architecturally executed SVE floating-point convert operation.

0x803b, ASE_SVE_FP_CVT_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point convert operations.

0x803c, SVE_FP_AREDUCE_SPEC

This event counts architecturally executed SVE floating-point accumulating reduction operations.

0x803d, ASE_FP_PREDUCE_SPEC

This event counts architecturally executed Advanced SIMD floating-point pairwise add step operations.

0x803e, SVE_FP_VREDUCE_SPEC

This event counts architecturally executed SVE floating-point vector reduction operation.

0x803f, ASE_SVE_FP_VREDUCE_SPEC

This event counts architecturally executed Advanced SIMD and SVE floating-point vector reduction operations.

0x8040, INT_SPEC

This event counts architecturally executed operations due to scalar, Advanced SIMD, and SVE instructions listed in Integer instructions section of ARMv9 Reference Manual.

0x8041, ASE_INT_SPEC

This event counts architecturally executed Advanced SIMD integer operations.

0x8042, SVE_INT_SPEC

This event counts architecturally executed SVE integer operations.

0x8043, ASE_SVE_INT_SPEC

This event counts architecturally executed Advanced SIMD and SVE integer operations.

0x8044, INT_DIV_SPEC

This event counts architecturally executed integer divide operation.

0x8045, INT_DIV64_SPEC

This event counts architecturally executed 64-bit integer divide operation.

0x8046, SVE_INT_DIV_SPEC

This event counts architecturally executed SVE integer divide operation.

0x8047, SVE_INT_DIV64_SPEC

This event counts architecturally executed SVE 64-bit integer divide operation.

0x8048, INT_MUL_SPEC

This event counts architecturally executed integer multiply operation.

0x8049, ASE_INT_MUL_SPEC

This event counts architecturally executed Advanced SIMD integer multiply operation.

0x804a, SVE_INT_MUL_SPEC

This event counts architecturally executed SVE integer multiply operation.

0x804b, ASE_SVE_INT_MUL_SPEC

This event counts architecturally executed Advanced SIMD and SVE integer multiply operations.

0x804c, INT_MUL64_SPEC

This event counts architecturally executed integer 64-bit x 64-bit multiply operation.

0x804d, SVE_INT_MUL64_SPEC

This event counts architecturally executed SVE integer 64-bit x 64-bit multiply operation.

0x804e, INT_MULH64_SPEC

This event counts architecturally executed integer 64-bit x 64-bit multiply returning high part operation.

0x804f, SVE_INT_MULH64_SPEC

This event counts architecturally executed SVE integer 64-bit x 64-bit multiply returning high part operations.

0x8058, NONFP_SPEC

This event counts architecturally executed non-floating-point operations.

0x8059, ASE_NONFP_SPEC

This event counts architecturally executed Advanced SIMD non-floating-point operations.

0x805a, SVE_NONFP_SPEC

This event counts architecturally executed SVE non-floating-point operations.

0x805b, ASE_SVE_NONFP_SPEC

This event counts architecturally executed Advanced SIMD and SVE non-floating-point operations.

0x805d, ASE_INT_VREDUCE_SPEC

This event counts architecturally executed Advanced SIMD integer reduction operation.

0x805e, SVE_INT_VREDUCE_SPEC

This event counts architecturally executed SVE integer reduction operation.

0x805f, ASE_SVE_INT_VREDUCE_SPEC

This event counts architecturally executed Advanced SIMD and SVE integer reduction operations.

0x8060, SVE_PERM_SPEC

This event counts architecturally executed vector or predicate permute operation.

0x8065, SVE_XPIPE_Z2R_SPEC

This event counts architecturally executed vector to general-purpose scalar cross-pipeline transfer operation.

0x8066, SVE_XPIPE_R2Z_SPEC

This event counts architecturally executed general-purpose scalar to vector cross-pipeline transfer operation.

0x8068, SVE_PGEN_SPEC

This event counts architecturally executed predicate-generating operation.

0x8069, SVE_PGEN_FLG_SPEC

This event counts architecturally executed predicate-generating operation that sets condition flags.

0x806d, SVE_PPERM_SPEC

This event counts architecturally executed predicate permute operation.

0x8074, SVE_PRED_SPEC

This event counts architecturally executed SIMD data-processing and load/store operations due to SVE instructions with a Governing predicate operand that determines the Active elements.

0x807c, SVE_MOVPRFX_SPEC

This event counts architecturally executed operations due to MOVPRFX instructions, whether or not they were fused with the prefixed instruction.

0x807d, SVE_MOVPRFX_Z_SPEC

This event counts architecturally executed operation counted by SVE_MOVPRFX_SPEC where the operation uses zeroing predication.

0x807e, SVE_MOVPRFX_M_SPEC

This event counts architecturally executed operation counted by SVE_MOVPRFX_SPEC where the operation uses merging predication.

0x807f, SVE_MOVPRFX_U_SPEC

This event counts architecturally executed operations due to MOVPRFX instructions that were not fused with the prefixed instruction.

0x8085, ASE_SVE_LD_SPEC

This event counts architecturally executed operations that read from memory due to SVE and Advanced SIMD load instructions.

0x8086, ASE_SVE_ST_SPEC

This event counts architecturally executed operations that write to memory due to SVE and Advanced SIMD store instructions.

0x8087, PRF_SPEC

This event counts architecturally executed prefetch operations due to scalar PRFM, PRFUM and SVE PRF instructions.

0x8089, BASE_LD_REG_SPEC

This event counts architecturally executed operations that read from memory due to an instruction that loads a general-purpose register.

0x808a, BASE_ST_REG_SPEC

This event counts architecturally executed operations that write to memory due to an instruction that stores a general-purpose register, excluding the "DC ZVA" instruction.

0x8091, SVE_LDR_REG_SPEC

This event counts architecturally executed operations that read from memory due to an SVE LDR instruction.

0x8092, SVE_STR_REG_SPEC

This event counts architecturally executed operations that write to memory due to an SVE STR instruction.

0x8095, SVE_LDR_PREG_SPEC

This event counts architecturally executed operations that read from memory due to an SVE LDR (predicate) instruction.

0x8096, SVE_STR_PREG_SPEC

This event counts architecturally executed operations that write to memory due to an SVE STR (predicate) instruction.

0x809f, SVE_PRF_CONTIG_SPEC

This event counts architecturally executed operations that prefetch memory due to an SVE predicated single contiguous element prefetch instruction.

0x80a1, SVE_LDNT_CONTIG_SPEC

This event counts architecturally executed operation that reads from memory with a non-temporal hint due to an SVE non-temporal contiguous element load instruction.

0x80a2, SVE_STNT_CONTIG_SPEC

This event counts architecturally executed operation that writes to memory with a non-temporal hint due to an SVE non-temporal contiguous element store instruction.

0x80a5, ASE_SVE_LD_MULTI_SPEC

This event counts architecturally executed operations that read from memory due to SVE and Advanced SIMD multiple vector contiguous structure load instructions.

0x80a6, ASE_SVE_ST_MULTI_SPEC

This event counts architecturally executed operations that write to memory due to SVE and Advanced SIMD multiple vector contiguous structure store instructions.

0x80ad, SVE_LD_GATHER_SPEC

This event counts architecturally executed operations that read from memory due to SVE non-contiguous gather-load instructions.

0x80ae, SVE_ST_SCATTER_SPEC

This event counts architecturally executed operations that write to memory due to SVE non-contiguous scatter-store instructions.

0x80af, SVE_PRF_GATHER_SPEC

This event counts architecturally executed operations that prefetch memory due to SVE non-contiguous gather-prefetch instructions.

0x80bc, SVE_LDFF_SPEC

This event counts architecturally executed memory read operations due to SVE First-fault and Non-fault load instructions.

0x80c0, FP_SCALE_OPS_SPEC

This event counts architecturally executed SVE arithmetic operations.
See FP_SCALE_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by (128 / CSIZE) and by twice that amount for operations that would also be counted by SVE_FP_FMA_SPEC.

0x80c1, FP_FIXED_OPS_SPEC

This event counts architecturally executed v8SIMD&FP arithmetic operations.
See FP_FIXED_OPS_SPEC of ARMv9 Reference Manual for more information.
The event counter is incremented by the specified number of elements for Advanced SIMD operations or by 1 for scalar operations, and by twice those amounts for operations that would also be counted by FP_FMA_SPEC.

0x80c2, FP_HP_SCALE_OPS_SPEC

This event counts architecturally executed SVE half-precision arithmetic operations.
See FP_HP_SCALE_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by 8, or by 16 for operations that would also be counted by SVE_FP_FMA_SPEC.

0x80c3, FP_HP_FIXED_OPS_SPEC

This event counts architecturally executed v8SIMD&FP half-precision arithmetic operations.
See FP_HP_FIXED_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by the number of 16-bit elements for Advanced SIMD operations, or by 1 for scalar operations, and by twice those amounts for operations that would also be counted by FP_FMA_SPEC.

0x80c4, FP_SP_SCALE_OPS_SPEC

This event counts architecturally executed SVE single-precision arithmetic operations.
See FP_SP_SCALE_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by 4, or by 8 for operations that would also be counted by SVE_FP_FMA_SPEC.

0x80c5, FP_SP_FIXED_OPS_SPEC

This event counts architecturally executed v8SIMD&FP single-precision arithmetic operations.
See FP_SP_FIXED_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by the number of 32-bit elements for Advanced SIMD operations, or by 1 for scalar operations, and by twice those amounts for operations that would also be counted by FP_FMA_SPEC.

0x80c6, FP_DP_SCALE_OPS_SPEC

This event counts architecturally executed SVE double-precision arithmetic operations.
See FP_DP_SCALE_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by 2, or by 4 for operations that would also be counted by SVE_FP_FMA_SPEC.

0x80c7, FP_DP_FIXED_OPS_SPEC

This event counts architecturally executed v8SIMD&FP double-precision arithmetic operations.
See FP_DP_FIXED_OPS_SPEC of ARMv9 Reference Manual for more information.
This event counter is incremented by 2 for Advanced SIMD operations, or by 1 for scalar operations, and by twice those amounts for operations that would also be counted by FP_FMA_SPEC.

0x80c8, INT_SCALE_OPS_SPEC

This event counts each integer ALU operation counted by SVE_INT_SPEC.
See ALU operation counts section of ARMv9 Reference Manual for information on the counter increment for different types of instruction.

0x80c9, INT_FIXED_OPS_SPEC

This event counts each integer ALU operation counted by INT_SPEC that is not counted by SVE_INT_SPEC.
See ALU operation counts section of ARMv9 Reference Manual for information on the counter increment for different types of instruction.

0x80f3, ASE_SVE_FP_DOT_SPEC

This event counts architecturally executed microarchitectural Advanced SIMD or SVE floating-point dot-product operation.

0x80f7, ASE_SVE_FP_MMLA_SPEC

This event counts architecturally executed microarchitectural Advanced SIMD or SVE floating-point matrix multiply operation.

0x80fb, ASE_SVE_INT_DOT_SPEC

This event counts architecturally executed microarchitectural Advanced SIMD or SVE integer dot-product operation.

0x80ff, ASE_SVE_INT_MMLA_SPEC

This event counts architecturally executed microarchitectural Advanced SIMD or SVE integer matrix multiply operation.

0x8128, DTLB_WALK_PERCYC

This event counts the number of DTLB_WALK events in progress on each Processor cycle.

0x8129, ITLB_WALK_PERCYC

This event counts the number of ITLB_WALK events in progress on each Processor cycle.

0x8136, DTLB_STEP

This event counts translation table walk access made by a refill of the data TLB.

0x8137, ITLB_STEP

This event counts translation table walk access made by a refill of the instruction TLB.

0x8138, DTLB_WALK_LARGE

This event counts translation table walk counted by DTLB_WALK where the result of the walk yields a large page size.

0x8139, ITLB_WALK_LARGE

This event counts translation table walk counted by ITLB_WALK where the result of the walk yields a large page size.

0x813a, DTLB_WALK_SMALL

This event counts translation table walk counted by DTLB_WALK where the result of the walk yields a small page size.

0x813b, ITLB_WALK_SMALL

This event counts translation table walk counted by ITLB_WALK where the result of the walk yields a small page size.

0x8144, L1D_CACHE_MISS

This event counts demand access that misses in the Level 1 data cache, causing an access to outside of the Level 1 caches of this PE.

0x8145, L1I_CACHE_HWPRF

This event counts access counted by L1I_CACHE that is due to a hardware prefetch.

0x814c, L2D_CACHE_MISS

This event counts demand access that misses in the Level 1 data and Level 2 caches, causing an access to outside of the Level 1 and Level 2 caches of this PE.

0x8154, L1D_CACHE_HWPRF

This event counts access counted by L1D_CACHE that is due to a hardware prefetch.

0x8155, L2D_CACHE_HWPRF

This event counts access counted by L2D_CACHE that is due to a hardware prefetch.

0x8158, STALL_FRONTEND_MEMBOUND

This event counts every cycle counted by STALL_FRONTEND when no instructions are delivered from the memory system.

0x8159, STALL_FRONTEND_L1I

This event counts every cycle counted by STALL_FRONTEND_MEMBOUND when there is a demand instruction miss in the first level of instruction cache.

0x815a, STALL_FRONTEND_L2I

This event counts every cycle counted by STALL_FRONTEND_MEMBOUND when there is a demand instruction miss in the second level of instruction cache.

0x815b, STALL_FRONTEND_MEM

This event counts every cycle counted by STALL_FRONTEND_MEMBOUND when there is a demand instruction miss in the last level of instruction cache within the PE clock domain or a non-cacheable instruction fetch in progress.

0x815c, STALL_FRONTEND_TLB

This event counts every cycle counted by STALL_FRONTEND_MEMBOUND when there is a demand instruction miss in the instruction TLB.

0x8160, STALL_FRONTEND_CPUBOUND

This event counts every cycle counted by STALL_FRONTEND when the frontend is stalled on a frontend processor resource, not including memory.

0x8161, STALL_FRONTEND_FLOW

This event counts every cycle counted by STALL_FRONTEND_CPUBOUND when the frontend is stalled on unavailability of prediction flow resources.

0x8162, STALL_FRONTEND_FLUSH

This event counts every cycle counted by STALL_FRONTEND_CPUBOUND when the frontend is recovering from a pipeline flush.

0x8163, STALL_FRONTEND_RENAME

This event counts every cycle counted by STALL_FRONTEND_CPUBOUND when operations are available from the frontend but at least one is not ready to be sent to the backend because no rename register is available.

0x8164, STALL_BACKEND_MEMBOUND

This event counts every cycle counted by STALL_BACKEND when the backend is waiting for a memory access to complete.

0x8165, STALL_BACKEND_L1D

This event counts every cycle counted by STALL_BACKEND_MEMBOUND when there is a demand data miss in L1D cache.

0x8166, STALL_BACKEND_L2D

This event counts every cycle counted by STALL_BACKEND_MEMBOUND when there is a demand data miss in L2D cache.

0x8167, STALL_BACKEND_TLB

This event counts every cycle counted by STALL_BACKEND_MEMBOUND when there is a demand data miss in the data TLB.

0x8168, STALL_BACKEND_ST

This event counts every cycle counted by STALL_BACKEND_MEMBOUND when the backend is stalled waiting for a store.

0x816a, STALL_BACKEND_CPUBOUND

This event counts every cycle counted by STALL_BACKEND when the backend is stalled on a processor resource, not including memory.

0x816b, STALL_BACKEND_BUSY

This event counts every cycle counted by STALL_BACKEND when operations are available from the frontend but the backend is not able to accept an operation because an execution unit is busy.

0x816c, STALL_BACKEND_ILOCK

This event counts every cycle counted by STALL_BACKEND when operations are available from the frontend but at least one is not ready to be sent to the backend because of an input dependency.

0x816d, STALL_BACKEND_RENAME

This event counts every cycle counted by STALL_BACKEND_CPUBOUND when operations are available from the frontend but at least one is not ready to be sent to the backend because no rename register is available.

0x816e, STALL_BACKEND_ATOMIC

This event counts every cycle counted by STALL_BACKEND_MEMBOUND when the backend is processing an Atomic operation.

0x816f, STALL_BACKEND_MEMCPYSET

This event counts every cycle counted by STALL_BACKEND_MEMBOUND when the backend is processing a Memory Copy or Set instruction.

0x8186, UOP_RETIRED

This event counts micro-operation that would be executed in a Simple sequential execution of the program.

0x8188, DTLB_WALK_BLOCK

This event counts translation table walk counted by DTLB_WALK where the result of the walk yields a Block.

0x8189, ITLB_WALK_BLOCK

This event counts translation table walk counted by ITLB_WALK where the result of the walk yields a Block.

0x818a, DTLB_WALK_PAGE

This event counts translation table walk counted by DTLB_WALK where the result of the walk yields a Page.

0x818b, ITLB_WALK_PAGE

This event counts translation table walk counted by ITLB_WALK where the result of the walk yields a Page.

0x81b8, L1I_CACHE_REFILL_HWPRF

This event counts hardware prefetch counted by L1I_CACHE_HWPRF that causes a refill of the Level 1 instruction cache from outside of the Level 1 instruction cache.

0x81bc, L1D_CACHE_REFILL_HWPRF

This event counts hardware prefetch counted by L1D_CACHE_HWPRF that causes a refill of the Level 1 data cache from outside of the Level 1 data cache.

0x81bd, L2D_CACHE_REFILL_HWPRF

This event counts hardware prefetch counted by L2D_CACHE_HWPRF that causes a refill of the Level 2 cache, or any Level 1 data and instruction cache of this PE, from outside of those caches.

0x81c0, L1I_CACHE_HIT_RD

This event counts demand fetch counted by L1I_CACHE_DM_RD that hits in the Level 1 instruction cache.

0x81c4, L1D_CACHE_HIT_RD

This event counts demand read counted by L1D_CACHE_RD that hits in the Level 1 data cache.

0x81c5, L2D_CACHE_HIT_RD

This event counts demand read counted by L2D_CACHE_RD that hits in the Level 2 data cache.

0x81c8, L1D_CACHE_HIT_WR

This event counts demand write counted by L1D_CACHE_WR that hits in the Level 1 data cache.

0x81c9, L2D_CACHE_HIT_WR

This event counts demand write counted by L2D_CACHE_WR that hits in the Level 2 data cache.

0x8200, L1I_CACHE_HIT

This event counts access counted by L1I_CACHE that hits in the Level 1 instruction cache.

0x8204, L1D_CACHE_HIT

This event counts access counted by L1D_CACHE that hits in the Level 1 data cache.

0x8205, L2D_CACHE_HIT

This event counts access counted by L2D_CACHE that hits in the Level 2 data cache.

0x8240, L1I_LFB_HIT_RD

This event counts demand access counted by L1I_CACHE_HIT_RD that hits a cache line that is in the process of being loaded into the Level 1 instruction cache.

0x8244, L1D_LFB_HIT_RD

This event counts demand access counted by L1D_CACHE_HIT_RD that hits a cache line that is in the process of being loaded into the Level 1 data cache.

0x8245, L2D_LFB_HIT_RD

This event counts demand access counted by L2D_CACHE_HIT_RD that hits a recently fetched line in the Level 2 cache.

0x8248, L1D_LFB_HIT_WR

This event counts demand access counted by L1D_CACHE_HIT_WR that hits a cache line that is in the process of being loaded into the Level 1 data cache.

0x8249, L2D_LFB_HIT_WR

This event counts demand access counted by L2D_CACHE_HIT_WR that hits a recently fetched line in the Level 2 cache.

0x8280, L1I_CACHE_PRF

This event counts fetch counted by either Level 1 instruction hardware prefetch or Level 1 instruction software prefetch.

0x8284, L1D_CACHE_PRF

This event counts fetch counted by either Level 1 data hardware prefetch or Level 1 data software prefetch.

0x8285, L2D_CACHE_PRF

This event counts fetch counted by either Level 2 data hardware prefetch or Level 2 data software prefetch.

0x8288, L1I_CACHE_REFILL_PRF

This event counts hardware prefetch counted by L1I_CACHE_PRF that causes a refill of the Level 1 instruction cache from outside of the Level 1 instruction cache.

0x828c, L1D_CACHE_REFILL_PRF

This event counts hardware prefetch counted by L1D_CACHE_PRF that causes a refill of the Level 1 data cache from outside of the Level 1 data cache.

0x828d, L2D_CACHE_REFILL_PRF

This event counts hardware prefetch counted by L2D_CACHE_PRF that causes a refill of the Level 2 data cache from outside of the Level 1 data cache.

0x8320, L1D_CACHE_REFILL_PERCYC

The counter counts by the number of cache refills counted by L1D_CACHE_REFILL in progress on each Processor cycle.

0x8321, L2D_CACHE_REFILL_PERCYC

The counter counts by the number of cache refills counted by L2D_CACHE_REFILL in progress on each Processor cycle.

0x8324, L1I_CACHE_REFILL_PERCYC

The counter counts by the number of cache refills counted by L1I_CACHE_REFILL in progress on each Processor cycle.

MONAKA Specific Events

0x0105, FP_MV_SPEC

This event counts architecturally executed floating-point move operations.

0x0108, PRD_SPEC

This event counts architecturally executed operations that using predicate register.

0x0109, IEL_SPEC

This event counts architecturally executed inter-element manipulation operations.

0x010a, IREG_SPEC

This event counts architecturally executed inter-register manipulation operations.

0x0112, FP_LD_SPEC

This event counts architecturally executed NOSIMD load operations that using SIMD&FP registers.

0x0113, FP_ST_SPEC

This event counts architecturally executed NOSIMD store operations that using SIMD&FP registers.

0x011a, BC_LD_SPEC

This event counts architecturally executed SIMD broadcast floating-point load operations.

0x011b, DCZVA_SPEC

This event counts architecturally executed zero blocking operations due to the "DC ZVA" instruction.

0x0121, EFFECTIVE_INST_SPEC

This event counts architecturally executed instructions, excluding the MOVPRFX instruction.

0x0123, PRE_INDEX_SPEC

This event counts architecturally executed operations that uses "pre-index" as its addressing mode.

0x0124, POST_INDEX_SPEC

This event counts architecturally executed operations that uses "post-index" as its addressing mode.

0x0139, UOP_SPLIT

This event counts the occurrence count of the micro-operation split.

0x0182, LD_COMP_WAIT_L1_MISS

This event counts every cycle that no instruction was committed because the oldest and uncommitted load/store/prefetch operation waits for L2 cache access.

0x0183, LD_COMP_WAIT_L1_MISS_EX

This event counts every cycle that no instruction was committed because the oldest and uncommitted integer load operation waits for L2 cache access.

0x0184, LD_COMP_WAIT

This event counts every cycle that no instruction was committed because the oldest and uncommitted load/store/prefetch operation waits for L1D cache, L2 cache and memory access.

0x0185, LD_COMP_WAIT_EX

This event counts every cycle that no instruction was committed because the oldest and uncommitted integer load operation waits for L1D cache, L2 cache and memory access.

0x0186, LD_COMP_WAIT_PFP_BUSY

This event counts every cycle that no instruction was committed due to the lack of an available prefetch port.

0x0187, LD_COMP_WAIT_PFP_BUSY_EX

This event counts the LD_COMP_WAIT_PFP_BUSY caused by an integer load operation.

0x0188, LD_COMP_WAIT_PFP_BUSY_SWPF

This event counts the LD_COMP_WAIT_PFP_BUSY caused by a software prefetch instruction.

0x0189, EU_COMP_WAIT

This event counts every cycle that no instruction was committed and the oldest and uncommitted instruction is an integer or floating-point/SIMD instruction.

0x018a, FL_COMP_WAIT

This event counts every cycle that no instruction was committed and the oldest and uncommitted instruction is a floating-point/SIMD instruction.

0x018b, BR_COMP_WAIT

This event counts every cycle that no instruction was committed and the oldest and uncommitted instruction is a branch instruction.

0x018c, ROB_EMPTY

This event counts every cycle that no instruction was committed because the CSE is empty.

0x018d, ROB_EMPTY_STQ_BUSY

This event counts every cycle that no instruction was committed because the CSE is empty and the store port (SP) is full.

0x018e, WFE_WFI_CYCLE

This event counts every cycle that the instruction unit is halted by the WFE/WFI instruction.

0x018f, RETENTION_CYCLE

This event counts every cycle that the instruction unit is halted by the RETENTION state.

0x0190, _0INST_COMMIT

This event counts every cycle that no instruction was committed, but counts at the time when commits MOVPRFX only.

0x0191, _1INST_COMMIT

This event counts every cycle that one instruction is committed.

0x0192, _2INST_COMMIT

This event counts every cycle that two instructions are committed.

0x0193, _3INST_COMMIT

This event counts every cycle that three instructions are committed.

0x0194, _4INST_COMMIT

This event counts every cycle that four instructions are committed.

0x0195, _5INST_COMMIT

This event counts every cycle that five instructions are committed.

0x0198, UOP_ONLY_COMMIT

This event counts every cycle that only any micro-operations are committed.

0x0199, SINGLE_MOVPRFX_COMMIT

This event counts every cycle that only the MOVPRFX instruction is committed.

0x019c, LD_COMP_WAIT_L2_MISS

This event counts every cycle that no instruction was committed because the oldest and uncommitted load/store/prefetch operation waits for L2 cache miss.

0x019d, LD_COMP_WAIT_L2_MISS_EX

This event counts every cycle that no instruction was committed because the oldest and uncommitted integer load operation waits for L2 cache miss.

0x01a0, EAGA_VAL

This event counts valid cycles of EAGA pipeline.

0x01a1, EAGB_VAL

This event counts valid cycles of EAGB pipeline.

0x01a3, PRX_VAL

This event counts valid cycles of PRX pipeline.

0x01a4, EXA_VAL

This event counts valid cycles of EXA pipeline.

0x01a5, EXB_VAL

This event counts valid cycles of EXB pipeline.

0x01a6, EXC_VAL

This event counts valid cycles of EXC pipeline.

0x01a7, EXD_VAL

This event counts valid cycles of EXD pipeline.

0x01a8, FLA_VAL

This event counts valid cycles of FLA pipeline.

0x01a9, FLB_VAL

This event counts valid cycles of FLB pipeline.

0x01aa, STEA_VAL

This event counts valid cycles of STEA pipeline.

0x01ab, STEB_VAL

This event counts valid cycles of STEB pipeline.

0x01ac, STFL_VAL

This event counts valid cycles of STFL pipeline.

0x01ad, STPX_VAL

This event counts valid cycles of STPX pipeline.

0x01b0, FLA_VAL_PRD_CNT

This event counts the number of 1's in the predicate bits of request in FLA pipeline, where it is corrected so that it becomes 32 when all bits are 1.

0x01b1, FLB_VAL_PRD_CNT

This event counts the number of 1's in the predicate bits of request in FLB pipeline, where it is corrected so that it becomes 32 when all bits are 1.

0x01b2, FLA_VAL_FOR_PRD

This event counts valid cycles of FLA pipeline.

0x01b3, FLB_VAL_FOR_PRD

This event counts valid cycles of FLB pipeline.

0x01f0, EA_CORE

This event counts energy consumption of core.

0x0200, L1D_CACHE_DM

This event counts L1D_CACHE caused by demand access.

0x0201 L1D_CACHE_DM_RD

This event counts L1D_CACHE caused by demand read access.

0x0202 L1D_CACHE_DM_WR

This event counts L1D_CACHE caused by demand write access.

0x0207 L1I_CACHE_DM_RD

This event counts L1I_CACHE caused by demand read access.

0x0208, L1D_CACHE_REFILL_DM

This event counts L1D_CACHE_REFILL caused by demand access.

0x0209, L1D_CACHE_REFILL_DM_RD

This event counts L1D_CACHE_REFILL caused by demand read access.

0x020a, L1D_CACHE_REFILL_DM_WR

This event counts L1D_CACHE_REFILL caused by demand write access.

0x020d, L1D_CACHE_BTC

This event counts demand access that hits cache line with shared status and requests exclusive access in the Level 1 data cache, causing a coherence access to outside of the Level 1 caches of this PE.

0x020f, L1I_CACHE_REFILL_DM_RD

This event counts L1I_CACHE_REFILL caused by demand read access.

0x0230, L1HWPF_STREAM_PF

This event counts streaming prefetch requests to L1D cache generated by hardware prefetcher.

0x0231, L1HWPF_STRIDE_PF

This event counts stride prefetch requests to L1D cache generated by hardware prefetcher.

0x0232, L1HWPF_PFTGT _PF

This event counts LDS prefetch requests to L1D cache generated by hardware prefetcher.

0x0234, L2HWPF_STREAM_PF

This event counts streaming prefetch requests to L2 cache generated by hardware prefetcher.

0x0235, L2HWPF_STRIDE_PF

This event counts stride prefetch requests to L2 cache generated by hardware prefetcher.

0x0237, L2HWPF_OTHER

This event counts prefetch requests to L2 cache generated by the other causes.

0x0238, L3HWPF_STREAM_PF

This event counts streaming prefetch requests to L3 cache generated by hardware prefetcher.

0x0239, L3HWPF_STRIDE_PF

This event counts stride prefetch requests to L3 cache generated by hardware prefetcher.

0x023b, L3HWPF_OTHER

This event counts prefetch requests to L3 cache generated by the other causes.

0x023c, L1IHWPF_NEXTLINE_PF

This event counts next line's prefetch requests to L1I cache generated by hardware prefetcher.

0x0240, L1_PIPE0_VAL

This event counts valid cycles of L1D cache pipeline#0.

0x0241, L1_PIPE1_VAL

This event counts valid cycles of L1D cache pipeline#1.

0x0242, L1_PIPE2_VAL

This event counts valid cycles of L1D cache pipeline#2.

0x0250, L1_PIPE0_COMP

This event counts completed requests in L1D cache pipeline#0.

0x0251, L1_PIPE1_COMP

This event counts completed requests in L1D cache pipeline#1.

0x025a, L1_PIPE_ABORT_STLD_INTLK

This event counts aborted requests in L1D pipelines that due to store-load interlock.

0x026c, L1I_PIPE_COMP

This event counts completed requests in L1I cache pipeline.

0x026d, L1I_PIPE_VAL

This event counts valid cycles of L1I cache pipeline.

0x0278, L1_PIPE0_VAL_IU_TAG_ADRS_SCE

This event counts requests in L1D cache pipeline#0 that its sce bit of tagged address is 1.

0x0279, L1_PIPE1_VAL_IU_TAG_ADRS_SCE

This event counts requests in L1D cache pipeline#1 that its sce bit of tagged address is 1.

0x02a0, L1_PIPE0_VAL_IU_NOT_SEC0

This event counts requests in L1D cache pipeline#0 that its sector cache ID is not 0.

0x02a1, L1_PIPE1_VAL_IU_NOT_SEC0

This event counts requests in L1D cache pipeline#1 that its sector cache ID is not 0.

0x02b0, L1_PIPE_COMP_GATHER_2FLOW

This event counts the number of times where 2 elements of the gather instructions became 2 flows because 2 elements could not be combined.

0x02b1, L1_PIPE_COMP_GATHER_1FLOW

This event counts the number of times where 2 elements of the gather instructions became 1 flow because 2 elements could be combined.

0x02b2, L1_PIPE_COMP_GATHER_0FLOW

This event counts the number of times where 2 elements of the gather instructions became 0 flow because both predicate values are 0.

0x02b3, L1_PIPE_COMP_SCATTER_1FLOW

This event counts the number of flows of the scatter instructions.

0x02b8, L1_PIPE0_COMP_PRD_CNT

This event counts the number of 1's in the predicate bits of request in L1D cache pipeline#0, where it is corrected so that it becomes 64 when all bits are 1.

0x02b9, L1_PIPE1_COMP_PRD_CNT

This event counts the number of 1's in the predicate bits of request in L1D cache pipeline#1, where it is corrected so that it becomes 64 when all bits are 1.

0x0300, L2D_CACHE_DM

This event counts L2D_CACHE caused by demand access.

0x0301, L2D_CACHE_DM_RD

This event counts L2D_CACHE caused by demand read access.

0x0302, L2D_CACHE_DM_WR

This event counts L2D_CACHE caused by demand write access.

0x0305, L2D_CACHE_HWPRF_ADJACENT

This event counts L2D_CACHE caused by hardware adjacent prefetch access.

0x0308, L2D_CACHE_REFILL_DM

This event counts L2D_CACHE_REFILL caused by demand access.

0x0309, L2D_CACHE_REFILL_DM_RD

This event counts L2D_CACHE_REFILL caused by demand read access.

0x030a, L2D_CACHE_REFILL_DM_WR

This event counts L2D_CACHE_REFILL caused by demand write access.

0x030b, L2D_CACHE_REFILL_DM_WR_EXCL

This event counts L2D_CACHE_REFILL caused by demand write exclusive access.

0x030c, L2D_CACHE_REFILL_DM_WR_ATOM

This event counts L2D_CACHE_REFILL caused by demand write atomic access.

0x030d, L2D_CACHE_BTC

This event counts demand access that hits cache line with shared status and requests exclusive access in the Level 1 data and Level 2 caches, causing a coherence access to outside of the Level 1 and Level 2 caches of this PE.

0x0330, L2_PIPE_VAL

This event counts valid cycles of L2 cache pipeline.

0x0350, L2_PIPE_COMP_ALL

This event counts completed requests in L2 cache pipeline.

0x0370, L2_PIPE_COMP_PF_L2MIB_MCH

This event counts operations where software or hardware prefetch hits an L2 cache refill buffer allocated by demand access.

0x0390, L2D_CACHE_REFILL_L3D_CACHE

This event counts operations that cause a cache access to the L3 cache.

0x0391, L2D_CACHE_REFILL_L3D_CACHE_DM

This event counts L2D_CACHE_REFILL_L3D_CACHE caused by demand access.

0x0392, L2D_CACHE_REFILL_L3D_CACHE_DM_RD

This event counts L2D_CACHE_REFILL_L3D_CACHE caused by demand read access.

0x0393, L2D_CACHE_REFILL_L3D_CACHE_DM_WR

This event counts L2D_CACHE_REFILL_L3D_CACHE caused by demand write access.

0x0394, L2D_CACHE_REFILL_L3D_CACHE_PRF

This event counts L2D_CACHE_REFILL_L3D_CACHE caused by prefetch access.

0x0395, L2D_CACHE_REFILL_L3D_CACHE_HWPRF

This event counts L2D_CACHE_REFILL_L3D_CACHE caused by hardware prefetch access.

0x0396, L2D_CACHE_REFILL_L3D_MISS

This event counts operations that cause a miss of the L3 cache.

0x0397, L2D_CACHE_REFILL_L3D_MISS_DM

This event counts L2D_CACHE_REFILL_L3D_MISS caused by demand access.

0x0398, L2D_CACHE_REFILL_L3D_MISS_DM_RD

This event counts L2D_CACHE_REFILL_L3D_MISS caused by demand read access.

0x0399, L2D_CACHE_REFILL_L3D_MISS_DM_WR

This event counts L2D_CACHE_REFILL_L3D_MISS caused by demand write access.

0x039a, L2D_CACHE_REFILL_L3D_MISS_PRF

This event counts L2D_CACHE_REFILL_L3D_MISS caused by prefetch access.

0x039b, L2D_CACHE_REFILL_L3D_MISS_HWPRF

This event counts L2D_CACHE_REFILL_L3D_MISS caused by hardware prefetch access.

0x039c, L2D_CACHE_REFILL_L3D_HIT

This event counts operations that cause a hit of the L3 cache.

0x039d, L2D_CACHE_REFILL_L3D_HIT_DM

This event counts L2D_CACHE_REFILL_L3D_HIT caused by demand access.

0x039e, L2D_CACHE_REFILL_L3D_HIT_DM_RD

This event counts L2D_CACHE_REFILL_L3D_HIT caused by demand read access.

0x039f, L2D_CACHE_REFILL_L3D_HIT_DM_WR

This event counts L2D_CACHE_REFILL_L3D_HIT caused by demand write access.

0x03a0, L2D_CACHE_REFILL_L3D_HIT_PRF

This event counts L2D_CACHE_REFILL_L3D_HIT caused by prefetch access.

0x03a1, L2D_CACHE_REFILL_L3D_HIT_HWPRF

This event counts L2D_CACHE_REFILL_L3D_HIT caused by hardware prefetch access.

0x03a2, L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT

This event counts the number of L3 cache misses where the requests hit the PFTGT buffer.

0x03a3, L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT_DM

This event counts L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT caused by demand access.

0x03a4, L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT_DM_RD

This event counts L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT caused by demand read access.

0x03a5, L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT_DM_WR

This event counts L2D_CACHE_REFILL_L3D_MISS_PFTGT_HIT caused by demand write access.

0x03a6, L2D_CACHE_REFILL_L3D_MISS_L_MEM

This event counts the number of L3 cache misses where the requests access the memory in the same socket as the requests.

0x03a7, L2D_CACHE_REFILL_L3D_MISS_FR_MEM

This event counts the number of L3 cache misses where the requests access the memory in the different socket from the requests.

0x03a8, L2D_CACHE_REFILL_L3D_MISS_L_L2

This event counts the number of L3 cache misses where the requests access the different L2 cache from the requests in the same Numa nodes as the requests.

0x03a9, L2D_CACHE_REFILL_L3D_MISS_NR_L2

This event counts the number of L3 cache misses where the requests access L2 cache in the different Numa nodes from the requests in the same socket as the requests.

0x03aa, L2D_CACHE_REFILL_L3D_MISS_NR_L3

This event counts the number of L3 cache misses where the requests access L3 cache in the different Numa nodes from the requests in the same socket as the requests.

0x03ab, L2D_CACHE_REFILL_L3D_MISS_FR_L2

This event counts the number of L3 cache misses where the requests access L2 cache in the different socket from the requests.

0x03ac, L2D_CACHE_REFILL_L3D_MISS_FR_L3

This event counts the number of L3 cache misses where the requests access L3 cache in the different socket from the requests.

0x03b0, L2D_CACHE_WB_VICTIM_CLEAN

This event counts every write-back of data from the L2 cache caused by L2 replace where the data is clean. In this case, the data will usually be written to L3 cache.

0x03b1, L2D_CACHE_WB_NT

This event counts every write-back of data from the L2 cache caused by non-temporal-store.

0x03b2, L2D_CACHE_WB_DCZVA

This event counts every write-back of data from the L2 cache caused by DC ZVA.

0x03b3, L2D_CACHE_FB

This event counts every flush-back (drop) of data from the L2 cache.

0x03f0, EA_L3

This event counts energy consumption of L3 cache.

0x03f1, EA_LDO_LOSS

This event counts energy consumption of LDO loss.

0x0880, GCYCLES

This event counts the number of cycles at 100MHz.

0x0890, FL0_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 0.

0x0891, FL1_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 1.

0x0892, FL2_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 2.

0x0893, FL3_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 3.

0x0894, FL4_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 4.

0x0895, FL5_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 5.

0x0896, FL6_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 6.

0x0897, FL7_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 7.

0x0898, FL8_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 8.

0x0899, FL9_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 9.

0x089a, FL10_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 10.

0x089b, FL11_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 11.

0x089c, FL12_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 12.

0x089d, FL13_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 13.

0x089e, FL14_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 14.

0x089f, FL15_GCYCLES

This event counts the number of cycles where the measured core is staying in the Frequency Level 15.

0x08a0, RETENTION_GCYCLES

This event counts the number of cycles where the measured core is staying in the RETENTION state.

0x08a1, RETENTION_COUNT

This event counts the number of changes from the normal state to the RETENTION state.

0x0c00, L1I_TLB_4K

This event counts operations that cause a TLB access to the L1I in 4KB page.

0x0c01, L1I_TLB_64K

This event counts operations that cause a TLB access to the L1I in 64KB page.

0x0c02, L1I_TLB_2M

This event counts operations that cause a TLB access to the L1I in 2MB page.

0x0c03, L1I_TLB_32M

This event counts operations that cause a TLB access to the L1I in 32MB page.

0x0c04, L1I_TLB_512M

This event counts operations that cause a TLB access to the L1I in 512MB page.

0x0c05, L1I_TLB_1G

This event counts operations that cause a TLB access to the L1I in 1GB page.

0x0c06, L1I_TLB_16G

This event counts operations that cause a TLB access to the L1I in 16GB page.

0x0c08, L1D_TLB_4K

This event counts operations that cause a TLB access to the L1D in 4KB page.

0x0c09, L1D_TLB_64K

This event counts operations that cause a TLB access to the L1D in 64KB page.

0x0c0a, L1D_TLB_2M

This event counts operations that cause a TLB access to the L1D in 2MB page.

0x0c0b, L1D_TLB_32M

This event counts operations that cause a TLB access to the L1D in 32MB page.

0x0c0c, L1D_TLB_512M

This event counts operations that cause a TLB access to the L1D in 512MB page.

0x0c0d, L1D_TLB_1G

This event counts operations that cause a TLB access to the L1D in 1GB page.

0x0c0e, L1D_TLB_16G

This event counts operations that cause a TLB access to the L1D in 16GB page.

0x0c10, L1I_TLB_REFILL_4K

This event counts operations that cause a TLB refill to the L1I in 4KB page.

0x0c11, L1I_TLB_ REFILL_64K

This event counts operations that cause a TLB refill to the L1I in 64KB page.

0x0c12, L1I_TLB_ REFILL_2M

This event counts operations that cause a TLB refill to the L1I in 2MB page.

0x0c13, L1I_TLB_ REFILL_32M

This event counts operations that cause a TLB refill to the L1I in 32MB page.

0x0c14, L1I_TLB_ REFILL_512M

This event counts operations that cause a TLB refill to the L1I in 512MB page.

0x0c15, L1I_TLB_ REFILL_1G

This event counts operations that cause a TLB refill to the L1I in 1GB page.

0x0c16, L1I_TLB_ REFILL_16G

This event counts operations that cause a TLB refill to the L1I in 16GB page.

0x0c18, L1D_TLB_ REFILL_4K

This event counts operations that cause a TLB refill to the L1D in 4KB page.

0x0c19, L1D_TLB_ REFILL_64K

This event counts operations that cause a TLB refill to the L1D in 64KB page.

0x0c1a, L1D_TLB_ REFILL_2M

This event counts operations that cause a TLB refill to the L1D in 2MB page.

0x0c1b, L1D_TLB_ REFILL_32M

This event counts operations that cause a TLB refill to the L1D in 32MB page.

0x0c1c, L1D_TLB_ REFILL_512M

This event counts operations that cause a TLB refill to the L1D in 512MB page.

0x0c1d, L1D_TLB_ REFILL_1G

This event counts operations that cause a TLB refill to the L1D in 1GB page.

0x0c1e, L1D_TLB_ REFILL_16G

This event counts operations that cause a TLB refill to the L1D in 16GB page.

0x0c20, L2I_TLB_4K

This event counts operations that cause a TLB access to the L2I in 4KB page.

0x0c21, L2I_TLB_64K

This event counts operations that cause a TLB access to the L2I in 64KB page.

0x0c22, L2I_TLB_2M

This event counts operations that cause a TLB access to the L2I in 2MB page.

0x0c23, L2I_TLB_32M

This event counts operations that cause a TLB access to the L2I in 32MB page.

0x0c24, L2I_TLB_512M

This event counts operations that cause a TLB access to the L2I in 512MB page.

0x0c25, L2I_TLB_1G

This event counts operations that cause a TLB access to the L2I in 1GB page.

0x0c26, L2I_TLB_16G

This event counts operations that cause a TLB access to the L2I in 16GB page.

0x0c28, L2D_TLB_4K

This event counts operations that cause a TLB access to the L2D in 4KB page.

0x0c29, L2D_TLB_64K

This event counts operations that cause a TLB access to the L2D in 64KB page.

0x0c2a, L2D_TLB_2M

This event counts operations that cause a TLB access to the L2D in 2MB page.

0x0c2b, L2D_TLB_32M

This event counts operations that cause a TLB access to the L2D in 32MB page.

0x0c2c, L2D_TLB_512M

This event counts operations that cause a TLB access to the L2D in 512MB page.

0x0c2d, L2D_TLB_1G

This event counts operations that cause a TLB access to the L2D in 1GB page.

0x0c2e, L2D_TLB_16G

This event counts operations that cause a TLB access to the L2D in 16GB page.

0x0c30, L2I_TLB_REFILL_4K

This event counts operations that cause a TLB refill to the L2Iin 4KB page.

0x0c31, L2I_TLB_ REFILL_64K

This event counts operations that cause a TLB refill to the L2I in 64KB page.

0x0c32, L2I_TLB_ REFILL_2M

This event counts operations that cause a TLB refill to the L2I in 2MB page.

0x0c33, L2I_TLB_ REFILL_32M

This event counts operations that cause a TLB refill to the L2I in 32MB page.

0x0c34, L2I_TLB_ REFILL_512M

This event counts operations that cause a TLB refill to the L2I in 512MB page.

0x0c35, L2I_TLB_ REFILL_1G

This event counts operations that cause a TLB refill to the L2I in 1GB page.

0x0c36, L2I_TLB_ REFILL_16G

This event counts operations that cause a TLB refill to the L2I in 16GB page.

0x0c38, L2D_TLB_ REFILL_4K

This event counts operations that cause a TLB refill to the L2D in 4KB page.

0x0c39, L2D_TLB_ REFILL_64K

This event counts operations that cause a TLB refill to the L2D in 64KB page.

0x0c3a, L2D_TLB_ REFILL_2M

This event counts operations that cause a TLB refill to the L2D in 2MB page.

0x0c3b, L2D_TLB_ REFILL_32M

This event counts operations that cause a TLB refill to the L2D in 32MB page.

0x0c3c, L2D_TLB_ REFILL_512M

This event counts operations that cause a TLB refill to the L2D in 512MB page.

0x0c3d, L2D_TLB_ REFILL_1G

This event counts operations that cause a TLB refill to the L2D in 1GB page.

0x0c3e, L2D_TLB_ REFILL_16G

This event counts operations that cause a TLB refill to the L2D in 16GB page.

MONAKA Specific Un-core (MAC) Events

0x000, MAC_CYCLES

This event counts MAC cycles at MAC frequency.

0x010, MAC_READ_COUNT

This event counts the number of read requests to MAC.

0x011, MAC_READ_COUNT_REQUEST

This event counts the number of read requests including retry to MAC.

0x012, MAC_READ_COUNT_RETURN

This event counts the number of read requests to MAC.

0x013, MAC_READ_COUNT_REQUEST_PFTGT

This event counts the number of read requests including retry with PFTGT flag.

0x014, MAC_READ_COUNT_REQUEST_NORMAL

This event counts the number of read requests including retry without PFTGT flag.

0x015, MAC_READ_COUNT_RETURN_PFTGT_HIT

This event counts the number of read requests which hit the PFTGT buffer.

0x016, MAC_READ_COUNT_RETURN_PFTGT_MISS

This event counts the number of read requests which miss the PFTGT buffer.

0x017, MAC_READ_WAIT

This event counts outstanding read requests issued by DDR memory controller per cycle.

0x020, MAC_WRITE_COUNT

This event counts the number of write requests to MAC (including zero write, full write, partial write, write cancel).

0x021, MAC_WRITE_COUNT_WRITE

This event counts the number of full write requests to MAC (not including zero write).

0x022, MAC_WRITE_COUNT_PWRITE

This event counts the number of partial write requests to MAC.

0x040, MAC_MEMORY_READ_COUNT

This event counts the number of read requests from MAC to memory.

0x050, MAC_MEMORY_WRITE_COUNT

This event counts the number of full write requests from MAC to memory.

0x060, MAC_MEMORY_PWRITE_COUNT

This event counts the number of partial write requests from MAC to memory.

0x080, EA_MAC

This event counts energy consumption of the MAC.

0x090, EA_MEMORY

This event counts energy consumption of the memory.

0x091, EA_MEMORY_MAC_READ

This event counts the number of read requests from MAC to memory.

0x092, EA_MEMORY_MAC_WRITE

This event counts the number of write requests from MAC to memory.

0x093, EA_MEMORY_MAC_PWRITE

This event counts the number of partial write requests from MAC to memory.

0x0a0, EA_HA

This event counts energy consumption of the HA.

MONAKA Specific Un-core (PCI) Events

0x000, PCI_PORT0_CYCLES

This event counts PCI cycles at PCI frequency in port0.

0x010, PCI_PORT0_READ_COUNT

This event counts read transactions for data transfer in port0.

0x014, PCI_PORT0_READ_COUNT_BUS

This event counts read transactions for bus usage in port0.

0x020, PCI_PORT0_WRITE_COUNT

This event counts write transactions for data transfer in port0.

0x024, PCI_PORT0_WRITE_COUNT_BUS

This event counts write transactions for bus usage in port0.

0x040, PCI_PORT1_CYCLES

This event counts PCI cycles at PCI frequency in port1.

0x050, PCI_PORT1_READ_COUNT

This event counts read transactions for data transfer in port1.

0x054, PCI_PORT1_READ_COUNT_BUS

This event counts read transactions for bus usage in port1.

0x060, PCI_PORT1_WRITE_COUNT

This event counts write transactions for data transfer in port1.

0x064, PCI_PORT1_WRITE_COUNT_BUS

This event counts write transactions for bus usage in port1.

0x080, EA_PCI

This event counts energy consumption of the PCI.