2D Filtering with Xilinx Artix-7 FPGA

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Real Time Imaging and Control

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Top Module

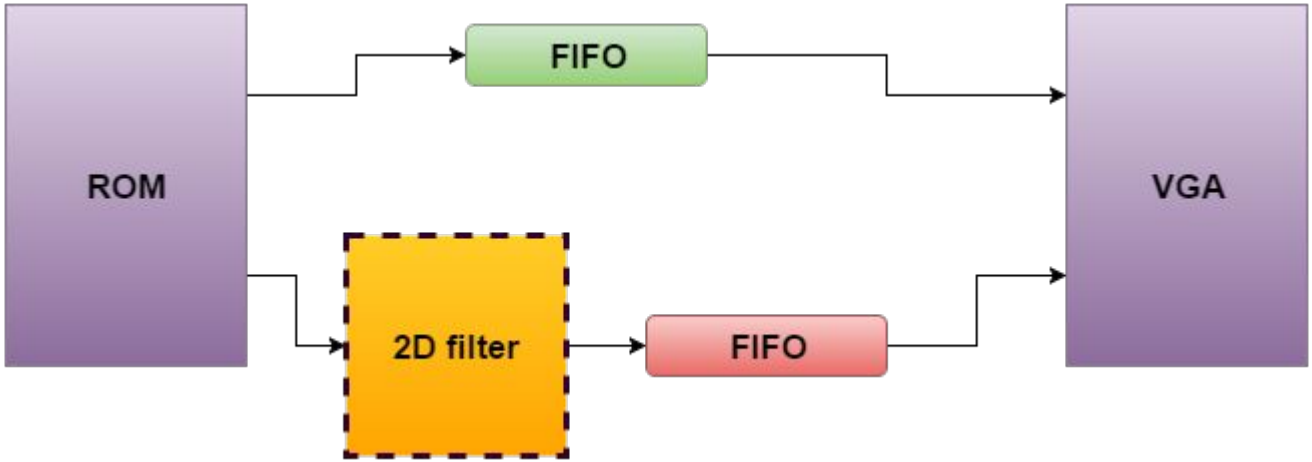


fig 0: Top Module

Filpflops and FIFOs

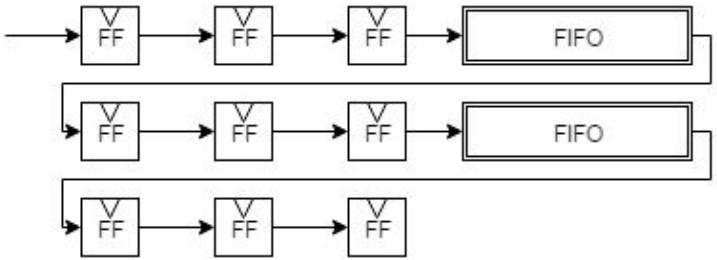


fig 1: flipflops and fifos’

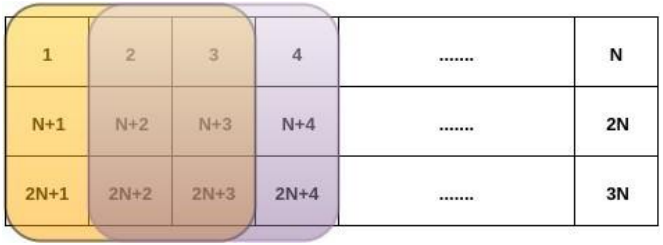
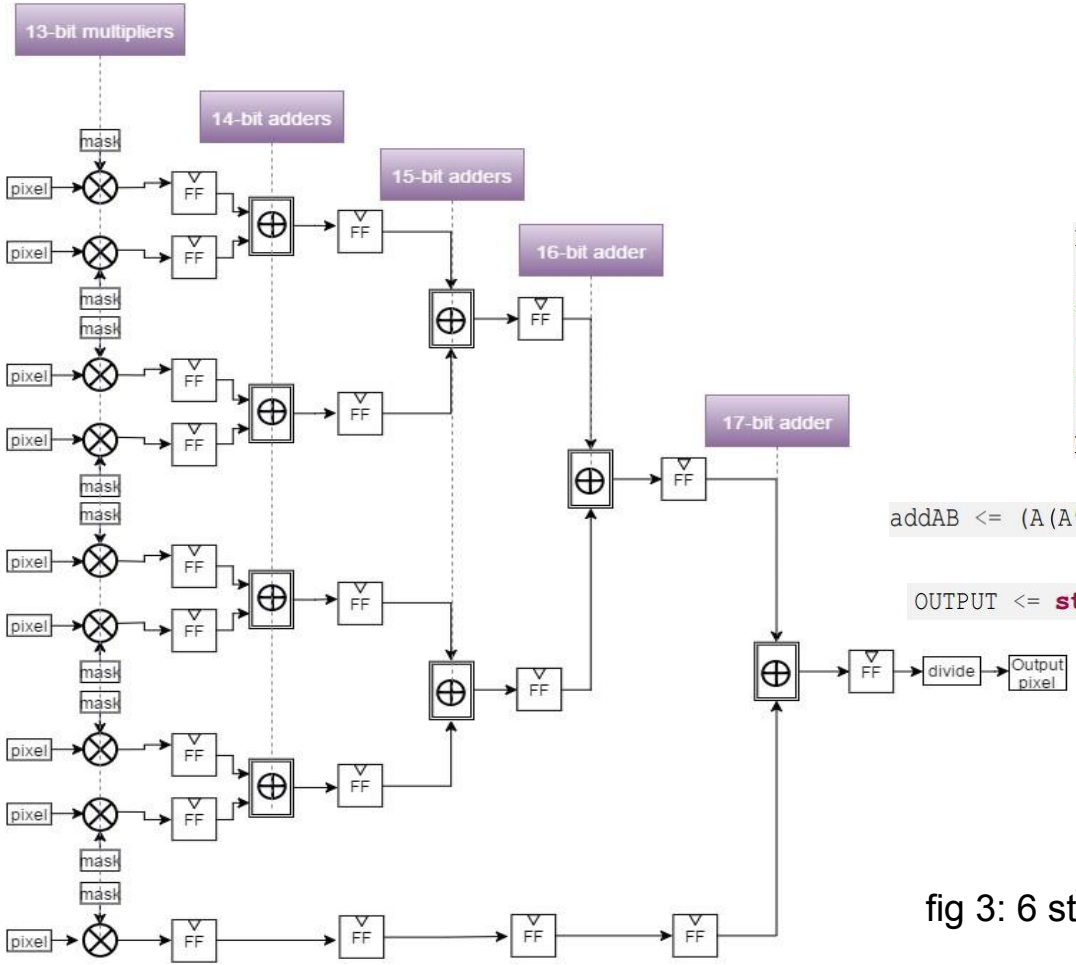


fig 2: Sliding Window

Algorithm




```
PIXEL : in std_logic_vector(7 downto 0);
--
signal product : signed(12 downto 0);
--
signal mask : signed(3 downto 0):=x"1";
--
product <= mask*signed( "0" & (PIXEL) );
```

```
addAB <= (A(A'left) & signed(A)) + (B(B'left) & signed(B));
```

```
OUTPUT <= std_logic_vector(absoluteSum(10 downto 3));
```

fig 3: 6 stage pipeline of 3 x 3 image filter

Scheduler

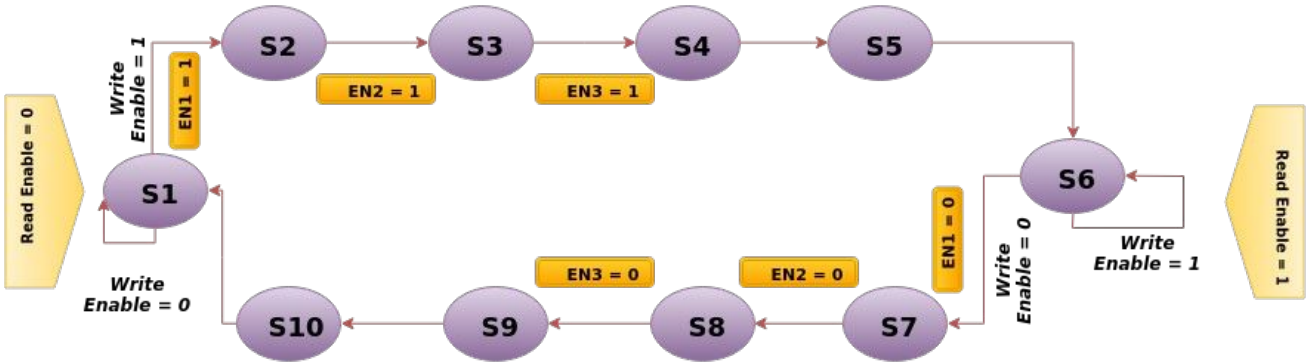


fig 4: state machine for convolution

Scheduler

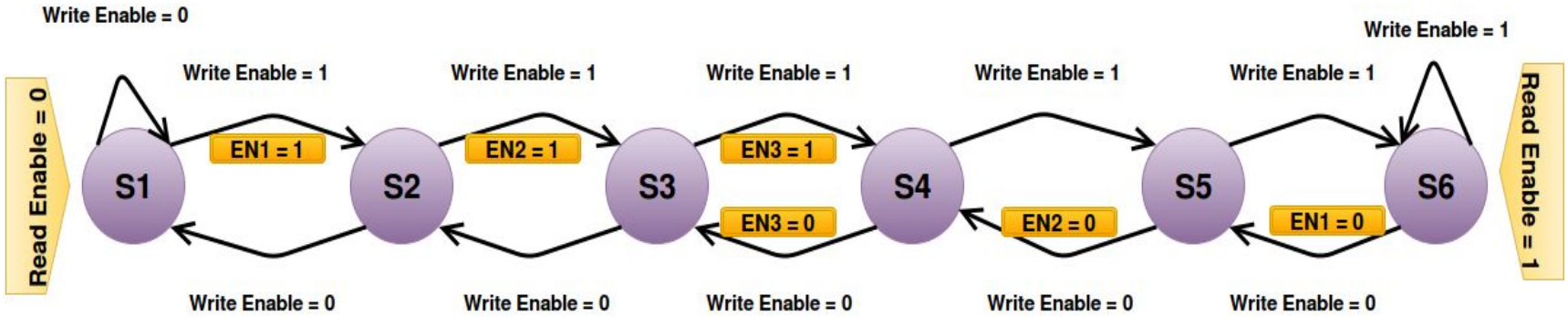
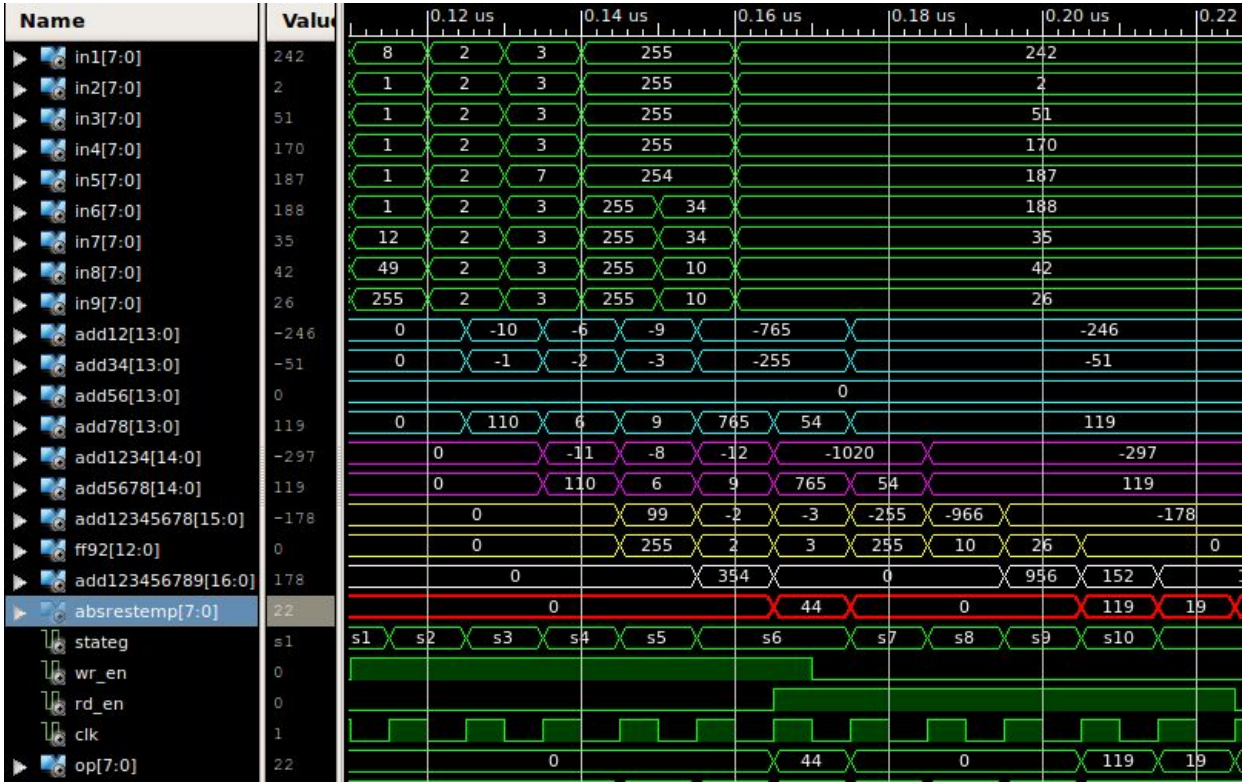


fig 5: Minimised version

Timing diagram



-1
-2
-1
0
0
0
1
2
1

fig 6: timing of kernel

Cache

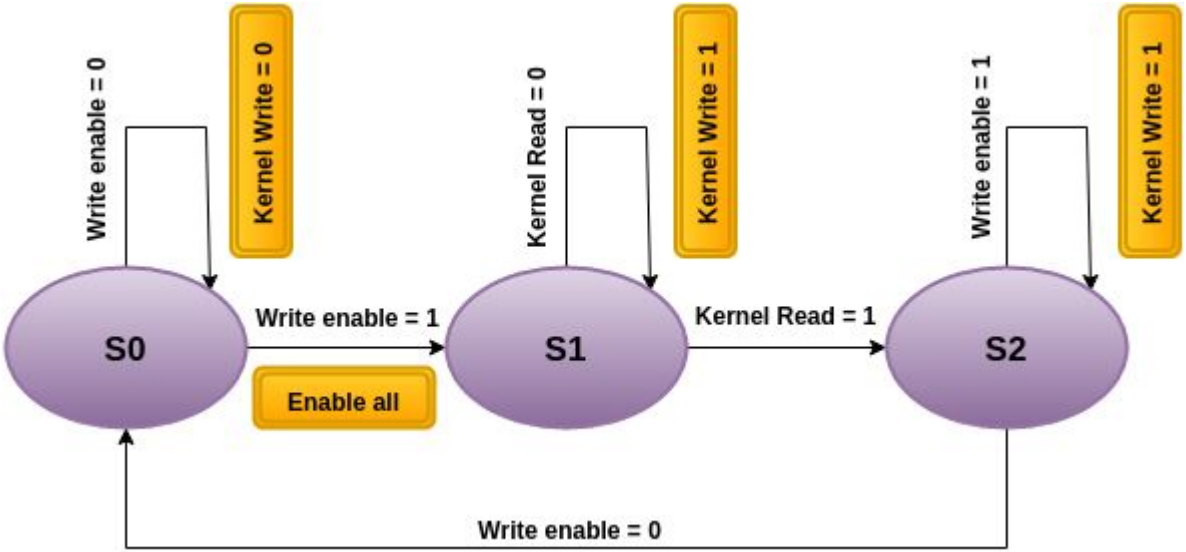


fig 7: State Machine for Cache

Top Module

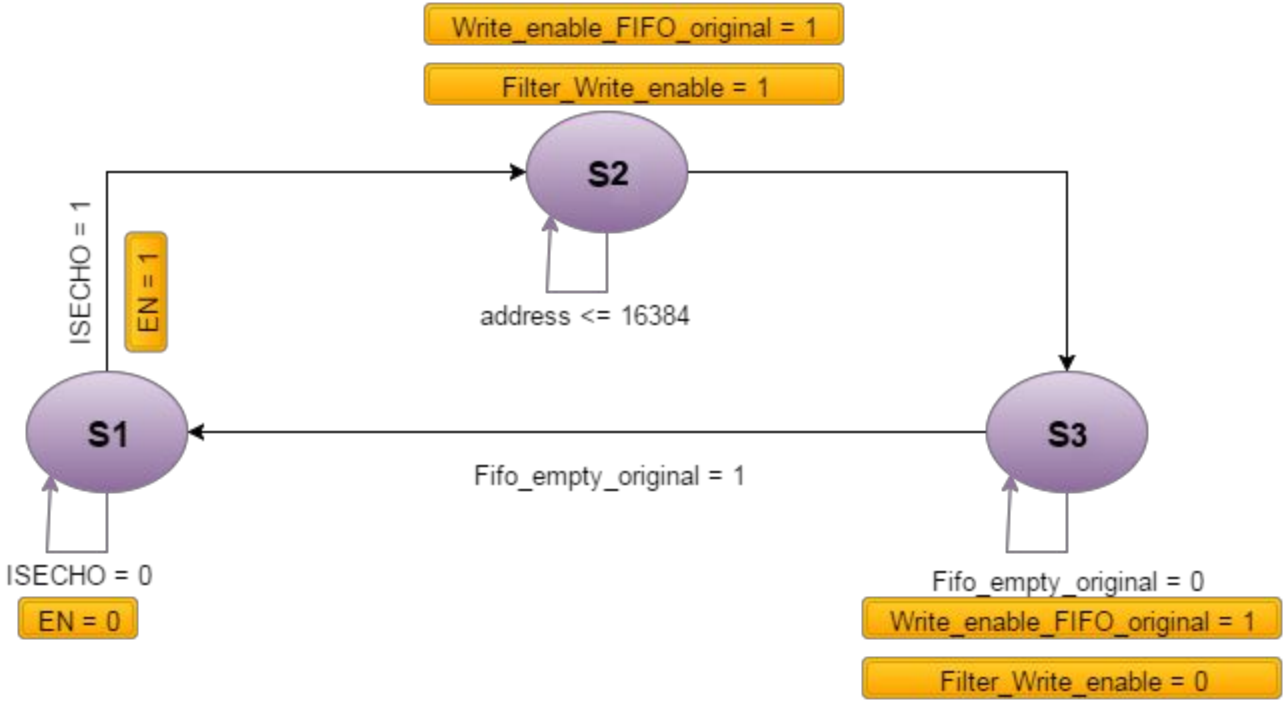


fig 8: state machine for top module

Comparison

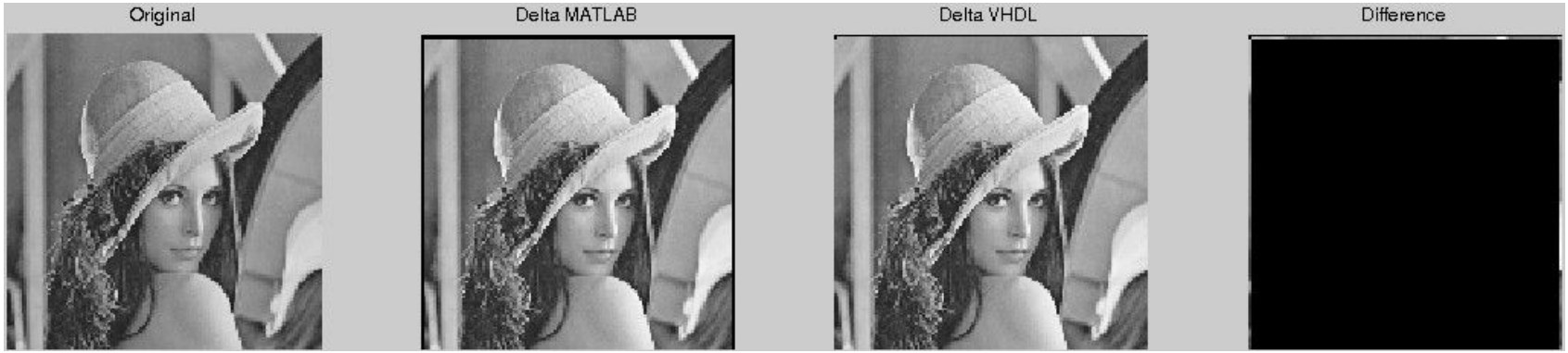


fig 9: Delta filter (matlab vs vhdl)

Comparison

fig 10: Blur filter (matlab vs vhdl)

Comparison

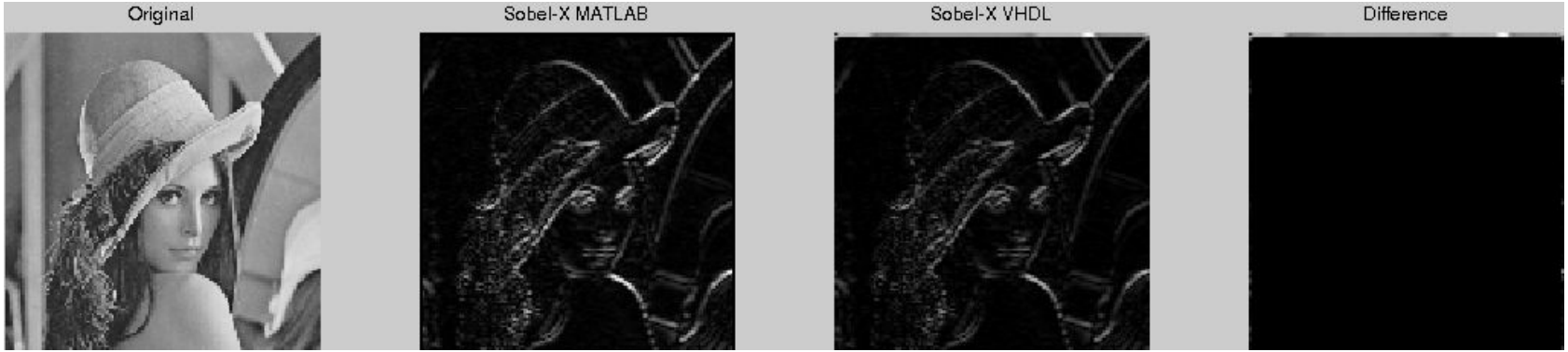


fig 11: Sobel-X filter (matlab vs vhdl)

Comparison

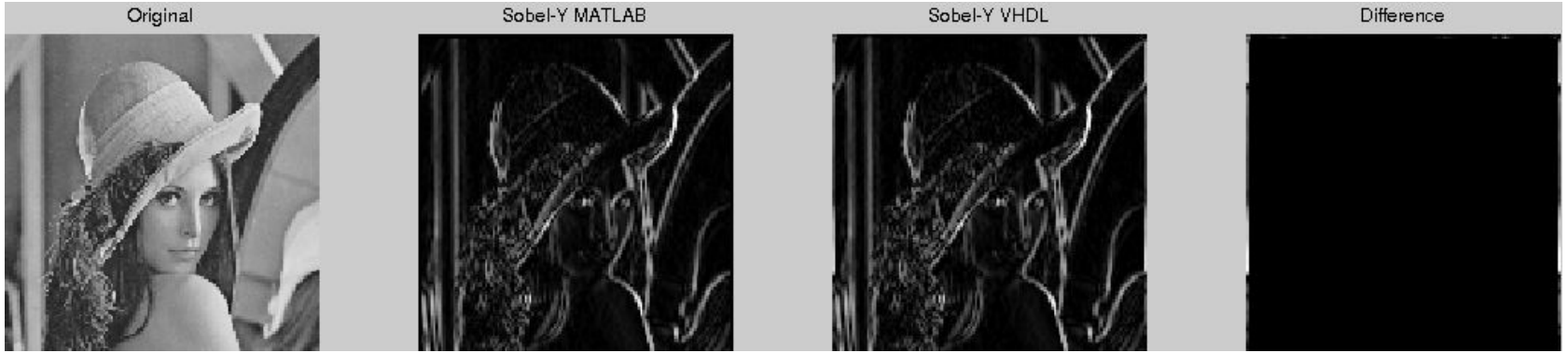


fig 12: Sobel-Y filter (matlab vs vhdl)

Comparison

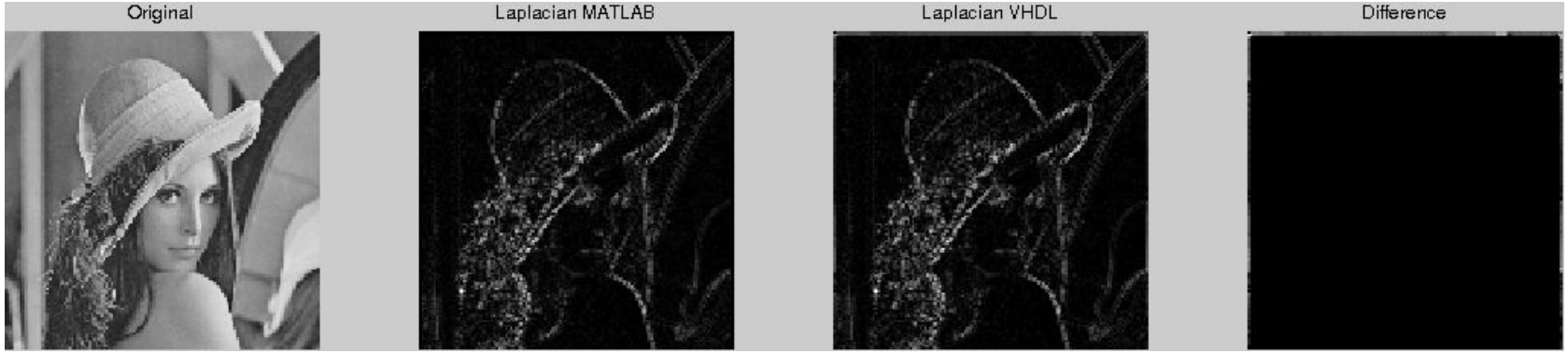


fig 13: Laplacian filter (matlab vs vhdl)

Thanks