Chapter 11 Introduction to Digital Signal Processing

Outline

- Digital Signal Processing Basics
- Converting Analog Signals to Digital
- Analog-to-Digital Conversion Methods
- Digital-to-Analog Conversion Methods

11.1 Digital Signal Processing Basics

- Naturally occurred signals are usually analog
- Analog signals should be converted to digital form before being further processed
- Digital signals should be converted back to analog form sometimes

Figure 11–1 An original analog signal (sine wave) and its "stairstep" approximation.

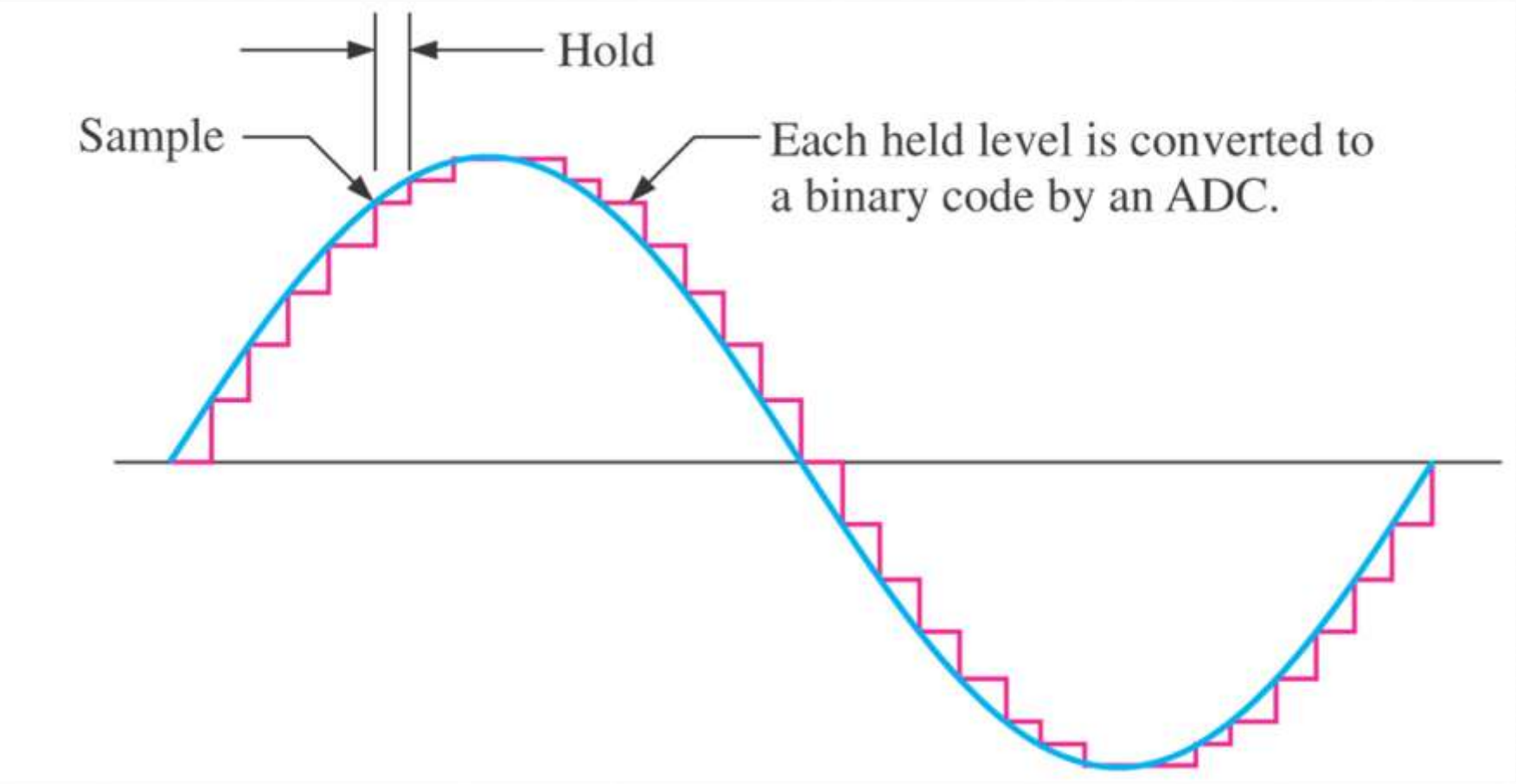
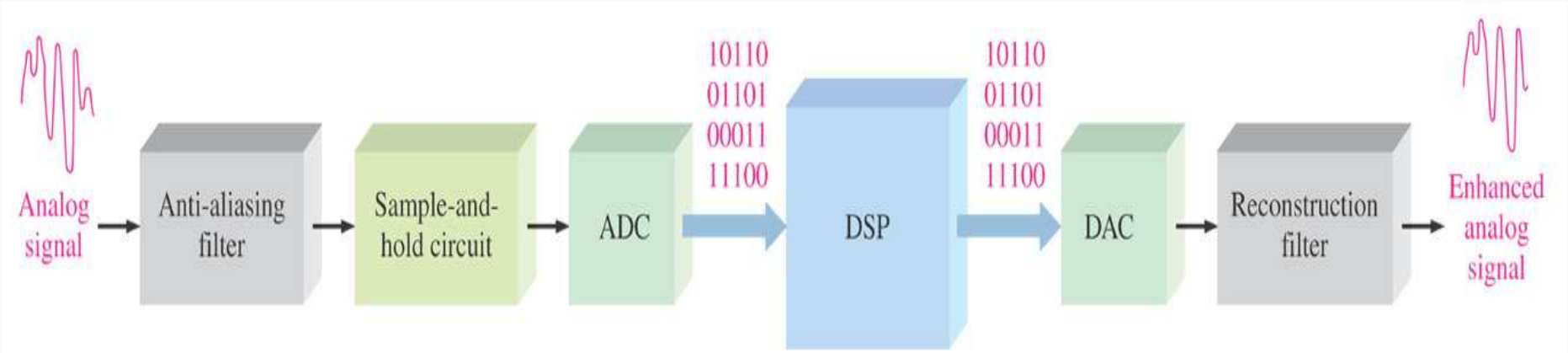


Figure 11–2 Basic block diagram of a typical digital signal processing system.



11.2 Converting analog signals to digital

- Sampling and filtering
- Holding the sampled value
- Analog-to-digital conversion

Sampling and Filtering

- Sampling
  - Take a sufficient number of discrete values at points on a waveform that defines the shape of waveform
  - Converts an analog signal into a series of impulses
- Filtering
  - Sampling theorem
    - The sampling frequency must be at least twice the highest frequency component of the analog signal
  - Nyquist frequency

Figure 13–3 Illustration of the sampling process.

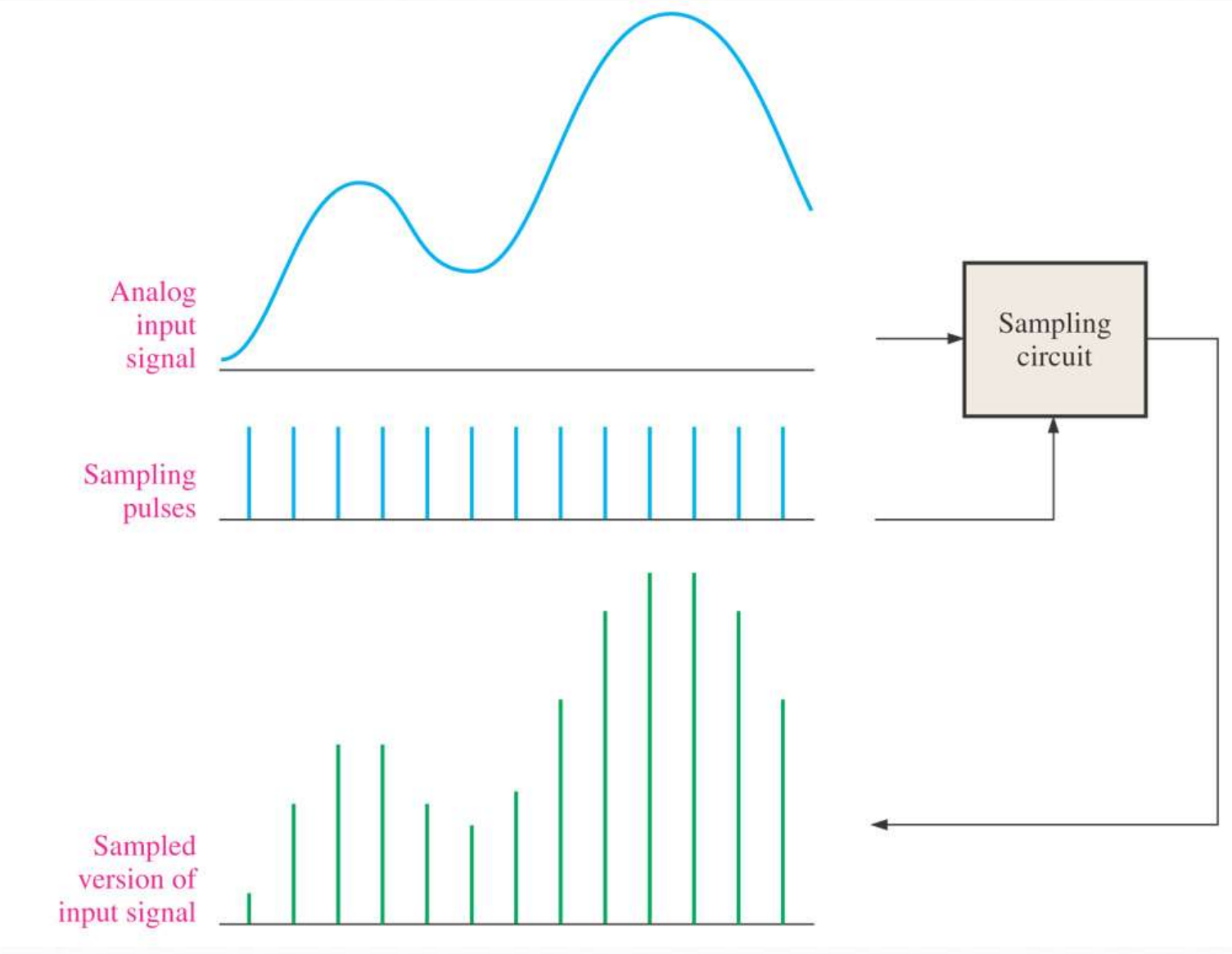
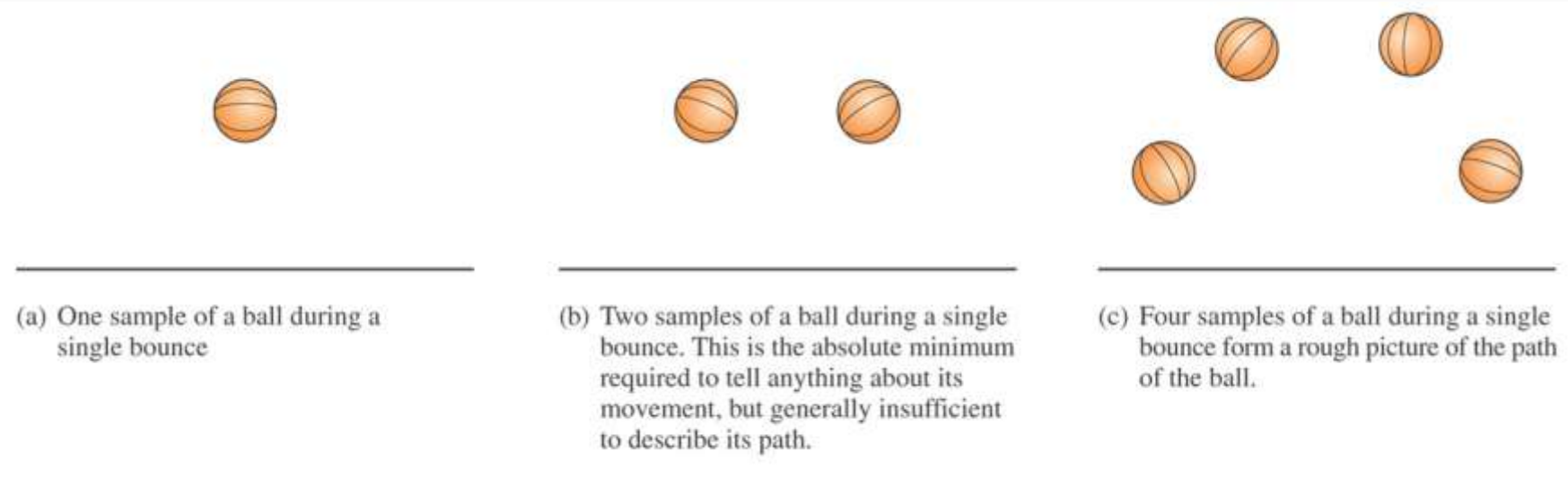


Figure 13–4 Bouncing ball analogy of sampling theory.

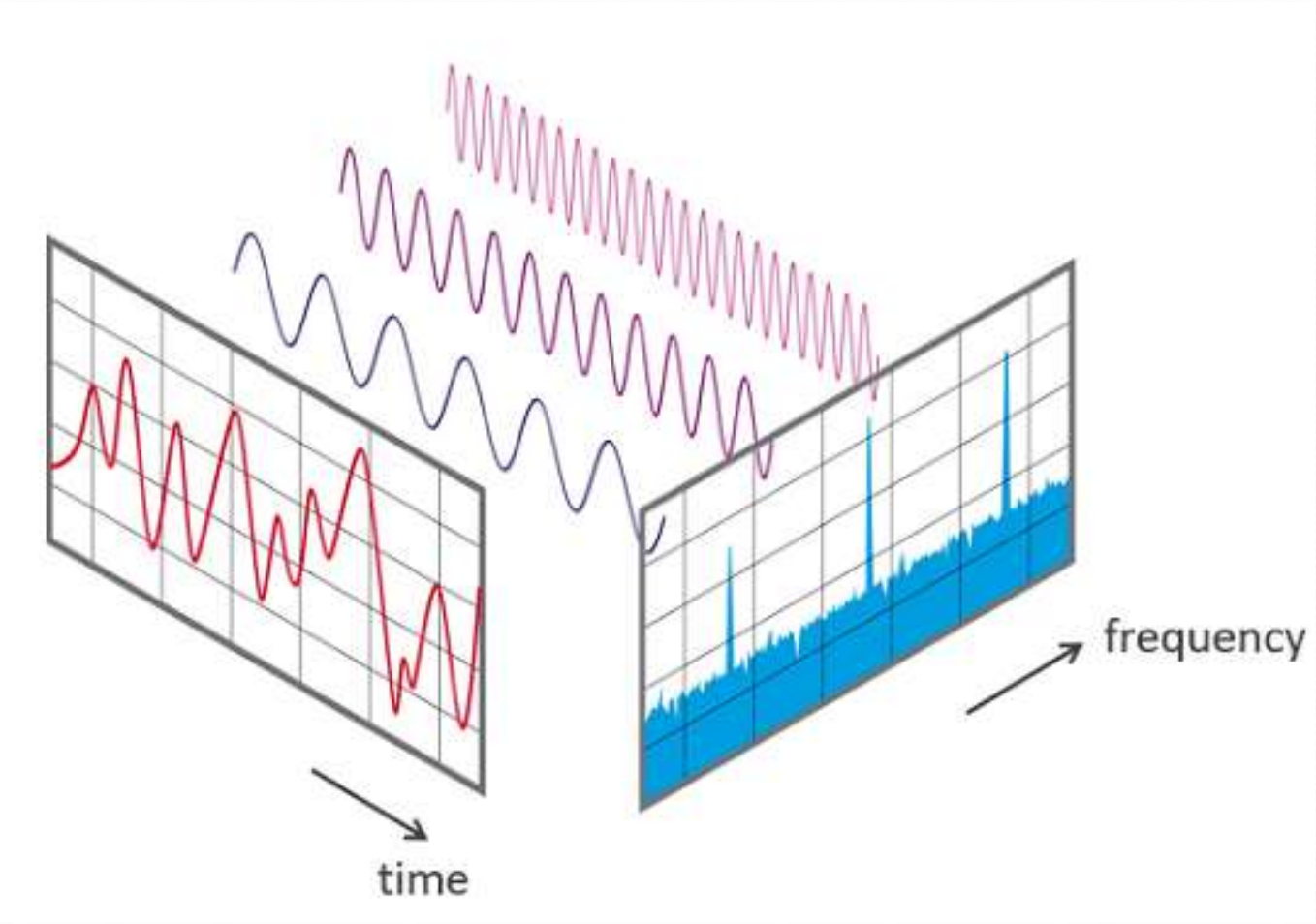


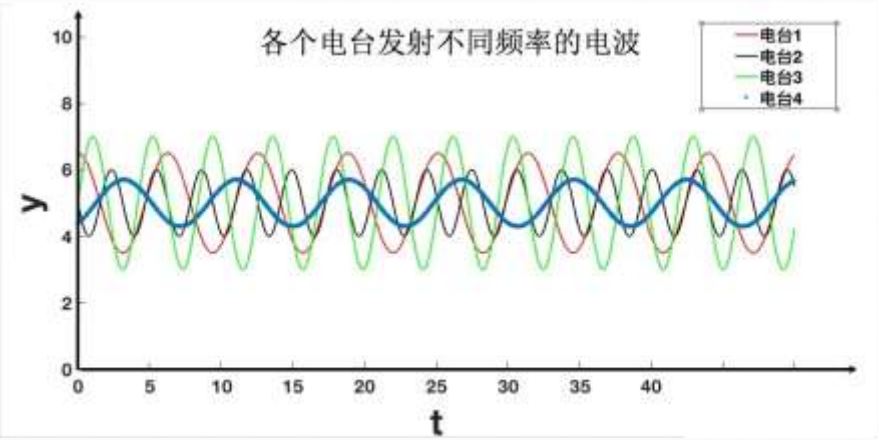
(a) One sample of a ball during a single bounce

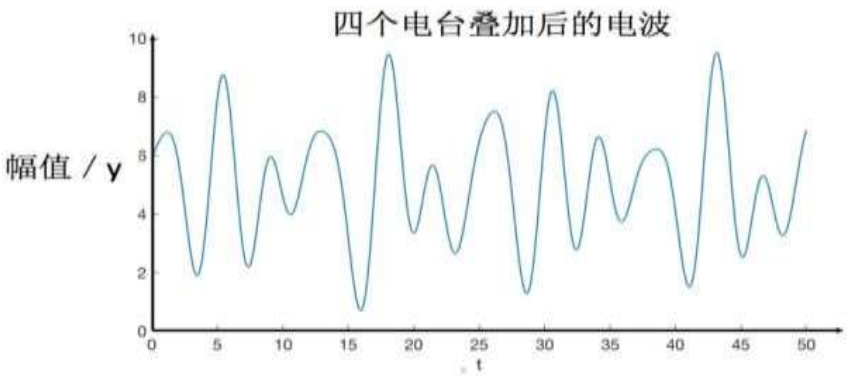
(b) Two samples of a ball during a single bounce. This is the absolute minimum required to tell anything about its movement, but generally insufficient to describe its path.

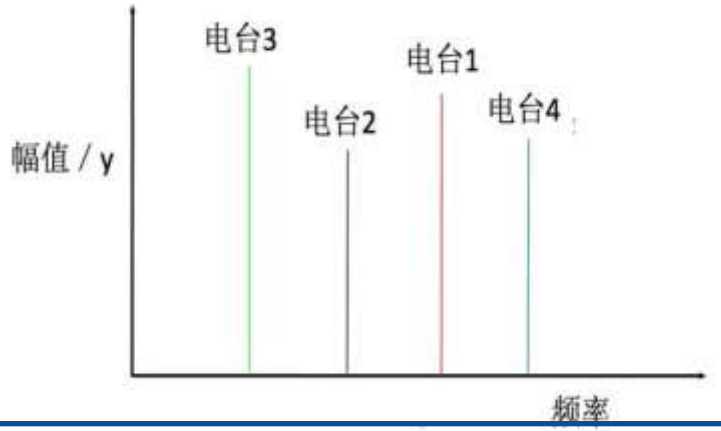
(c) Four samples of a ball during a single bounce form a rough picture of the path of the ball.

How many photos need to be taken to keep the path of the ball?


frequency
time


各个电台发射不同频率的电波
电台1
电台2
电台3
电台4
y
t


四个电台叠加后的电波
幅值 / y
t


电台3
电台1
电台2
电台4
幅值 / y
频率

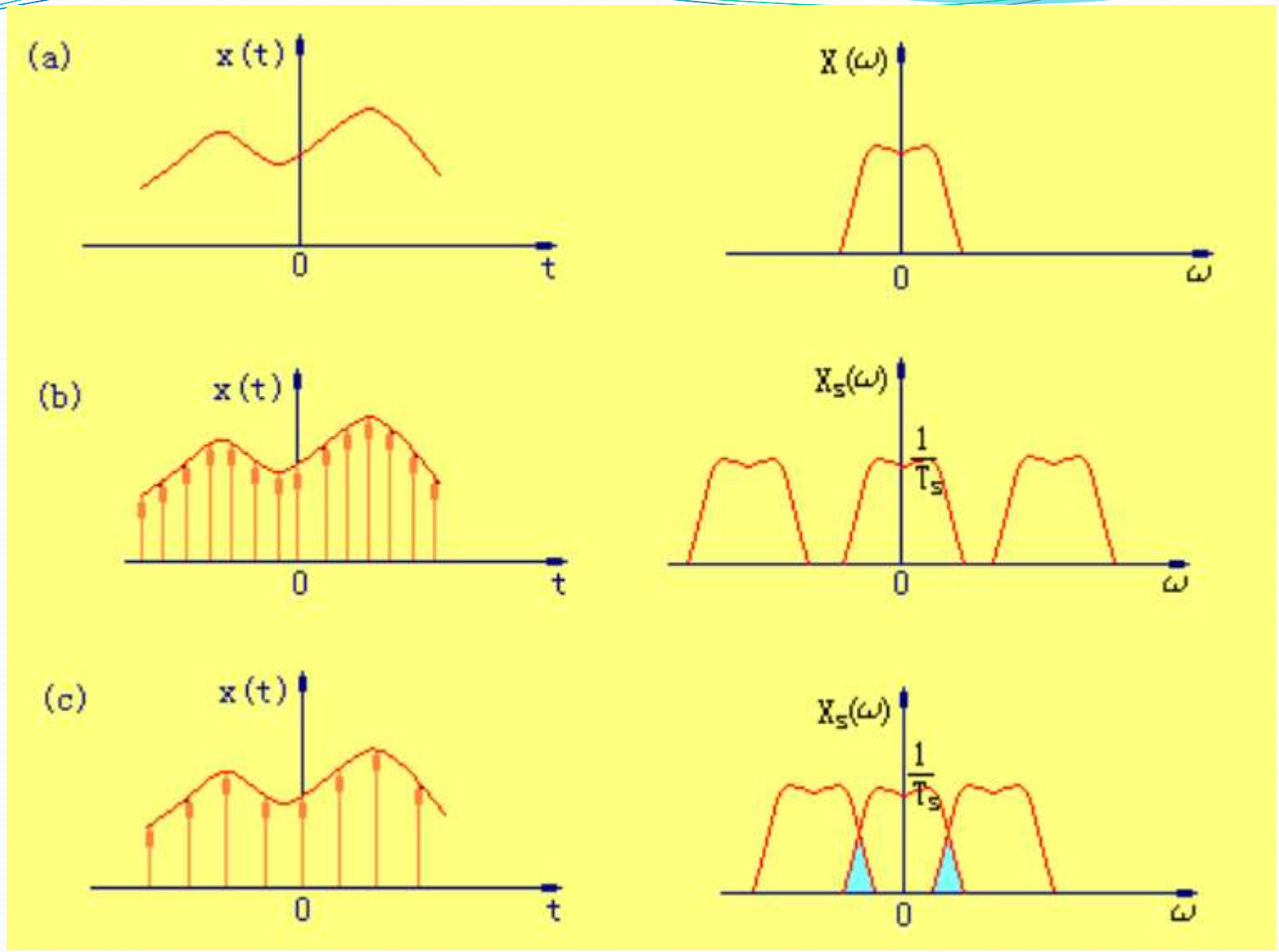
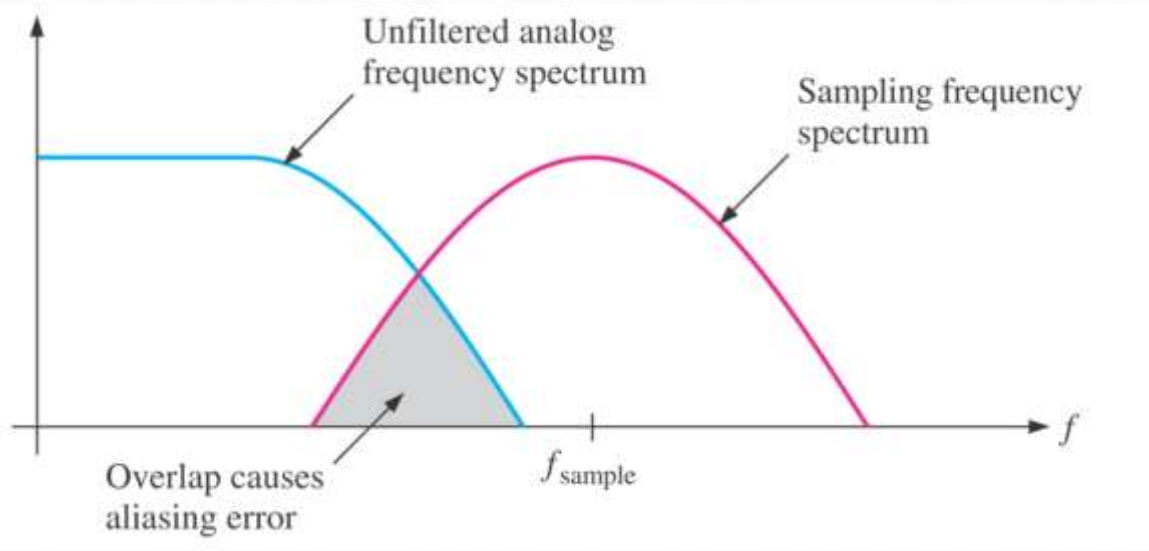
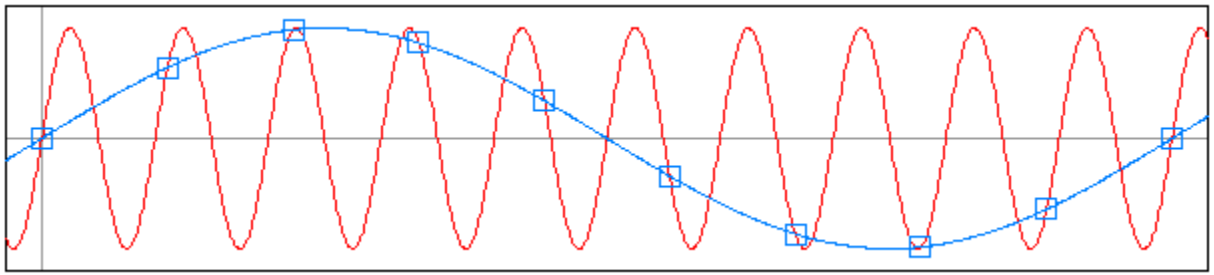
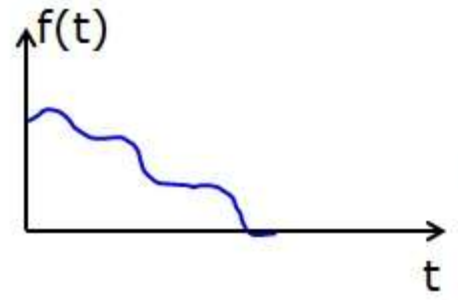

(a)
x(t)
0
t
X(ω)
0
ω
(b)
x(t)
0
t
Xs(ω)
1/Ts
0
ω
(c)
x(t)
0
t
Xs(ω)
1/Ts
0
ω

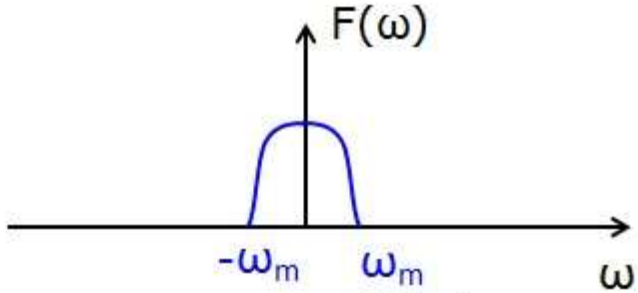
Figure 11–6 After low-pass filtering, the frequency spectra of the analog and the sampling signals do not overlap, thus eliminating aliasing error.



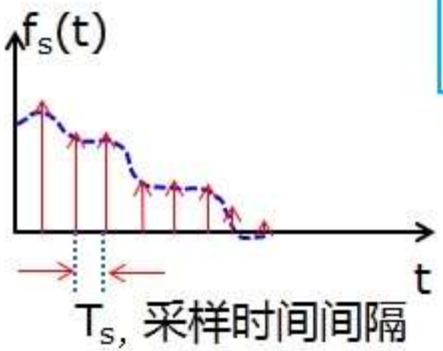


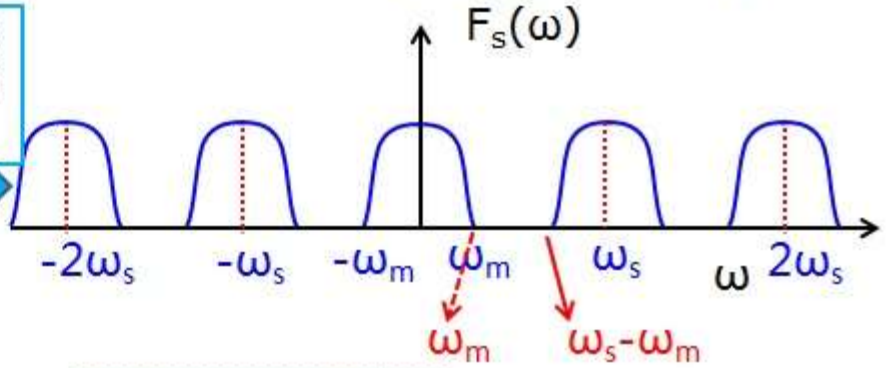


原始信号频谱



信号采样后频谱被搬移形成完全相同重复分布于$n\omega_s$处的频谱





采样后的信号要在频域进行低通滤波然后才能还原，还原的条件是采样后的频谱不会出现交叠部分，由上图可知即要求： $\omega_s - \omega_m > \omega_m$,

采样频率要大于信号最高频率的2倍

$\omega_s > 2\omega_m$ → $f_s > 2f_m$, $f_s = 1/T_s$

fs采样频率

$T_s < 1/(2f_m)$

$f_m < 0.5\ f_s = f_N$

f_N 为Nyquist频率

Holding the Sampled Value

- The sampled level must be held constant until the next sample occur.
- It is necessary for ADC to have time to process the sampled value.

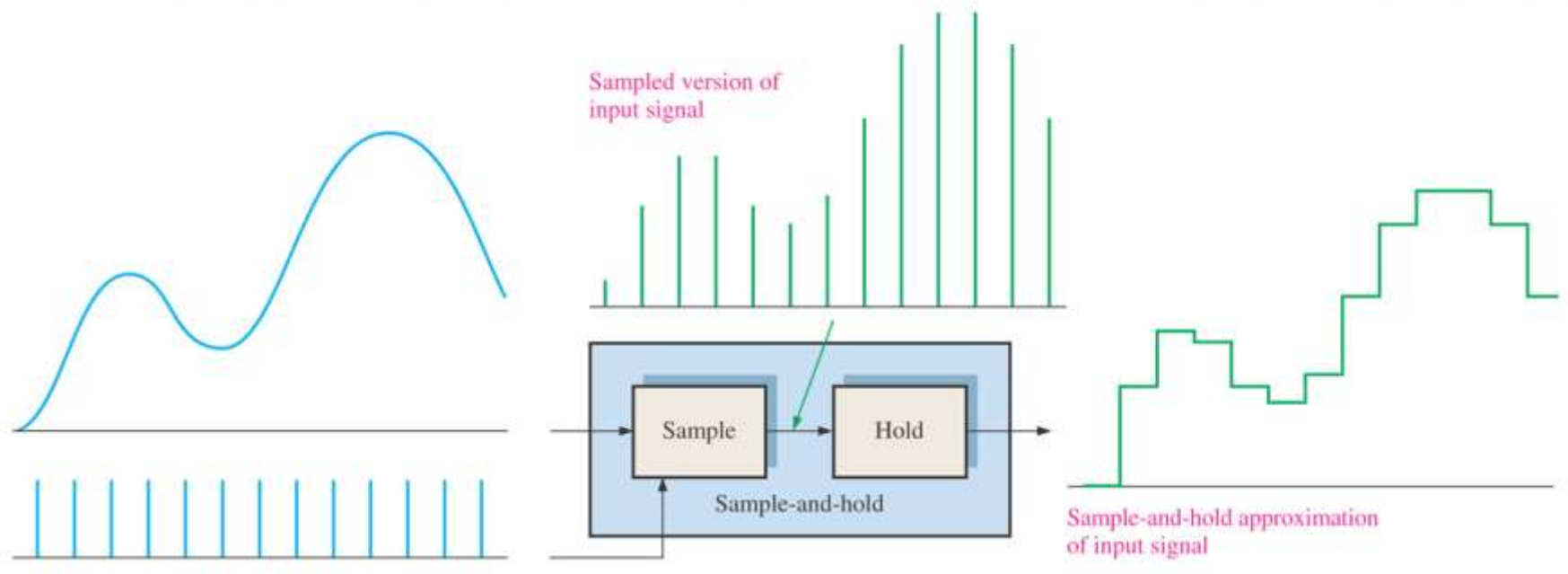
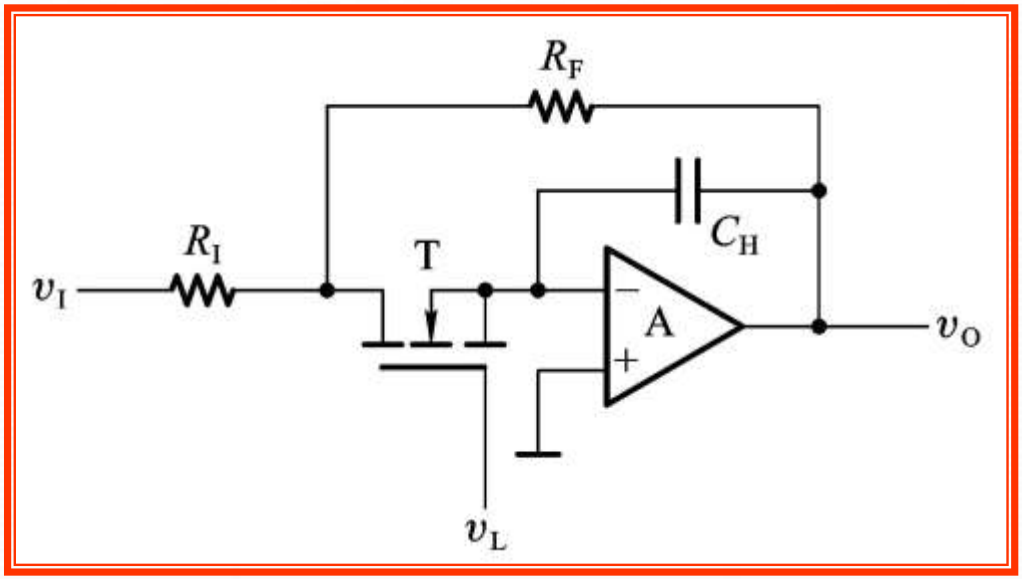


Figure 11–7 Illustration of a sample-and-hold operation.

Holding Circuit



- When v_L is High, NMOS is on, and v_I charges C_H through R_I and T. If $R_I = R_F$, then $v_o = v_c = -v_I$

- When v_L is Low, NMOS is off, and voltage of C_H stays the same and v_o also stays the same.

Analog-to-Digital Conversion

- Convert the output of the sample-and-hold circuit to a series of binary codes.
- ADC must complete the conversion between sample pulses (within the conversion interval).

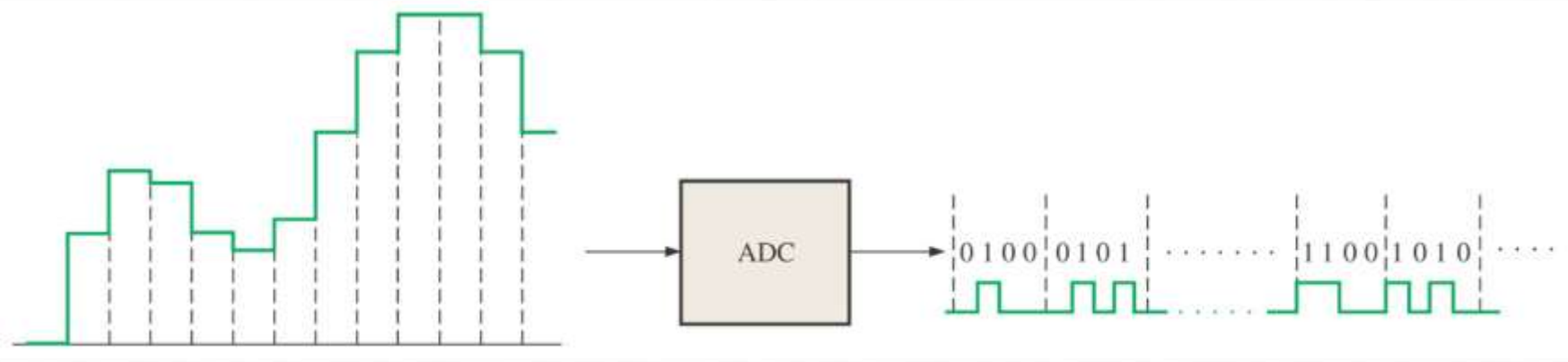


Figure 11–8 Basic function of an analog-to-digital (ADC) converter (The binary codes and number of bits are arbitrarily chosen for illustration only). The ADC output waveform that represents the binary codes is also shown.

Figure 11–9 Sample-and-hold output waveform with four quantization levels. The original analog waveform is shown in light gray for reference.

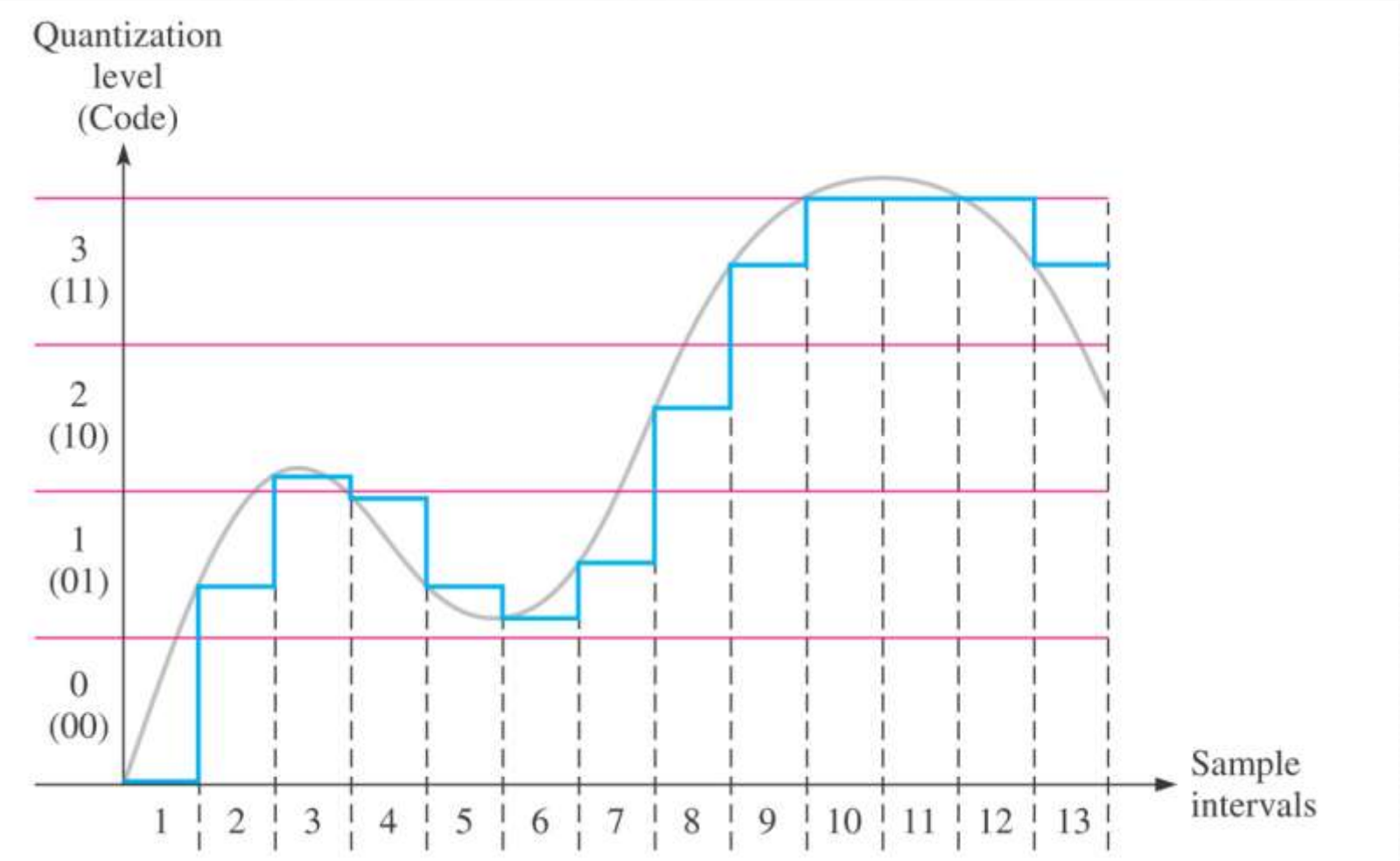


Figure 11–10 The reconstructed waveform in Figure 11–9 using four quantization levels (2 bits). The original analog waveform is shown in light gray for reference.

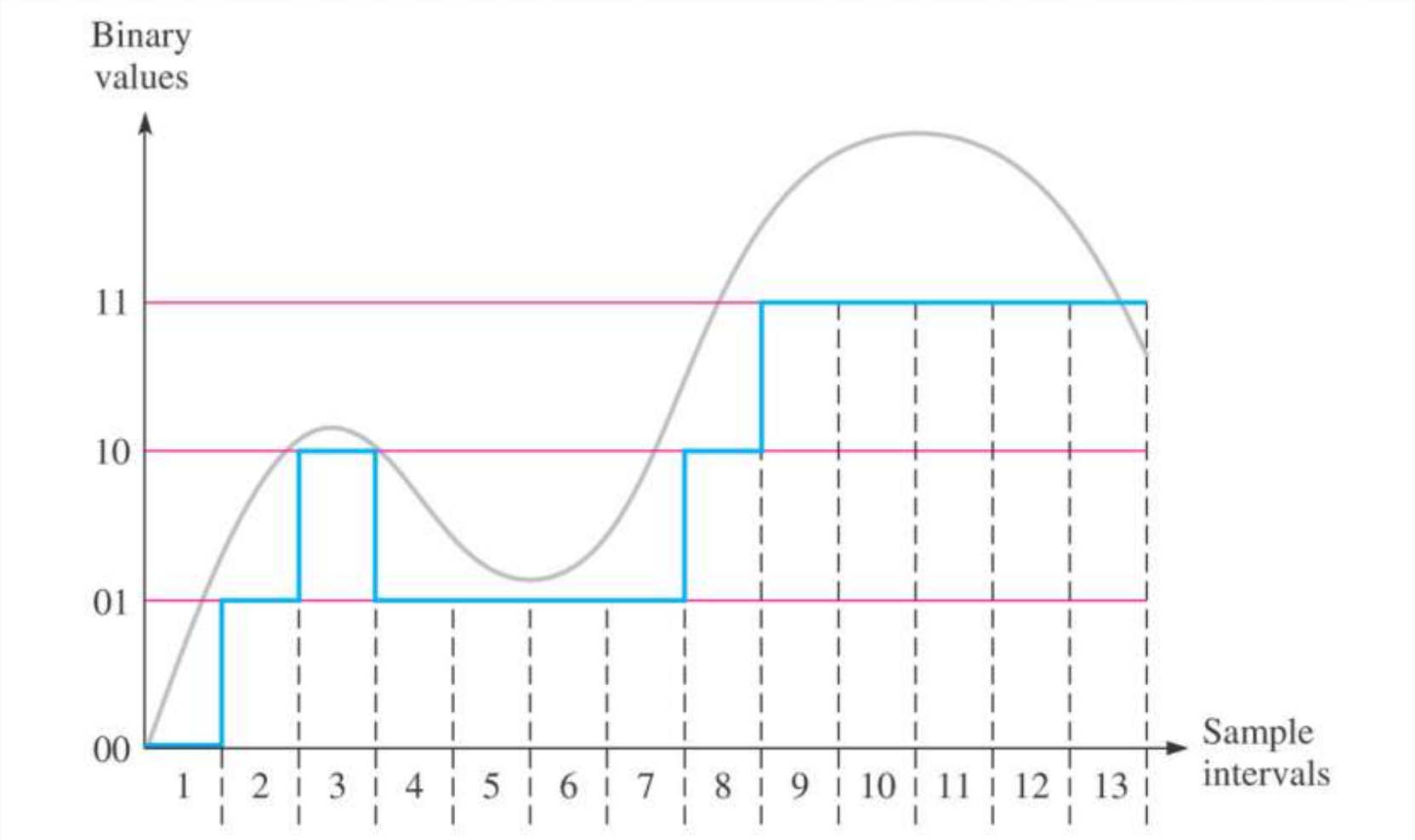
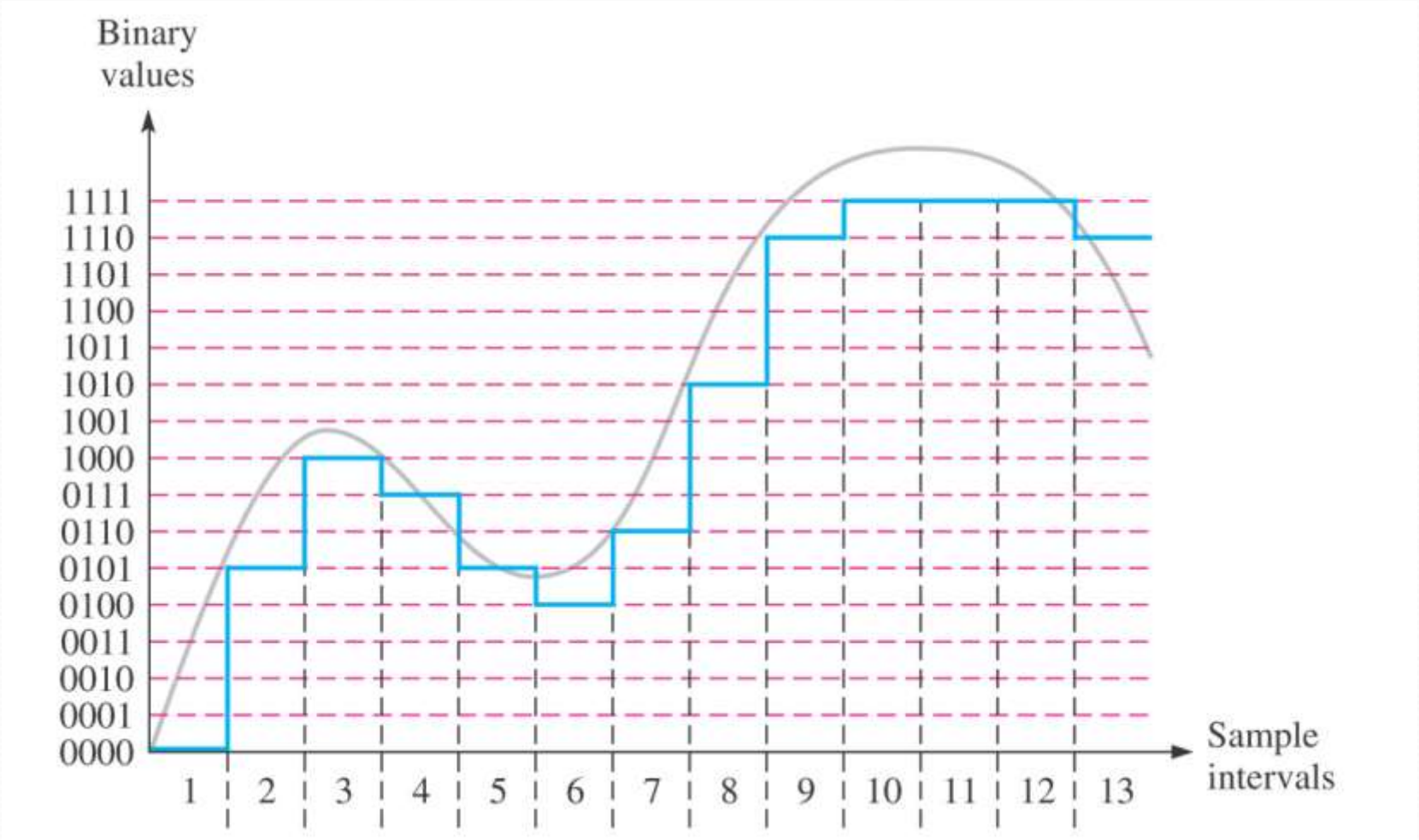


Figure 11–11 The reconstructed waveform in Figure 11–10 using sixteen quantization levels (4 bits). The original analog waveform is shown in light gray for reference.



As a summary for the procedure of A/D conversion

- Sampling
- Holding
- Quantization
- Coding

11.3 Analog-to-digital conversion methods

- Operational amplifier
- A/D conversion methods
- ADC parameters
  - Resolution – the number of bits
  - Throughput – the sampling rate an ADC can handle in units of samples per second (sps)

Operational Amplifier

- Working as a comparator
- The op-amp is driven into one of its two saturated output states, either HIGH or LOW, depending on which input voltage is greater

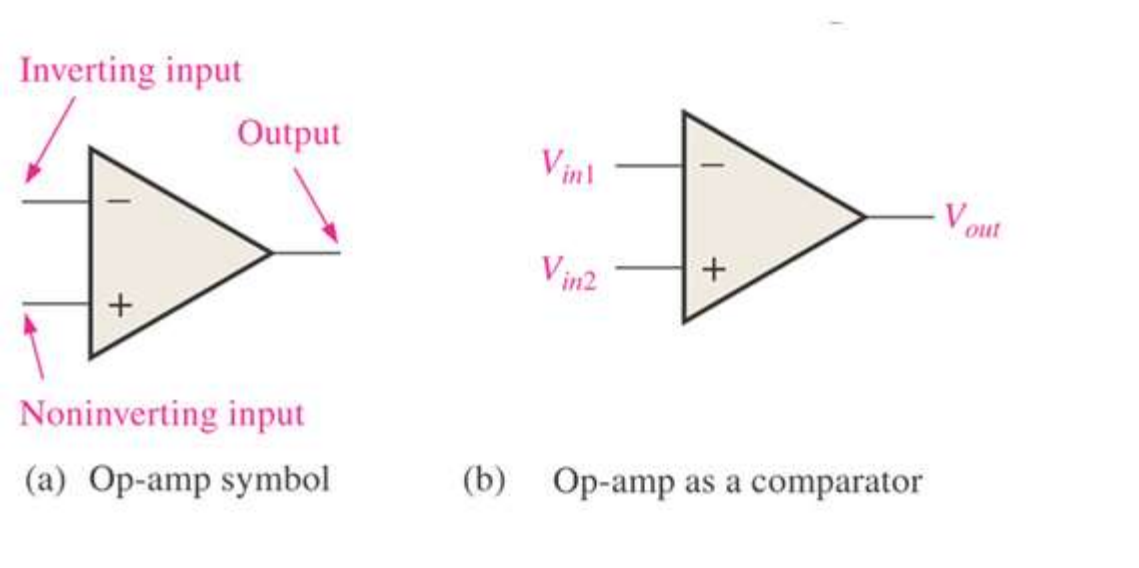


Figure 11–13 The operational amplifier (op-amp).

Operational Amplifier

- Working as an amplifier

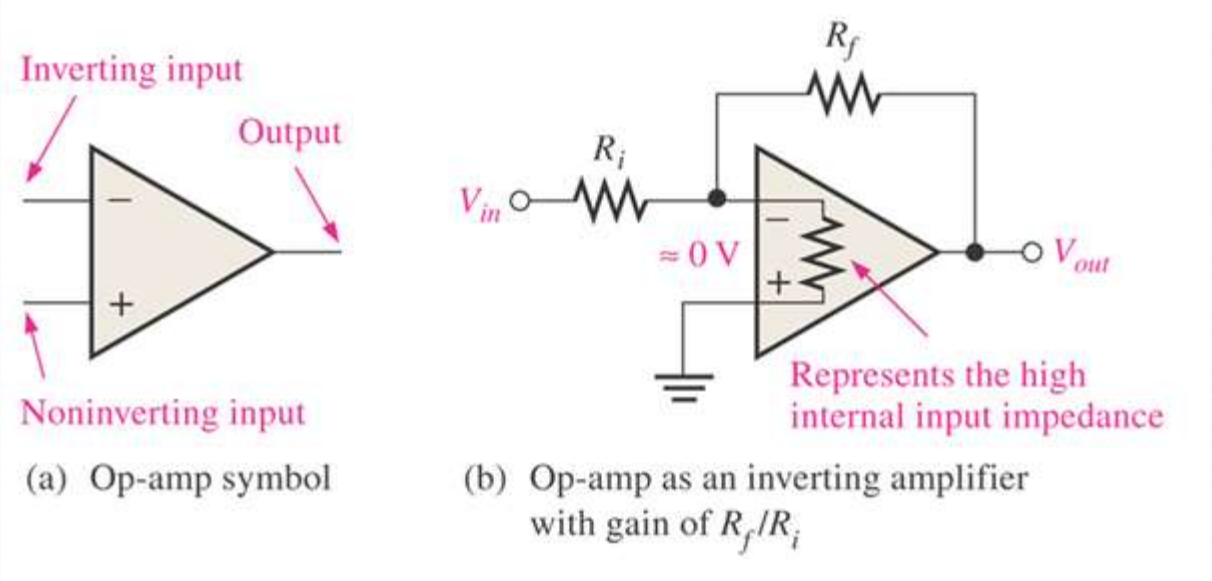
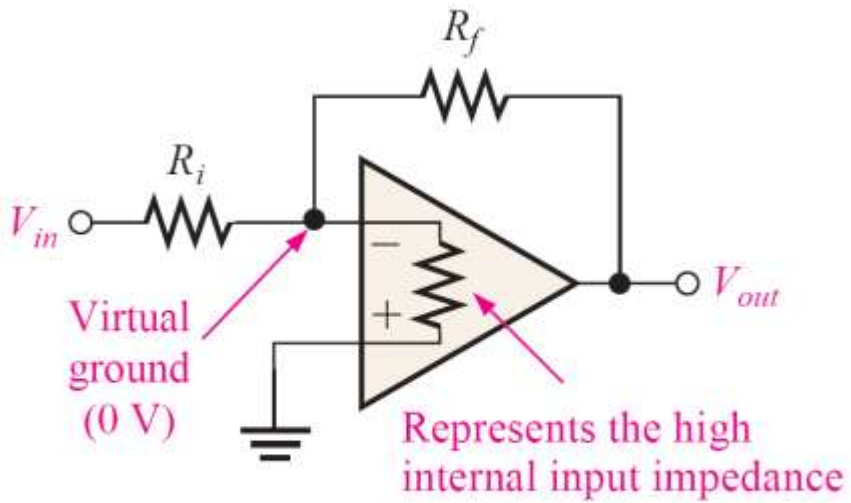


Figure 11–13 The operational amplifier (op-amp).

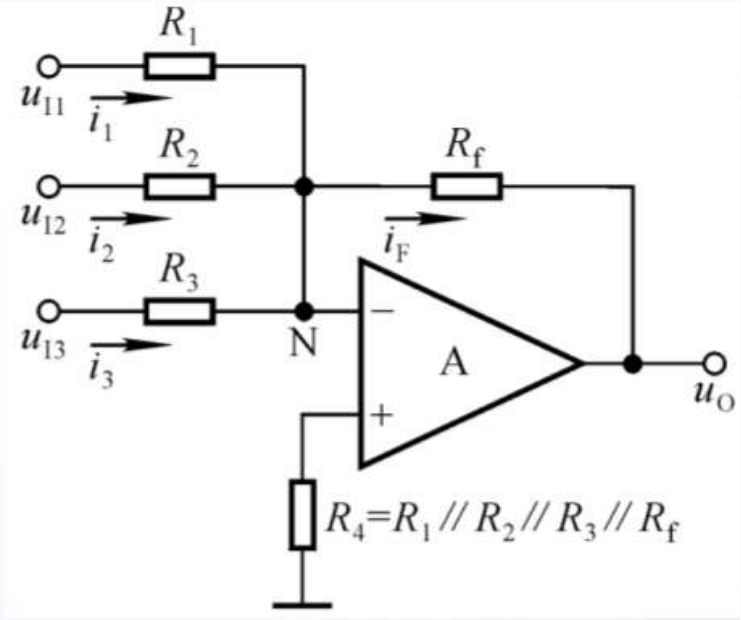
Operational Amplifier



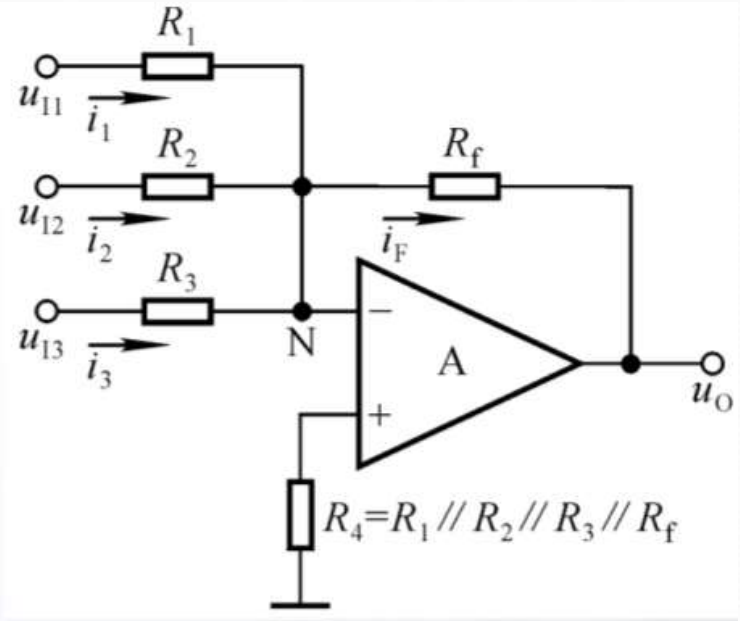
(b) Op-amp as an inverting amplifier with gain of R_f/R_i

$$V_{out} = -\frac{R_f}{R_i} V_{in}$$

Q: What is the output u_o



Q: What is the output u_o



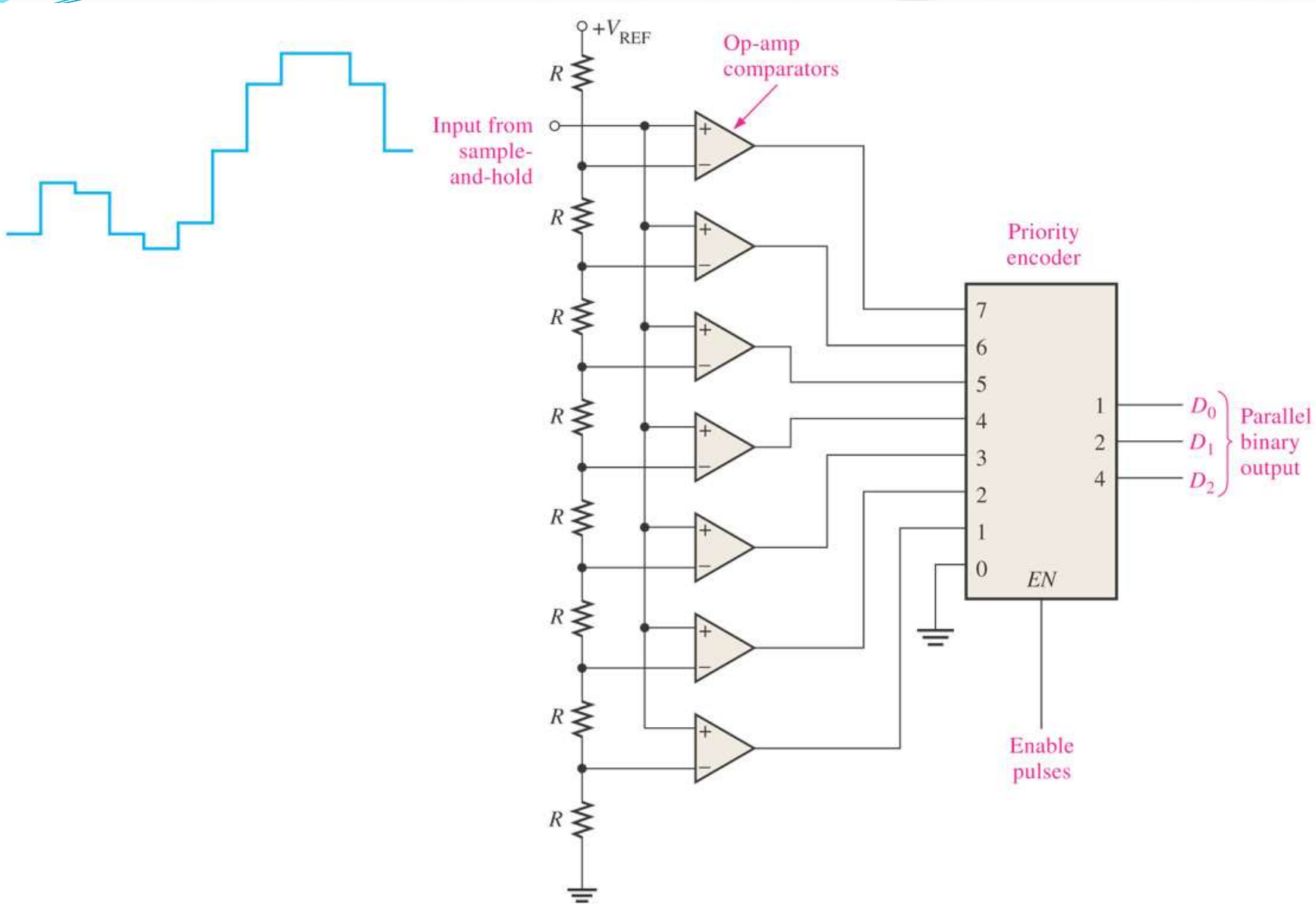
$$u_N = u_P = 0$$

$$i_F = i_{R1} + i_{R2} + i_{R3}$$

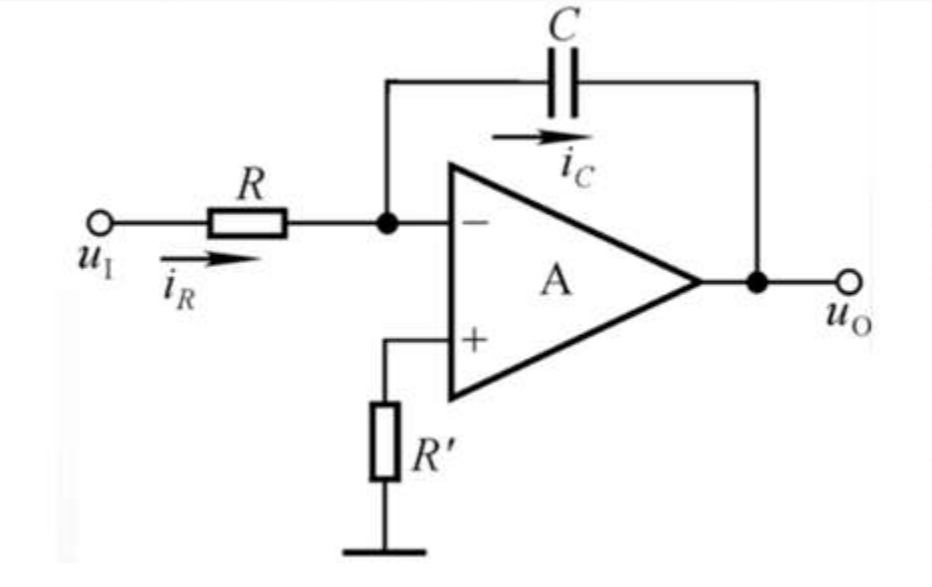
$$= \frac{u_{I1}}{R_1} + \frac{u_{I2}}{R_2} + \frac{u_{I3}}{R_3}$$

$$u_O = -i_F R_f = -R_f\left(\frac{u_{I1}}{R_1} + \frac{u_{I2}}{R_2} + \frac{u_{I3}}{R_3}\right)$$

Figure 11–14 A 3-bit flash ADC.



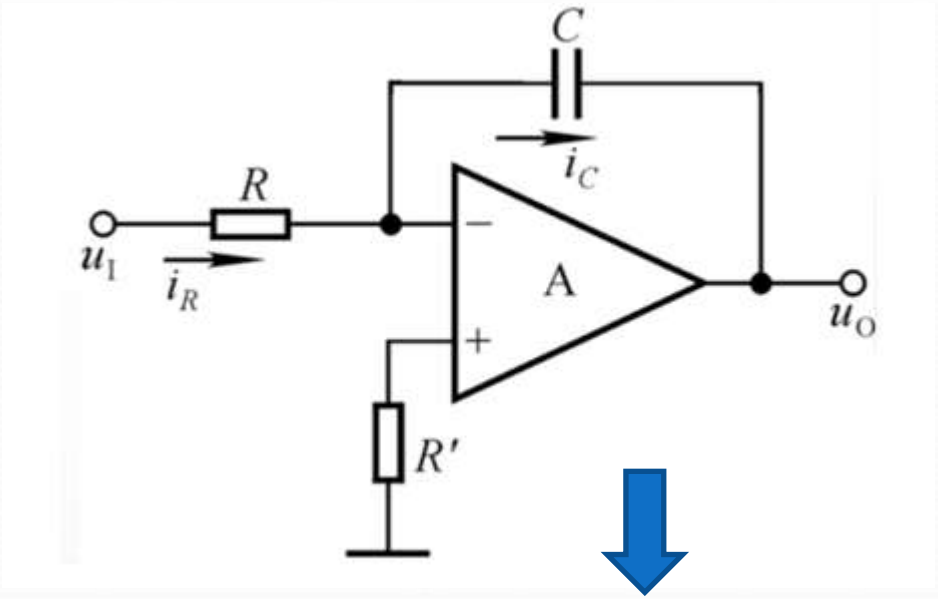
Operational amplifier integrator



$$i_C = i_R = \frac{u_I}{R}$$

$$u_O = -\frac{1}{RC}\int_{t_1}^{t_2} u_I \mathrm{d}t + u_O(t_1)$$

若u_I在$t_1 \sim t_2$为常量，则 $u_O = -\frac{1}{RC}\cdot u_I(t_2 - t_1) + u_O(t_1)$


C
i_C
R
u_I
i_R
A
u_O
R′

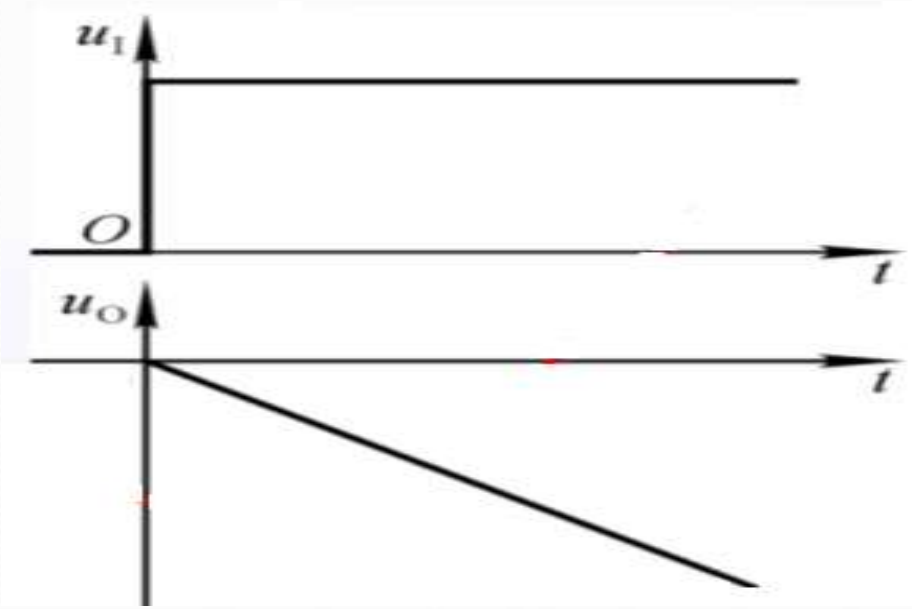
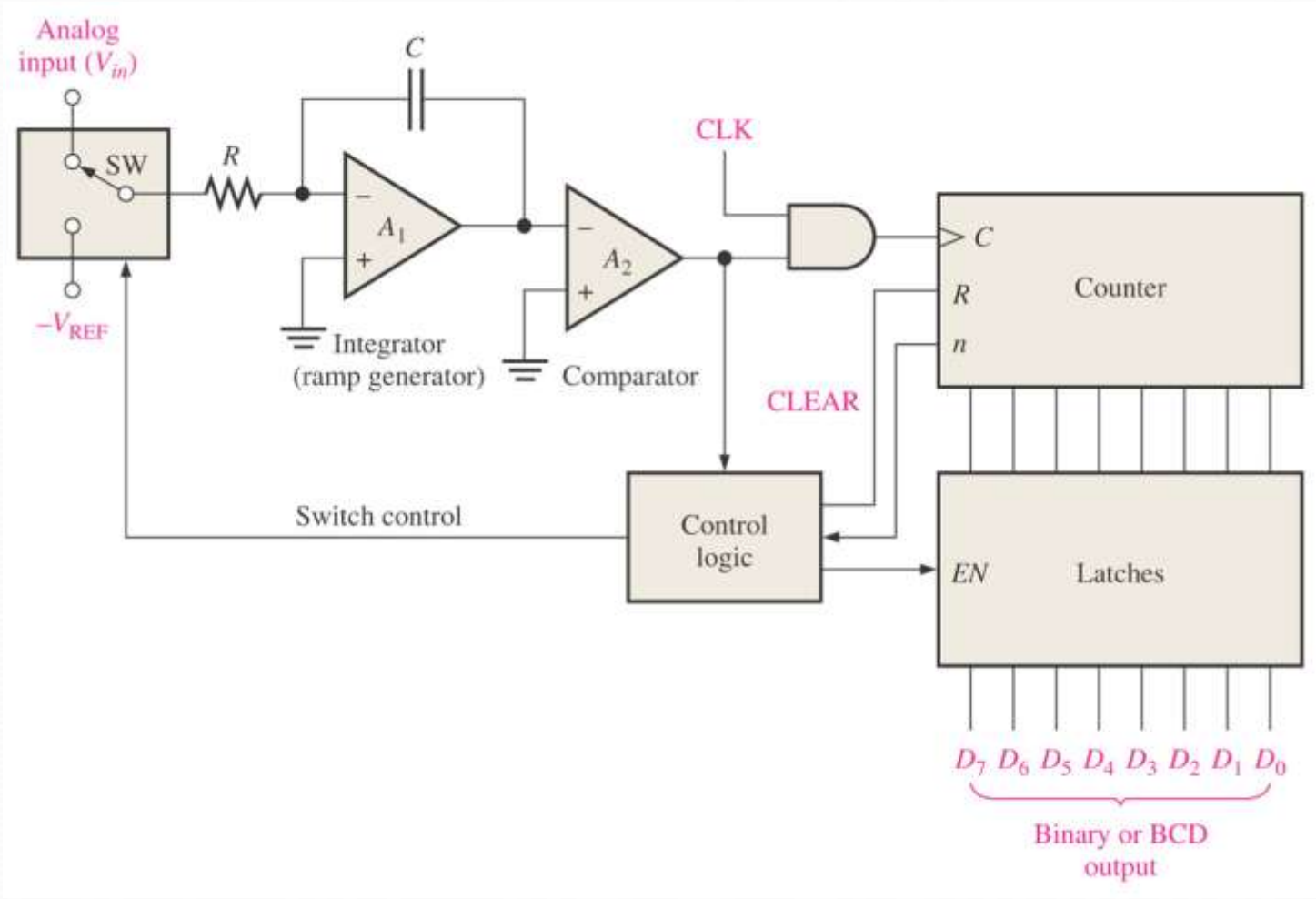
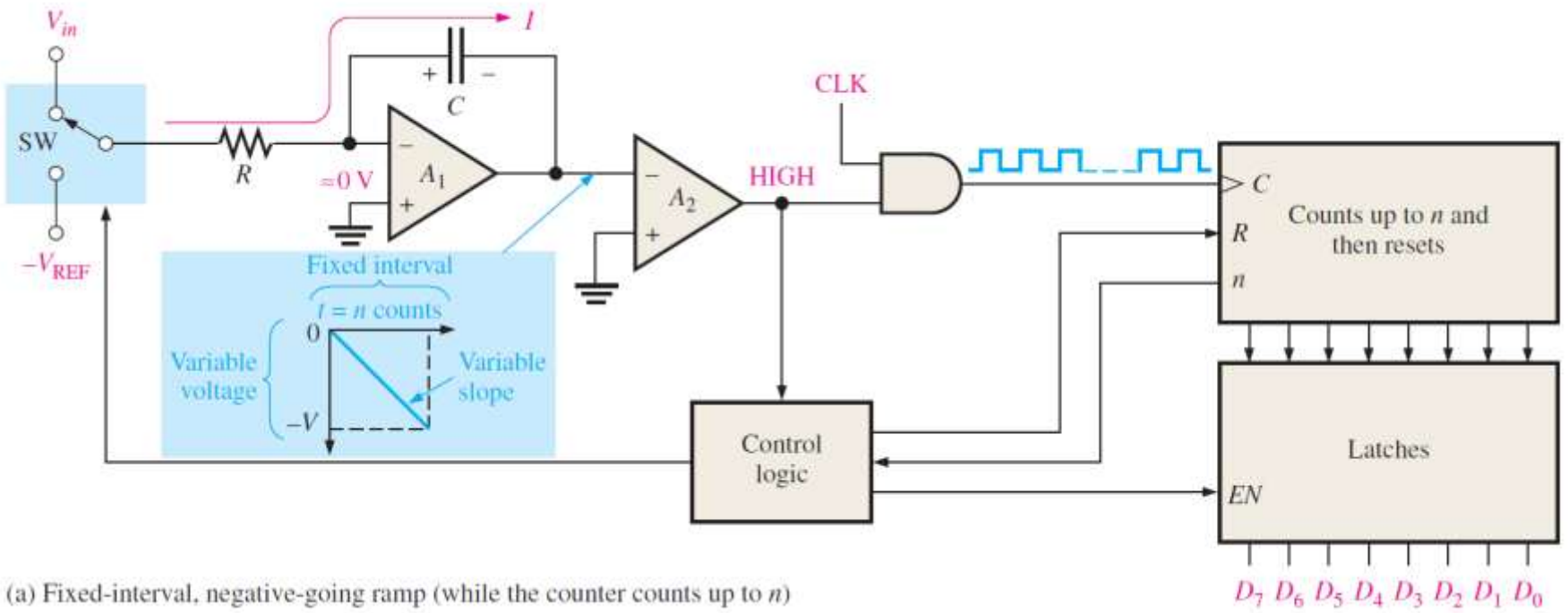
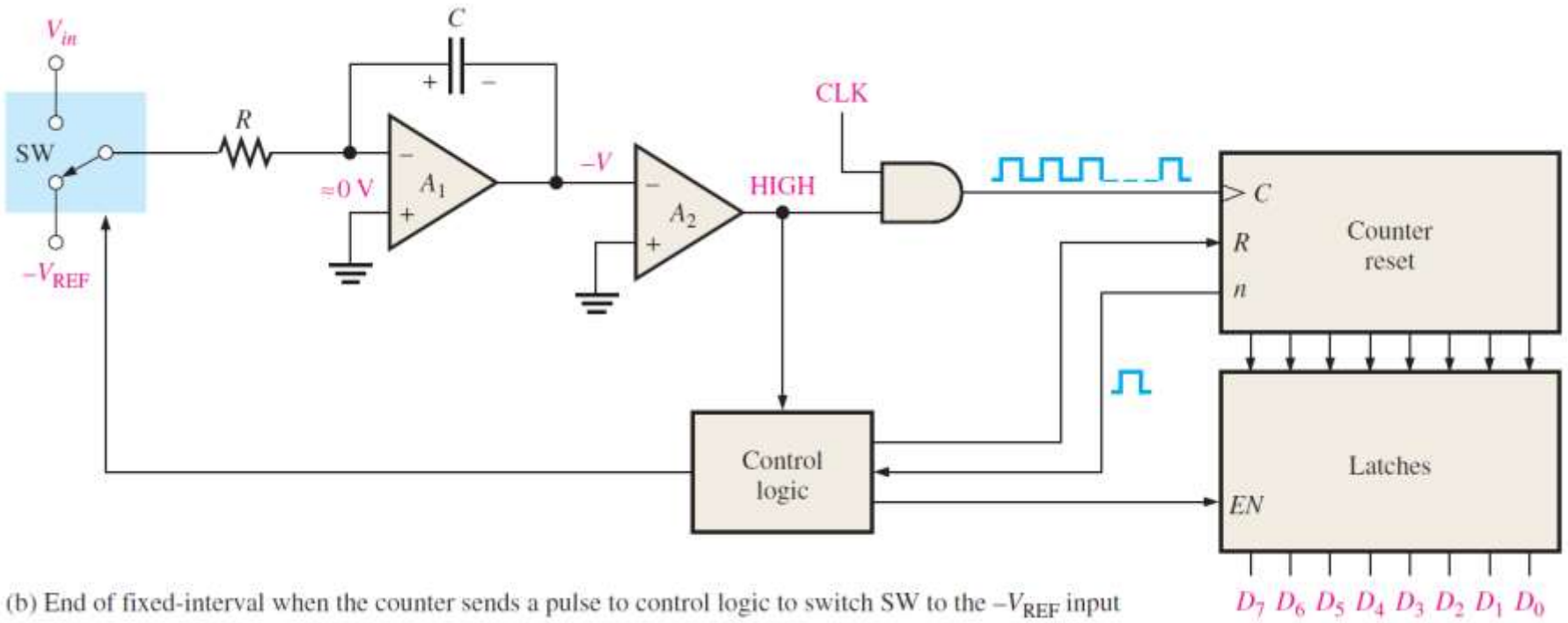

u_I
O
t
u_O
t

Figure 13–17 Basic dual-slope ADC.

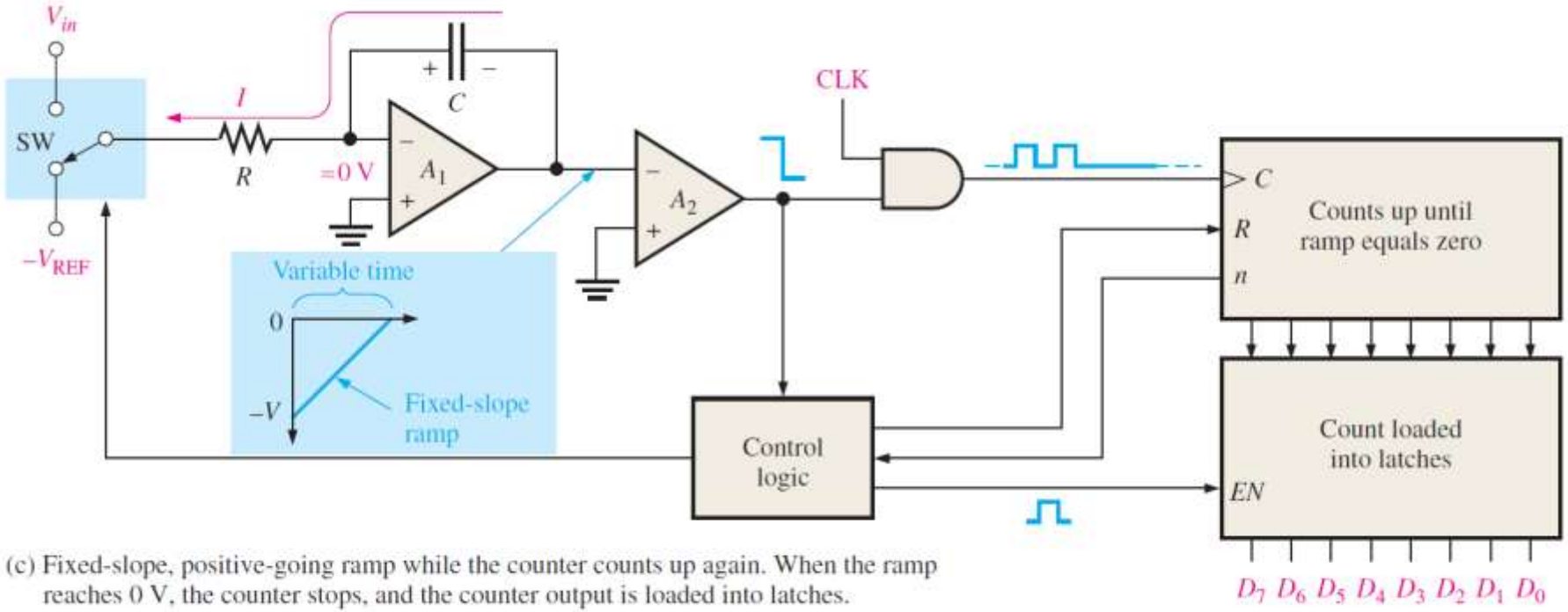




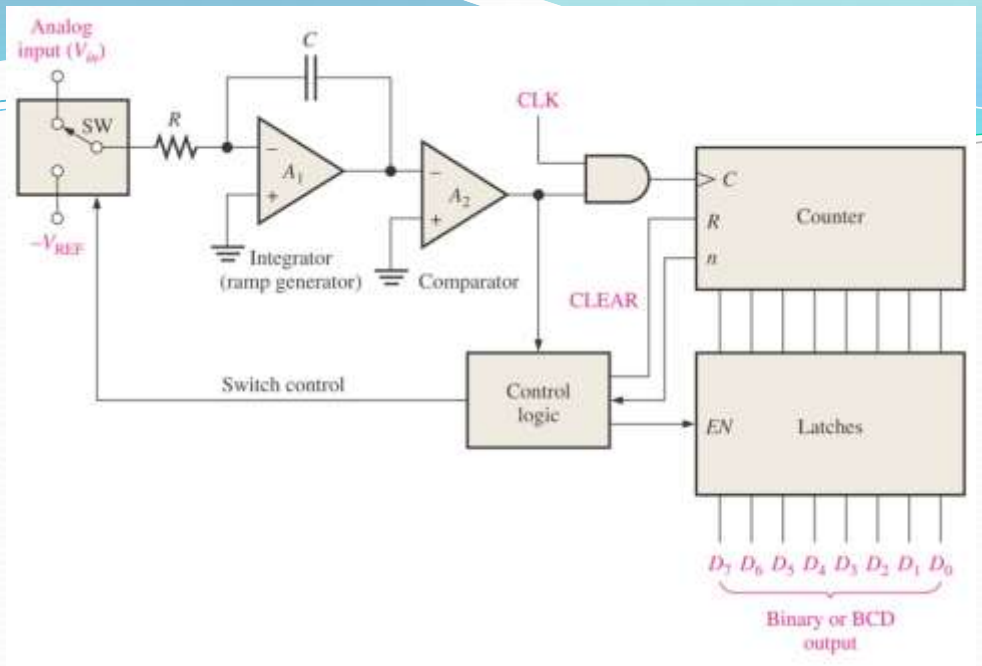
(a) Fixed-interval, negative-going ramp (while the counter counts up to n)

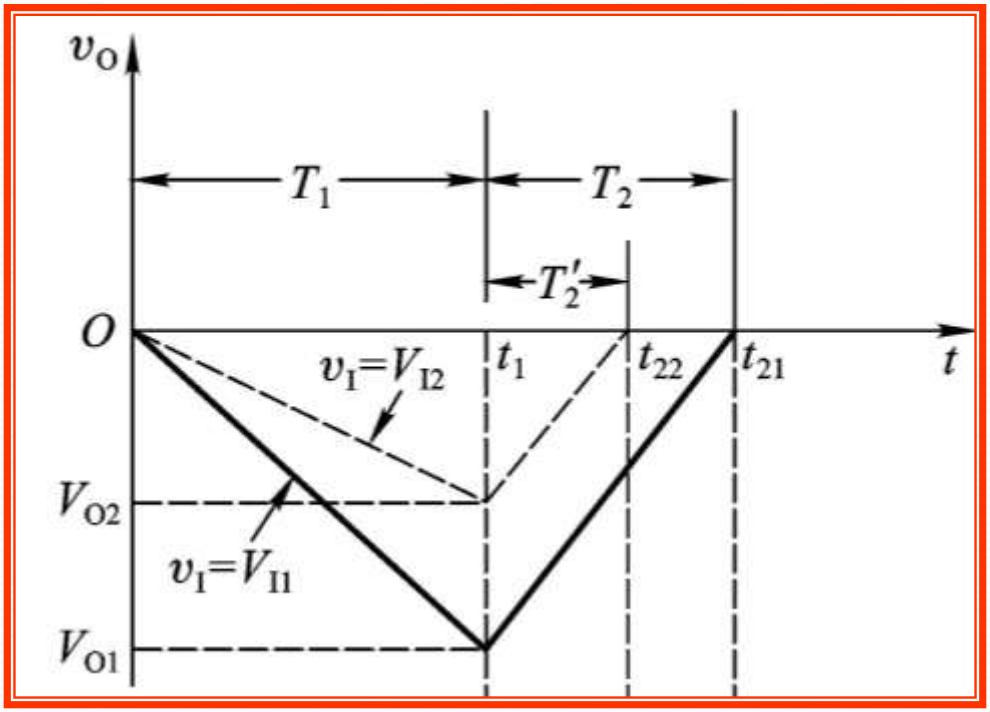


(b) End of fixed-interval when the counter sends a pulse to control logic to switch SW to the $-V_{REF}$ input



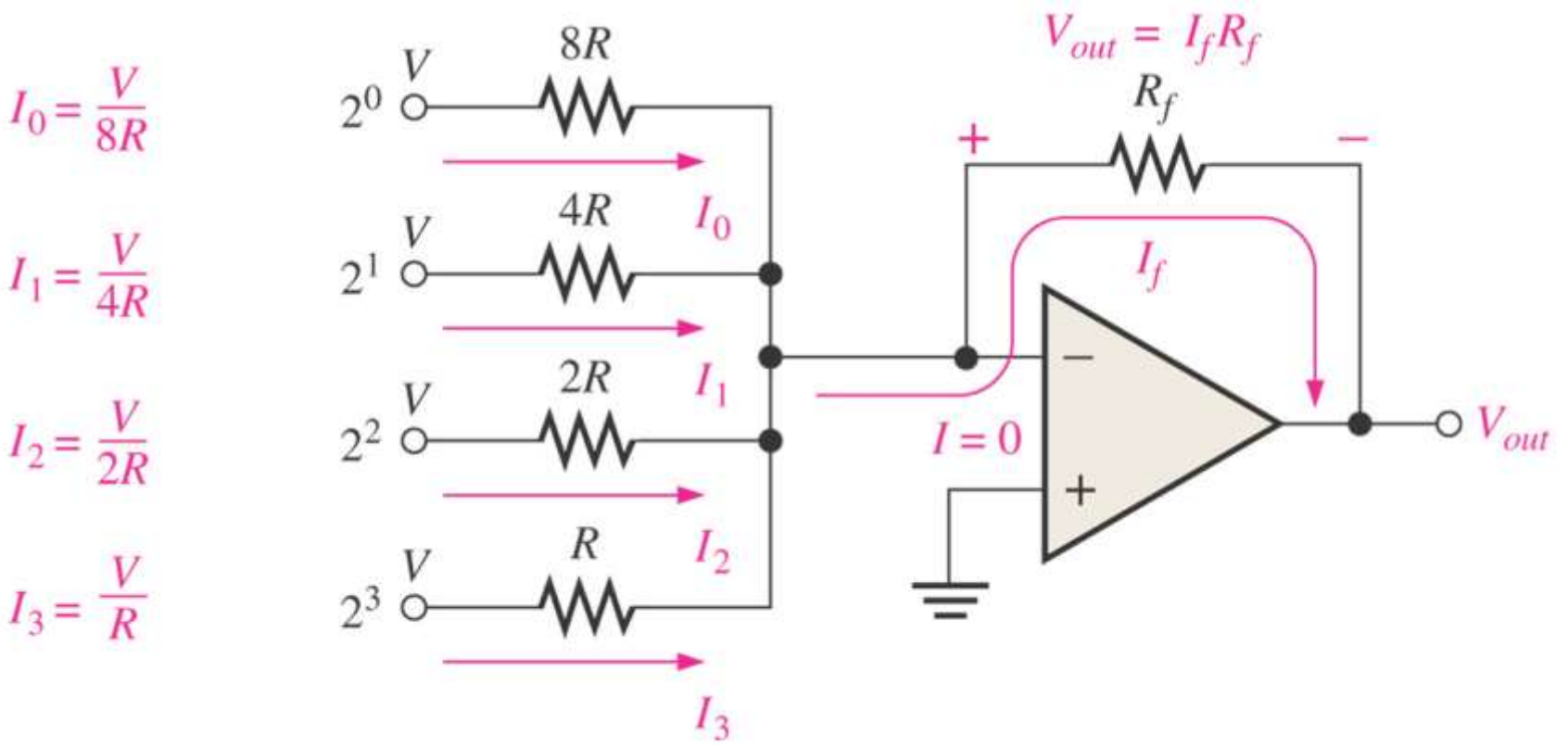
(c) Fixed-slope, positive-going ramp while the counter counts up again. When the ramp reaches 0 V, the counter stops, and the counter output is loaded into latches.


Analog input (V_{in})
SW
$-V_{REF}$
R
C
A_1
A_2
Integrator (ramp generator)
Comparator
CLK
CLEAR
Switch control
Control logic
C
R
n
Counter
EN
Latches
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
Binary or BCD output

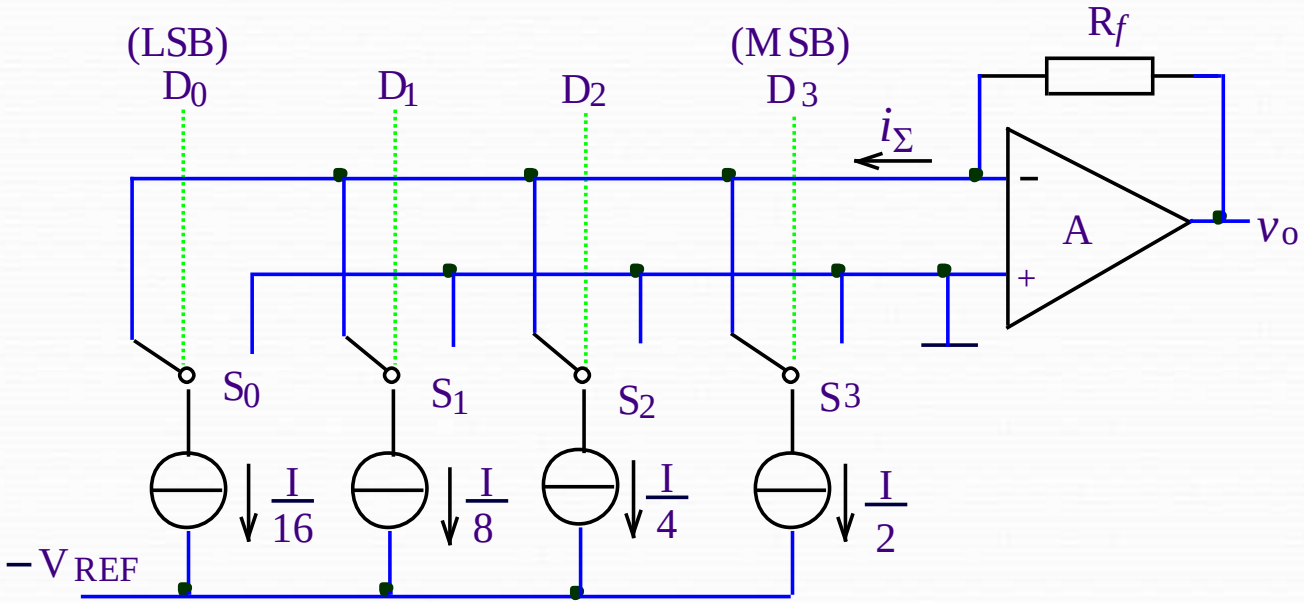

v_O
T_1
T_2
T_2'
O
$v_I = V_{I2}$
t_1
t_{22}
t_{21}
t
V_{O2}
$v_I = V_{I1}$
V_{O1}

11.4 Digital-to-analog conversion methods

Figure 11–36 A 4-bit DAC with binary-weighted inputs.



Some other DACs

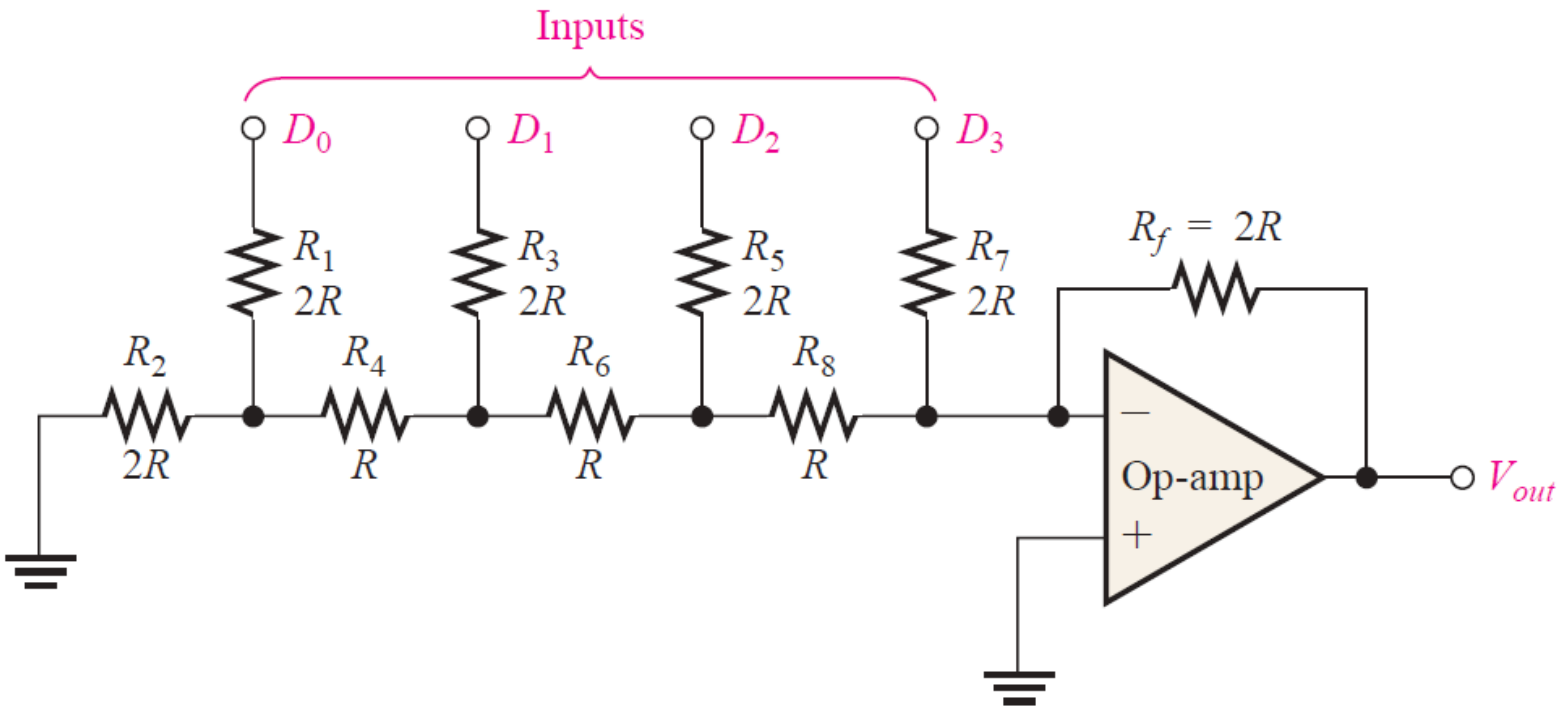


$$v_O = i_\Sigma R_f = R_f\left(\frac{I}{2}D_3 + \frac{I}{4}D_2 + \frac{I}{8}D_1 + \frac{I}{16}D_0\right)$$

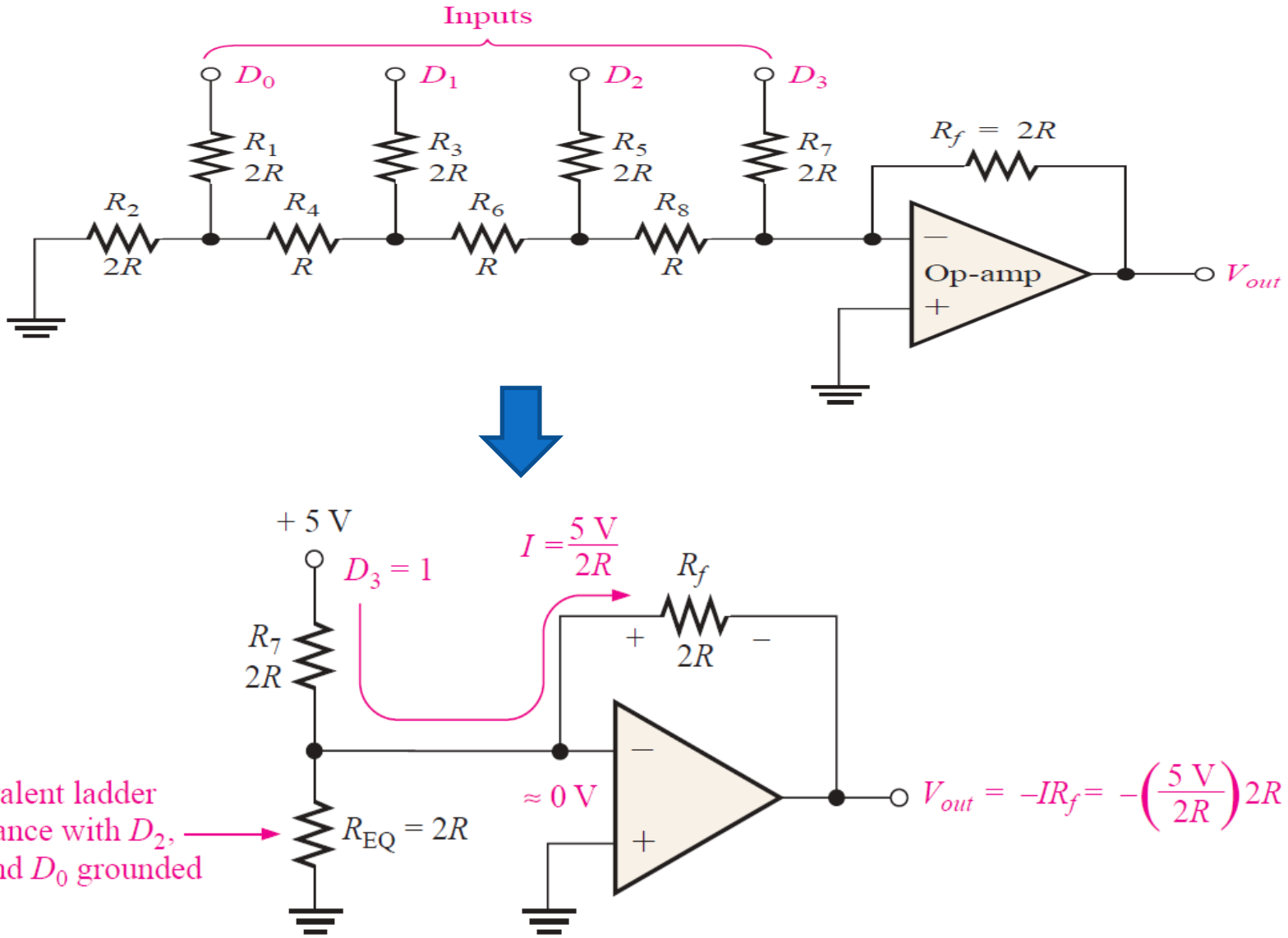
$$= \frac{I}{2^4}\cdot R_f\left(D_3\cdot 2^3 + D_2\cdot 2^2 + D_1\cdot 2^1 + D_0\cdot 2^0\right)$$

$$= \frac{I}{2^4}\cdot R_f\sum_{i=0}^{3} D_i\cdot 2^i$$

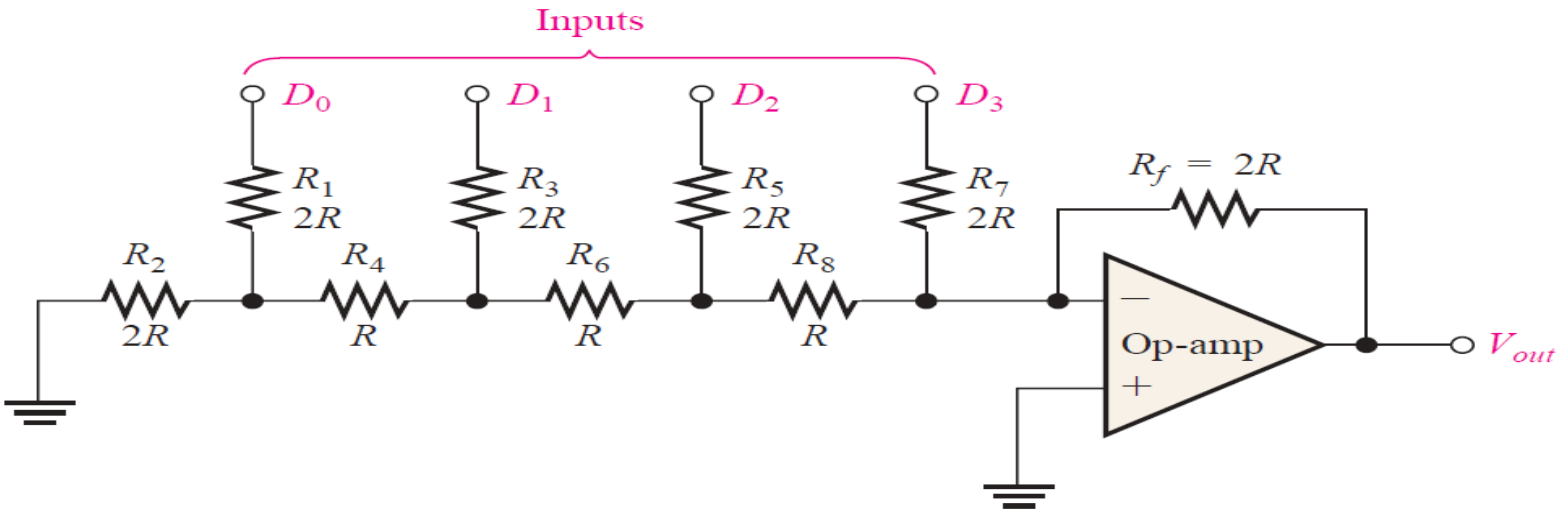
Some other DACs

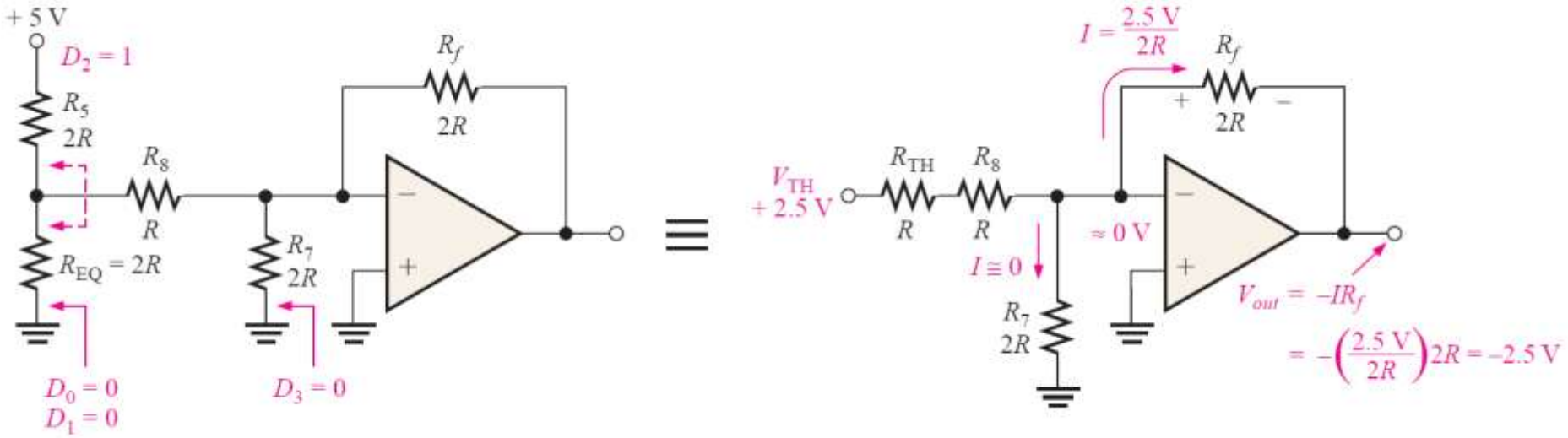


An *R*/2*R* ladder DAC



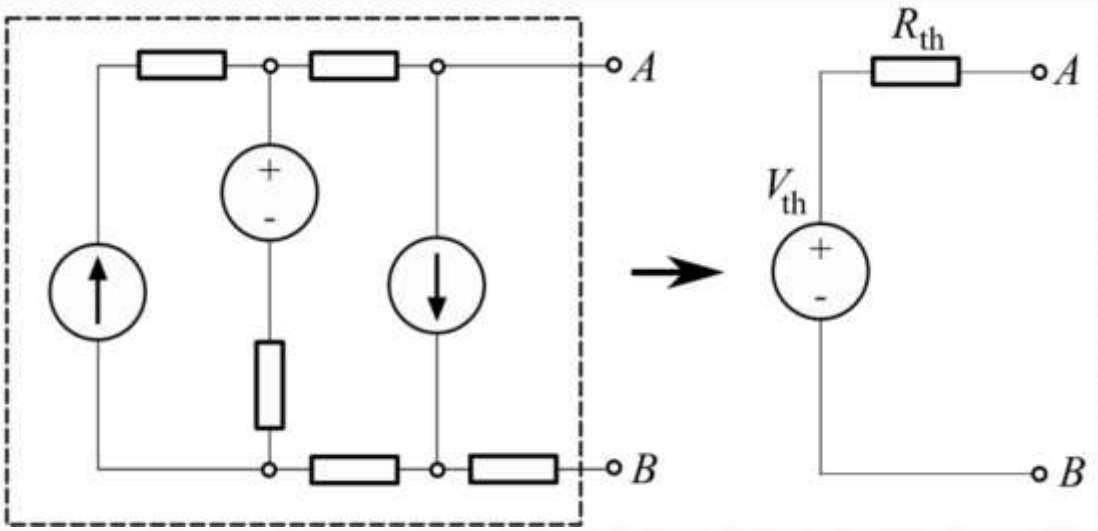
(a) Equivalent circuit for $D_3 = 1$, $D_2 = 0$, $D_1 = 0$, $D_0 = 0$



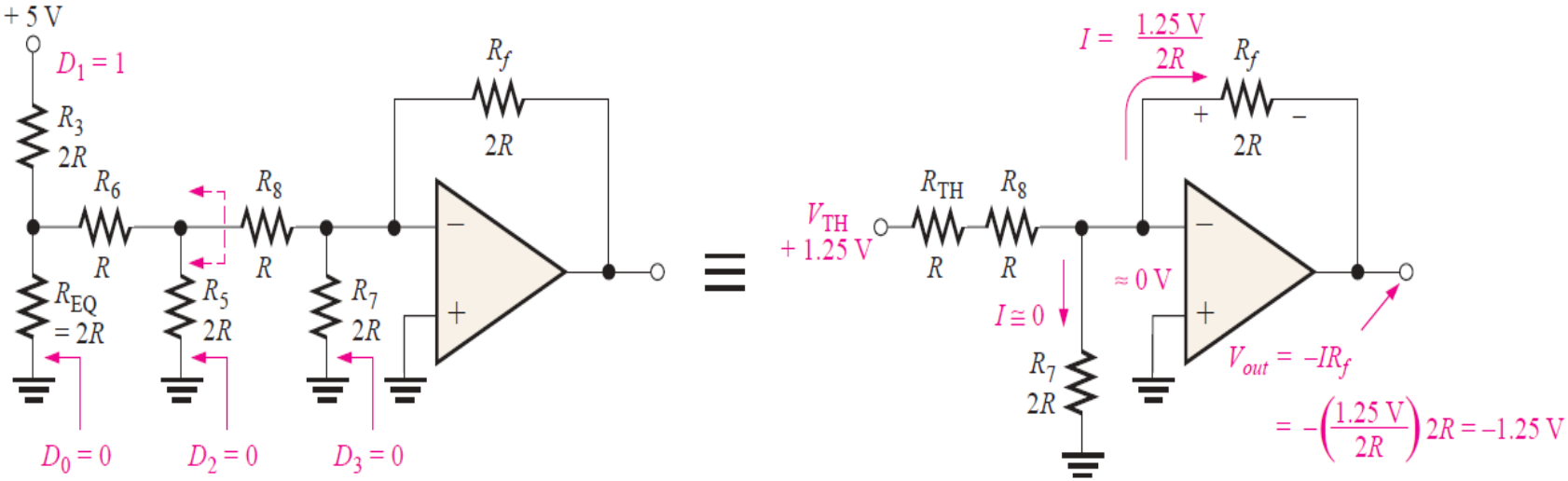


(b) Equivalent circuit for $D_3 = 0, D_2 = 1, D_1 = 0, D_0 = 0$

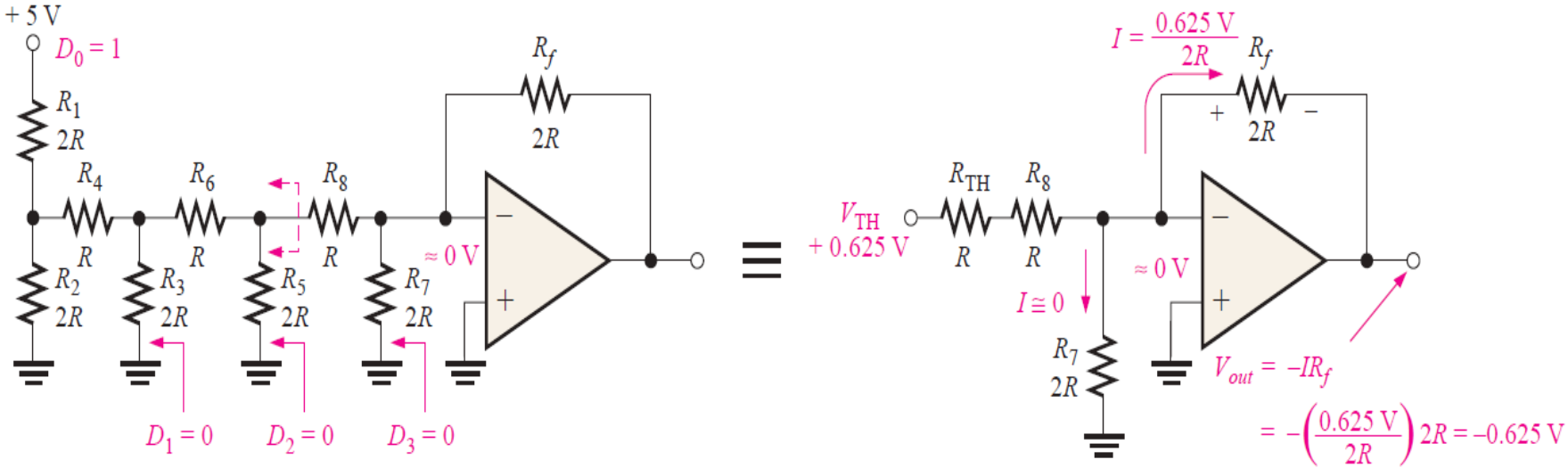
Thevenin's Theorem



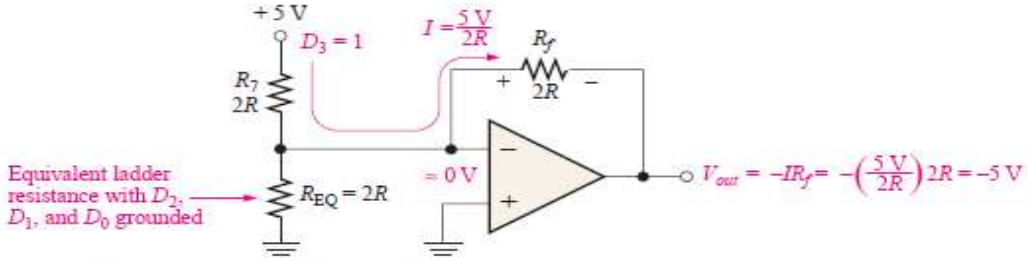
- The equivalent voltage Vth is the voltage obtained at terminals A-B of the network with terminals A-B open circuited.
- The equivalent resistance Rth is the resistance that the circuit between terminals A and B would have if all ideal voltage sources in the circuit were replaced by a short circuit and all ideal current sources were replaced by an open circuit.



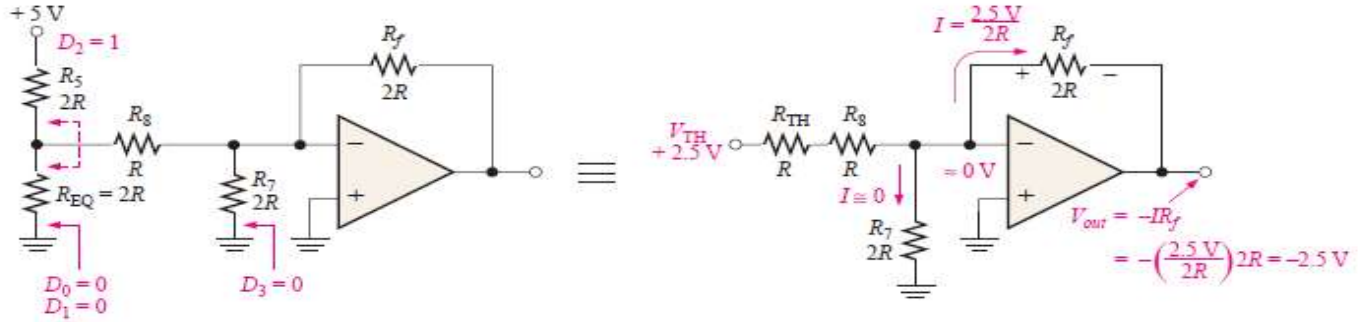
(c) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 1, D_0 = 0$



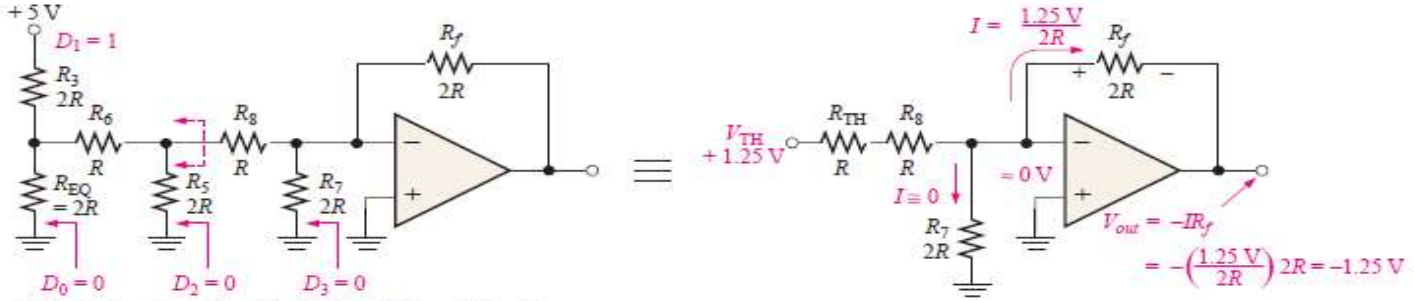
(d) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 0, D_0 = 1$



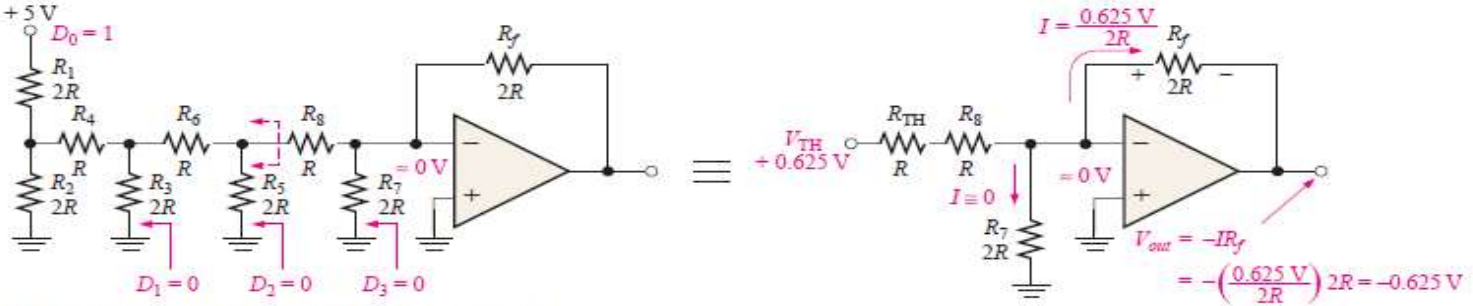
(a) Equivalent circuit for $D_3 = 1, D_2 = 0, D_1 = 0, D_0 = 0$



(b) Equivalent circuit for $D_3 = 0, D_2 = 1, D_1 = 0, D_0 = 0$



(c) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 1, D_0 = 0$



(d) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 0, D_0 = 1$

Summary

- Digital Signal Processing Basics
- Sampling and reconstruction
- AD and ADC
  - Sampling, holding, quantization, coding
- DA and DAC