Chapter 8 Counters

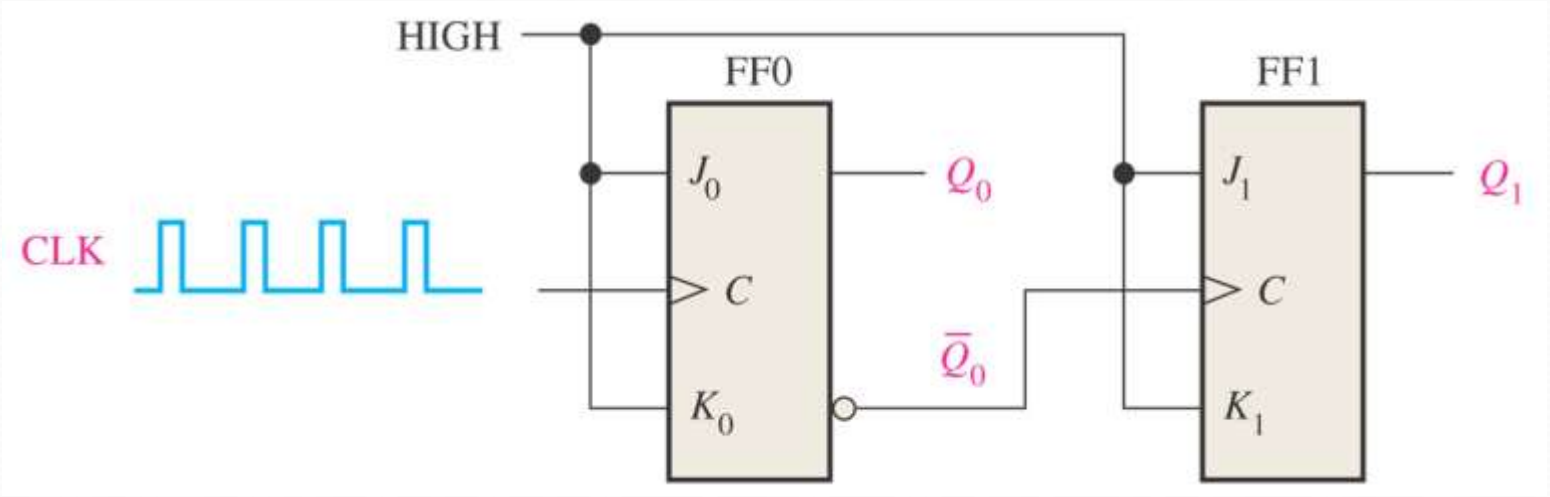
Outline

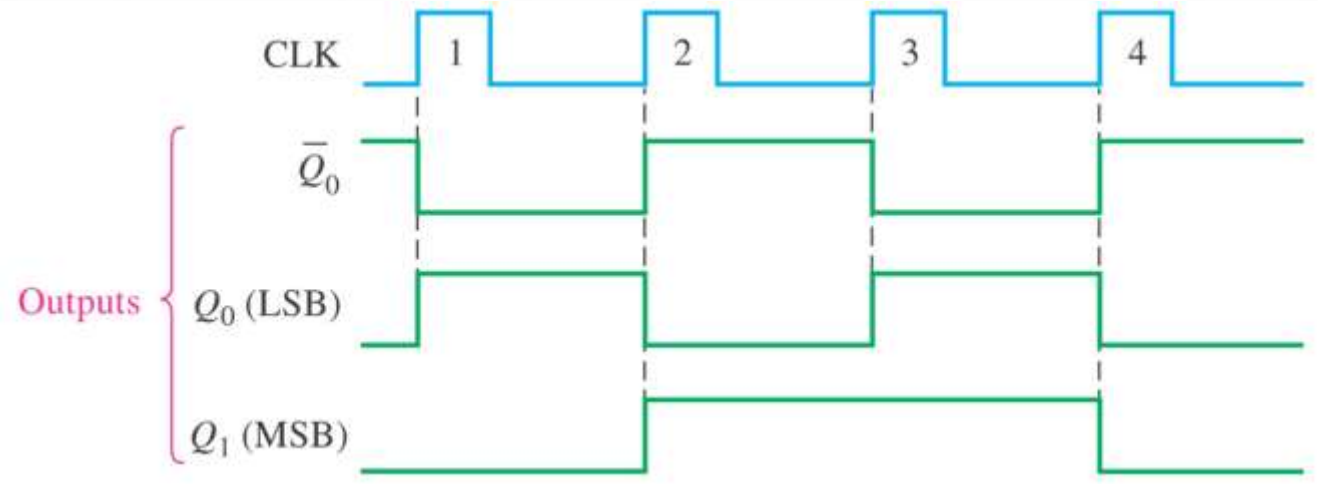
- Asynchronous Counter Operation
- Synchronous Counter Operation
- Up/Down Synchronous Counters
- Design of Synchronous Counters
- Cascaded Counters
- Counter Decoding
- Counter Applications

8.1 Asynchronous Counter Operation

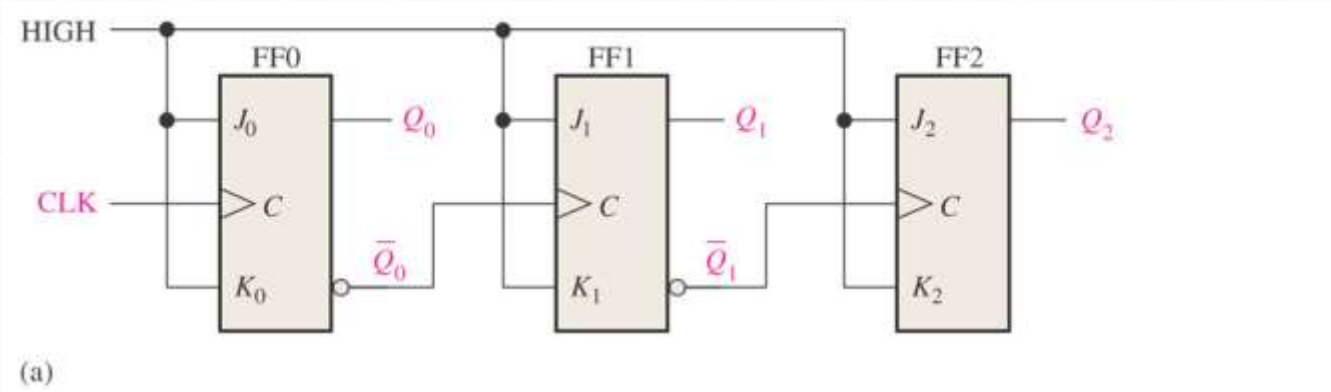
- Asynchronous
  - Events do not have a fixed time relationship with each other
  - Events do not occur at the same time
- An asynchronous counter
  - The Flip-flops within the counter do not change states at exactly the same time
  - The Flip-flops within the counter do not have a common clock pulse

A 2-bit Asynchronous Binary Counter

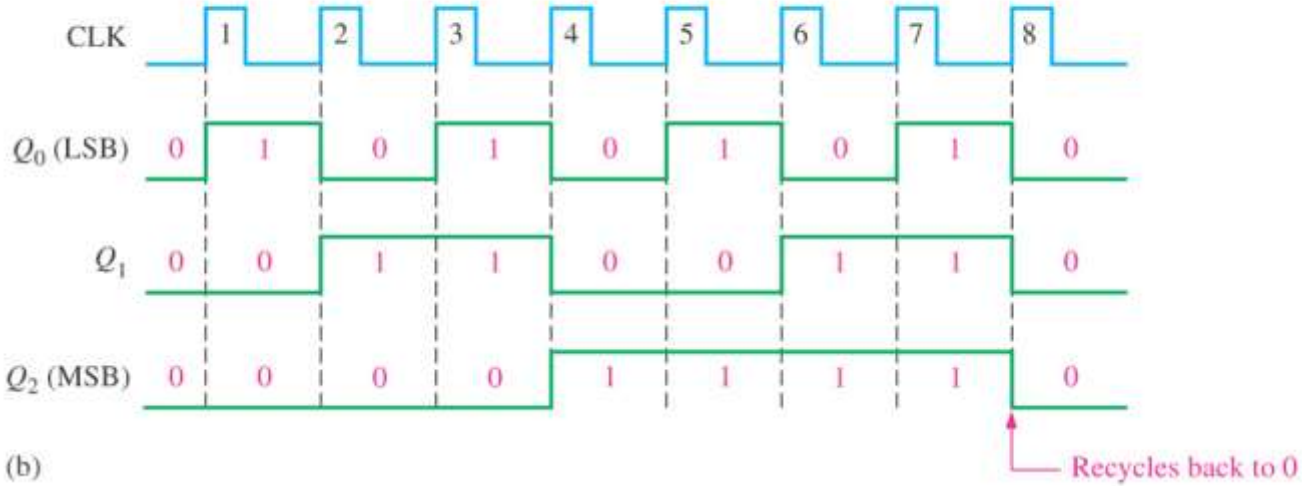




A 3-bit Asynchronous Binary Counter



(a)



(b)

Propagation Delay

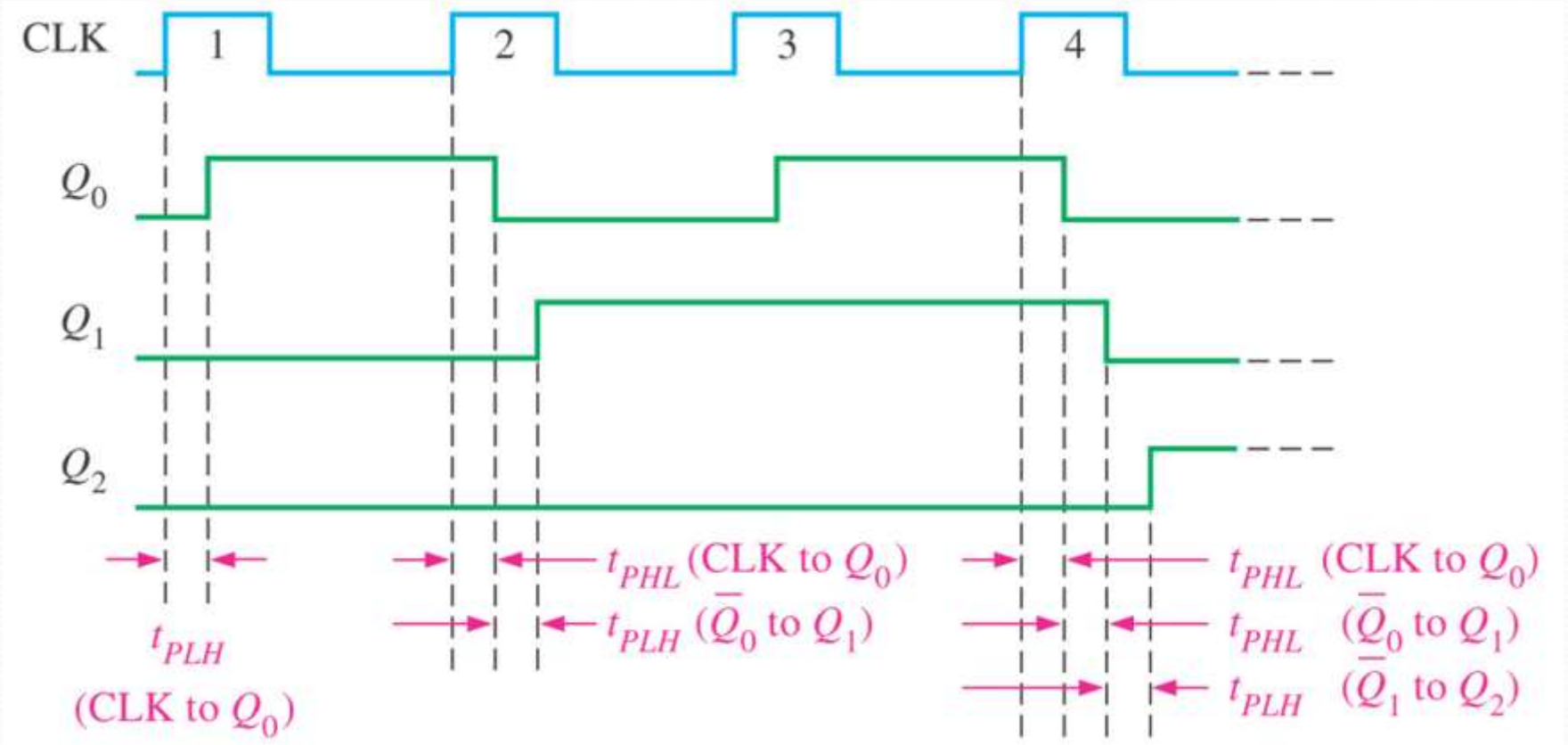


Figure 8–4 Propagation delays in a 3-bit asynchronous (ripple-clocked) binary counter.

Asynchronous Decade Counters

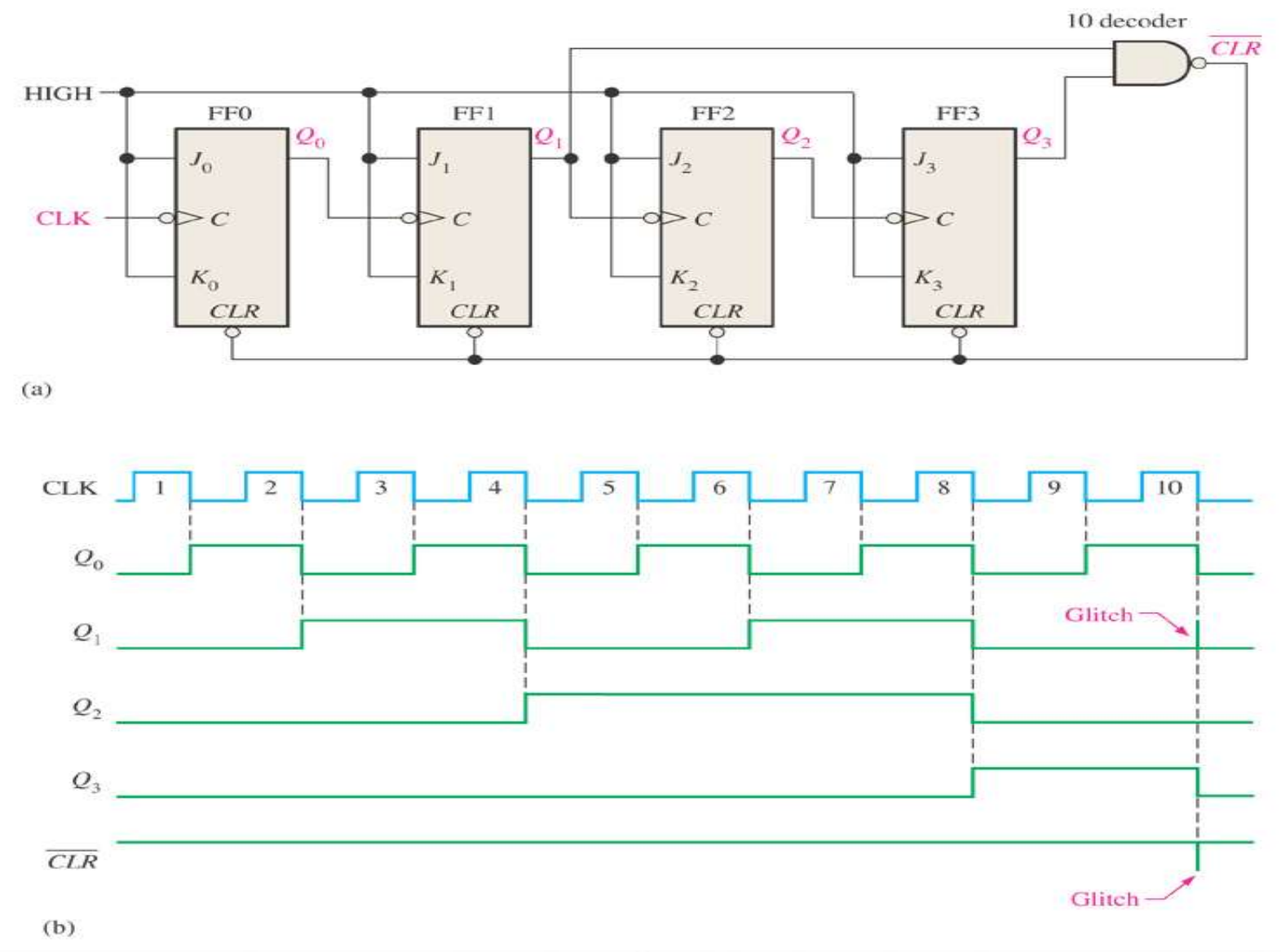
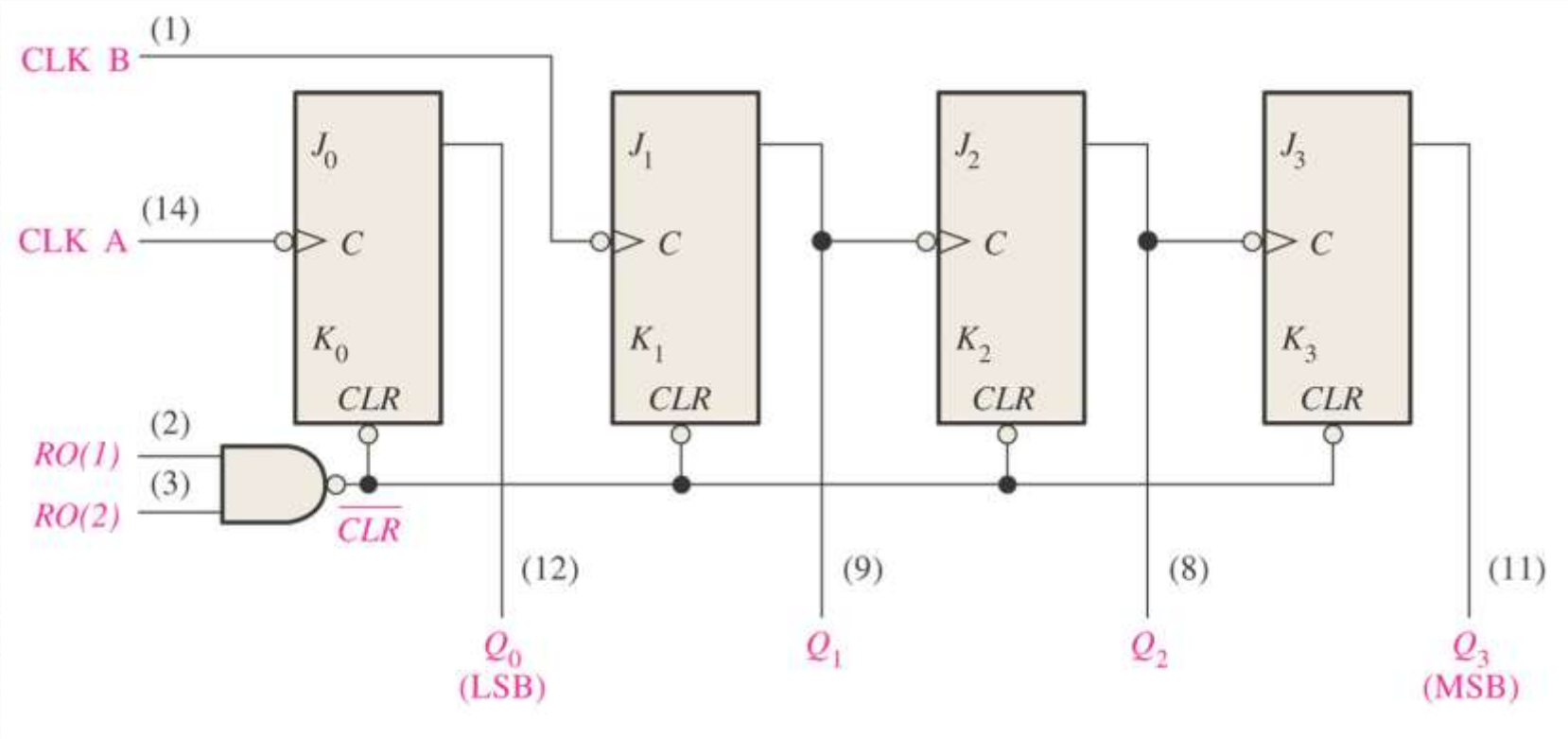


Figure 8–6 An asynchronously clocked decade counter with asynchronous recycling.

74LS93


CLK B
(1)
CLK A
(14)
J_0
C
K_0
CLR
J_1
C
K_1
CLR
J_2
C
K_2
CLR
J_3
C
K_3
CLR
(2)
RO(1)
(3)
RO(2)
$\overline{CLR}$
(12)
Q_0
(LSB)
(9)
Q_1
(8)
Q_2
(11)
Q_3
(MSB)

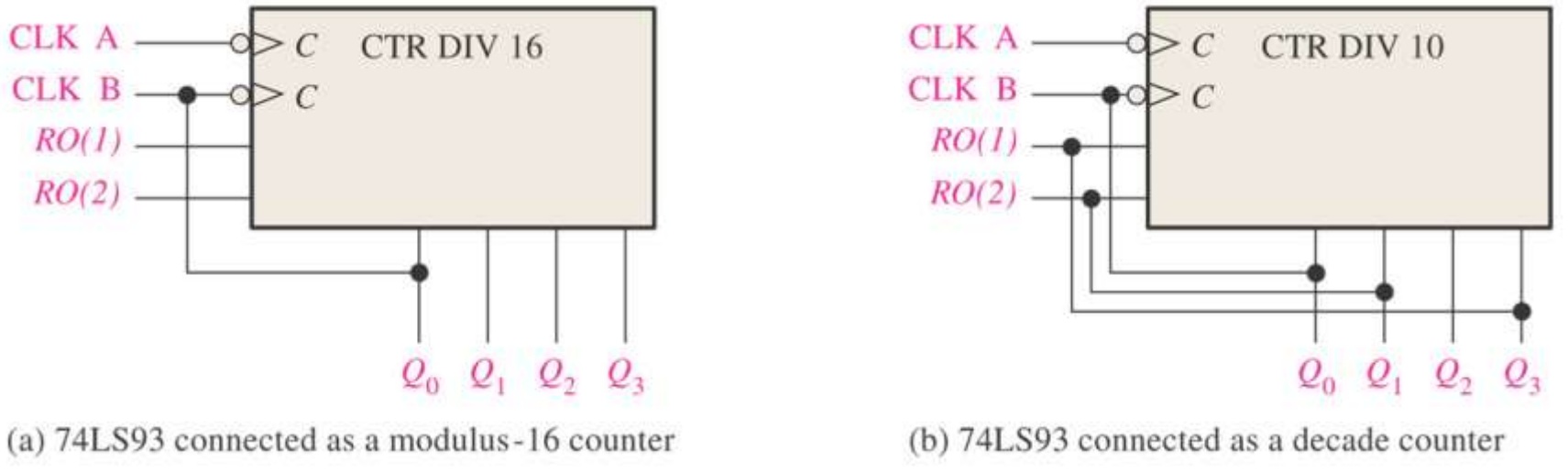


Figure 8–9 Two configurations of the 74LS93 asynchronous counter.

How to use 74LS93 as a modulus-12 counter?

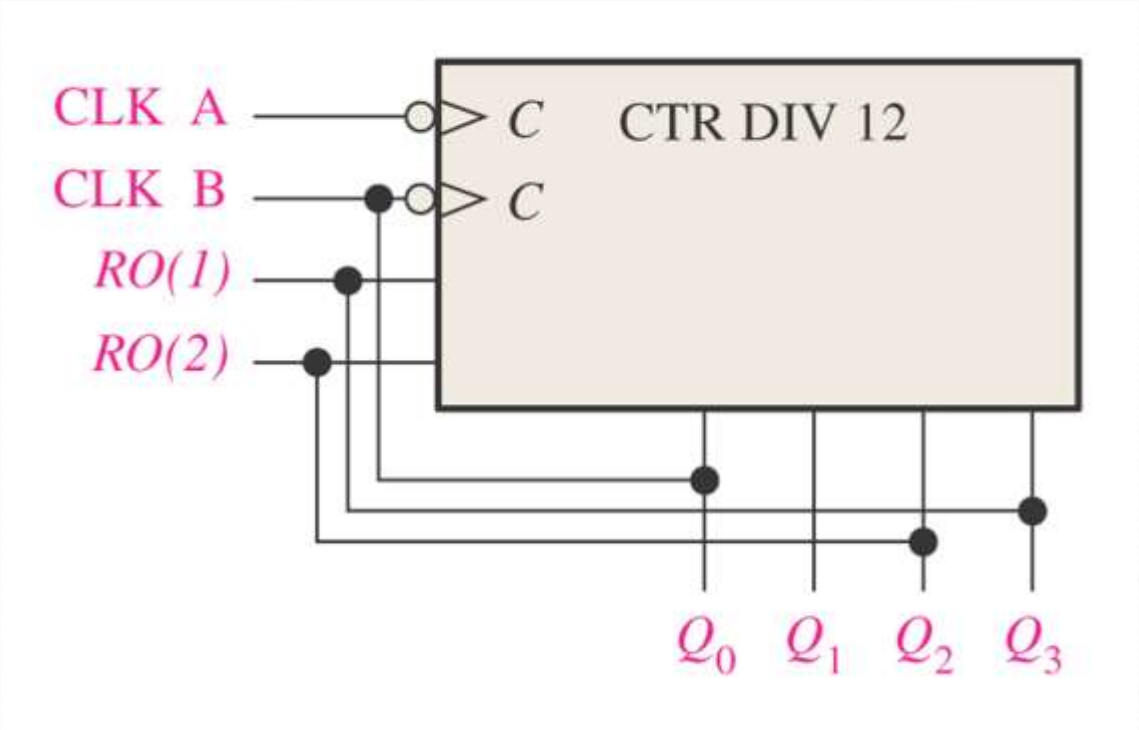


Figure 8–10 74LS93 connected as a modulus-12 counter.

8.2 Synchronous Counter Operation

- Synchronous
  - Events have a fixed time relationship with each other
- A synchronous counter
  - All Flip-flops within the counter are clocked at the same time by a common clock pulse

A 2-bit Synchronous Binary Counter

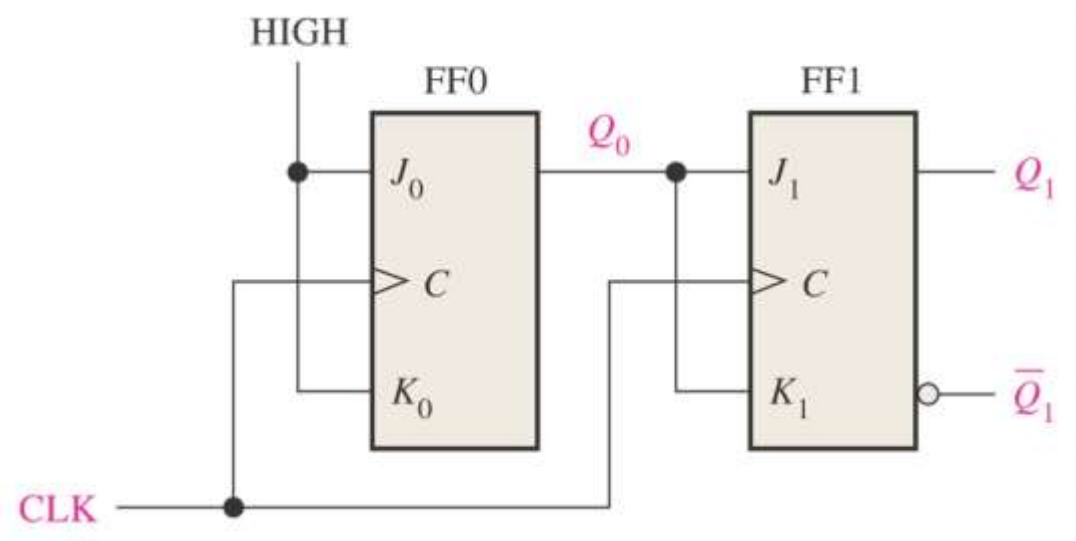
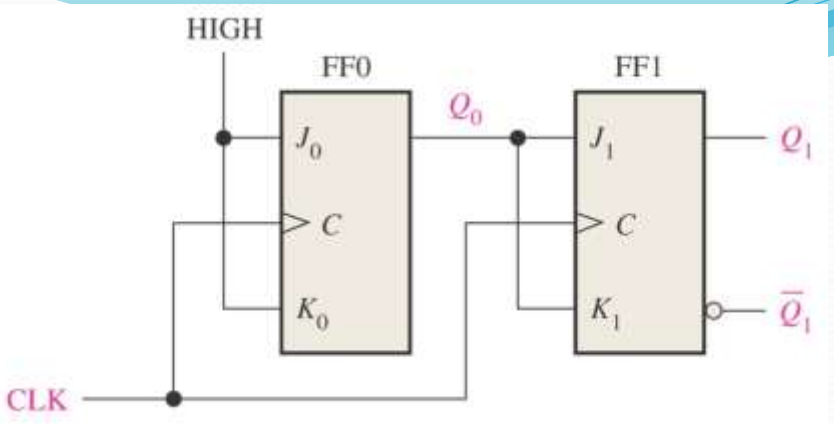


Figure 8–11 A 2-bit synchronous binary counter.

Figure 8–12 Timing details for the 2-bit synchronous counter operation (the propagation delays of both flip-flops are assumed to be equal).



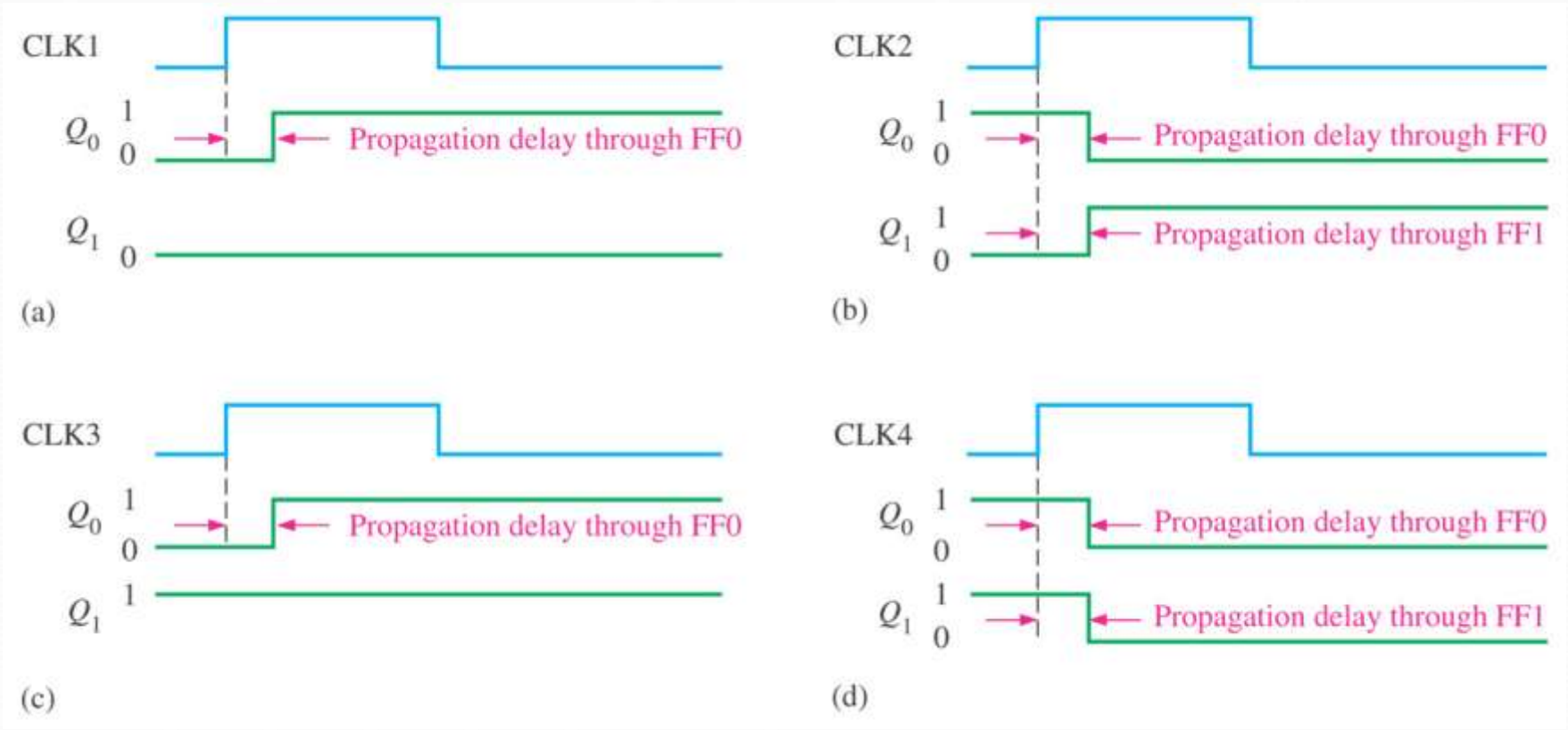
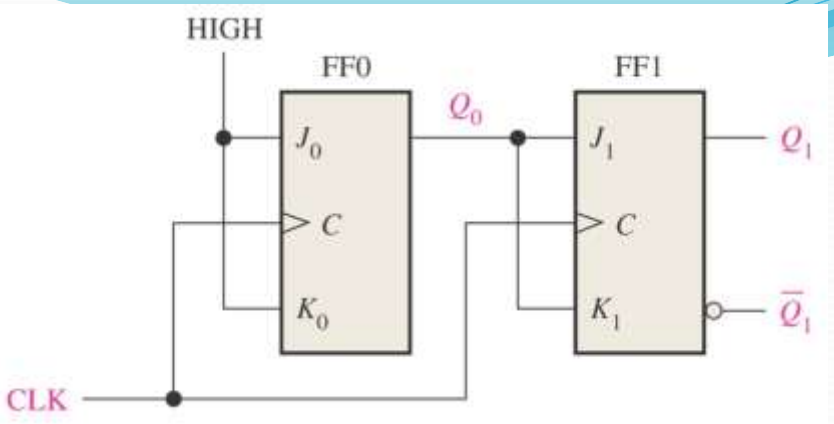


Figure 8–13 Timing diagram for the counter of Figure 8–11.



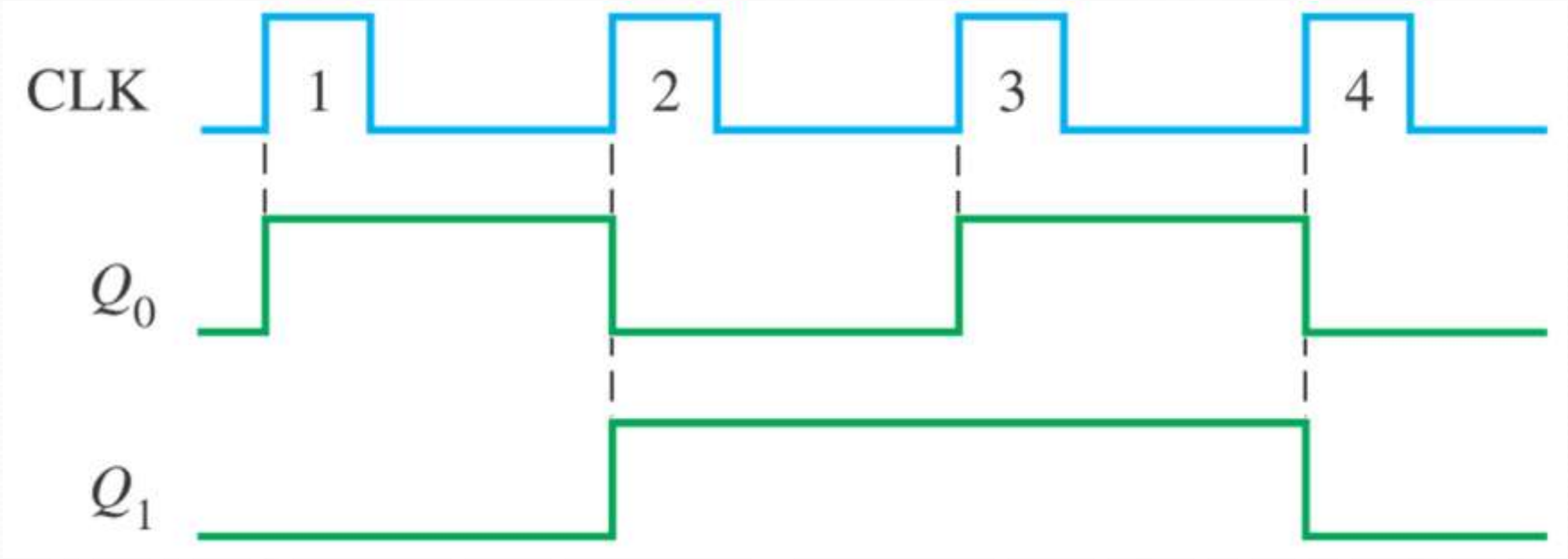
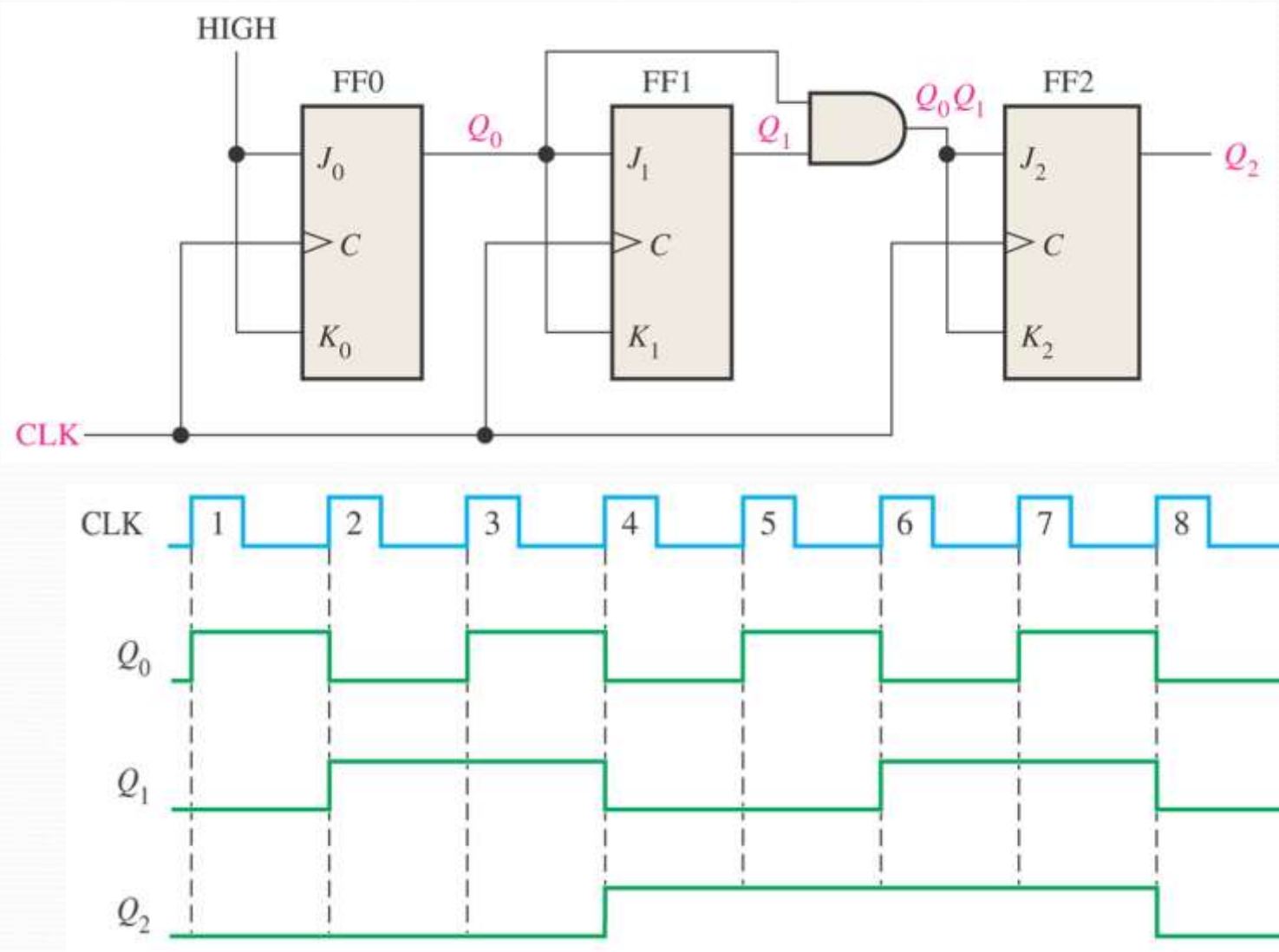


Figure 8–14 A 3-bit synchronous binary counter.



What is the function of the counter below?

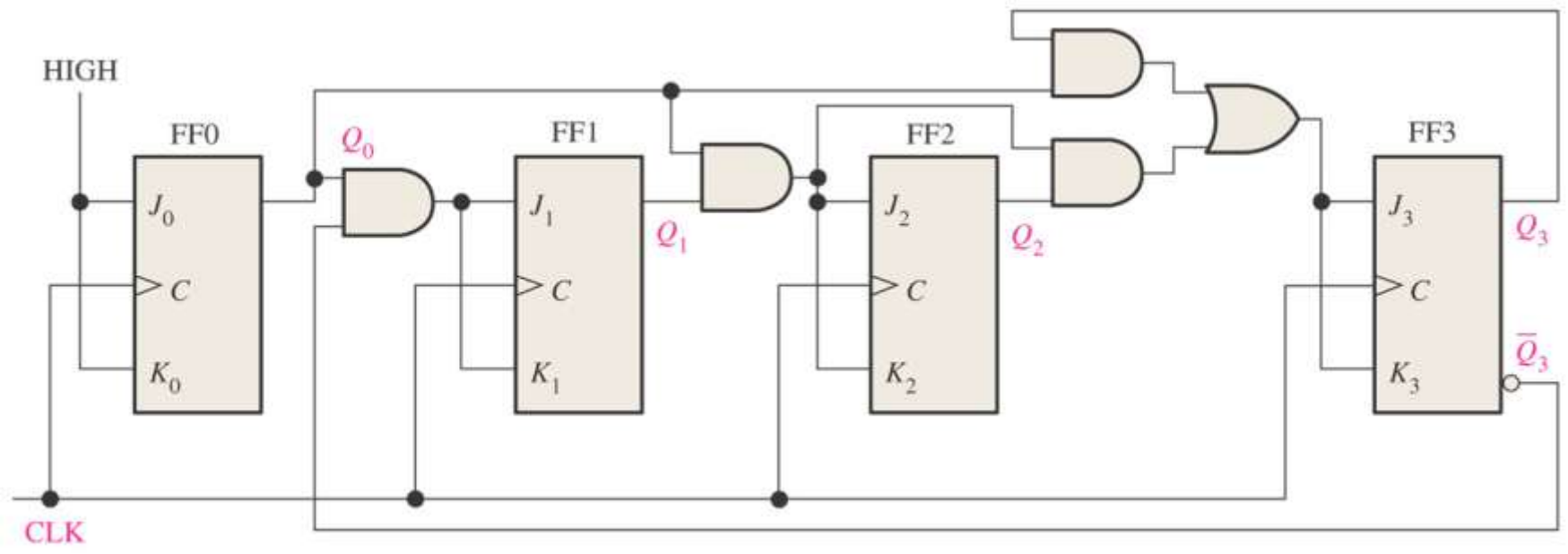
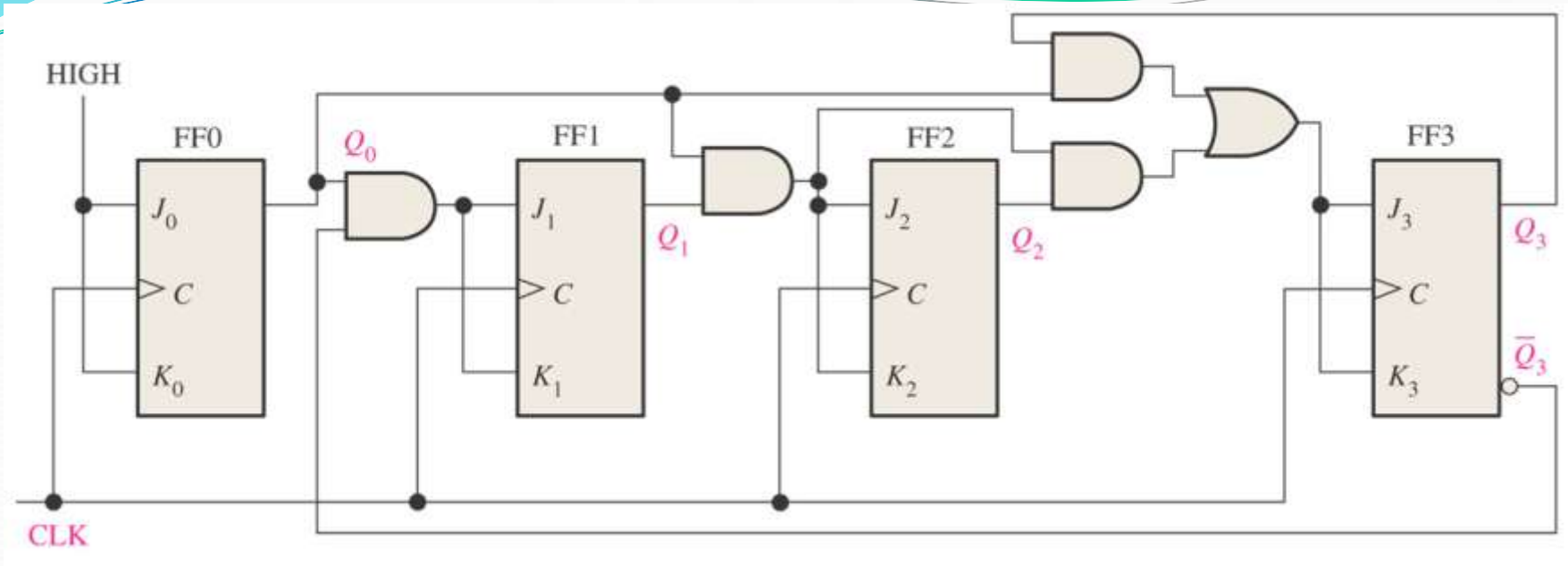


Figure 8–17 A synchronous BCD decade counter.



$$J_0 = K_0 = 1$$
$$J_1 = K_1 = Q_0\overline{Q_3}$$
$$J_2 = K_2 = Q_0Q_1$$
$$J_3 = K_3 = Q_0Q_3 + Q_0Q_1Q_2$$

$$Q^{n+1} = J\overline{Q^n} + \overline{K}Q^n$$

$$J_0 = K_0 = 1$$
$$J_1 = K_1 = Q_0\overline{Q_3}$$
$$J_2 = K_2 = Q_0Q_1$$
$$J_3 = K_3 = Q_0Q_3 + Q_0Q_1Q_2$$

$$Q^{n+1} = J\overline{Q^n} + \overline{K}Q^n$$

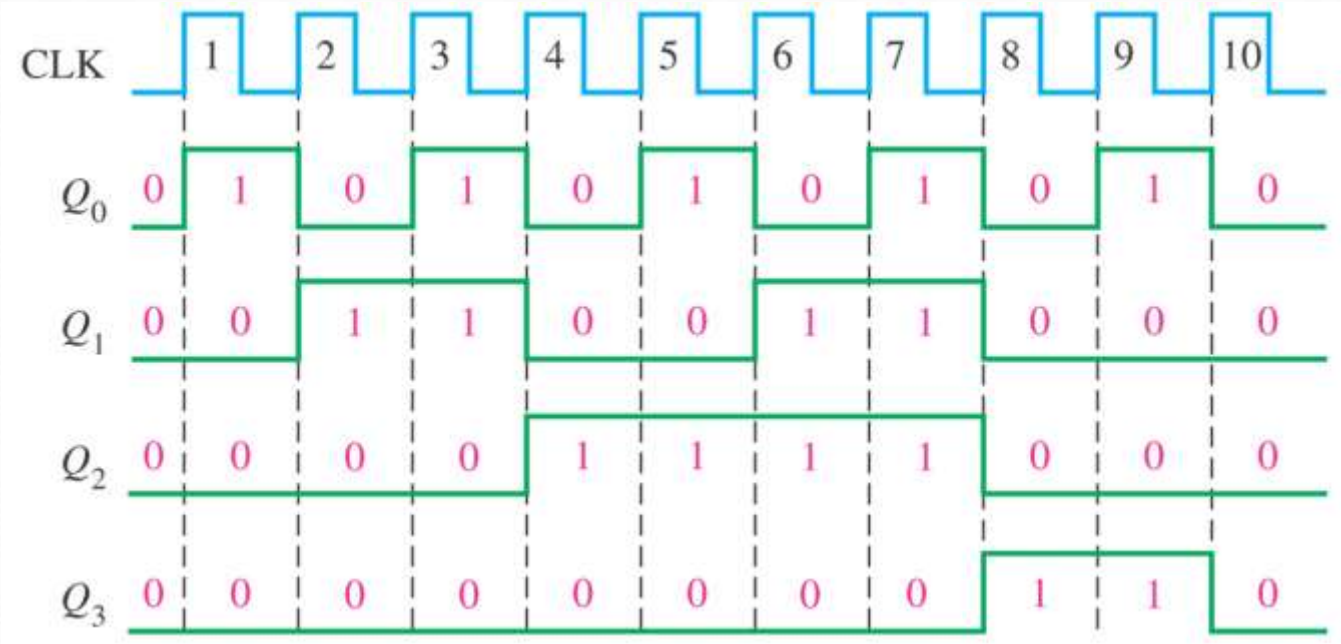
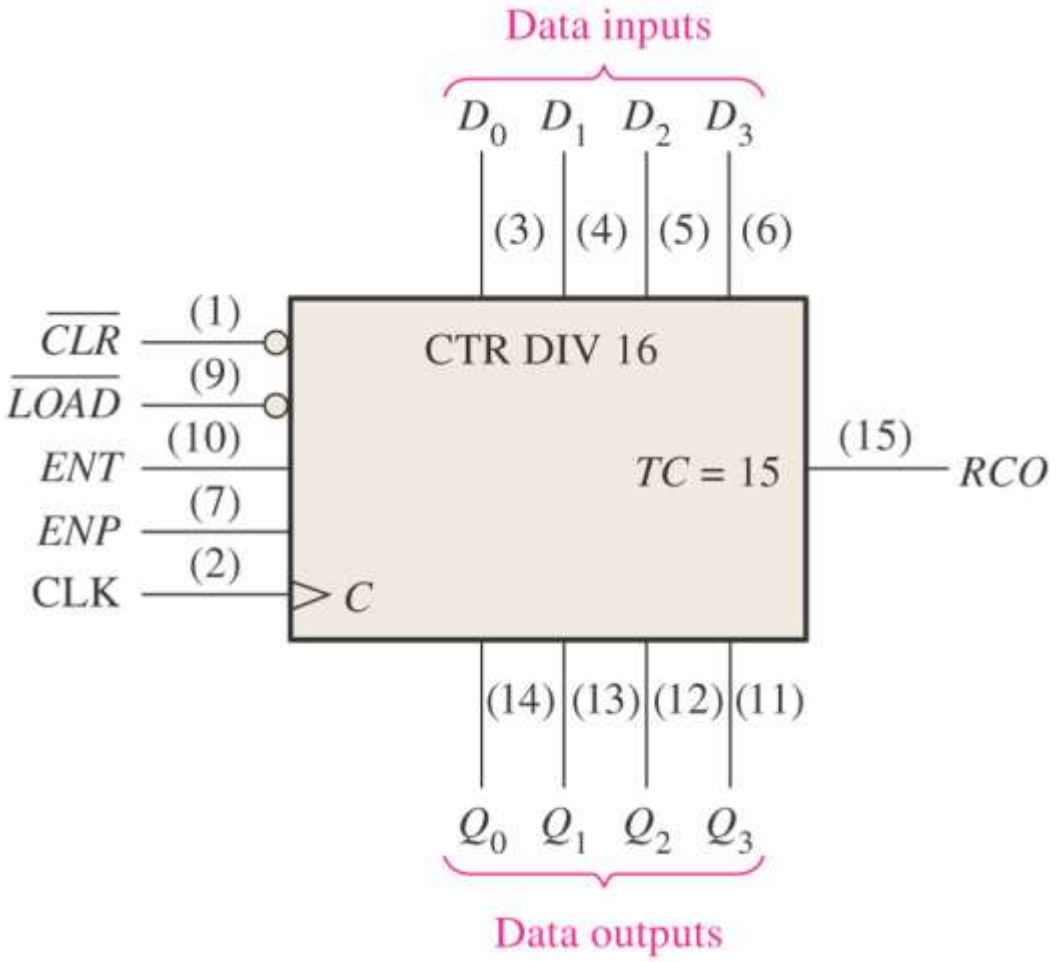


Figure 8–19 The 74HC163 4-bit synchronous binary counter.



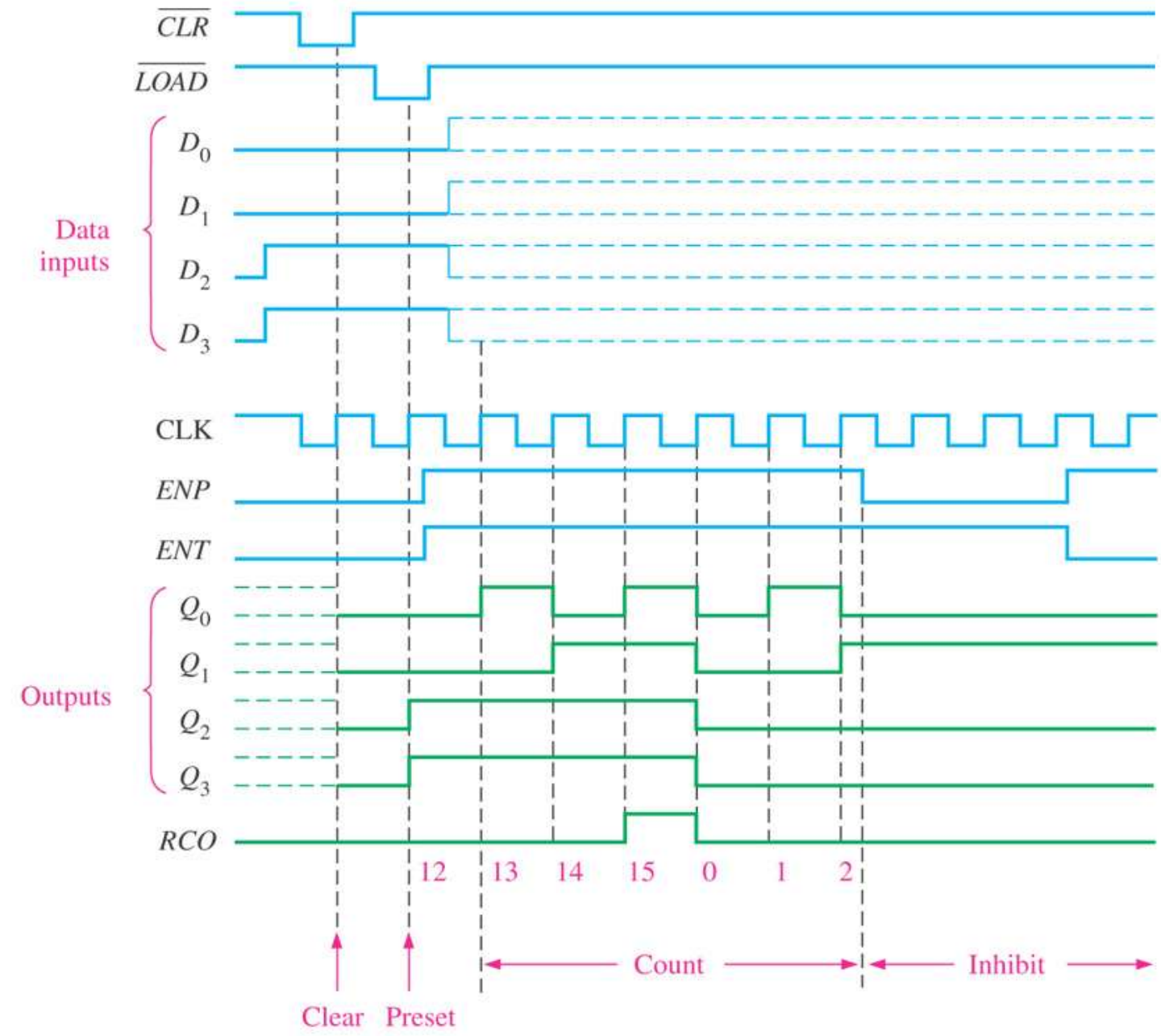
$\overline{LOAD}$: Load inputs (S)

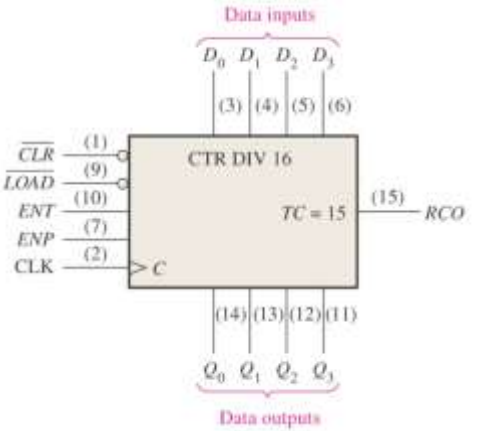
$\overline{CLR}$: Clear inputs (S)

ENT, ENP : Enable inputs

RCO : Goes High when the counter reaches the last state in its sequence of fifteen.

Figure 8–20 Timing example for a 74HC163.





8.3 Up/Down Synchronous Counters

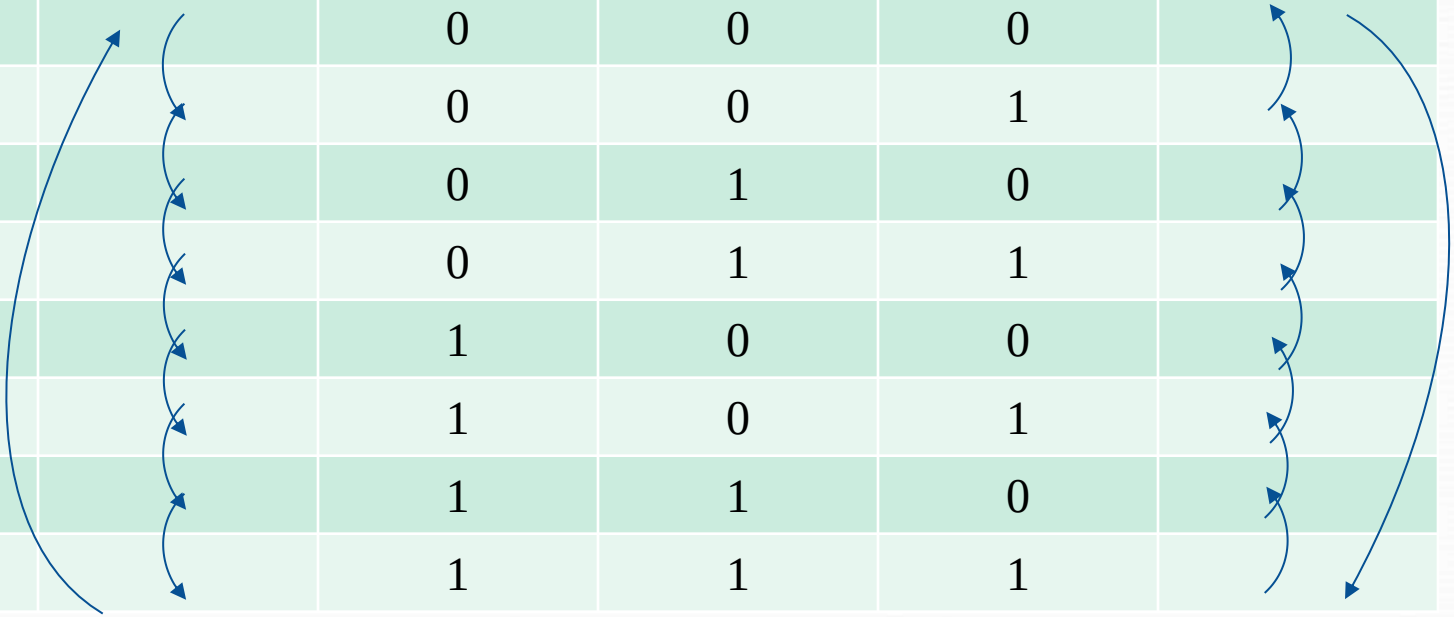
- Be capable of progressing in either direction through a certain sequence.
- Also be called as a bidirectional counter

Up/Down sequence for a 3-bit binary counter

CLOCK PULSE	UP	Q2	Q1	Q0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

Up/Down sequence for a 3-bit binary counter

CLOCK PULSE	UP	Q2	Q1	Q0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

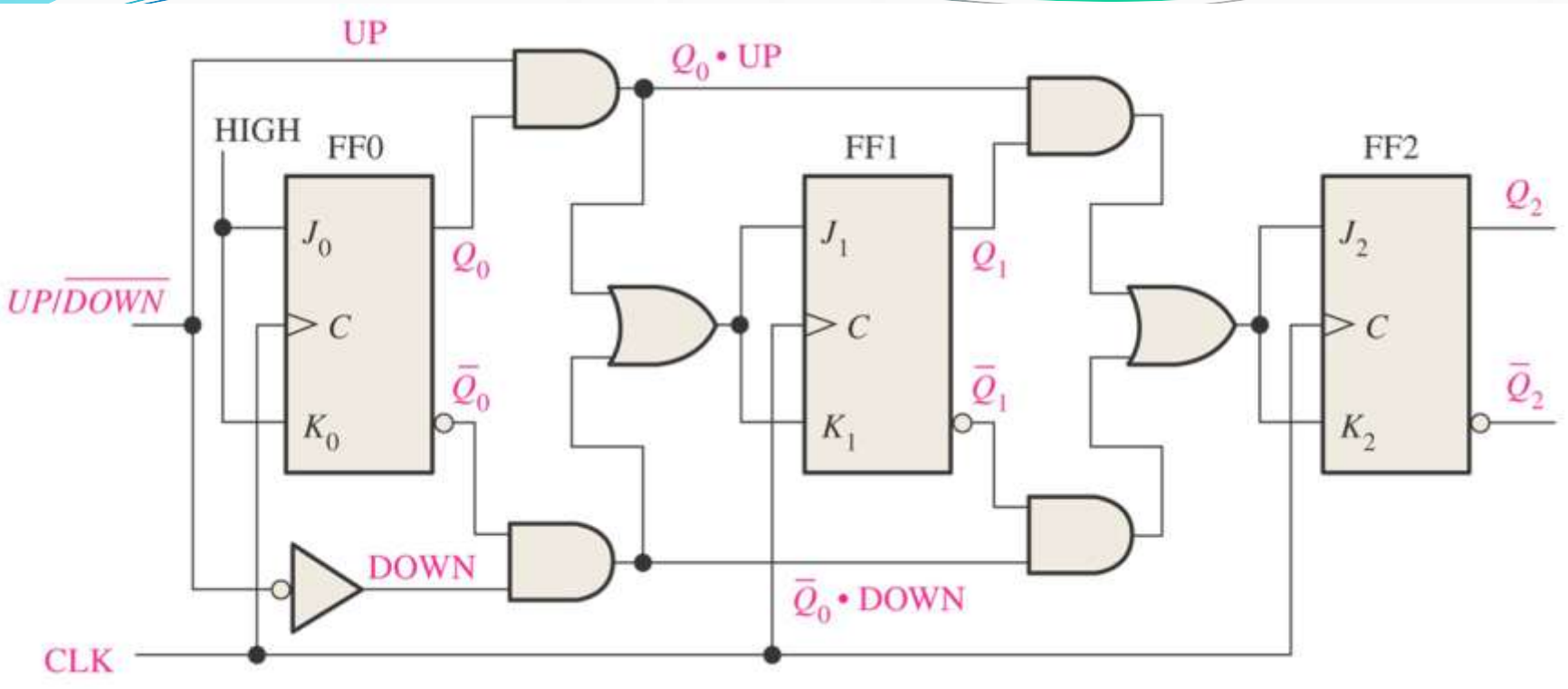


$$J_0 = K_0 = 1$$

$$J_1 = K_1 = \left(Q_0 \bullet UP\right) + \left(\overline{Q_0} \bullet DOWN\right)$$

$$J_2 = K_2 = \left(Q_0 \bullet Q_1 \bullet UP\right) + \left(\overline{Q_0} \bullet \overline{Q_1} \bullet DOWN\right)$$

Figure 8–23 A basic 3-bit up/down synchronous counter.

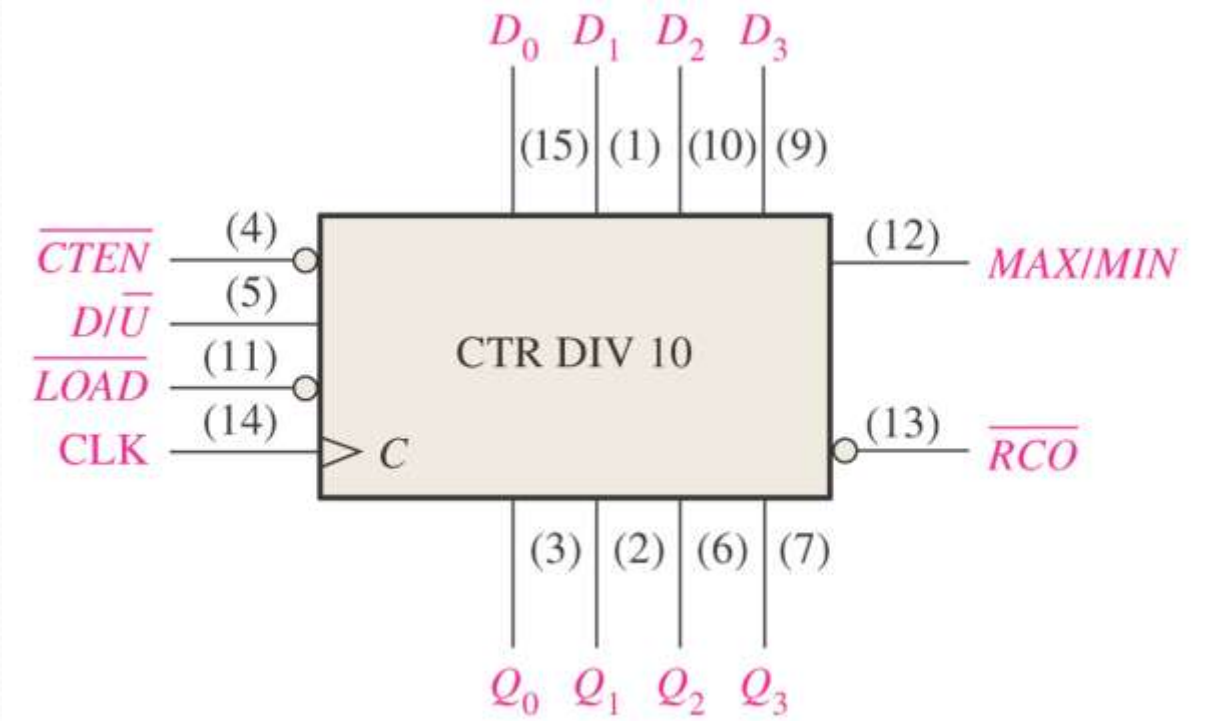


$$J_0 = K_0 = 1$$

$$J_1 = K_1 = (Q_0 \bullet UP) + (\overline{Q_0} \bullet DOWN)$$

$$J_2 = K_2 = (Q_0 \bullet Q_1 \bullet UP) + (\overline{Q_0} \bullet \overline{Q_1} \bullet DOWN)$$

Figure 8–25 The 74HC190 up/down synchronous **decade** counter.

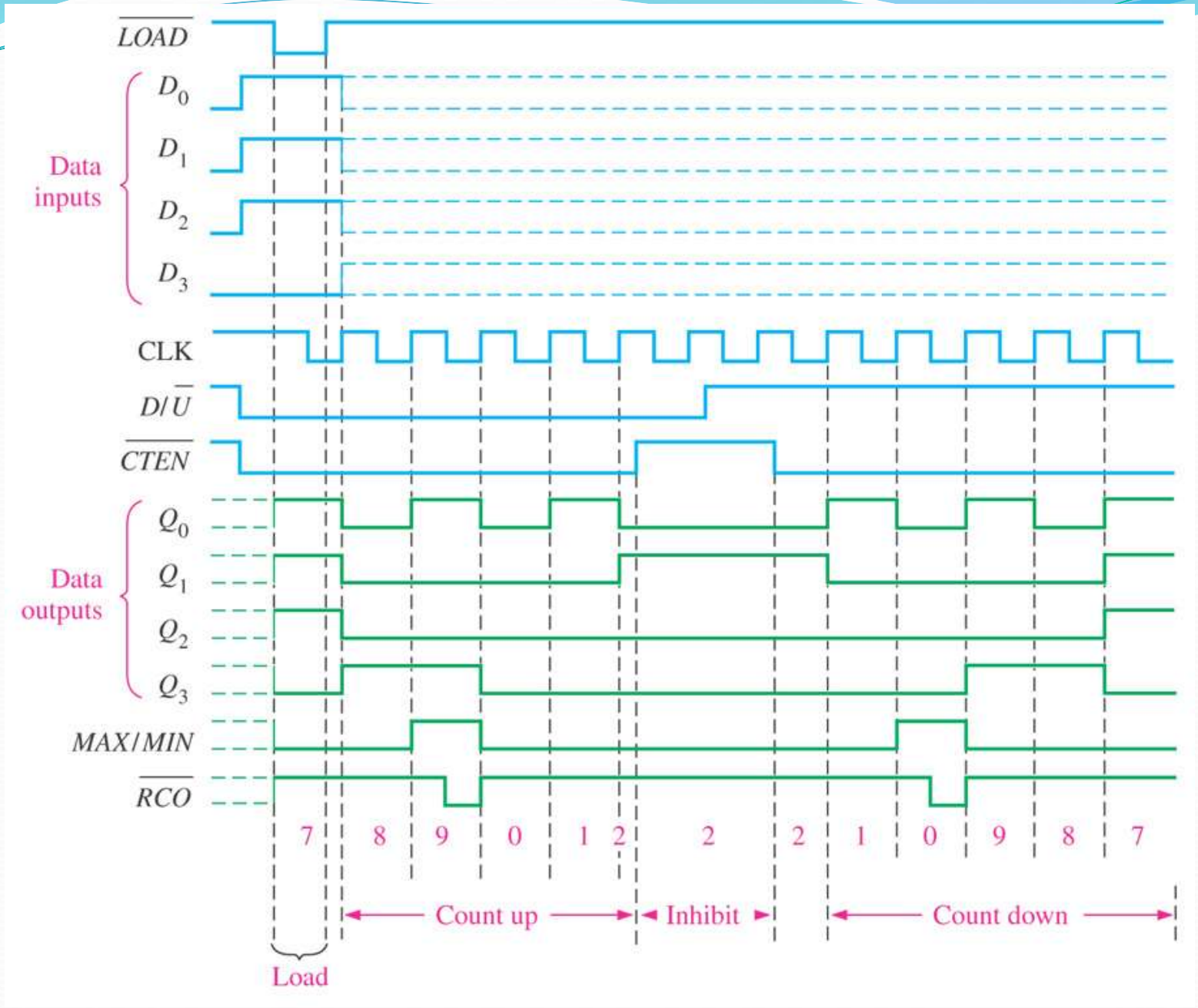


MAX / MIN Produces a HIGH pulse when the terminal count nine (1001) is reached in the UP mode or when the terminal count zero (0000) is reached in the DOWN mode.

$\overline{CTEN}$ Count enable input

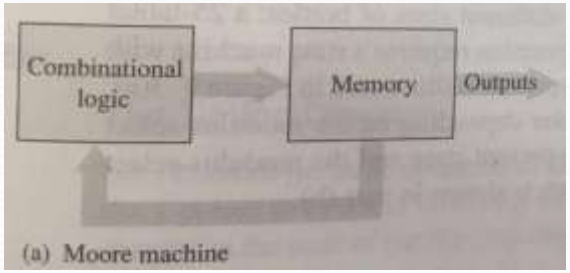
$\overline{RCO}$ Ripple clock output

Figure 8–26 Timing example for a 74HC190.

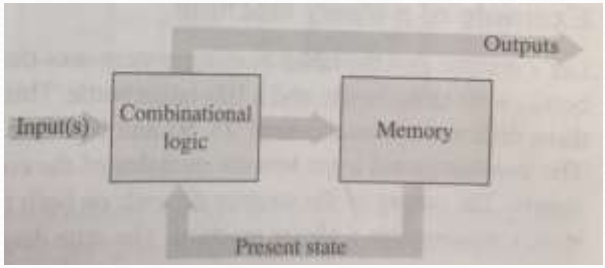


8.4 Design of Synchronous Counters

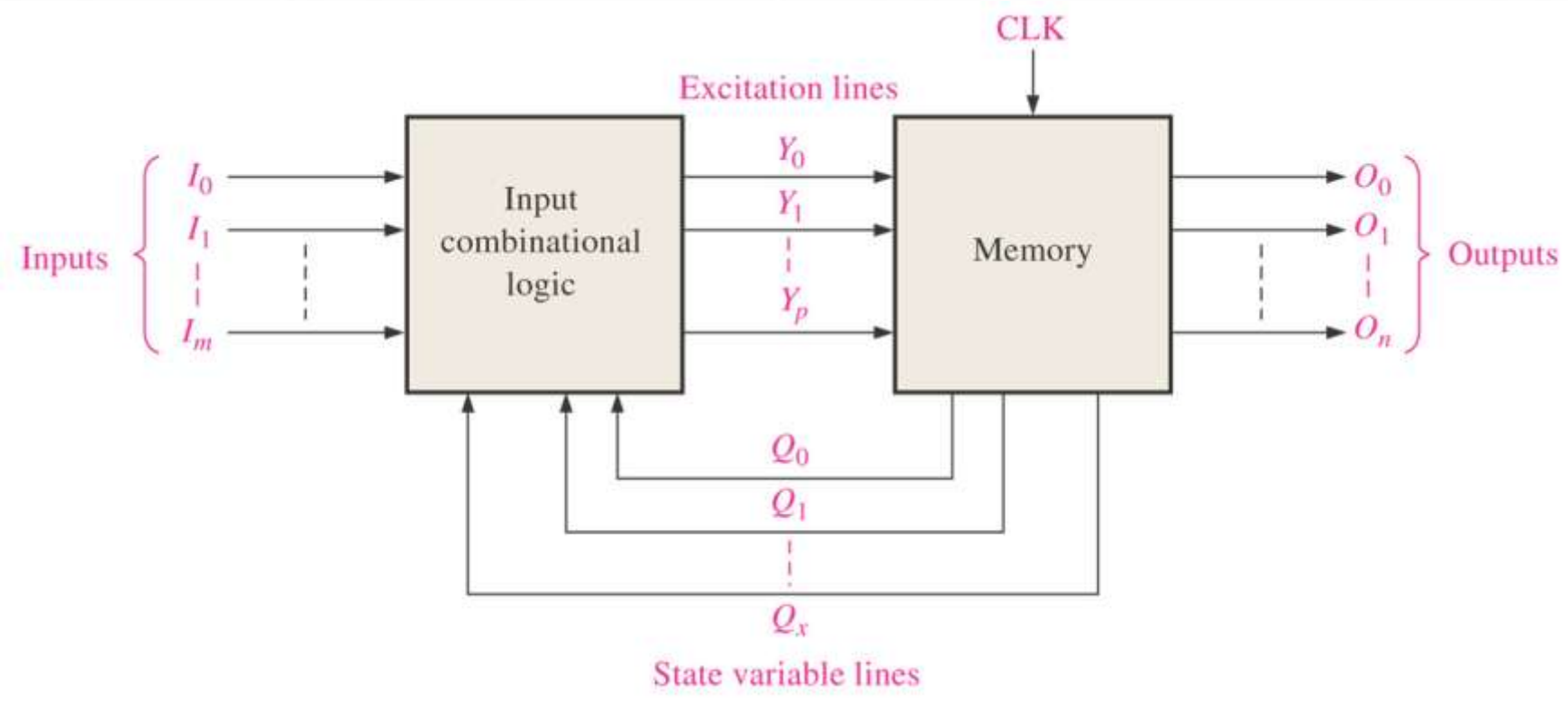
- Moore circuits
  - The output or outputs depend only on the present internal state

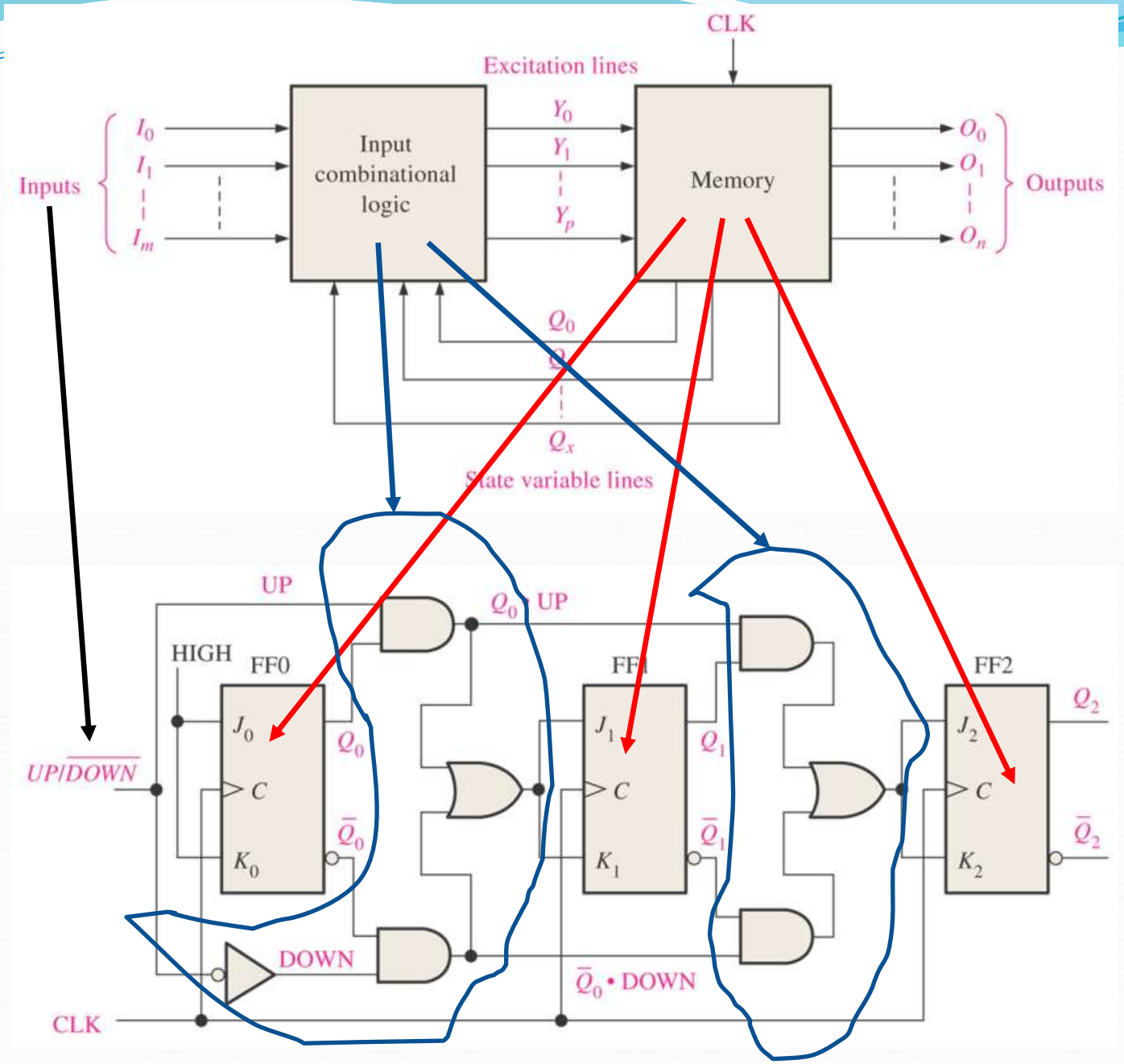


- Mealy circuits
  - The output or outputs depend on both the present state and the input or inputs



General Model of a Sequential Circuit



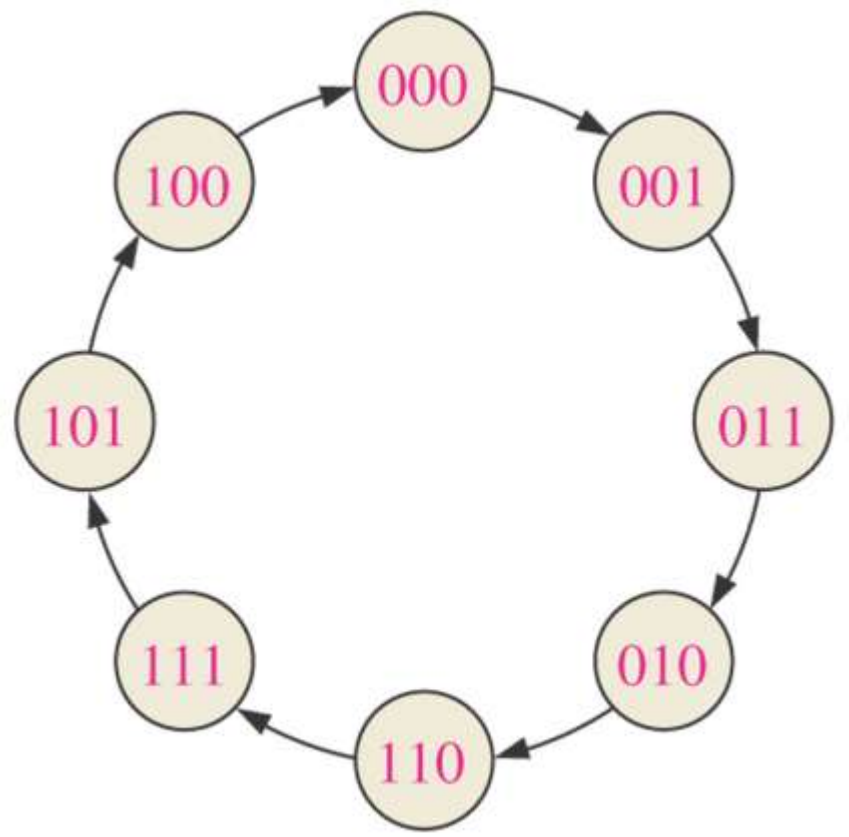

CLK
Excitation lines
Inputs
I_0
I_1
I_m
Input combinational logic
Y_0
Y_1
Y_p
Memory
O_0
O_1
O_n
Outputs
Q_0
Q_x
State variable lines
UP
Q_0 UP
HIGH
FF0
FF1
FF2
J_0
C
K_0
Q_0
$\overline{Q}_0$
J_1
K_1
Q_1
$\overline{Q}_1$
J_2
K_2
Q_2
$\overline{Q}_2$
UP/$\overline{DOWN}$
DOWN
$\overline{Q}_0$ • DOWN
CLK

A general design procedure for sequential circuits

- State Diagram
- Next-State Table
- Flip-Flop Transition Table
- Karnaugh Maps
- Logic Expressions for Flip-Flop Inputs
- Counter Implementation

Example: Design of a basic 3-bit Gray code counter.

Step 1: State Diagram



Step 2: Next-State Table

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

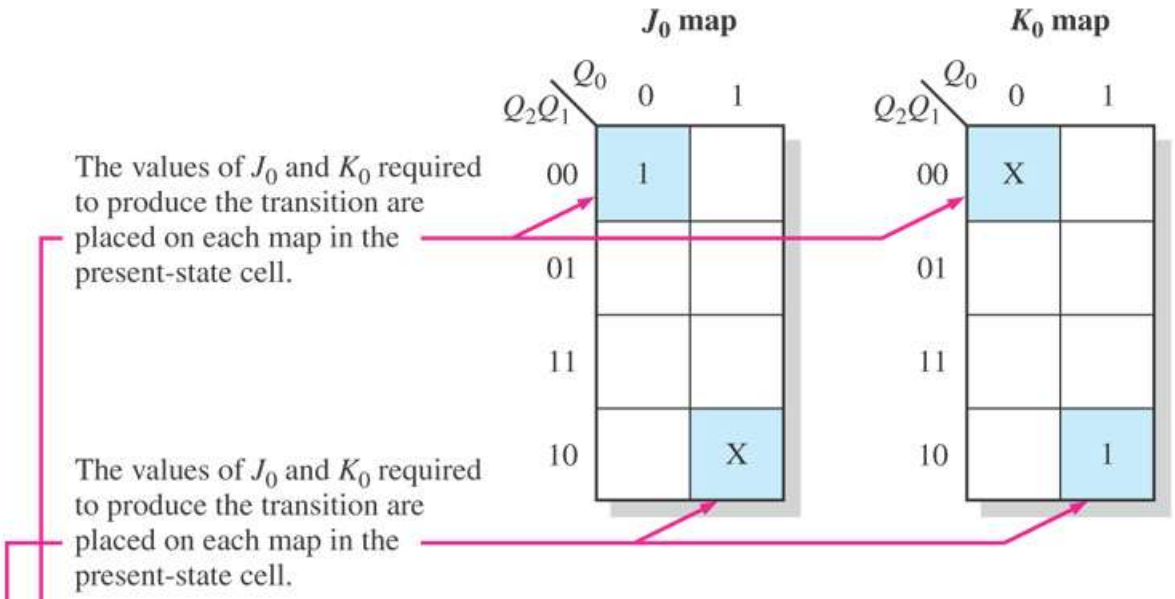
Step 3: Flip-Flop Transition Table

Transition table for a J-K flip-flop

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0
Q_N: present state				
Q_{N+1}: next state				
X: “don’t care”				

$$Q_{N+1} = J\overline{Q_N} + \overline{K}Q_N$$

Step 4: Karnaugh Map



Output Transitions Q_N	Q_{N+1}	Flip-Flop Inputs J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

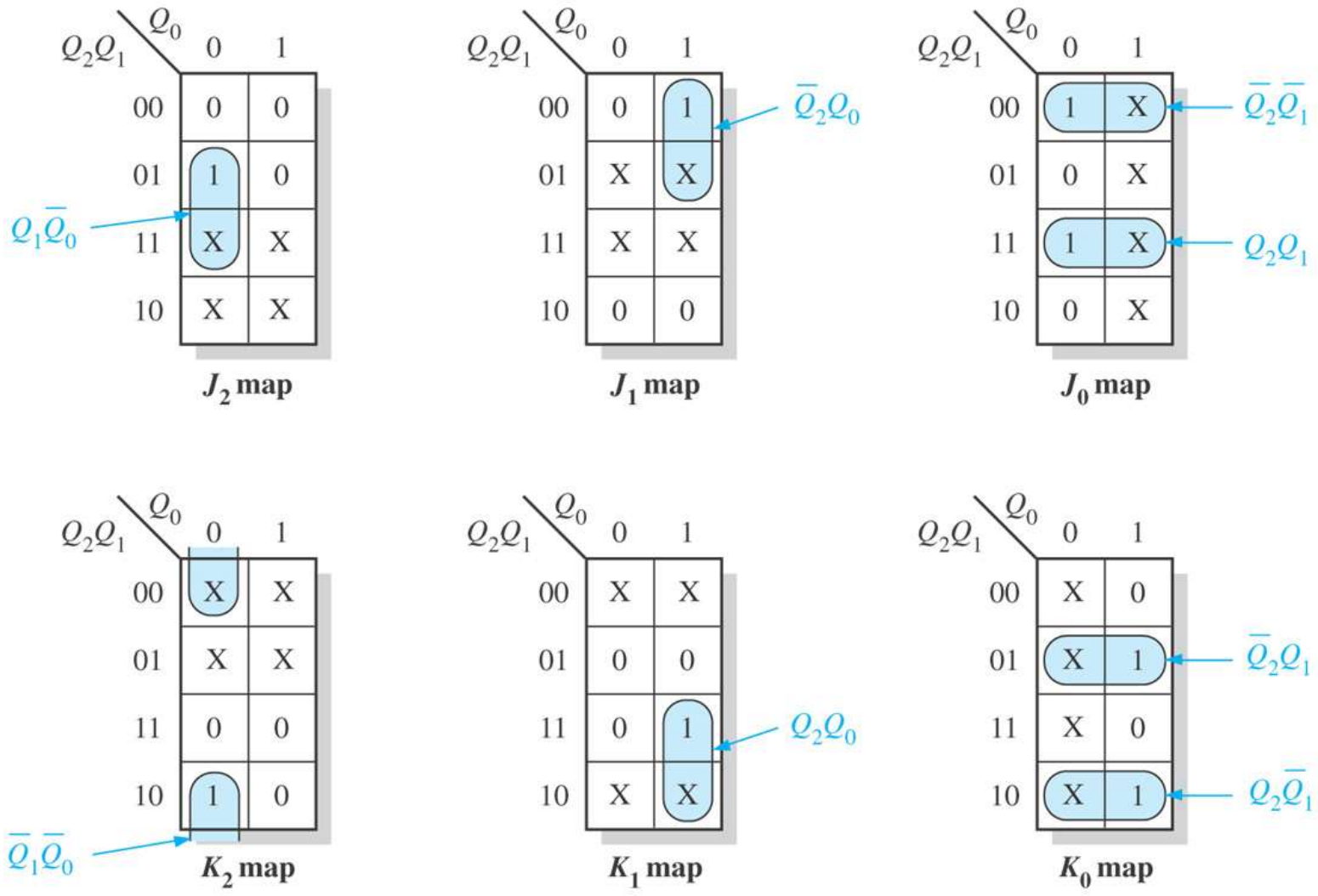
Flip-flop transition table

Present State Q_2	Q_1	Q_0	Next State Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Next-state table

For the present state 000, Q_0 makes a transition from 0 to 1 to the next state.

For the present state 101, Q_0 makes a transition from 1 to 0 to the next state.


Q_2Q_1 Q_0 0 1
00 0 0
01 1 0
11 X X
10 X X
$Q_1\overline{Q}_0$
J_2 map
Q_2Q_1 Q_0 0 1
00 0 1
01 X X
11 X X
10 0 0
$\overline{Q}_2Q_0$
J_1 map
Q_2Q_1 Q_0 0 1
00 1 X
01 0 X
11 1 X
10 0 X
$\overline{Q}_2\overline{Q}_1$
Q_2Q_1
J_0 map
Q_2Q_1 Q_0 0 1
00 X X
01 X X
11 0 0
10 1 0
$\overline{Q}_1\overline{Q}_0$
K_2 map
Q_2Q_1 Q_0 0 1
00 X X
01 0 0
11 0 1
10 X X
Q_2Q_0
K_1 map
Q_2Q_1 Q_0 0 1
00 X 0
01 X 1
11 X 0
10 X 1
$\overline{Q}_2Q_1$
$Q_2\overline{Q}_1$
K_0 map

Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2 Q_1 + \overline{Q_2}\,\overline{Q_1} = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2 \overline{Q_1} + \overline{Q_2} Q_1 = Q_2 \oplus Q_1$$

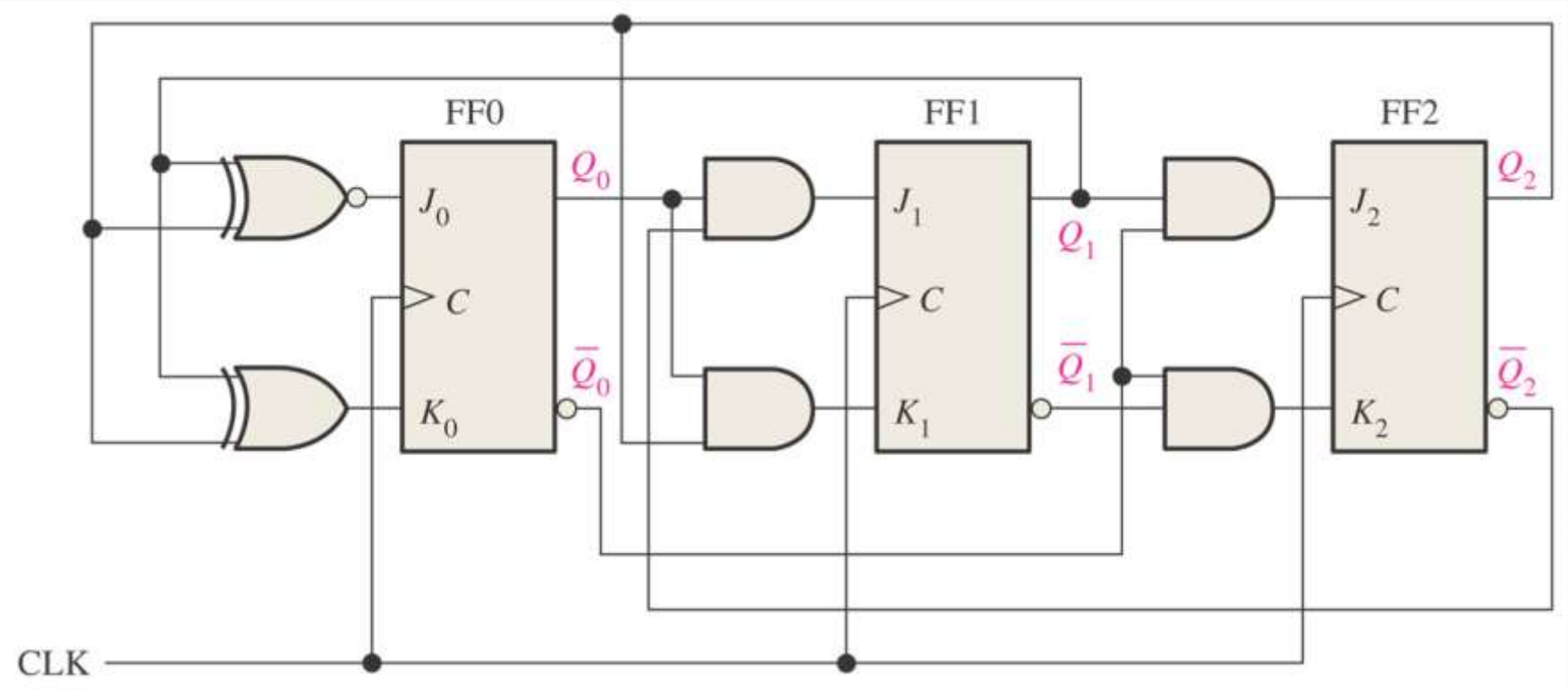
$$J_1 = \overline{Q_2} Q_0$$

$$K_1 = Q_2 Q_0$$

$$J_2 = Q_1 \overline{Q_0}$$

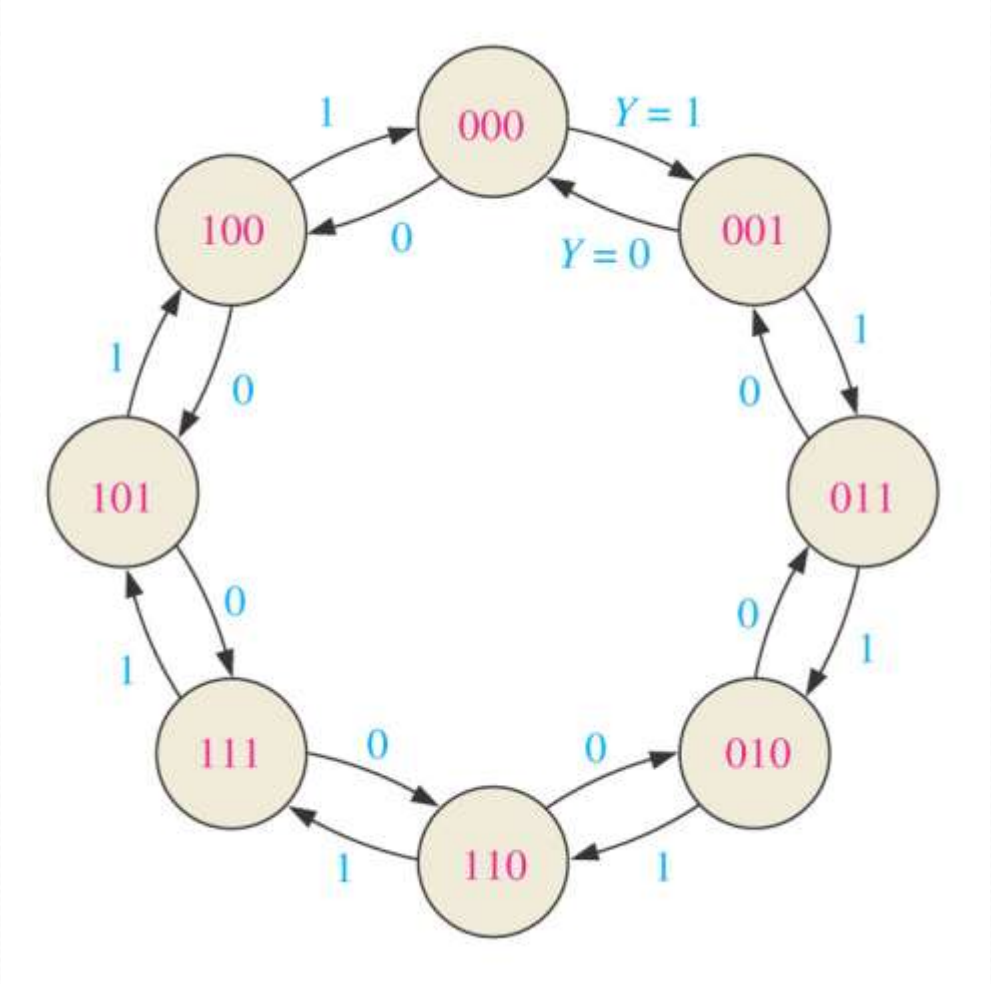
$$K_2 = \overline{Q_1}\,\overline{Q_0}$$

Step 6: Counter Implementation



Example: Develop a synchronous 3-bit up/down counter with a Gray code sequence.

Step 1: State Diagram



Step 2: Next-State Table

Present State			Next State					
			Y=0 (DOWN)			Y=1 (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

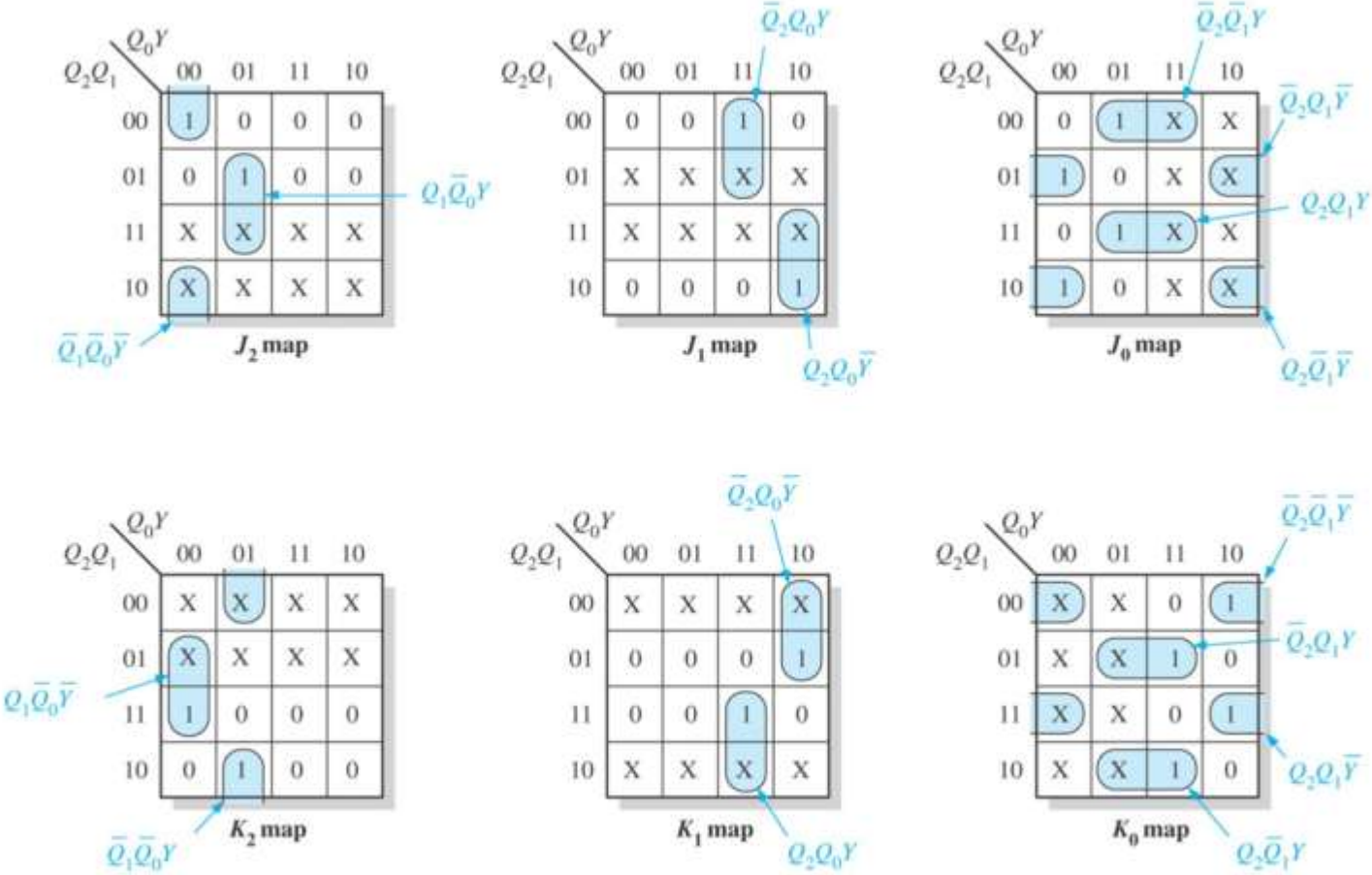
Step 3: Flip-Flop Transition Table

Transition table for a J-K flip-flop

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0
Q_N: present state				
Q_{N+1}: next state				
X: “don’t care”				

Step 4: Karnaugh Map

Figure 8–36 *J* and *K* maps for Table 8–11. The UP $\sqrt{\text{DOWN}}$ control input, *Y*, is treated as a fourth variable.



Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2 Q_1 Y + Q_2 \overline{Q_1}\,\overline{Y} + \overline{Q_2}\,\overline{Q_1} Y + \overline{Q_2} Q_1 \overline{Y}$$

$$K_0 = \overline{Q_2}\,\overline{Q_1}\,\overline{Y} + \overline{Q_2} Q_1 Y + Q_2 \overline{Q_1} Y + Q_2 Q_1 \overline{Y}$$

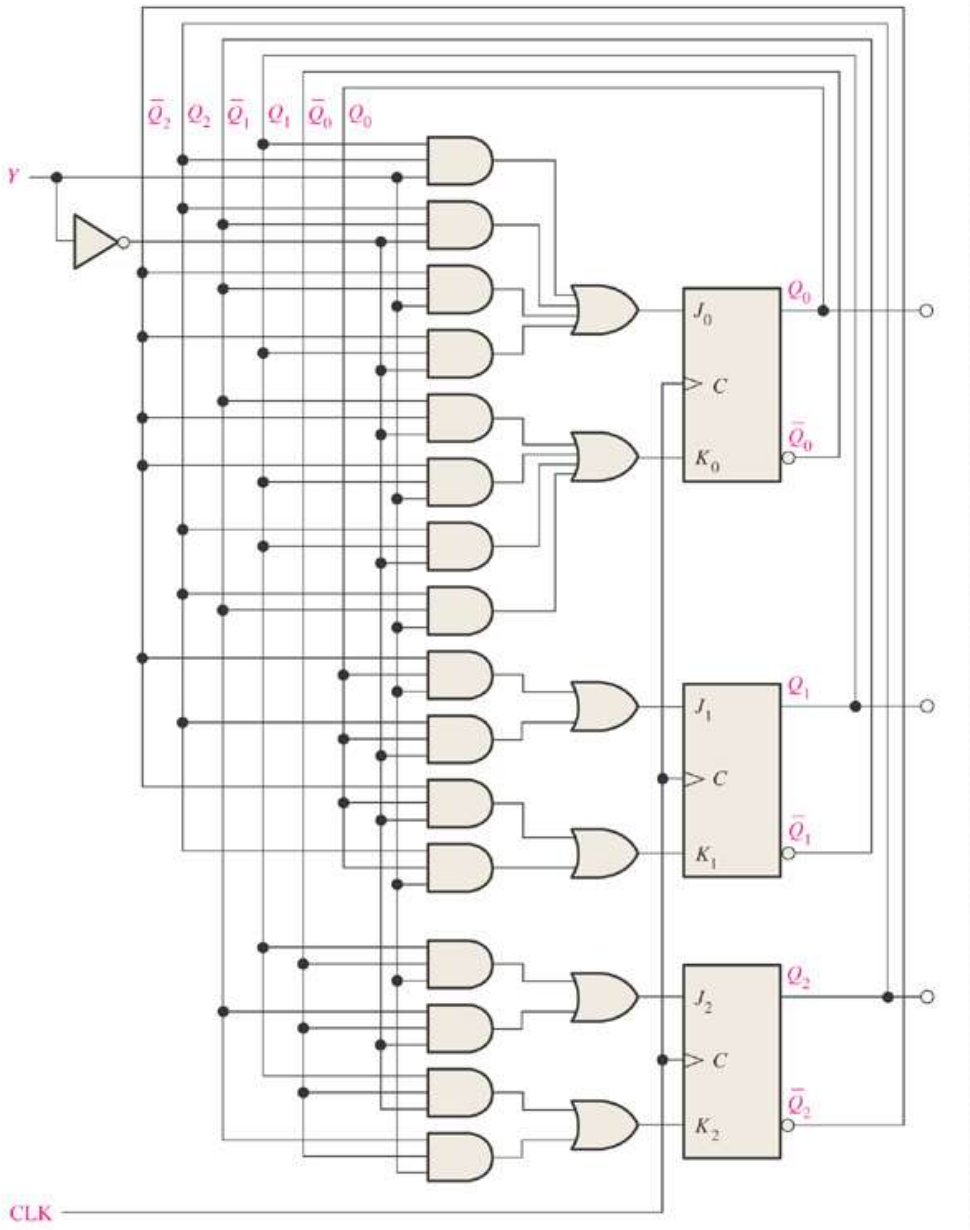
$$J_1 = \overline{Q_2} Q_0 Y + Q_2 Q_0 \overline{Y}$$

$$K_1 = \overline{Q_2} Q_0 \overline{Y} + Q_2 Q_0 Y$$

$$J_2 = Q_1 \overline{Q_0} Y + \overline{Q_1}\,\overline{Q_0}\,\overline{Y}$$

$$K_2 = Q_1 \overline{Q_0}\,\overline{Y} + \overline{Q_1}\,\overline{Q_0} Y$$

Step 6: Counter Implementation



8.5 Cascaded Counters

- Connect counter to achieve higher-modulus operation
- Cascading
  - The last-stage output of one counter drives the input of the next counter

Figure 8–38 Two cascaded counters (all *J* and *K* inputs are HIGH).

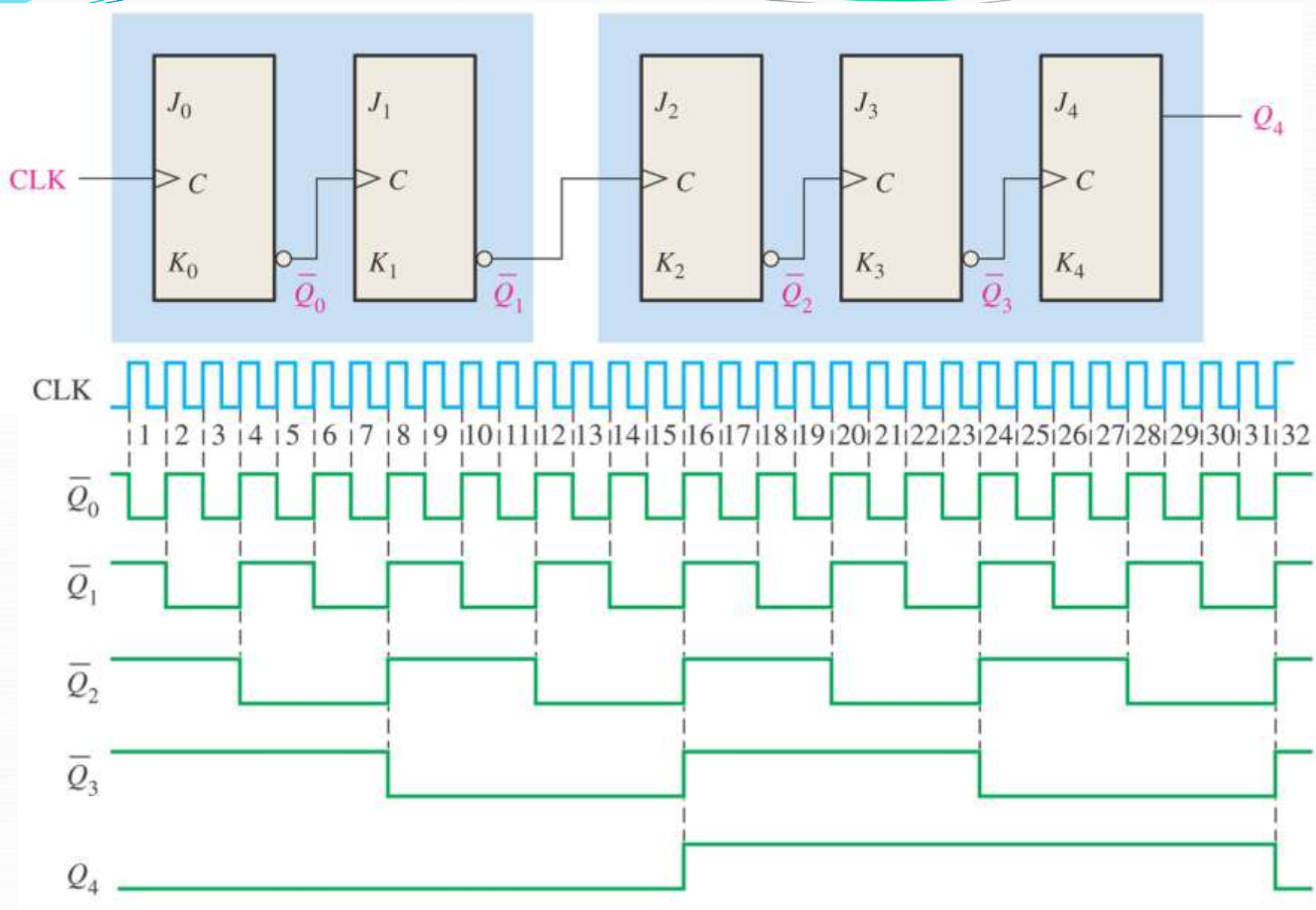


Figure 8–40 A modulus-100 counter using two cascaded decade counters.

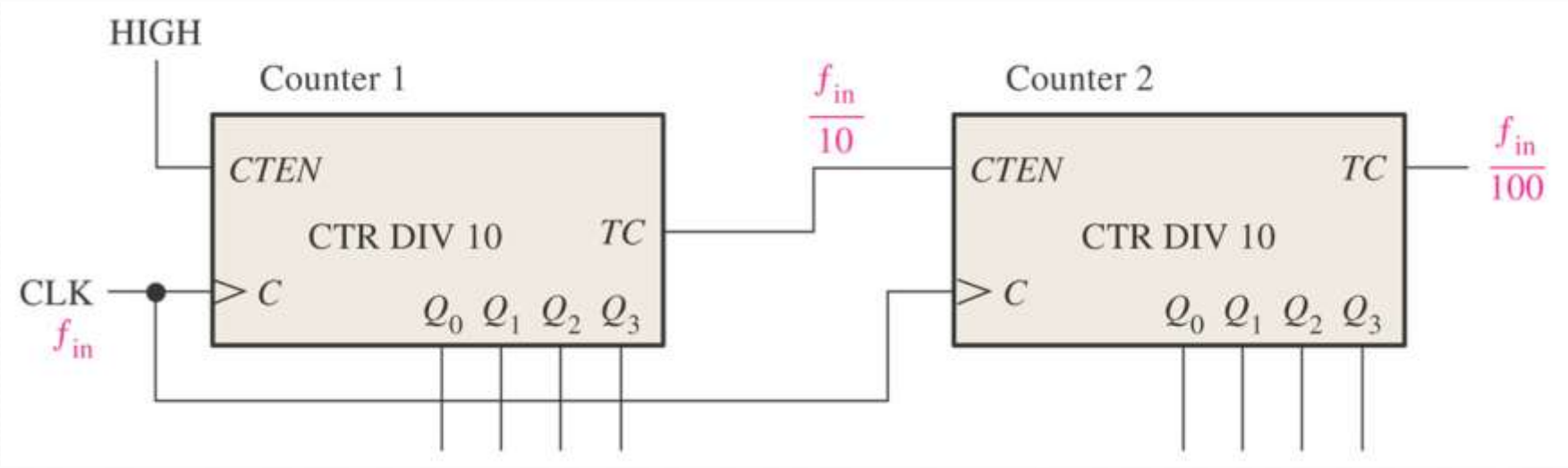
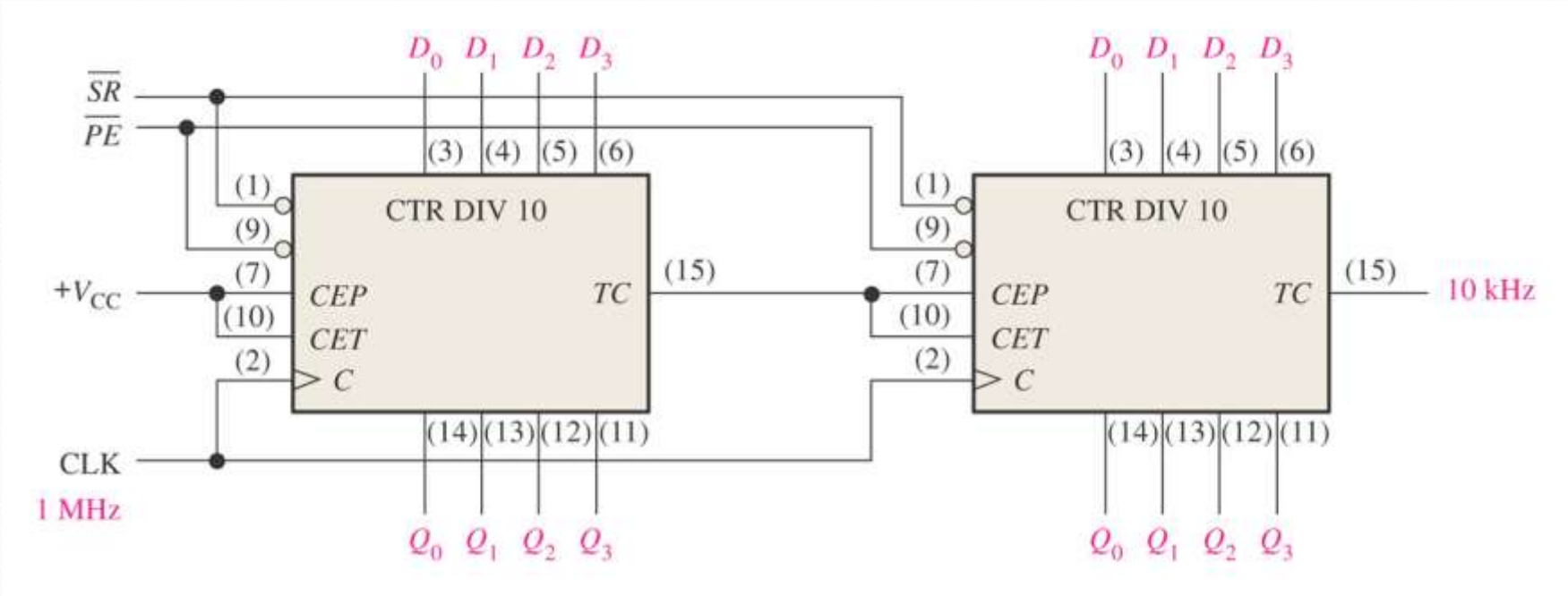


Figure 8–43 A divide-by-100 counter using two 74F162 decade counters.



$\overline{PE}$: preset to any BCD count

$\overline{SR}$: reset the counter

Cascaded Counters with Truncated Sequences

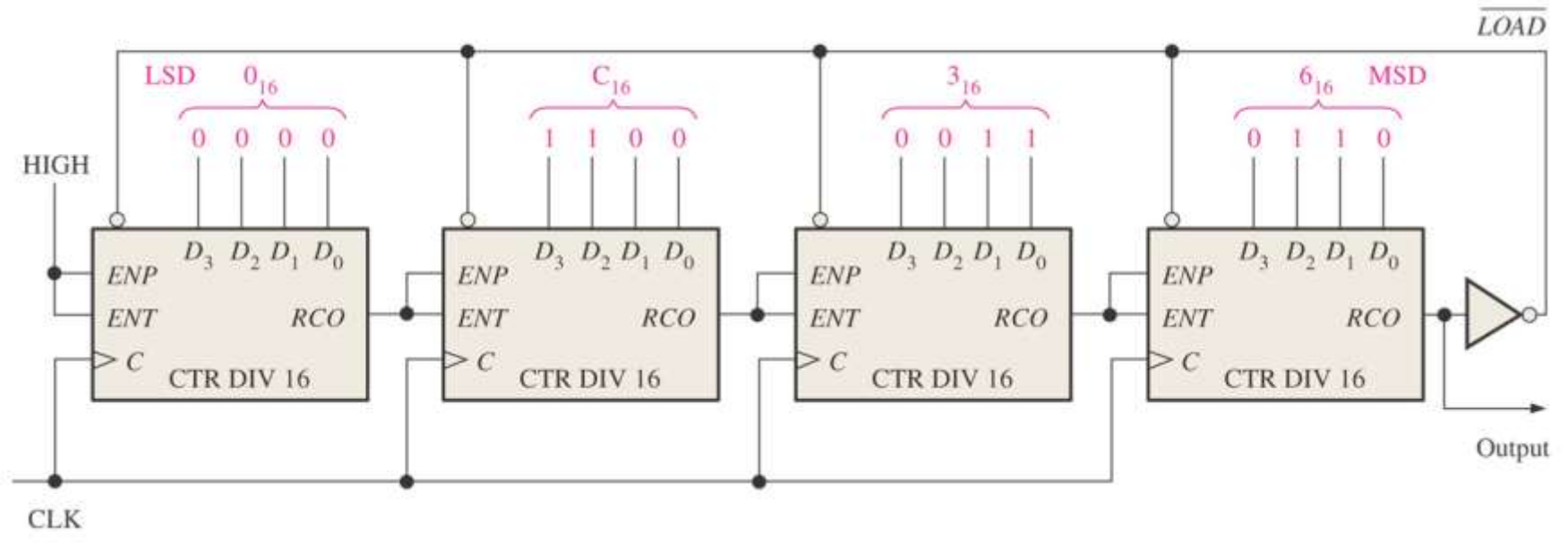


Figure 8–44 A divide-by-40,000 counter using 74HC161 4-bit binary counters. Note that each of the parallel data inputs is shown in binary order (the right-most bit D_0 is the LSB in each counter).

$$2^{16} - 40000 = 65536 - 40000 = 25536 = 63C0H$$

8.6 Counter Decoding

Figure 8–45 Decoding of state 6 (110).

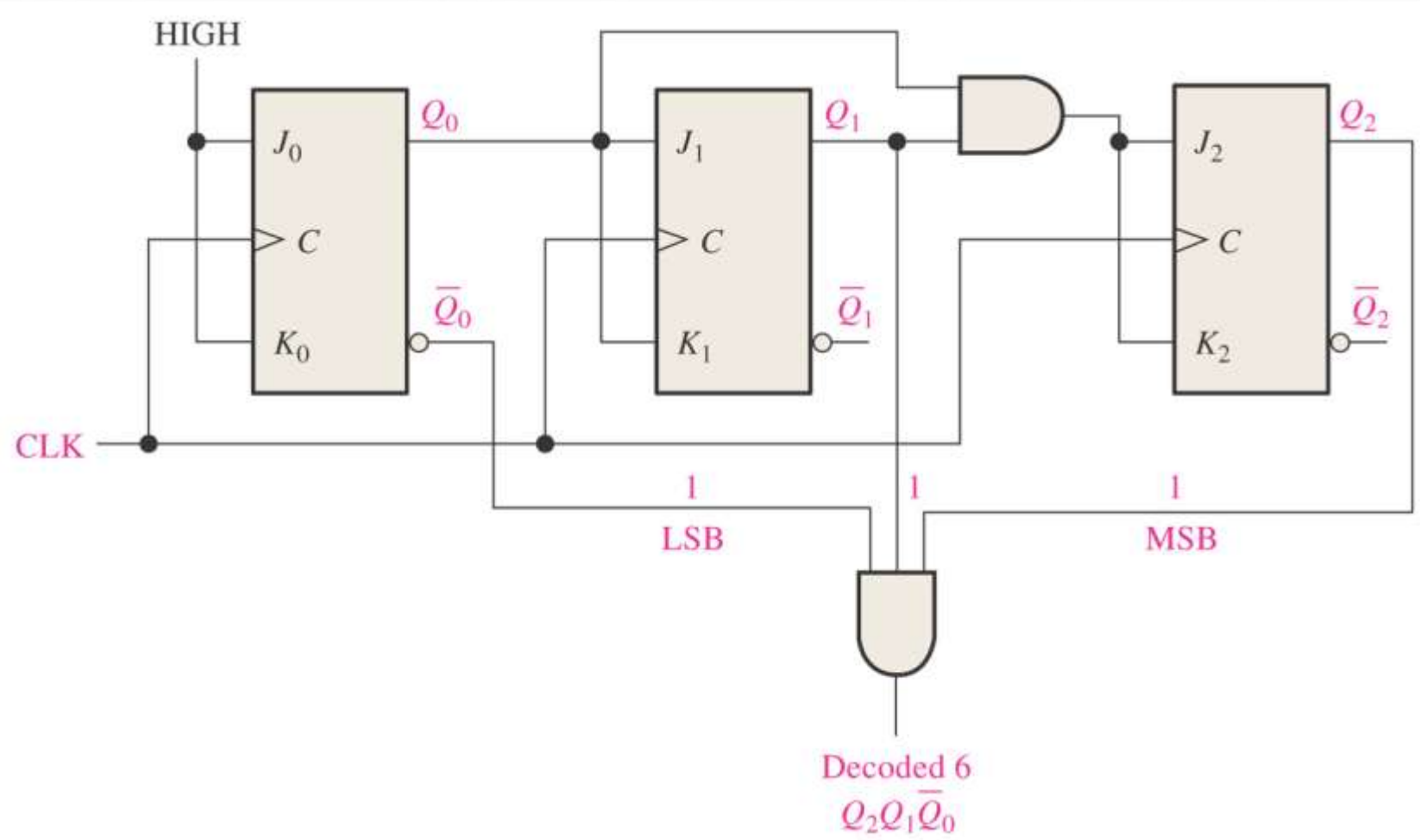
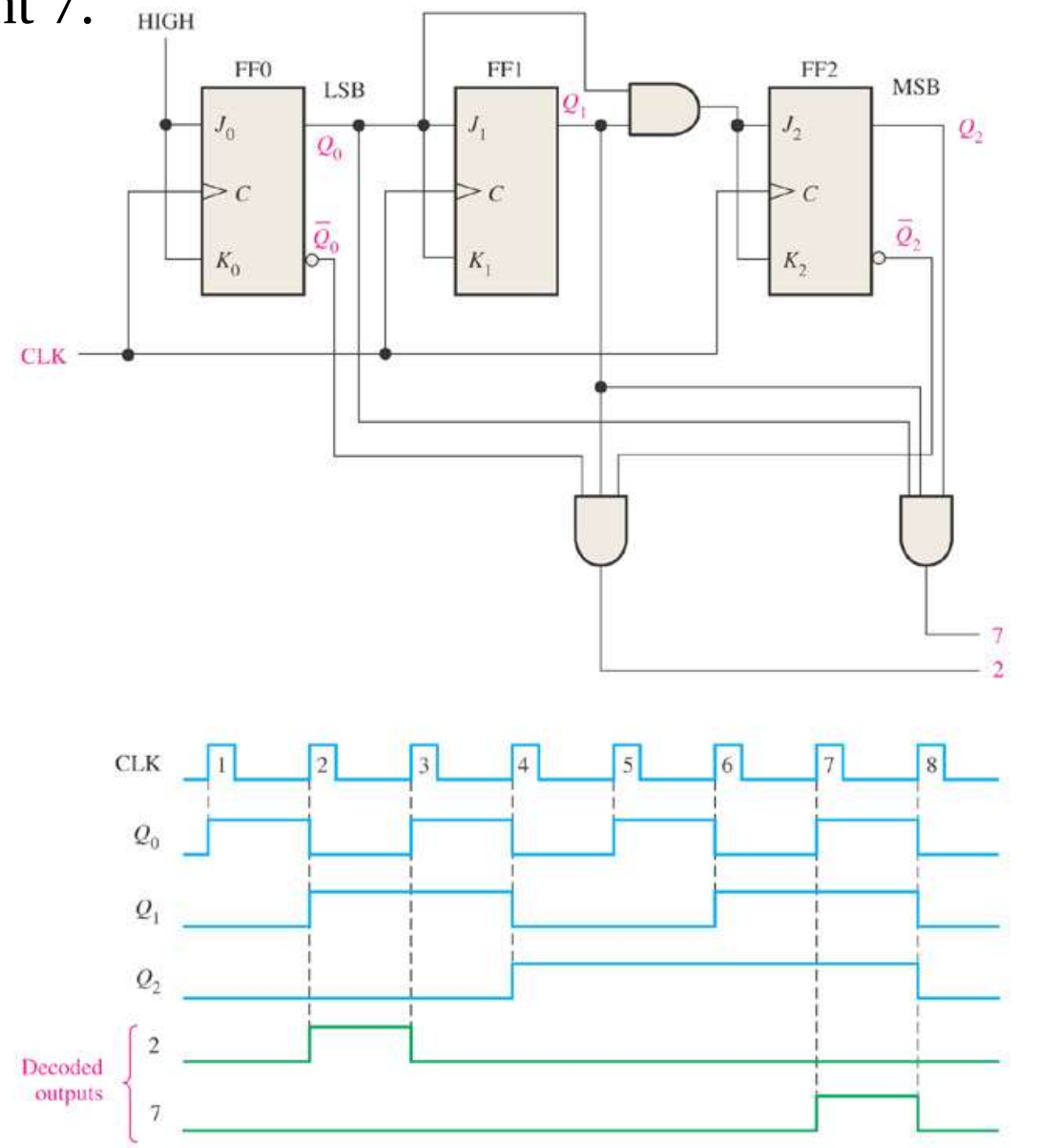


Figure 8–46 A 3-bit counter with active-HIGH decoding of count 2 and count 7.



8.7 Counter Applications

Figure 8–51 Simplified logic diagram for a 12-hour digital clock.

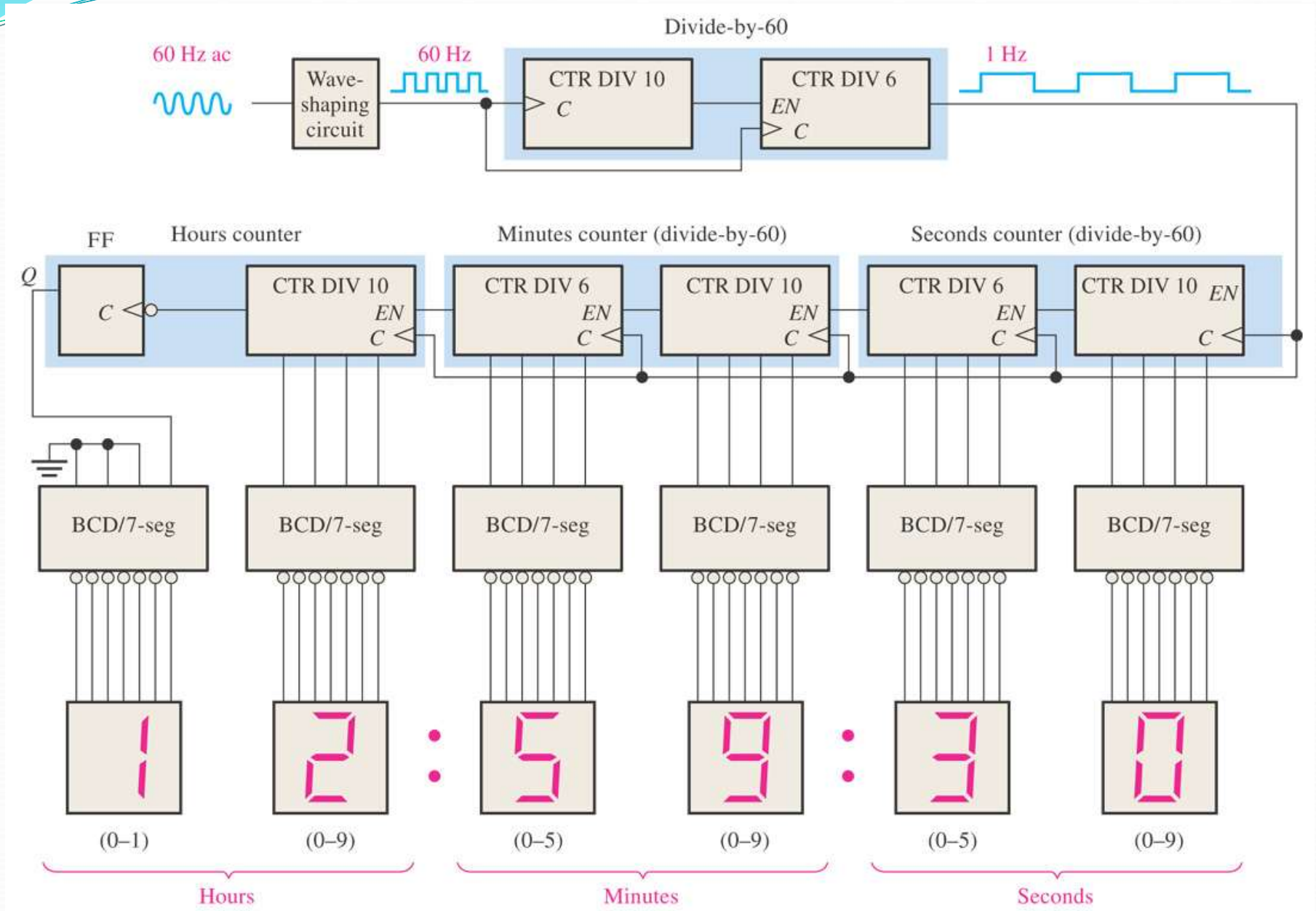
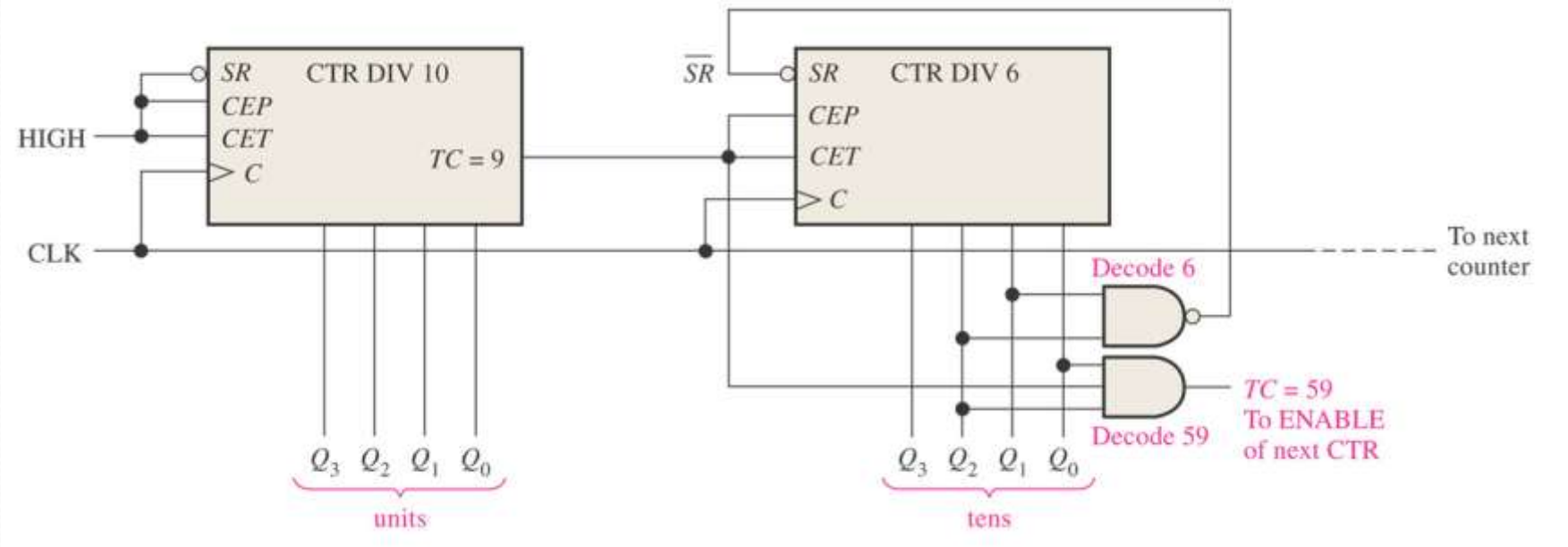
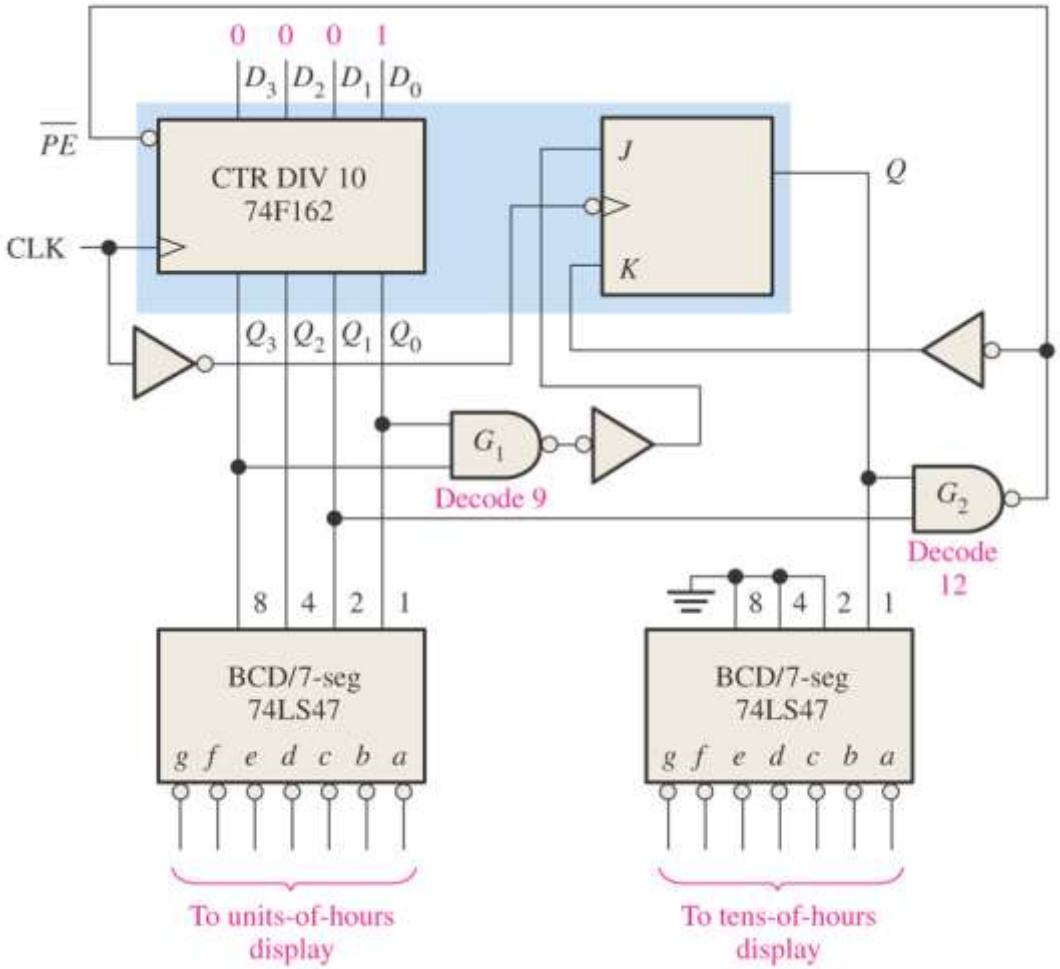


Figure 8–52 Logic diagram of typical divide-by-60 counter using 74F162 synchronous decade counters. Note that the outputs are in binary order (the right-most bit is the LSB).



$\overline{SR}$: Asynchronously reset the counter

Figure 8–53 Logic diagram for hours counter and decoders. Note that on the counter inputs and outputs, the right-most bit is the LSB.



$\overline{PE}$: Synchronously preset the counter

Summary

- Asynchronous counter and synchronous counter
  - concepts
- Up/down synchronous counter
- How to design a synchronous counter?
  - methods
- Cascaded counter
  - methods
- Applications

HW

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Detailed design procedure is required!