

Chapter 3 Logic Gates

Outline

- **Basic Logic Gates**

3.1 Basic Logic Gates

- **Inverter**
- **AND Gate**
- **OR Gate**
- **NAND Gate**
- **NOR Gate**
- **Exclusive-OR**
- **Exclusive-NOR Gate**

3.1.1 The Inverter

- Changes one logic level to the opposite level
 - **A 1 to B 0**
 - **A 0 to B 1**
- Inverter *Truth Table*

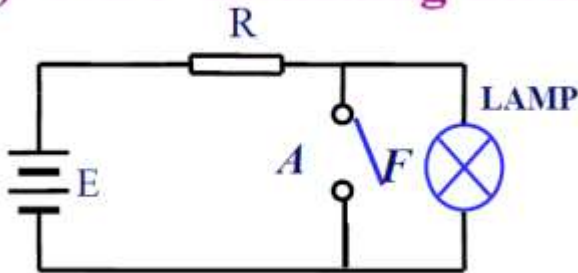
| INPUT | OUTPUT |
|----------|----------|
| Low (0) | High (1) |
| High (1) | Low (0) |

The Inverter

- Inverter *Truth Table*

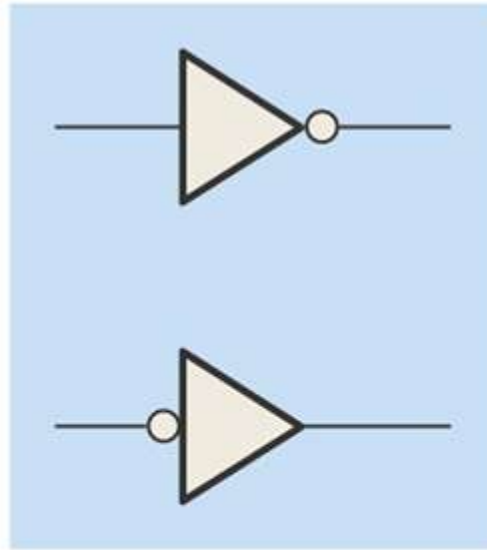
| INPUT | OUTPUT |
|----------|----------|
| Low (0) | High (1) |
| High (1) | Low (0) |

1) NOT Switching Circuit 非开关电路



$$A \begin{cases} 1 & \text{on} \\ 0 & \text{off} \end{cases}$$

$$F \begin{cases} 1 & \text{on} \\ 0 & \text{off} \end{cases}$$



Distinctive shape symbols
with negation indicators

Figure 3–1 Standard logic symbols for the inverter (ANSI/IEEE Std. 91-1984).

Inverter Operation and Timing Diagram

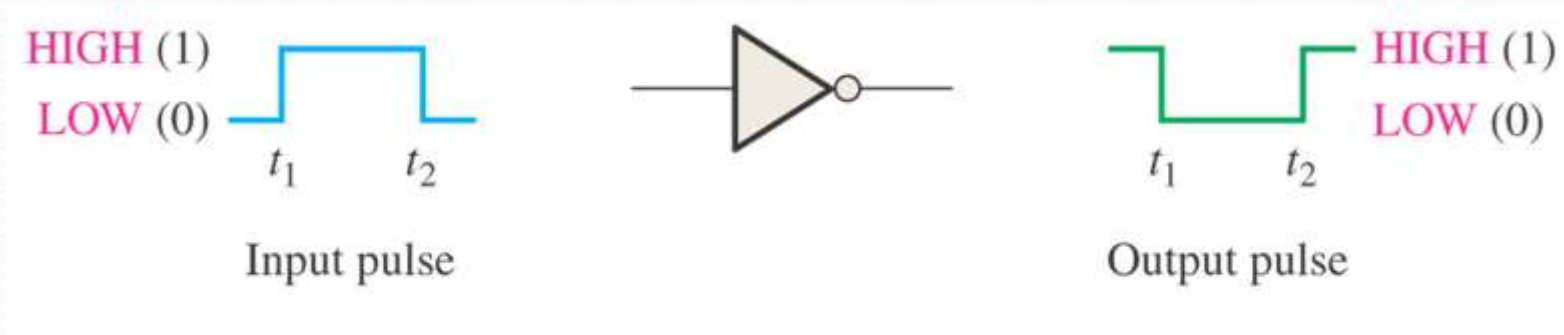


Figure 3–2 Inverter operation with a pulse input.

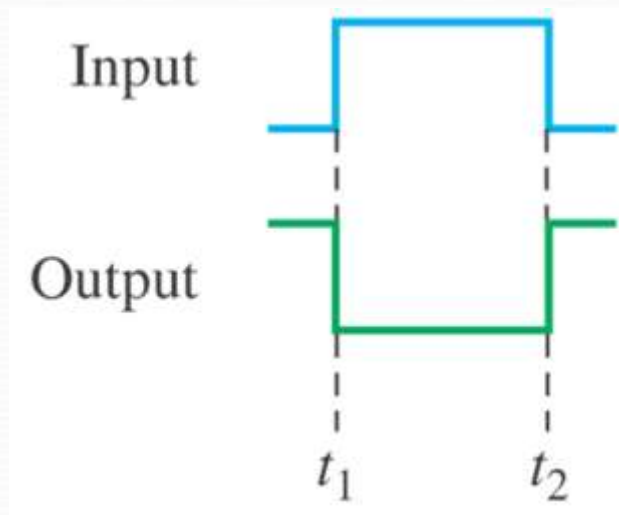
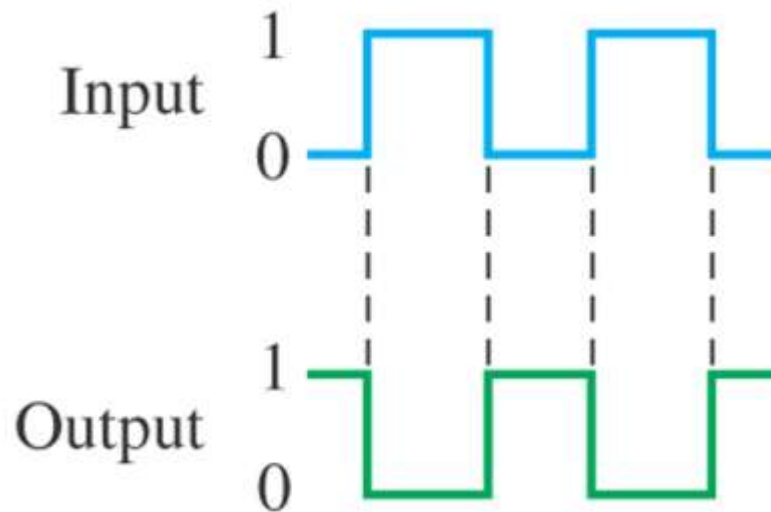
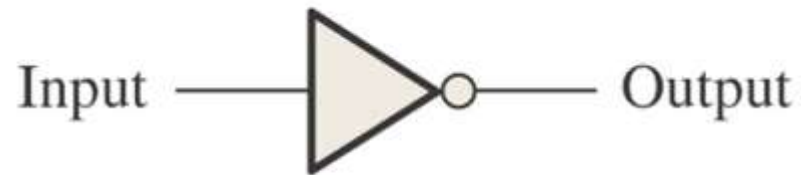


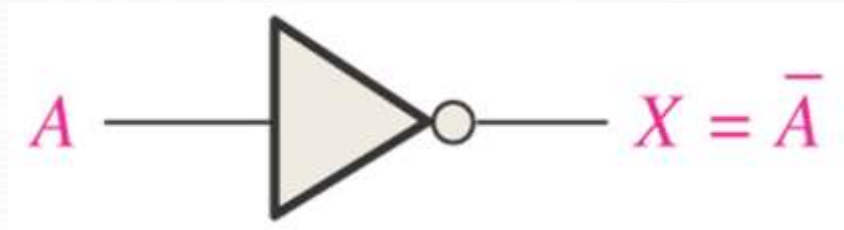
Figure 3–3 Timing diagram for the case in Figure 3–2.

Example.

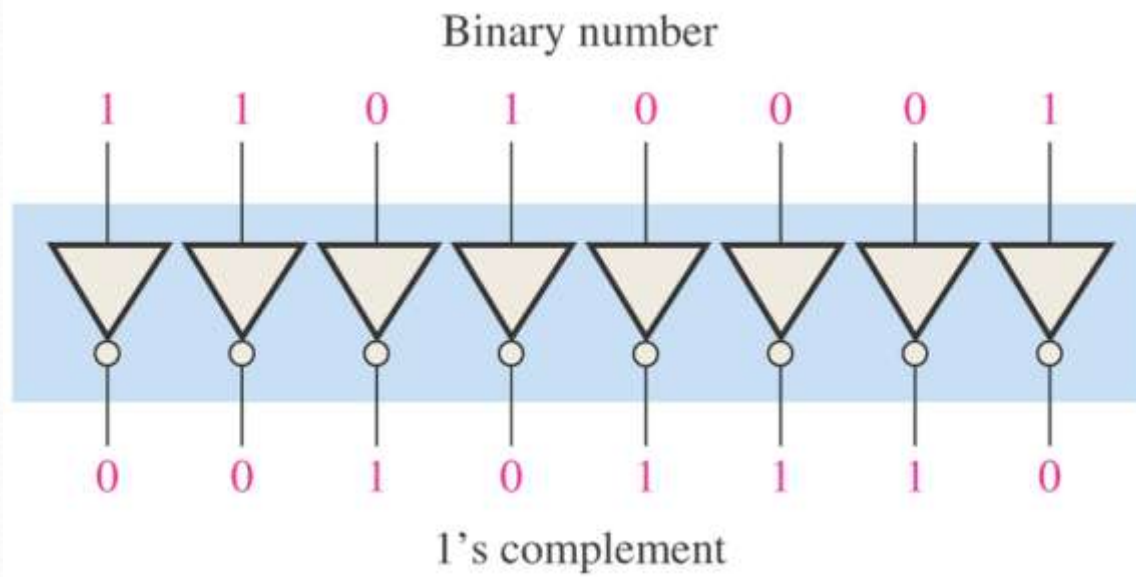
Determine the output waveform corresponding to the input and show the timing diagram.



Logic Expression for an Inverter

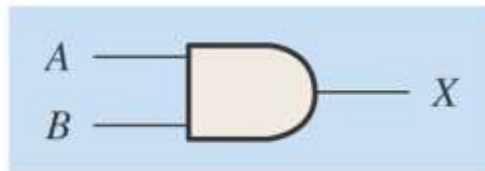


Example of a 1's complement circuit using inverters.

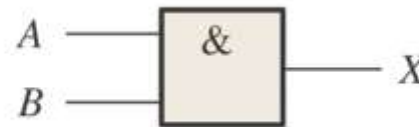


3.1.2 The AND Gate

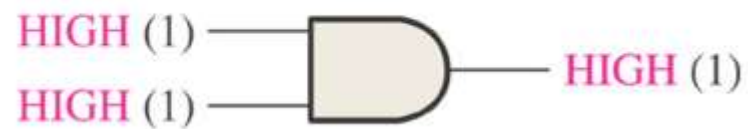
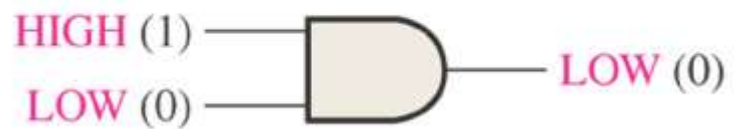
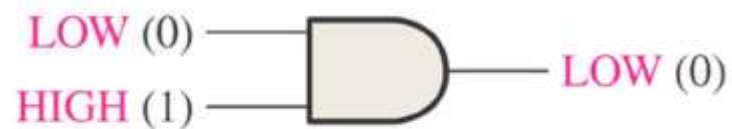
- One of the basic gates that can be combined to form any logic function
- Have two or more inputs and one output
- Produce a HIGH output only when all of the inputs are HIGH



(a) Distinctive shape



(b) Rectangular outline with the AND (&) qualifying symbol



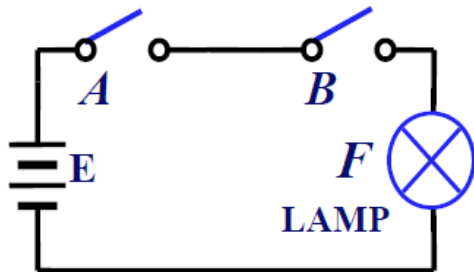
Truth Table for a 2-input AND gate

| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | X |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Truth Table for a 2-input AND gate

| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | X |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

1) And Switching Circuit 与开关电路



$$A, B \begin{cases} 1 & \text{on} \\ 0 & \text{off} \end{cases}$$

$$F \begin{cases} 1 & \text{on} \\ 0 & \text{off} \end{cases}$$

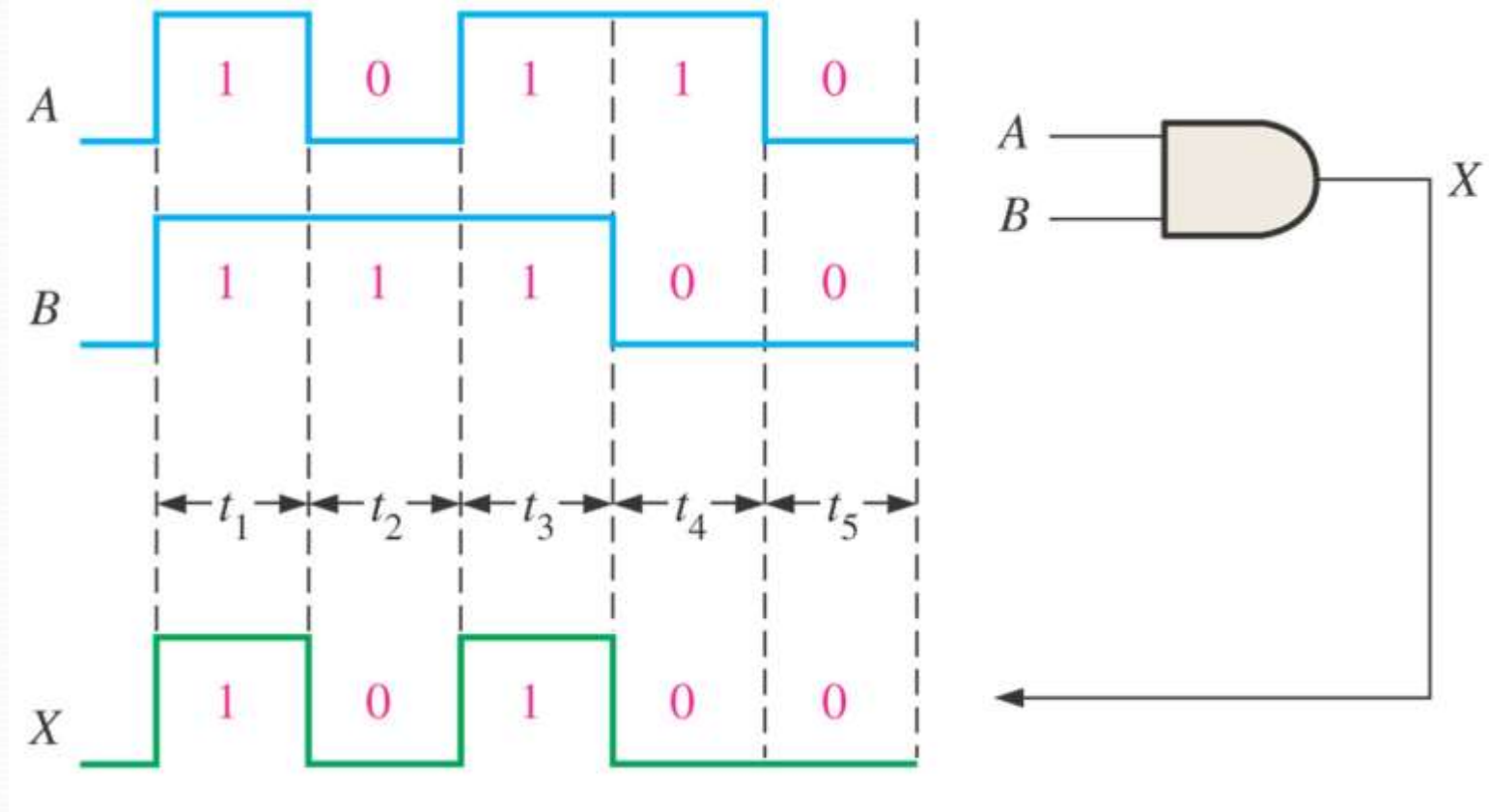
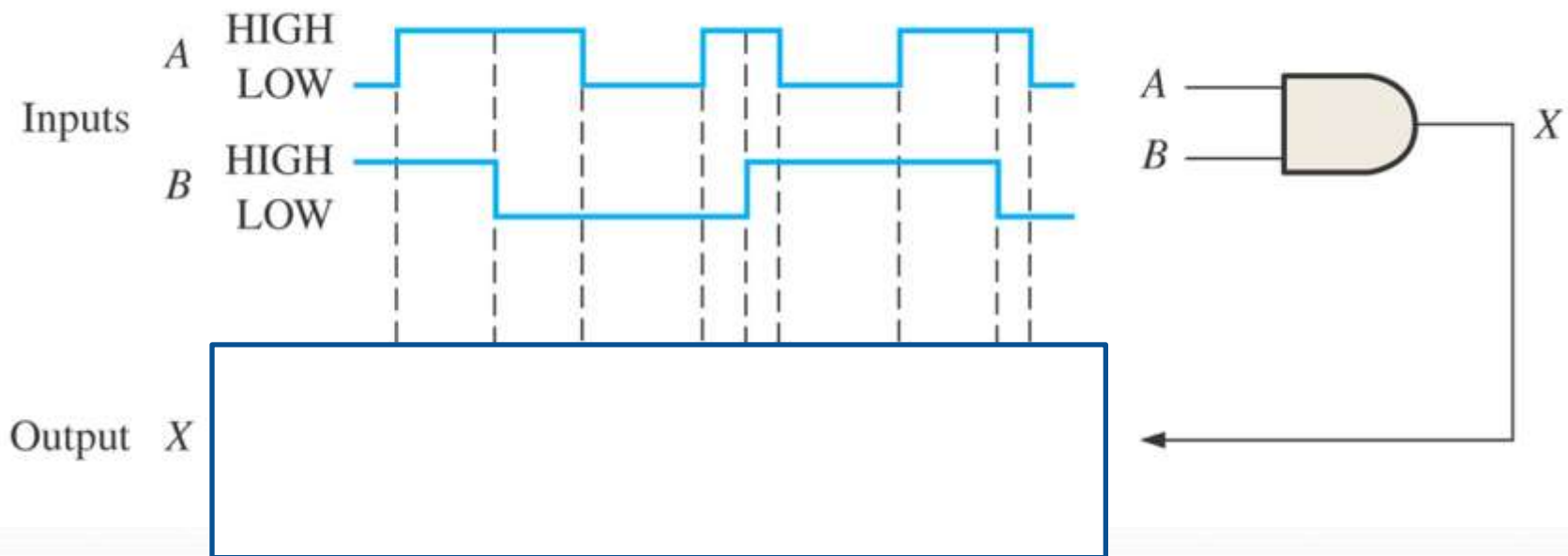


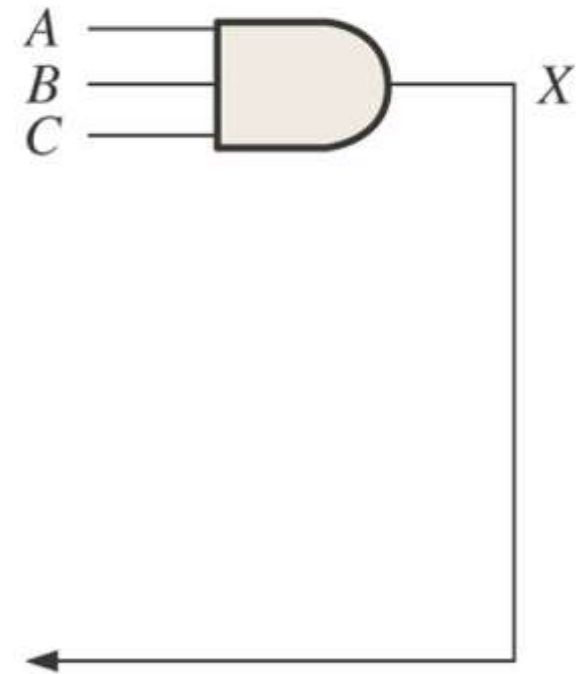
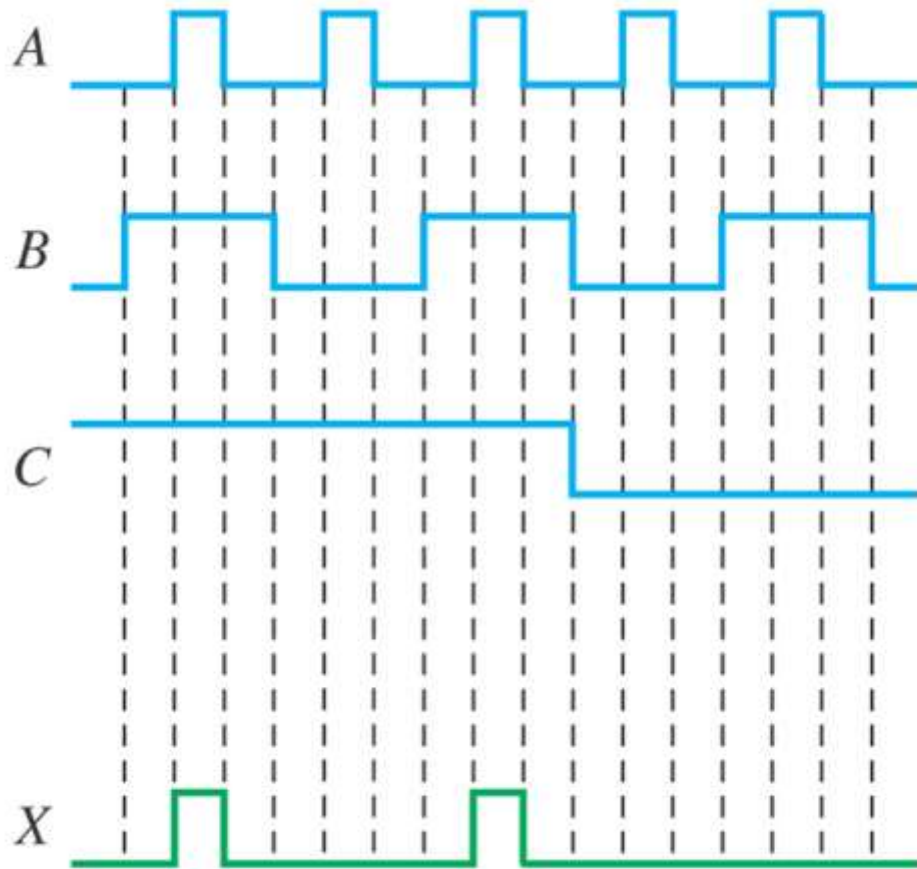
Figure 3–10 Example of AND gate operation with a timing diagram showing input and output relationships.

Example

For the two input waveforms, A and B, show the output waveform with its proper relation to the input.



Example of an AND gate with three-input



Logic Expressions for an AND Gate

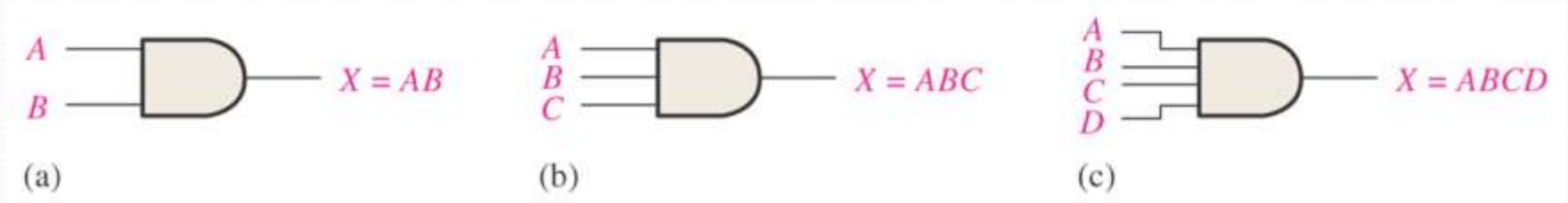
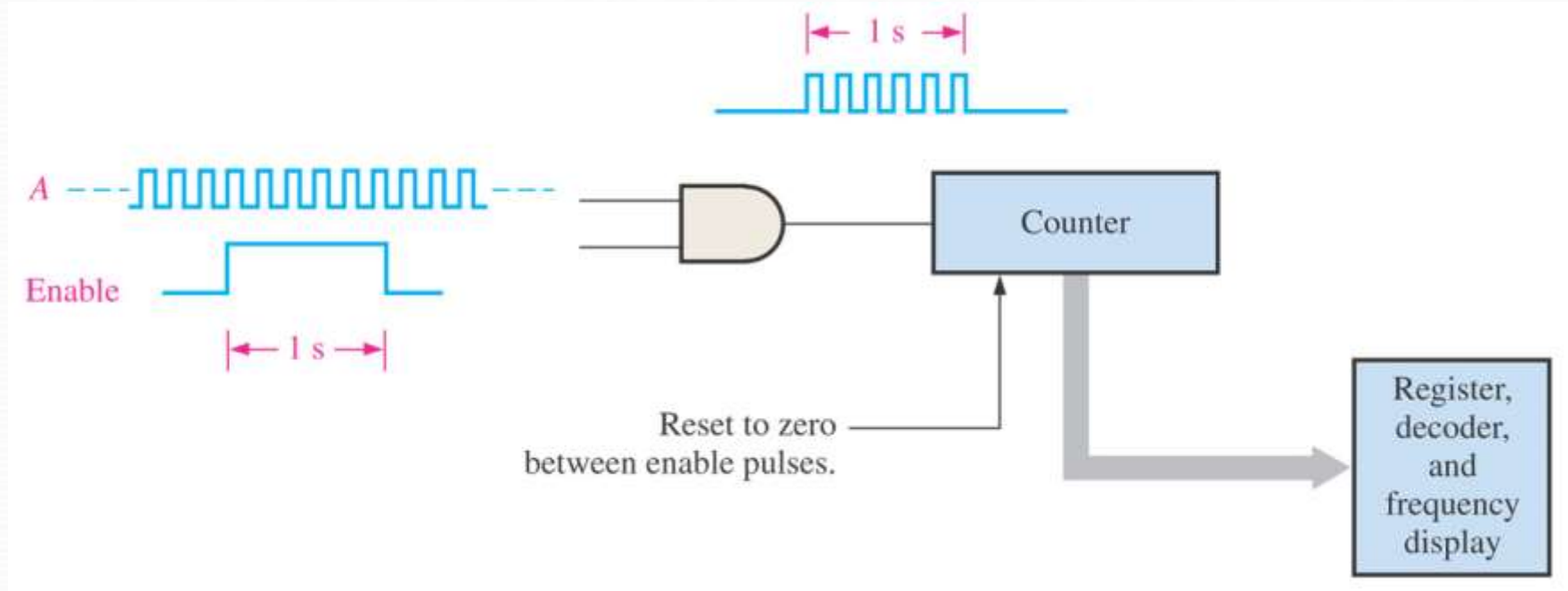
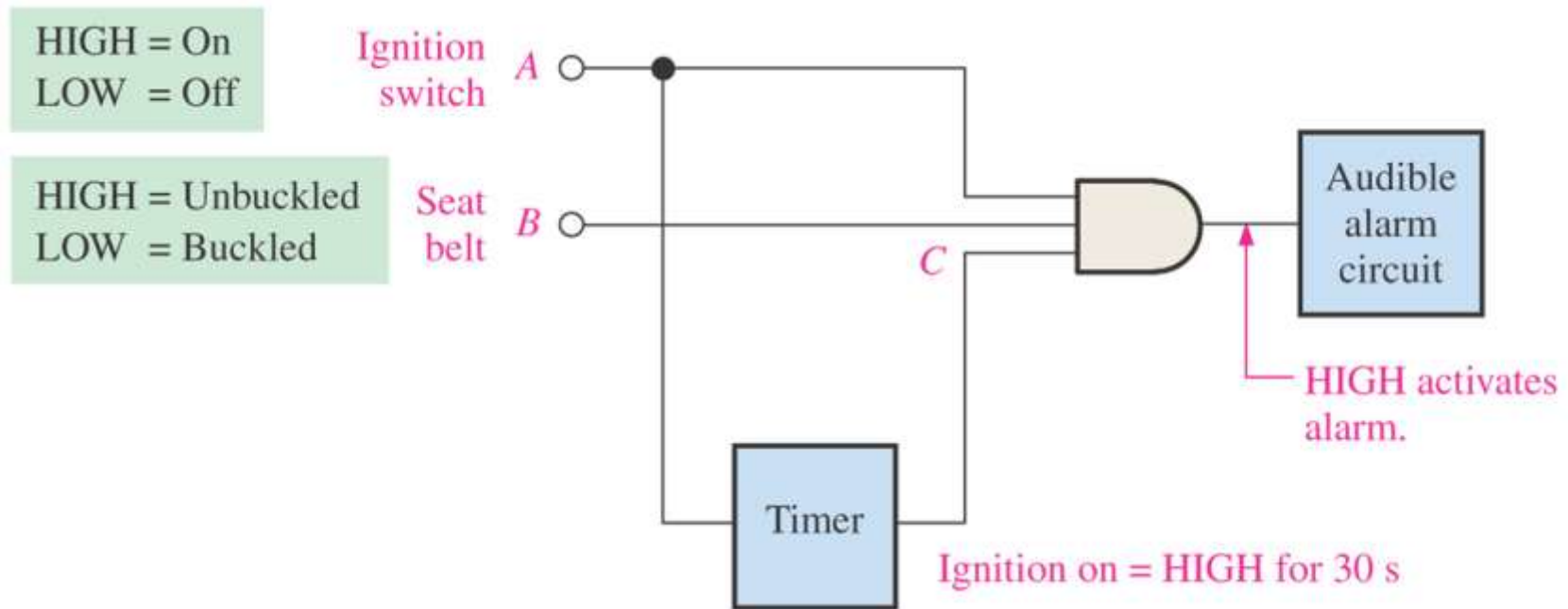


Figure 3–14 Boolean expressions for AND gates with two, three, and four inputs.

Application An AND gate performing an enable/inhibit function for a frequency counter.

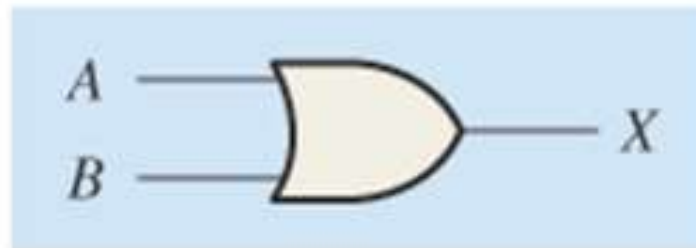


Application A simple seat belt alarm circuit using an AND gate.



3.1.3 The OR Gate

- One of the basic gates
- Have two or more inputs



(a) Distinctive shape

Operation of an OR Gate

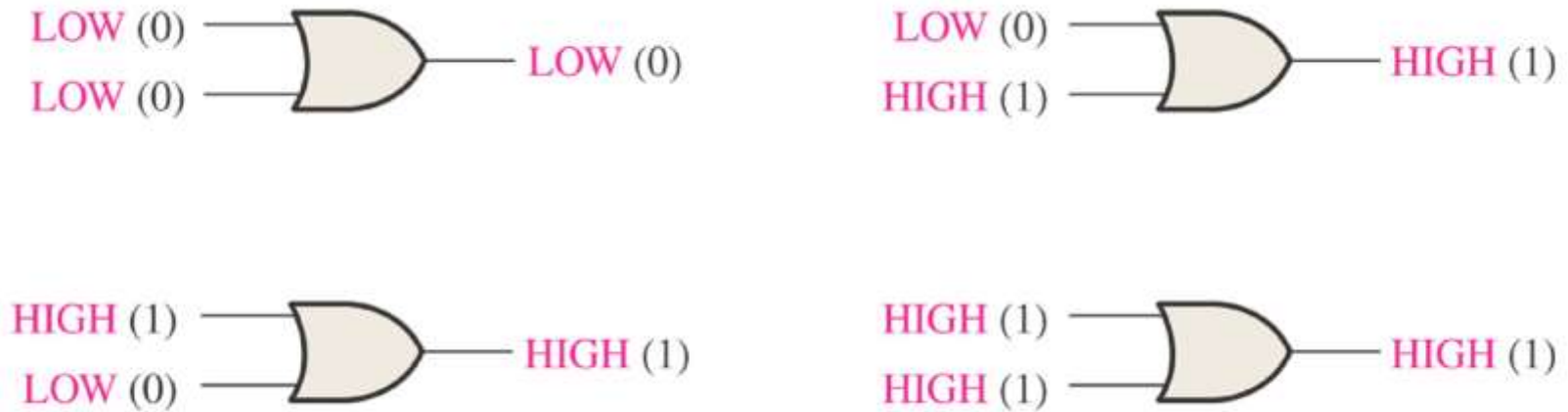


Figure 3–18 All possible logic levels for a 2-input OR gate.

Truth Table for a 2-input OR gate

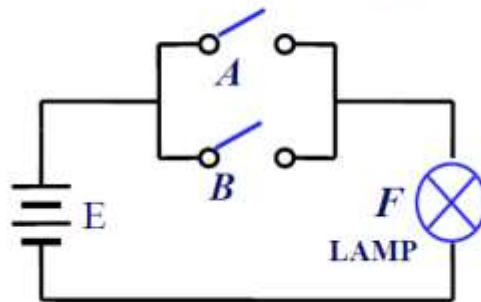
| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | X |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Operation of an OR Gate

Truth Table for a 2-input OR gate

| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | X |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

1) OR Switching Circuit 或开关电路



$$A, B \begin{cases} 1 & \text{on} \\ 0 & \text{off} \end{cases}$$

$$F \begin{cases} 1 & \text{on} \\ 0 & \text{off} \end{cases}$$

Operation with Waveform Inputs

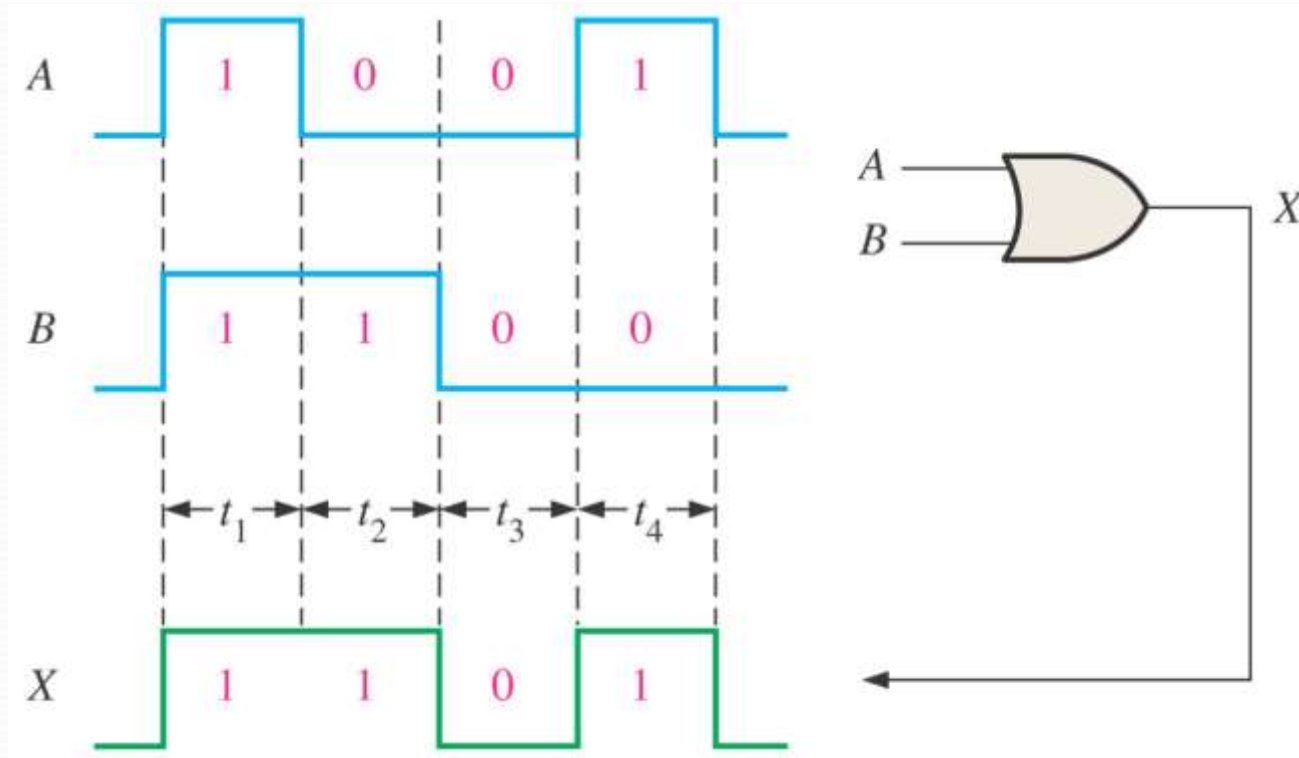


Figure 3–19 Example of OR gate operation with a timing diagram showing input and output time relationships.

Figure 3–21

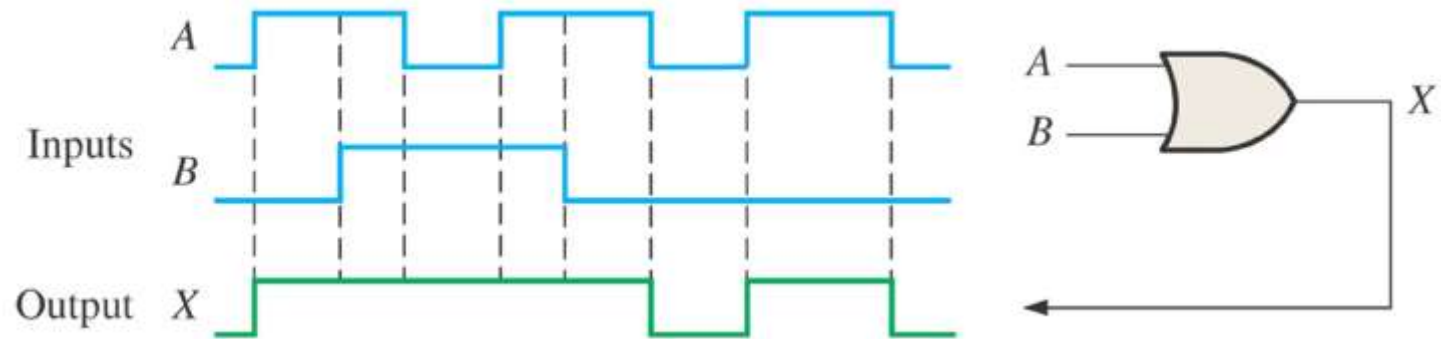
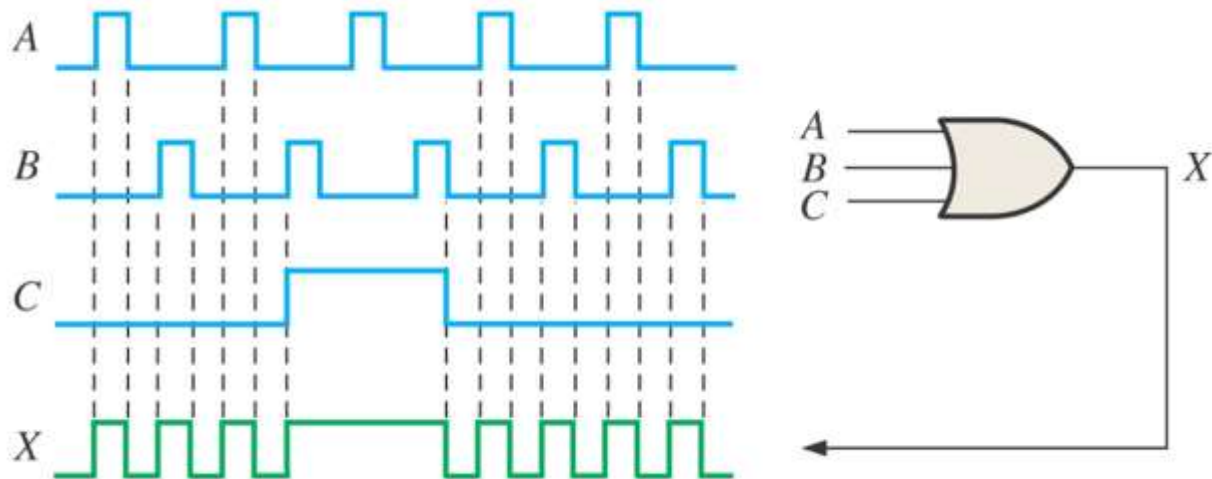
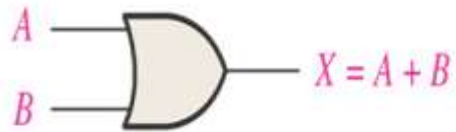


Figure 3–22



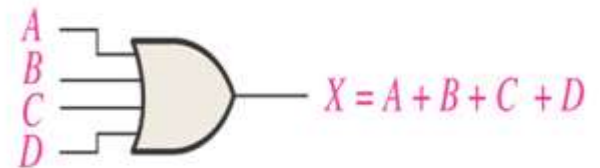
Boolean expressions for OR gates with two, three, and four inputs.



(a)

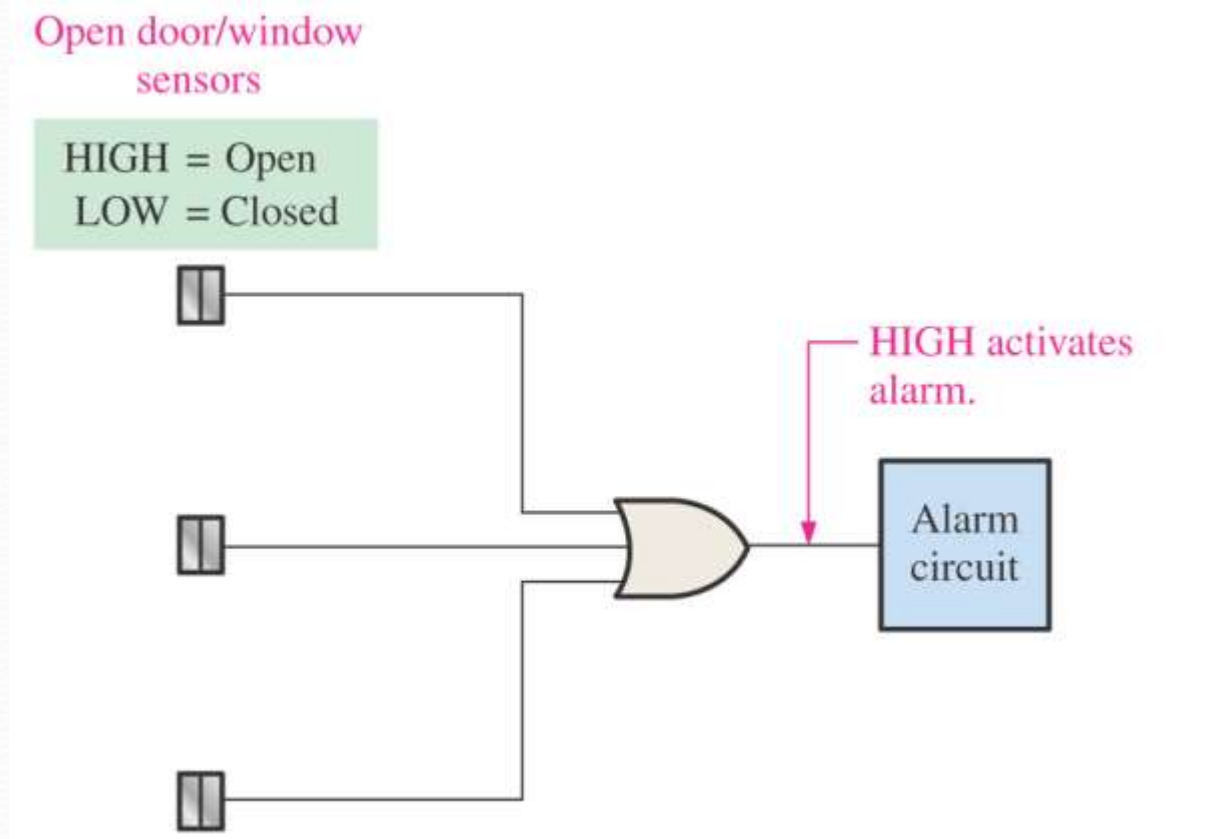


(b)

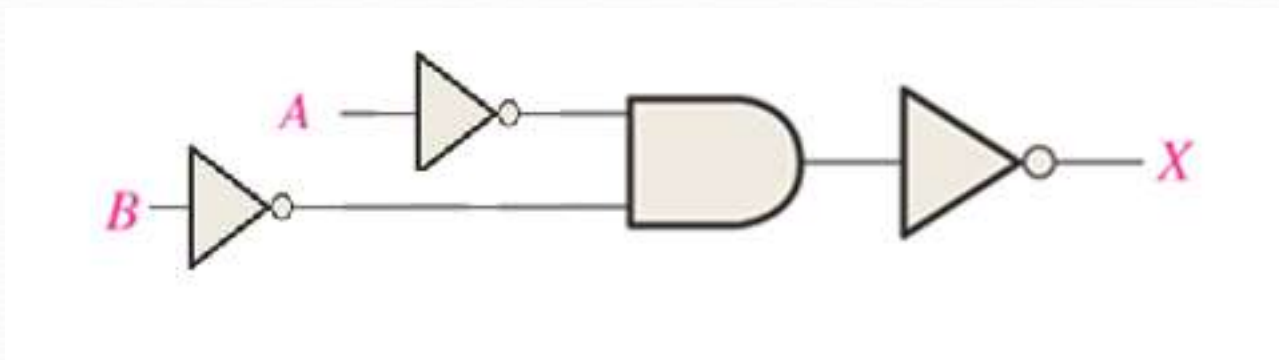
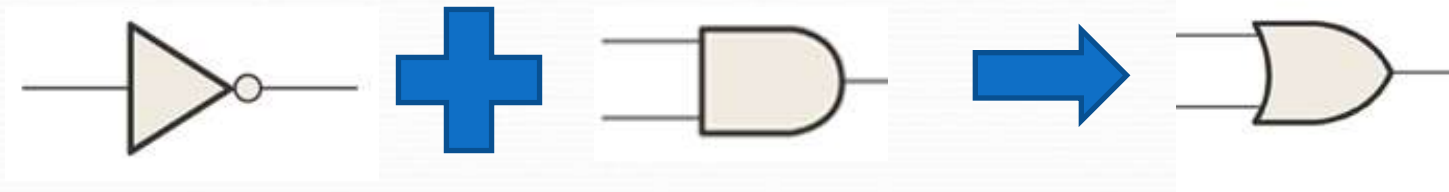


(c)

An application: A simplified intrusion detection system using an OR gate.

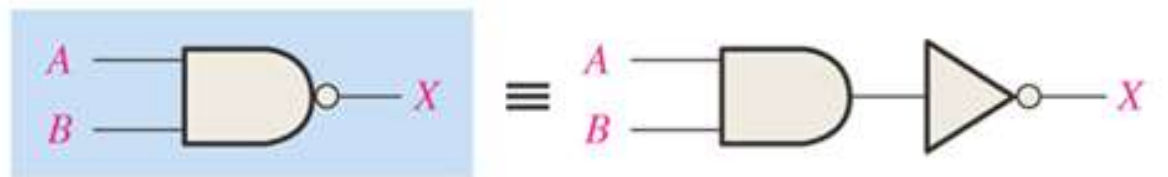


Question: Can we design OR gate using Inverter and AND gate?



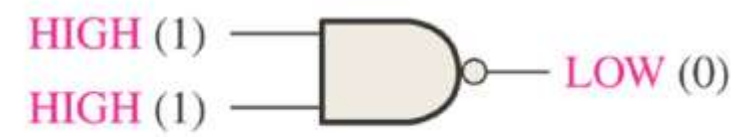
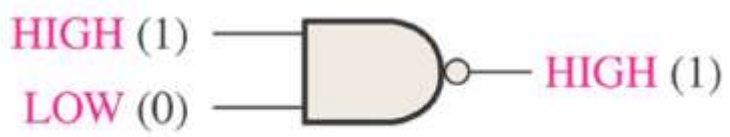
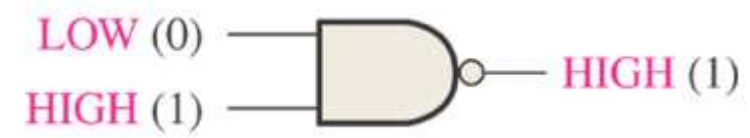
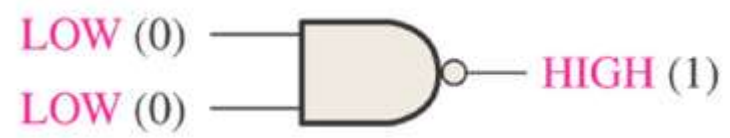
3.1.4 The NAND Gate

- A popular logic element
- Can be used in combination to perform the AND, OR, and inverter operation.

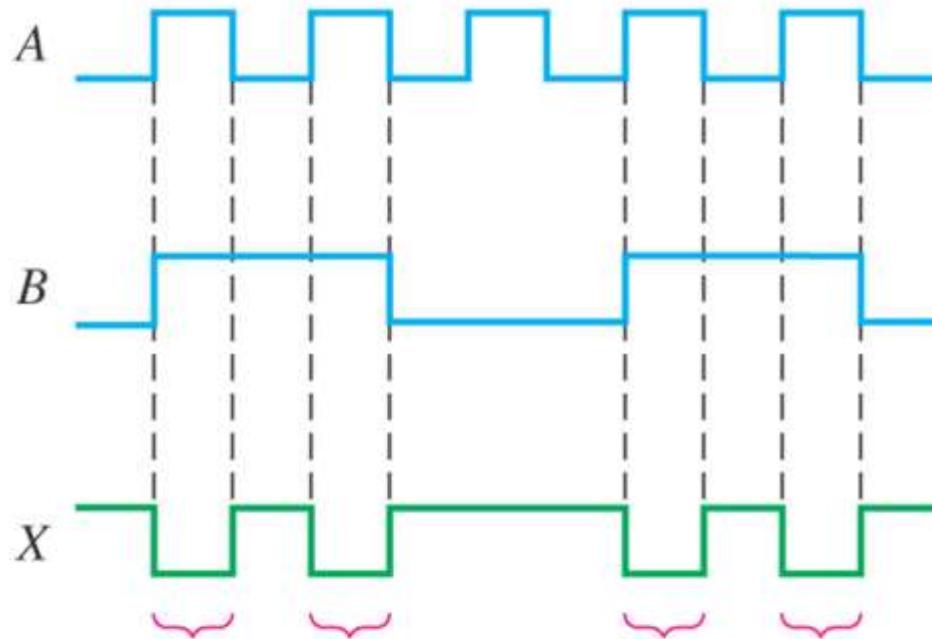


(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent

Operation of a 2-input NAND gate.



Operation with Waveform Inputs



A and B are both HIGH during these four time intervals. Therefore X is LOW.

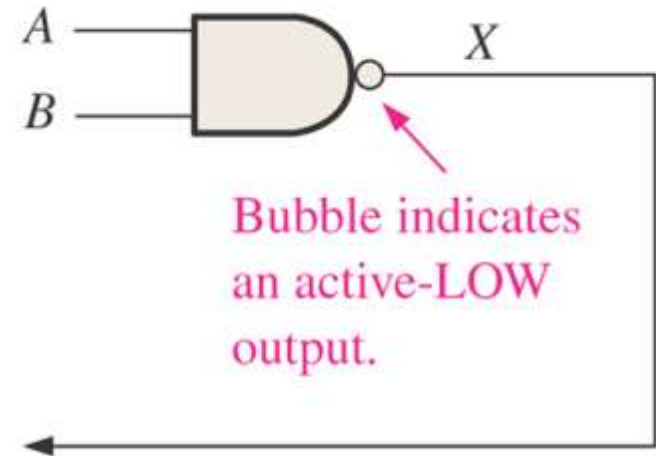
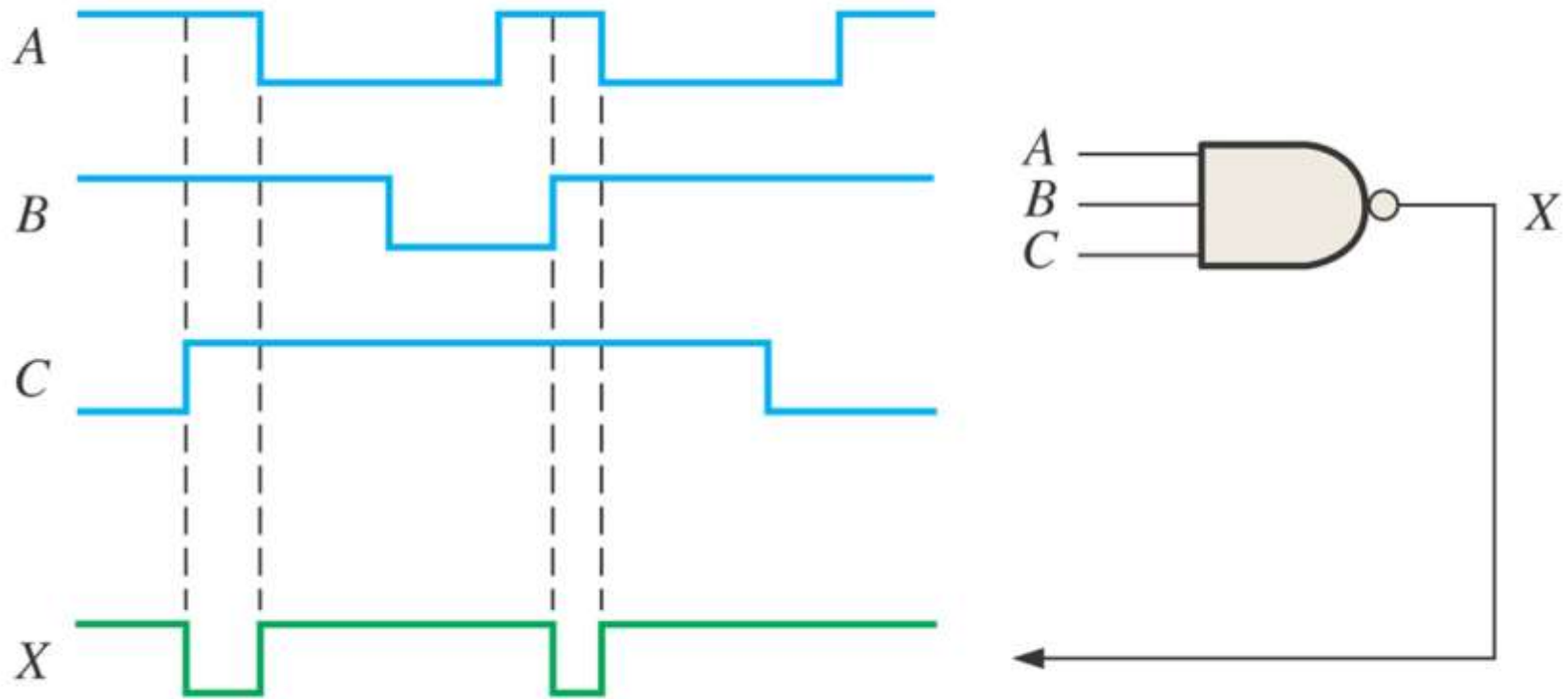


Figure 3–28



Negative-OR Equivalent Operation of a NAND Gate

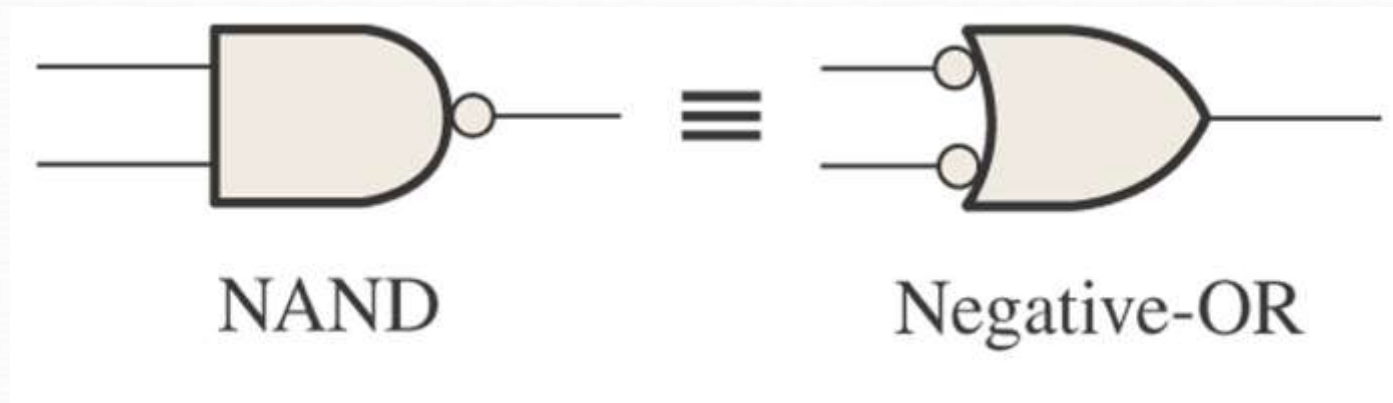


Figure 3–29 Standard symbols representing the two equivalent operations of a NAND gate.

Logic Expressions for a NAND Gate

$$X = \overline{AB}$$

Figure 3–30 An application

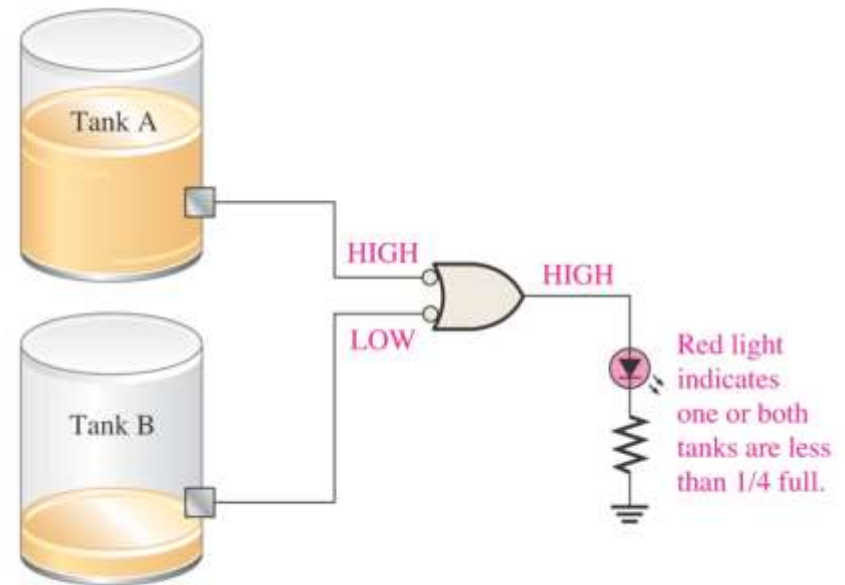
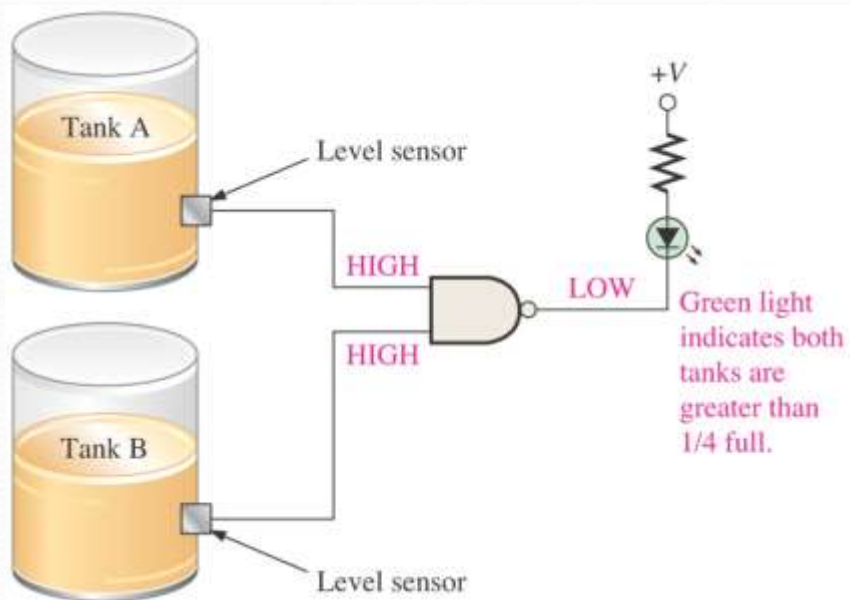
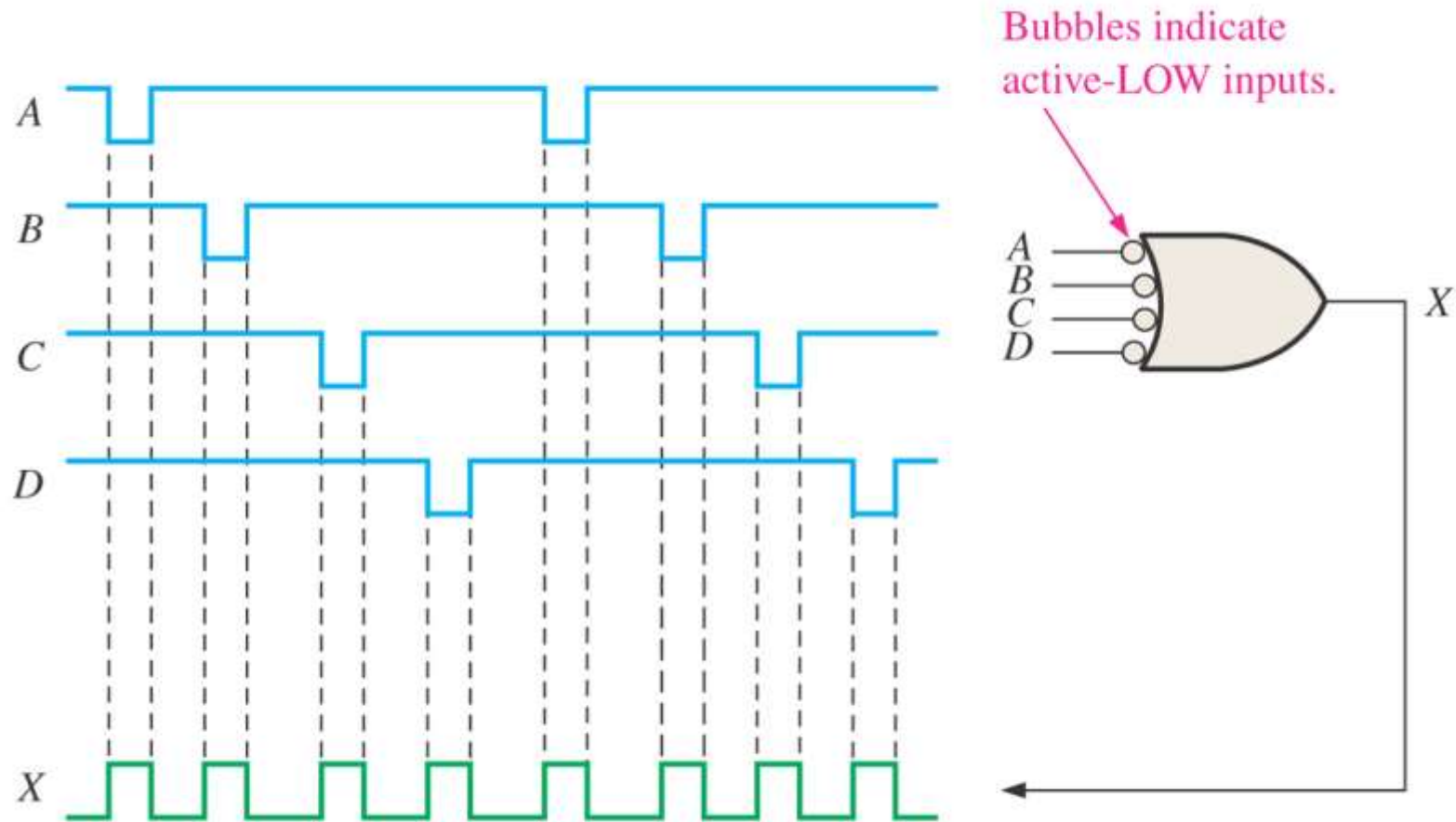
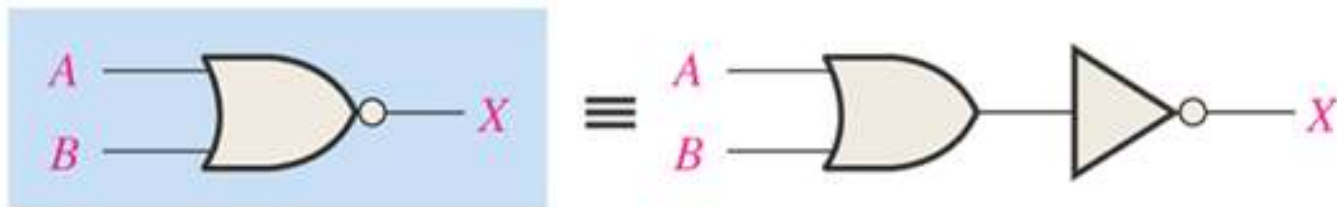


Figure 3–32 For the 4-input NAND gate, operating as a negative-OR, determine the output with respect to the inputs



3.1.5 The NOR Gate


- A useful logic element
- Can be used in combination to perform the AND, OR, and inverter operations.



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent

Figure 3–34 Operation of a 2-input NOR gate.


LOW (0) —
LOW (0) —



HIGH (1)

A 2-input NOR gate symbol with two inputs on the left and one output on the right. The output line has a small circle at the end, indicating inversion.

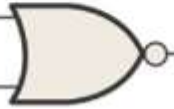
LOW (0) —
HIGH (1) —



LOW (0)

A 2-input NOR gate symbol with two inputs on the left and one output on the right. The output line has a small circle at the end, indicating inversion.

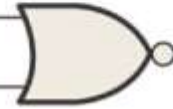
HIGH (1) —
LOW (0) —



LOW (0)

A 2-input NOR gate symbol with two inputs on the left and one output on the right. The output line has a small circle at the end, indicating inversion.

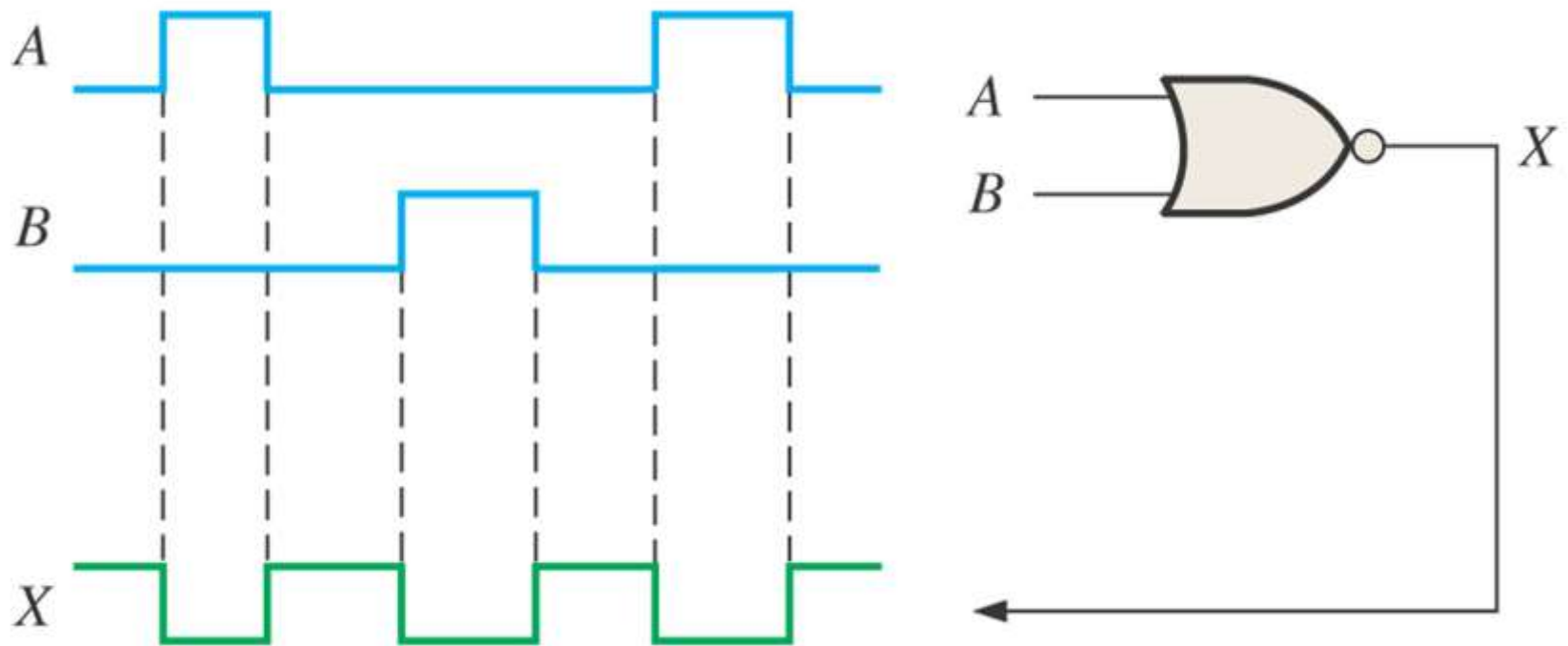
HIGH (1) —
HIGH (1) —



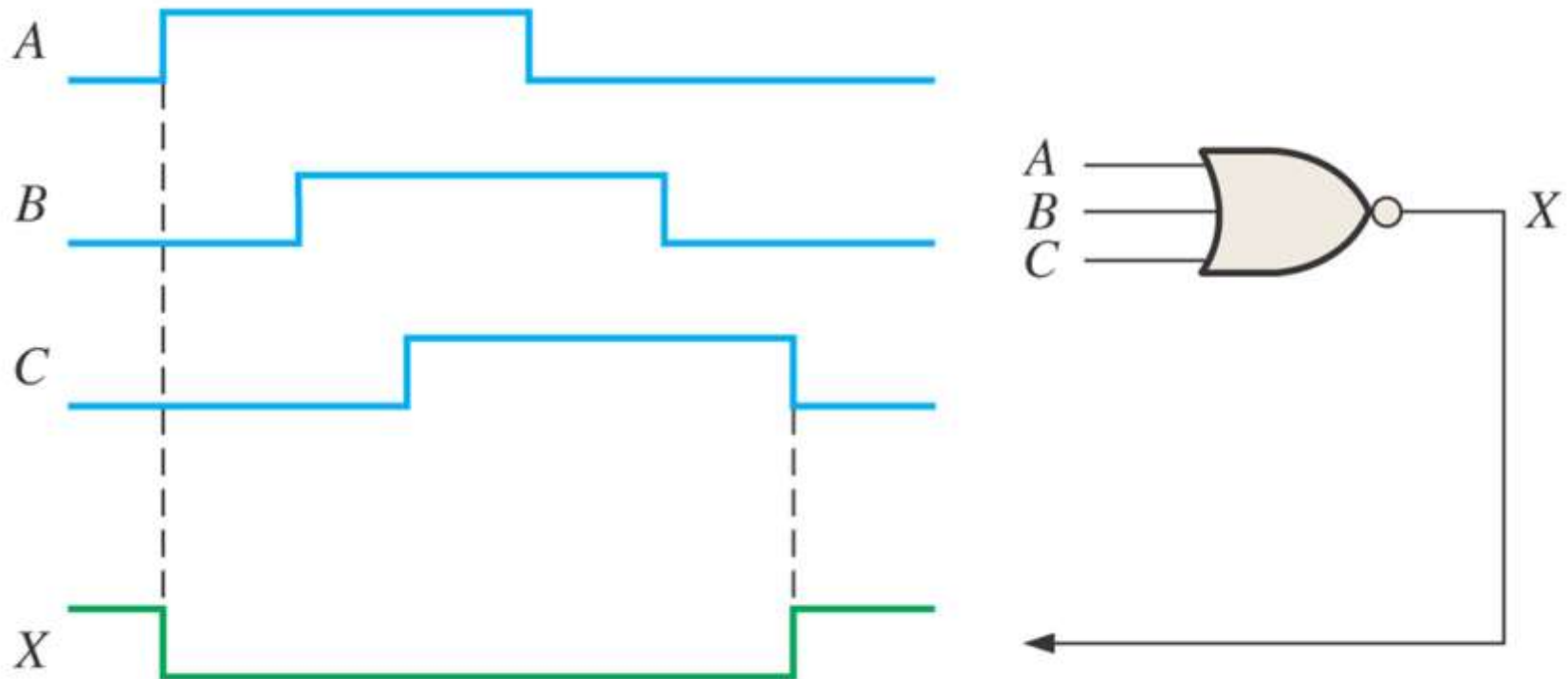
LOW (0)

A 2-input NOR gate symbol with two inputs on the left and one output on the right. The output line has a small circle at the end, indicating inversion.

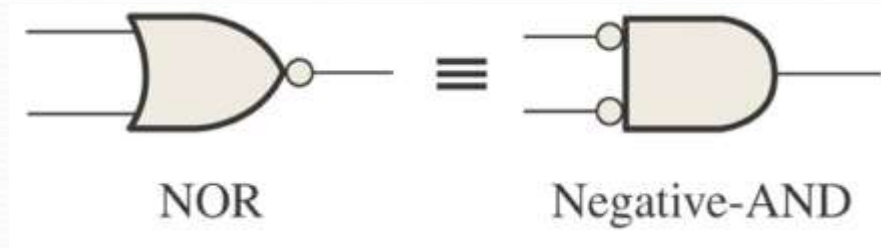
Example



Example



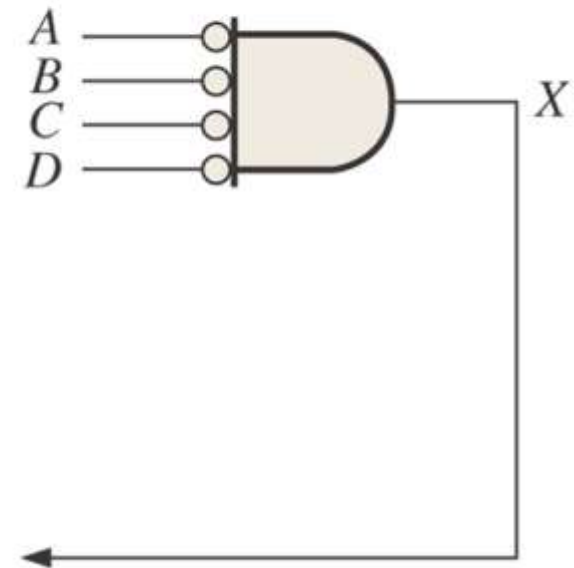
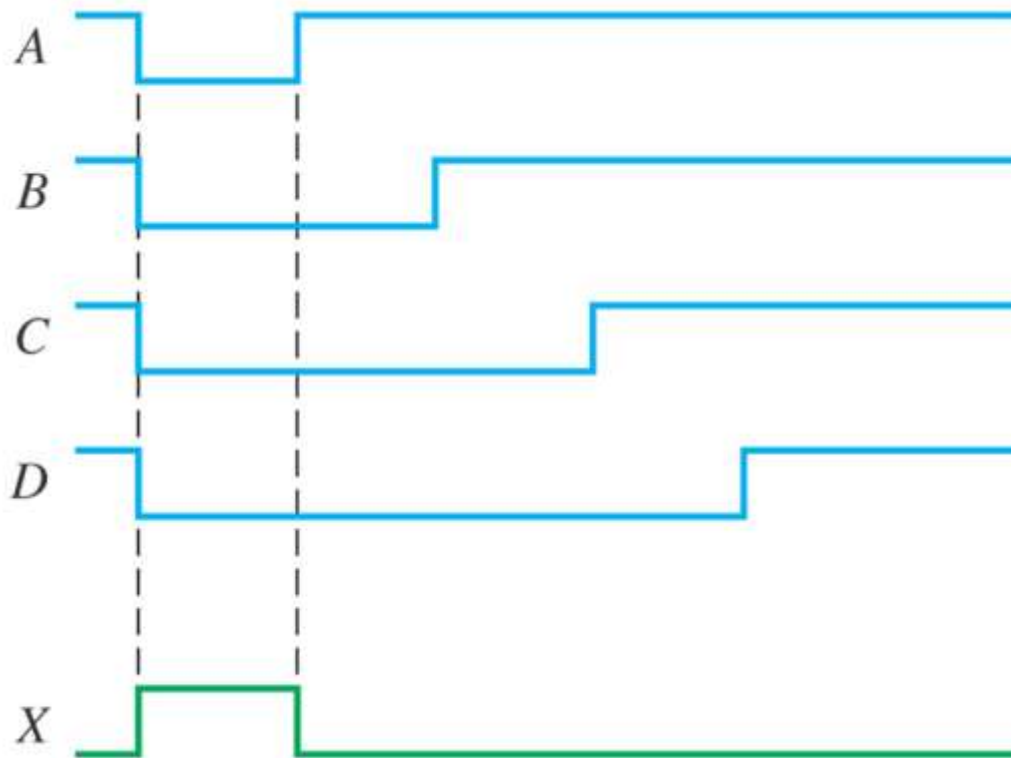
Negative-AND Equivalent Operation of the NOR Gate



Logic Expressions for a NOR Gate

$$X = \overline{A + B}$$

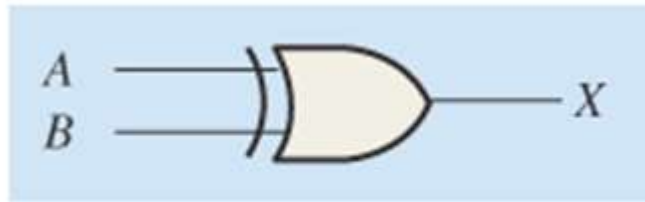
Example: For the 4-input NOR gate operating as a negative-AND, determine the output relative to the inputs.



3.1.6 The Exclusive-OR and Exclusive-NOR Gates

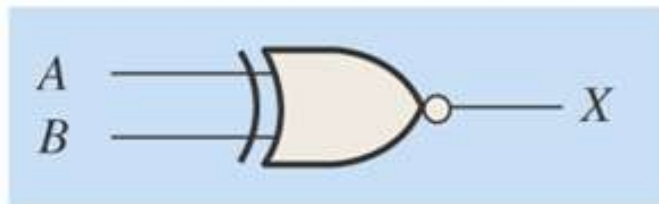
- Are formed by a combination of other gates
- Are often treated as basic logic elements with their own unique symbols

The Exclusive-OR (异或) Gate



(a) Distinctive shape

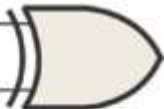
The Exclusive-NOR (异或非, 同或) gate



(a) Distinctive shape


Figure 3–42 All possible logic levels for an **exclusive-OR** gate.

LOW (0) —
LOW (0) —




LOW (0)

LOW (0) —
HIGH (1) —



HIGH (1)

HIGH (1) —
LOW (0) —



HIGH (1)

HIGH (1) —
HIGH (1) —



LOW (0)

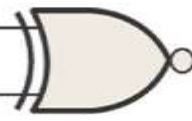
Figure 3–45 All possible logic levels for an **exclusive-NOR** gate.

LOW (0) —
LOW (0) —



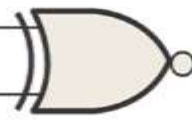
HIGH (1)

LOW (0) —
HIGH (1) —




LOW (0)

HIGH (1) —
LOW (0) —



LOW (0)

HIGH (1) —
HIGH (1) —



HIGH (1)

Figure 3–46 Example of exclusive-OR gate operation with pulse waveform inputs.

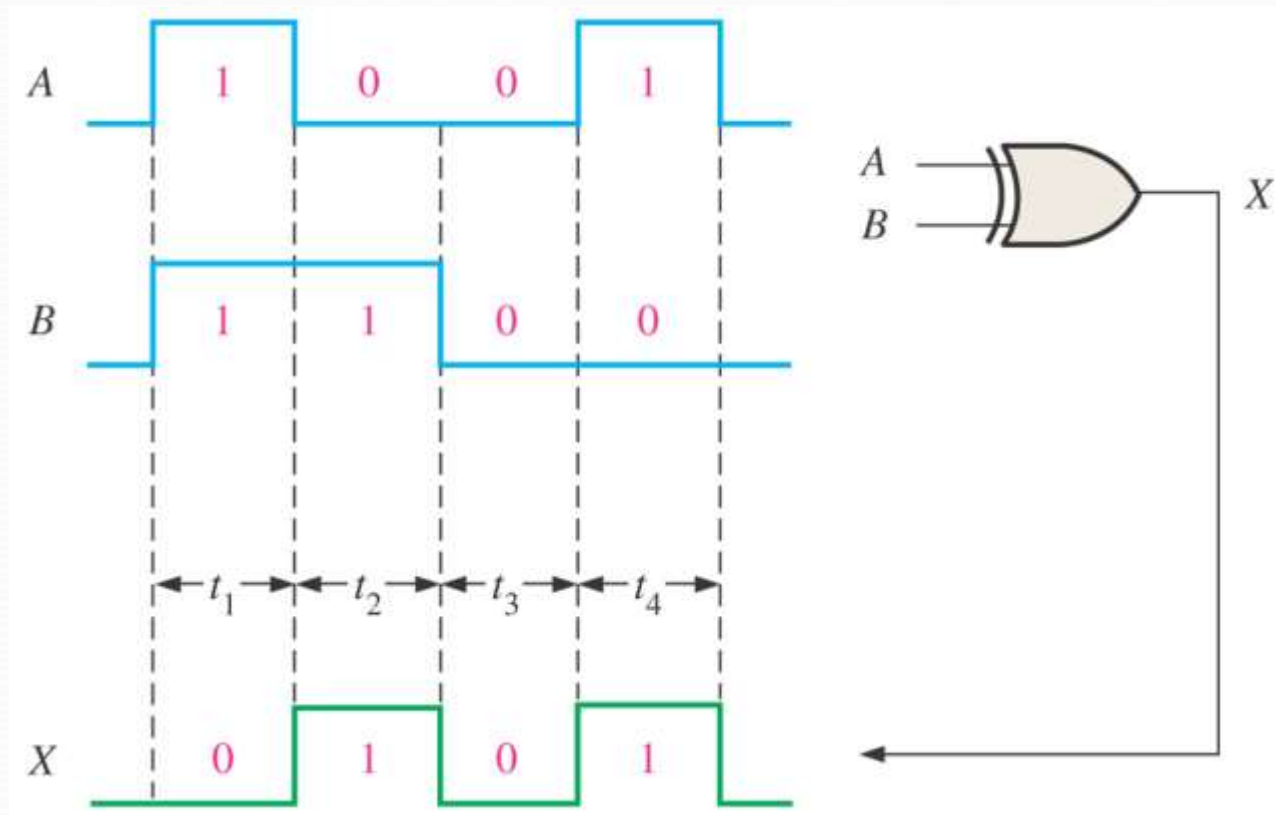
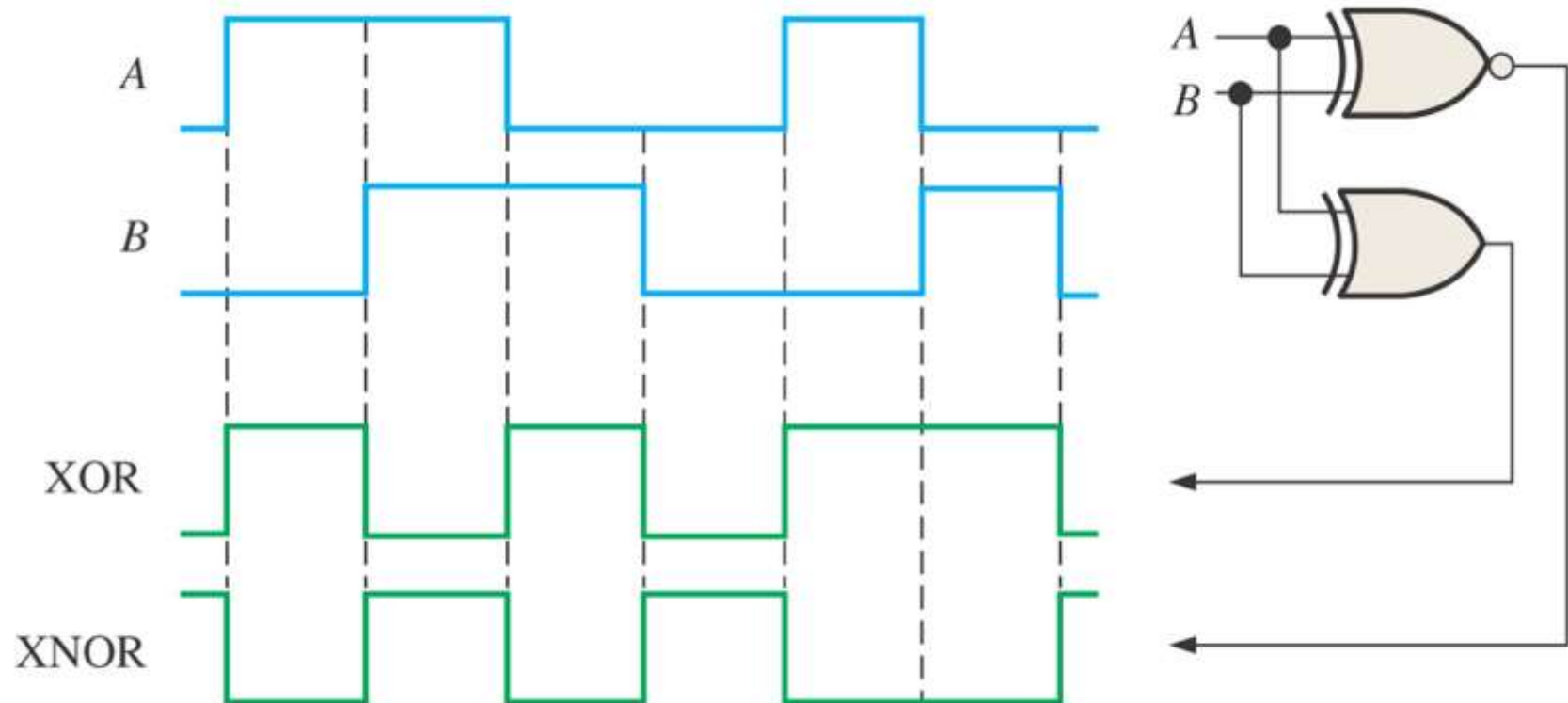
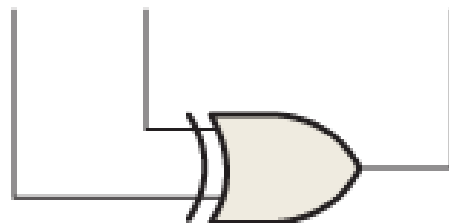


Figure 3–47

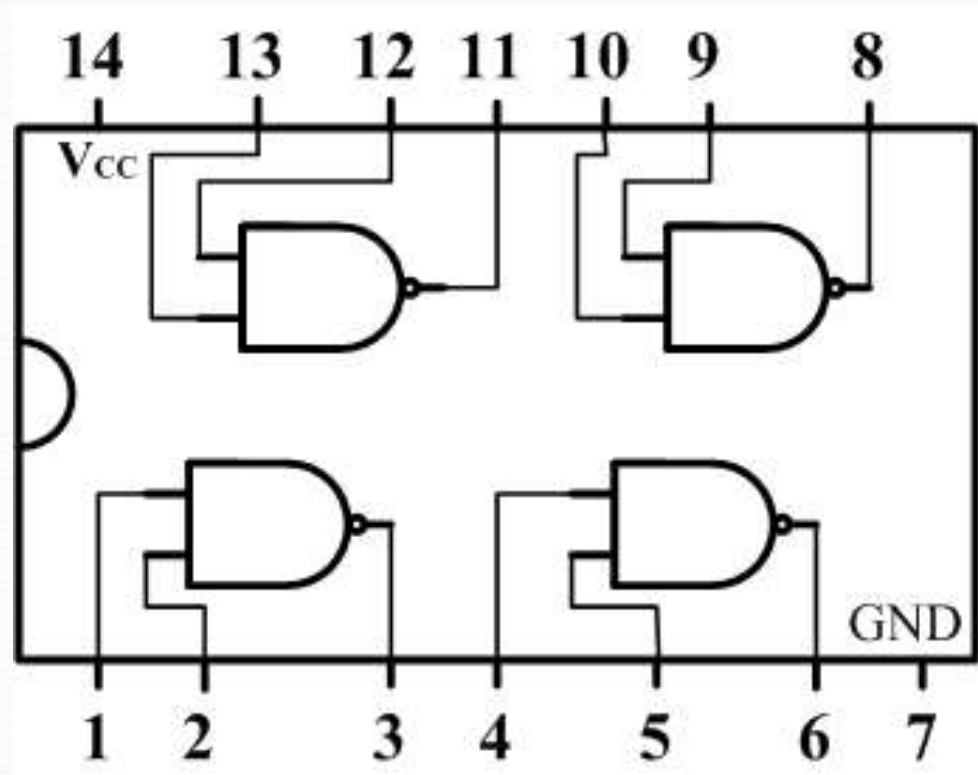


An application: An XOR gate used to add two bits.

| Input bits | | Output (sum) |
|------------|----------|---------------------|
| <i>A</i> | <i>B</i> | Σ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 (without 1 carry) |



All the logic gates introduced in this slide are commercially available in integrated circuit (IC) form.



Block diagram of 7400 IC chip

Some of the available IC gates

| IC NO. | Description | PINs |
|---------------|----------------------------------|-------------|
| 7400 | Quad 2-input NAND gates | 14 |
| 7402 | Quad 2-input NOR gates | 14 |
| 7404 | Hex inverters | 14 |
| 7408 | Quad 2-input AND gates | 14 |
| 7410 | Triple 3-input NAND gates | 14 |
| 7427 | Triple 3-input NOR gates | 14 |
| 7432 | Quad 2-input OR gates | 14 |
| 7486,74386 | Quad EX-OR gates | 14 |
| 74135 | Quad EX-OR/NOR gates | 14 |

Summary

Basic Logic Gates

- Inverter
- AND Gate
- OR Gate
- NAND Gate
- NOR Gate
- Exclusive-OR
- Exclusive-NOR Gate

HW

- Page 93~94 (11th edition)
 - 7
 - 14
 - 18
 - 20
- Page 102~104 (10th edition)
 - 7
 - 12
 - 20
 - 22