SHIFANI MANOHARAN

950 Marietta Street NW, Atlanta, Georgia E-mail: smanoharan30@gatech.edu Contact: +1-404-643-6204

OBJECTIVE

To obtain a Full-time position in Computer architecture and VLSI Design at Oracle starting January 2016

EDUCATION

Georgia Institute of Technology, Atlanta, Georgia **Expected date of graduation: December 2015**
Master of Science in Electrical and Computer Engineering ***GPA: 3.75***
Specialization*: VLSI Systems and Computer Architecture*

Relevant Coursework: GPU Architecture, Advanced VLSI Systems, High Performance Computer Architecture, Parallel and Distributed Computer Architecture, Advanced Programming Techniques, Physical Design Automation

University of Mumbai, India **August 2010-June 2014**
Bachelor of Engineering in Electronics and Telecommunication ***GPA: 3.75***

PROFESSIONAL EXPERIENCE

Intel Corporation, Austin, TX **May 2015-Aug 2015**
Design Automation Intern- Custom Design Team

Static timing analysis in the physical design flow using PrimeTime

- Understood the tool flow to perform Timing Analysis and generated reports using PT shell
- Developed new design rules in Tcl to be added in the caliber rule list for Atom CPU processors
- Tested and validated new timing report methodology for latches for both full chip and smaller blocks

MINMAX window for worst case setup and hold slack

- Developed a Perl script to generate a table with MAXMIN window for worst case setup and hold timing for every path across different corner cases
- This helped in the checking and correction of hold violations without violating the setup slack and vice versa
- Optimized the script for runtime by using multithreading

Development of scripts to automate the extraction and categorize the relevant data from the Primetime log files

- Implemented Perl and Tcl script to extract information about nets from the primetime log file and categorized them based on the slack values
- Wrote Tcl script to isolate and collect unique points in a log file and sort through them

TECHNICAL SKILLS

- **Programming languages:** C, C++, Verilog
- **Scripting Languages :** Tcl, Perl
- **Simulation software**: Cadence Virtuoso, Spectre, PSpice, LT Spice, SoC Encounter, ModelSim, PrimeTime
- **Operating Systems:** Linux, Windows
- **Digital Design and Testing:** Static Timing Analysis, Functional Verification

PROJECTS

Designed and Implemented a HARP ISA Emulator based on Harmonica GPU in C++ **Sep 2015-Oct 2015**

- Designed and built up a emulator based on the Harmonica GPU
- Implemented the entire HARP Instruction Set Architecture in C++
- Designed the whole Fetch, Decode and the Functional Units and implemented it using Classes and Structure in C++
- Handled Warp scheduling and Control Divergence along with multiple threads
- Ran the emulator for a number of Binaries and verified correctness and optimized it to reduce runtime

Implemented 2-D convolution of a given input image using CUDA programming **Aug 2015-Sep 2015**

- Read the given input image and a variable mask size and used the kernel to perform 2-D convolution
- Ensured correctness by using the CPU also to match the output of the kernel
- Optimized the kernel code to reduce the global memory accesses by using shared memory, tiling and read only memory
- Got the global accesses down to 20200 from 306500000

Custom Design of a 16X4 SRAM array with its peripherals **Sep 2015-Dec 2015**

- Designing an SRAM array along with its decoders and registers for 1Ghz clock frequency
- Designing the layout for the same and carrying out extraction and optimizing the design for low power and timing

Design of a Neural Processing Unit **Feb 2015-Apr 2015**

- Implemented of a low power hardware accelerator, NPU
- Conducted a comprehensive study of the different technique to implement the Sigmoid Unit
- Developed a parameterized sigmoid unit in Verilog using look up tables to include activation functions like Gaussian
- Implemented a test bench for the NPU identifying different corner cases to test the functionality and simulated the RTL design using Modelsim

Parallel programming of 2-D DFT using MPI **Sep 2015-Oct 2015**

- Implementing distributed 2-D Discrete Fourier Transform and Inverse Transform using pthreads and barriers
- Barriers are implemented to synchronize the threads
- Implementing the Danielson–Lanczos Lemma to reduce the complexity of the computation to $N\log_2 N$

Bounded Radius Routing Algorithm **Mar 2015-Apr 2015**

- Developed a BPRIM and BRBC routing algorithms in C/C++ aiming runtime optimization
- Developed a GUI using Matlab to demonstrate and observe the actual routing for given circuits
- Implemented a modification of the BRBC algorithm with better or equal results for most benchmarks

Superscalar Pipelined Processor using Tomasulo Algorithm **Sept 2014-Oct 2014**

- Designed a simulator of superscalar processor that uses the Tomasulo algorithm to implement out-of-order execution pipelining in C++
- Simulated various configurations of out-of-order machine and carried out tests on various data traces

Cache Coherence Simulator **Nov 2014-Dec 2014**

- Designed a simulator in C++ that maintained cache coherence for multi core system using bus based snoopy protocols
- Implemented the MSI, MESI, MOSI, MOESI and MOESIF protocols
- Carried out analysis of different multi-processor configurations using the simulator and determined the most apt protocol based on type of data sharing pattern

Cache Simulator **Aug 2014-Sept 2014**

- Developed an optimized cache simulator implementing L1 cache, prefetching and victim cache in C
- Carried out experimentation for various cache configuration on data trace files and determined the most suitable configuration giving minimum Average Access Time

Custom Design of a 4 tap FIR Filter Design in Cadence Virtuoso **Oct 2014-Dec 2014**

- Developed a cell library by designing schematic and layout of basic gates (NAND, NOR, XOR, NOT, D Flip Flop)
- Implemented a 4 tap FIR filter using the cell library developed above and simulated it using Spectre
- Designed the layout of the Adder and Multiplier used in the FIR filter and cleared DRC and LVS checks
- Optimized the filter for minimum delay
- Performed sleep-gating on the circuit to minimize the power consumption

Parallel programming of 2-D DFT using MPI **Aug 2015-Sept2015**

- Implemented distributed 2-D Discrete Fourier Transform and Inverse Transform using Message Passing Interface in C++
- Point to point communication was used for message passing and synchronized using barriers

INTERESTS AND ACTIVITIES

- Sports' Secretary of the TSEC College Student Council and Captain of the college soccer team for the year 2013-14
- As Sports Secretary organized a national level sports festival and headed a committee of 50 students that involved collection of funds, marketing, publicity
- Part of the NGO, 'Save Our Soul', India since its induction, teaching deaf and mute children to handle technology