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Systematic and Random Defect Control with Design Based Metrology

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ABSTRACT

As technology node of memory devices is approaching around 30nm, the process window is becoming much narrower and production yield is getting more sensitive to tiny defects which used to be not, if ever, so critical. So it would be very hard to expect the same production yield as now in near future.
It is possible to classify wafer defects into systematic and random defects. Systematic defects can be also divided into design related and process related defects. Narrow process window, generally, is thought to be the source of these systematic defects and we have to extend process window with Design for Manufacturing (DFM) and control process variation with Advanced Process Control (APC) to ensure the production yield.
The sensitivity of random defects, however, has something to do with the smaller design rule itself. For example, the narrower spaces between lines are subject to bridge defects and the smaller lines, to pinch defects.
Die to data base (DB) Design Based Metrology (DBM) has mainly been in use for detecting systematic defects and feedback to DFM and APC so far. We are trying to extend the application of DBM to random defects control. The conventional defect inspection systems are reaching its highest limit due to the low signal to noise ratio for extremely small feature sizes of below 40nm. It is found that Die to DB metrology tool is capable of detecting small but critical defects with reliability.

In this paper, we explore the possibility of controlling random defects as well as systematic defects with Die to DB metrology and the results are presented in detail.

Key words: Design Based Metrology, Systematic defects, Random defects

1. DESIGN BASED METROLOGY TOOL

A die to data base (DB) inspection system which can compare the pattern on wafer to the design layout has been developed. NGR2100^{TM} can compare the real printing images with designed target layout and measure the CD of all the features in a chip. It consists mainly of two parts, the hardware to acquire wafer images and the software to compare wafer images with CAD layout and analyze the edge placement error. The former is called Electron Image Acquiring System (EIAS) and the latter, Geometry Verification Engine (GVE).

The key feature of EIAS is the high-resolution and high-speed secondary electron acquisition capability to acquire images without field distortion over wide scan field. GVE compares the target GDS layout with SEM images acquired at EIAS and measures the displacement of the edge of SEM images from the target GDS layout.

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Considering corner rounding of real feature images, the target GDS layout is converted into reference geometry. The displacement of the edge of SEM image from the reference geometry is called a bias and this bias is calculated pixel-by-pixel and can be compared with the criterion defined by the user. The measurement flow using NGR2100^{TM} is illustrated in Fig. 1.

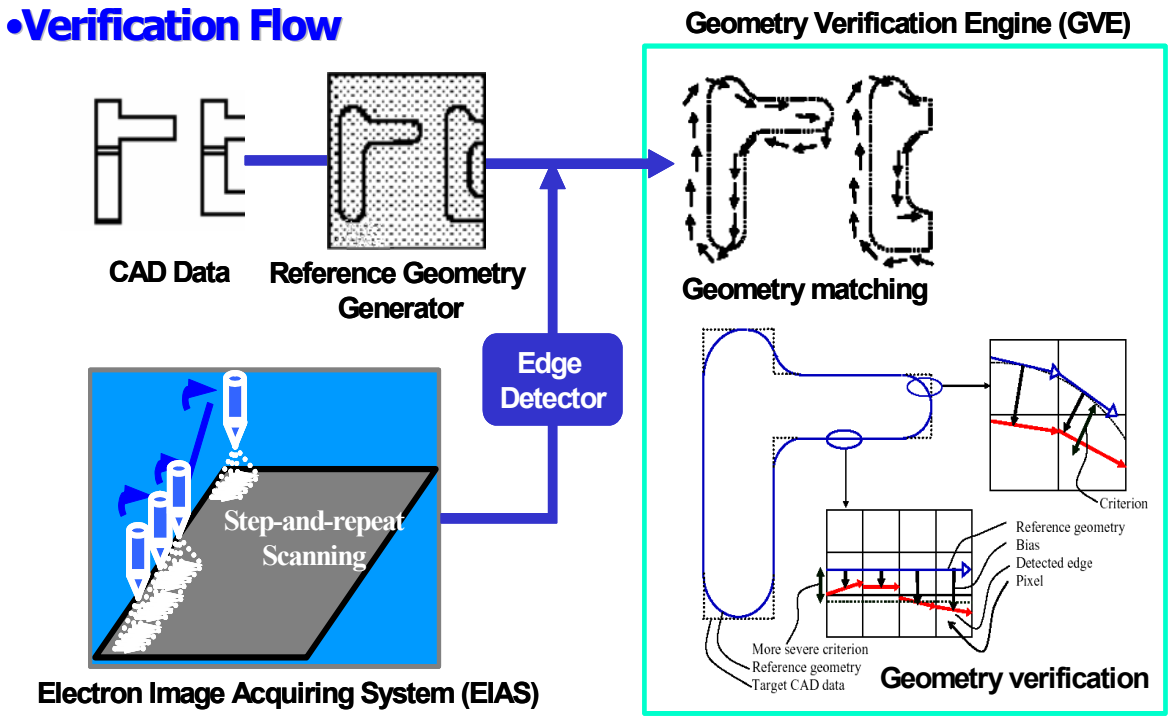

Figure 1. CD Verification flow of NGR2100^{TM}

There are two types of inspection modes in NGR2100^{TM}. One is CGV (Critical Geometry Verification) mode which corresponds to a fast 2-dimensional GDS SEM and measures all the CD values in the inspection area with high accuracy. CGV mode is used as a verification tool for the hot spots which simulation predicted in MBV step or for the precise CDU analysis of some specific features.
The other is RDI (Repeated Defect Inspection) mode which detects repeated defects in a full chip with higher throughput. If the distance between detected edge and a line of the reference geometry exceeds a certain criterion, it is recognized as a defect having edge placement error. With RDI mode, all the systematic defects in a full chip can be identified. So, RDI mode is used as a verification tool for the unpredicted hot spots by simulation.

2. SYSTEMATIC DEFECT CONTROL

The layout of typical DRAM chip is illustrated in Fig. 2, which is composed of cell, core and peripheral area. The cell layout has rather simple and periodic but very small sized features. The core layout has 2-dimensional complex features with a little bit larger than cell features. The peripheral layout has totally random but large sized features. Since the feature size and complexity differ in each area, random defects also have different impacts on each area respectively.

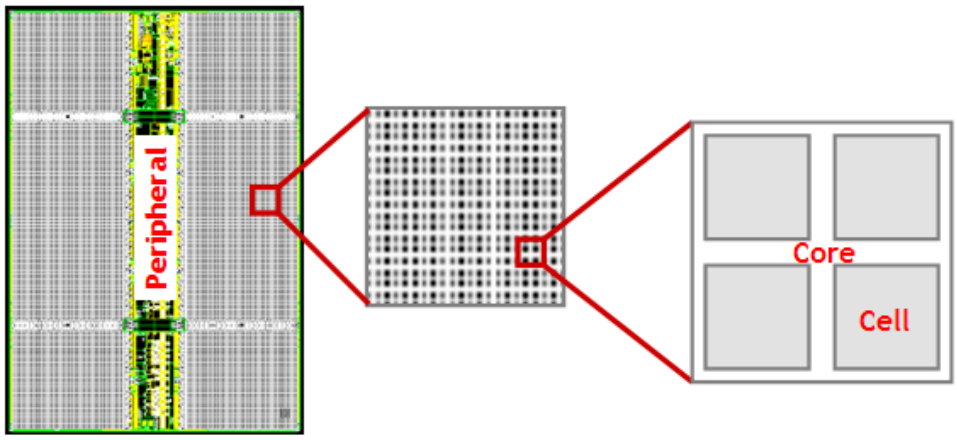

Figure 2. The layout of typical DRAM chip

It is possible to classify wafer defects into systematic and random defects. Systematic defects also can be divided into two categories, design related and process related defects. Since designers are not well aware of lithography technology, when drawing some layouts, they just follow the design rules provided by lithography process engineers. However, the design rules generally contain the minimum requirements for layout drawing and cannot cover all the complex 2-dimensional features in a full chip. That's why Design for manufacturing has been proposed for optimizing layouts for wider process window.

As technology node of memory devices is approaching the minimum resolution limit of ArF immersion lithography, the maximum NA of lens over 1.30 and various resolution enhancement technologies are required for the process. As a result, the process window is, however, becoming much narrower. In addition, the shrink of design rule also increases the difficulty of other processes and the integration of them for memory devices. The narrow process window of lithography and the increased difficulty in other processes are thought to be the main cause of process related systematic defects.

2.1 Process Window Qualification

Process Window Qualification is a useful method to detect systematic defects caused by narrow process window. The full chip inspection capability of NGR2100^{TM} makes it possible to do PWQ of the whole features in a chip. Fig. 3 shows the PWQ results of a memory device.

The procedure for PWQ is as follows

1. Define a preliminary Process Window with some specific feature (Center of Fig. 2).
2. Choose the 4 corner boundary fields of process window as Inspection fields to detect *Hot Spots (No 1~4 fields)*
3. Inspect the 4 corner boundary fields in RDI mode and review all the *Hot Spots* and select typical *Hot Spots* of each field.
4. Define Process Windows of each typical *Hot Spots* (4 corners of Fig. 2)
5. Obtain *Real Process Window* by overlapping Process Windows of each *Hot Spots*

PWQ can provide the typical hot spot information which should be monitored for process control and would be fed back to OPC or Design step for correction to ensure wider process window.

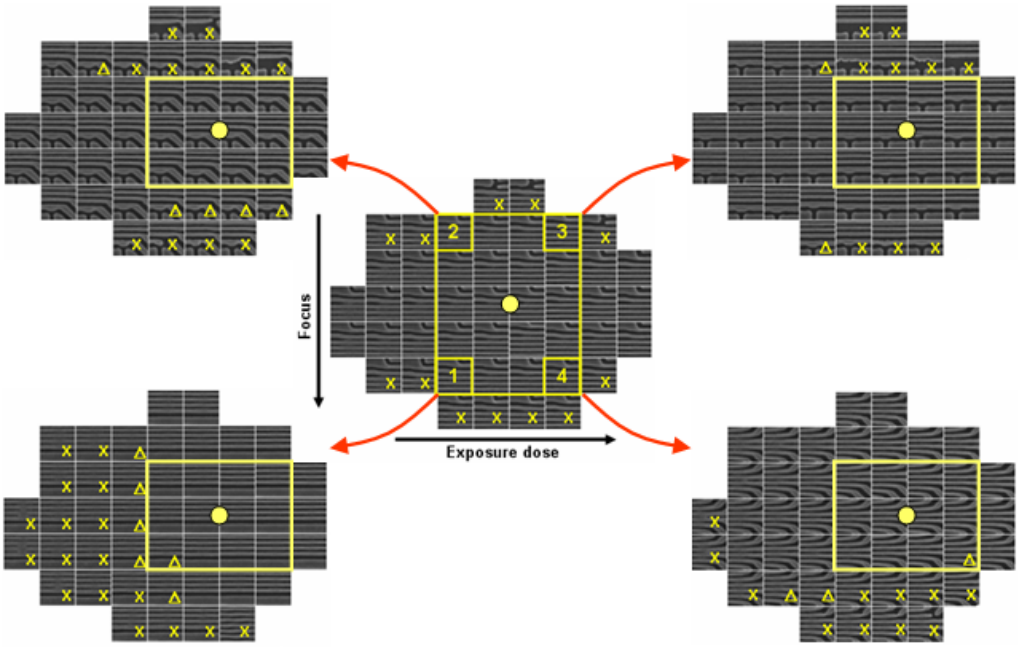

Figure 3. Process Window Qualification

In case of the systematic defects originated from narrow process window, PWQ can be an effective method to detect hot spots at the edge of process window.

2.2 Design related systematic defects

Designers or OPC engineers can make errors while layout drawing or OPC, but most of the layout errors are filtered by some filtering systems such as design rule check or simulation based verification system. There are, however, exceptional occasions that layout errors slip out through the filtering systems and cause failure of chip operation.

Some critical defects caused by layout error are not detected in conventional die to die inspection systems, but found at failure analysis of a chip in the end.

The image #1 in Fig. 4 is a pattern missing defect caused by layout error. The design rule which prohibits the isolated small lines has been violated and the isolated pattern was missing. The image #2 in Fig. 4 shows a bridge defect also caused by minimum design rule violation. The conventional die to die inspection systems sometimes fail to detect the design error induced defects, because die to die inspection method cannot detect them if the dies for comparison also have the same pattern shapes. But Design Based Metrology can detect this kind of pattern missing or bridge defects caused by design rule violation.

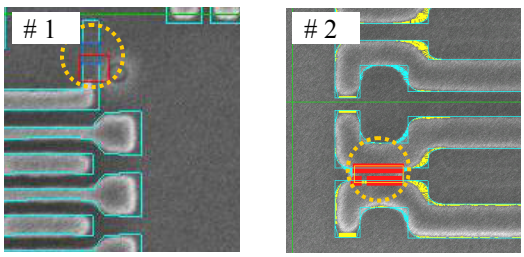

Figure 4. Design related systematic defects

2.3 Process related systematic defects

As discussed before, die to die inspection systems are not able to detect certain defects if all the dies have the same shapes. The images #3 and #4 in Fig. 5 are the examples of process related systematic defects. These are the images of resist pattern in ion implantation mask layers. The pattern shapes are deformed by the step height of substrates underneath, but this kind of defect was also not detected by conventional die to die inspection systems. DBM can filter these defects, because it measures the edge placement error of the image compared to the original layout.

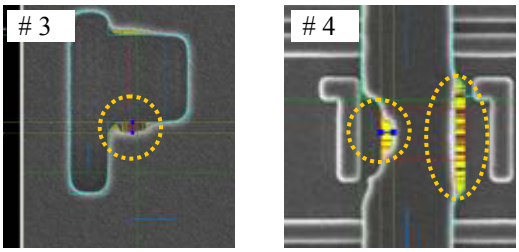

Figure 5. Process related systematic defects

3. RANDOM DEFECT CONTROL

3.1 Random defects in the cell area

As the technology node of memory devices is approaching around 30nm, very tiny defects in cell area can cause micro-bridge defects whose signal is so weak that it is very hard to detect with conventional die to die inspection systems (especially bright field optical inspection tools). Design based metrology, however, measures the CD deviation from the target layout and it is possible, in theory, to detect any kind of defects whose sizes are larger than the criterion set by users.

The capability to detect tiny defects on 3X nm node memory device cell was compared with both inspection systems. GATE layer wafer of 3X nm node memory device was used for this evaluation.

The test result shows that conventional die to die inspection tool has detected around 10 bridges in a die, whereas DBM has found more than 40 bridges in a die including micro-bridges. Fig. 6 (image #5~#7) shows the defects found by both inspection methods. The images in Fig. 7 (#8~#11) are the additional micro-bridge defects detected by DBM. The defect density was more than 4 times larger for DBM inspection method than for conventional die to die inspection system.

In case of cell layout, a few defects can be tolerated to some extent because a number of redundancy cells are spared. But, if the defect density exceeds the tolerance, the device cannot operate properly. So it is very important to analyze how much defect density the cell area has. DBM can provide a criterion to determine whether the defect density is over critical level or not in the cell area.

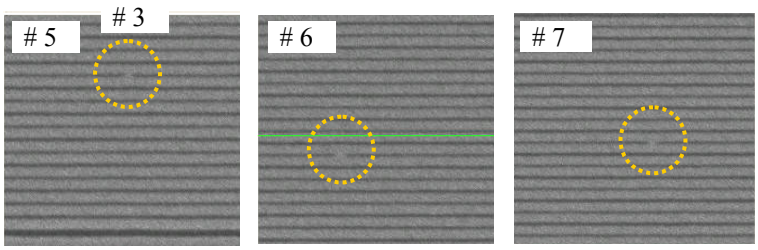

Figure 6. The defects found by both inspection methods

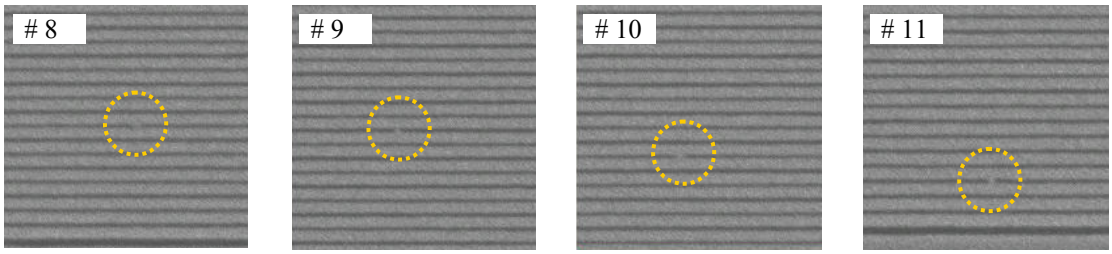

Figure 7. The additional defects detected by DBM

3.2 Random defects in the core area

The K1 factor of lithography has decreased down to around 0.3, resolution enhancement technologies (RET) such as extremely high sigma illuminations are applied for cell layout in memory devices. The typical core area layout in Bit-line layer has 2-dimensional complex features and the process window of complex 2-D features in the core area has been reduced because of the application of such RET's for the cell layout. Besides, likewise the cell features, the size of core area features, also, has become smaller, so that it is hard to detect random defects in the core area with the conventional die to die inspection systems. It means that the core area layouts need to be inspected with DBM as well as with conventional die to die inspection systems.

Fig. 8 shows the defects detected by both inspection systems in the core area of Bit line layer of a DRAM device. These (image #12 and #13) are relatively large bridge defects detected by conventional inspection system.

Fig. 9 shows micro-bridges (image #14~#17) detected by DBM only, whose size is smaller than around 30nm. But, these micro-bridges also can give much impact on the operation of DRAM devices.

The images of Fig. 10 (image #18~21) are narrow space defects detected by DBM only. These narrow spaces can become nuisance defects because they may pass the normal Prove Test, but will be filtered at reliability test in the end. So it would be very helpful to control narrow space defects at in-line inspection step using DBM.

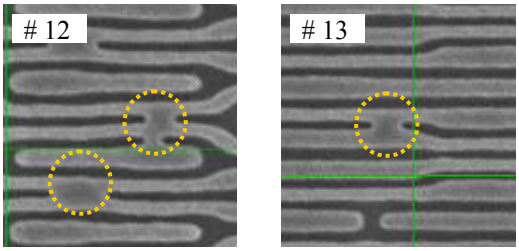

Figure 8. The defects detected by both inspection systems in the core area

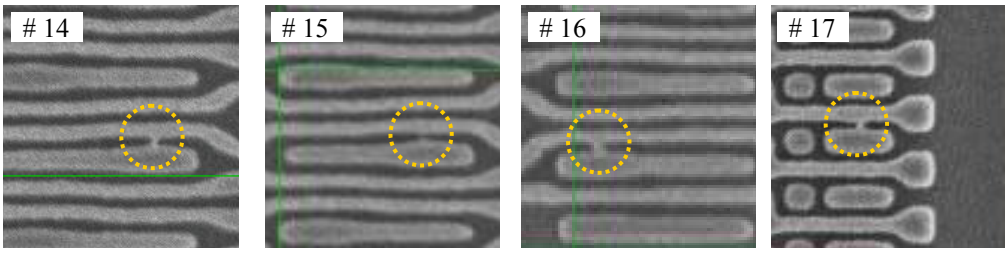

Figure 9. The micro-bridge defects detected DBM in the core area

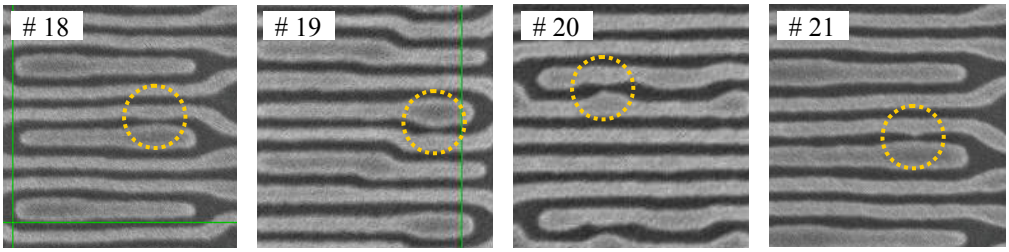

Figure 10. The narrow space defects detected by DBM in the core area

3.3 Random defects in the peripheral area

The peripheral layout has larger features and more relaxed pitch sizes than the core and cell layouts in memory devices. So the process window of the peripheral layout is not so critical as that of other layouts. But, because even a single defect in the peripheral area can kill the operation of a chip, the defect control in the peripheral area is of greater importance than in the core or cell area.
In general, the layout of peripheral area has features of random shapes, and the conventional die to die inspection system has to apply random mode whose detection capability is relatively low.
The images (#22 and #23) in Fig. 11 are the examples of the top-loss defects on the peripheral area which are not found by conventional inspection system, but detected by DBM and these defects are thought to be the killer defects of the chip.

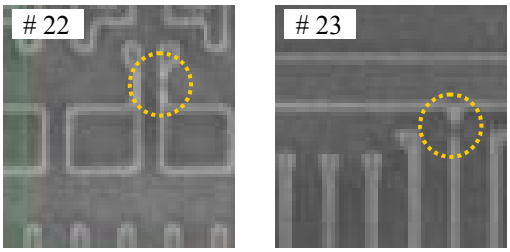

Figure 11. The top-loss defects detected by DBM in the peripheral area

As a result, it would be possible to control systematic and random defects with DBM at 3Xnm technology node.

4. CONCLUSIONS AND DISCUSSIONS

The possibility of systematic and random defect control with DBM has been explored successfully.
However, as the inspection speed of DBM is not enough to cover a large area in a wafer, so it is favorable to combine both inspection systems for full wafer inspection. For example, DBM can provide conventional inspection systems with preliminary information of some micro-defects on a limited area as a reference, so that the recipes of conventional inspection system, such as brightness, sensitivity level and so on, can be fine tuned for better detection ratio of micro-defects.

- The systematic and random defect control with design based metrology has been demonstrated.
- In case of systematic defects originated from narrow process window, PWQ can be an effective method to detect hot spots at the edge of process window
- The conventional die to die inspection systems have difficulty in detecting design error induced defects or process induced defects, if the dies for comparison have the same pattern shapes.
- It was possible to find systematic defects including design related or process related defects with DBM.
- The impact of micro-defects sharply increases at 3Xnm node, but it is very hard to detect tiny micro-defects with the conventional die to die inspection systems
- The random defects in the cell, core and peripheral area were able to be detected by DBM successfully
- It would be possible to control systematic and random defects with the combination of conventional inspection systems and DBM beyond 3Xnm node

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