Patterning hot spot verification using high speed e-beam metrospection with D2DB at foundry high volume manufacturing environment

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2021 International Workshop on Advanced Patterning Solutions (IWAPS) | 978-1-6654-2079-2/21/$31.00 ©2021 IEEE | DOI: 10.1109/IWAPS54037.2021.9671249

***Abstract*—Patterning hot spot (HS) often leads to abnormal critical dimension (CD) behavior, process window degradation, defect generation and ultimately impacts wafer yield. With continued device features shrinkage at an accelerated rate from node to node, the impact of the patterning HS on final yield increases. Patterning HS problems, if not solved properly, can result in a major delay in the qualification of a technology or product. While identifying and verifying HS in high volume manufacturing (HVM) are increasingly challenging with conventional methods, as the critical HS defects size can be much smaller than the resolution of conventional inspection tools, brightfield inspection (BFI). This can lead to a low detection rate for HS marginality defects. The defect SEM review step after BFI adds extra cycle time. In addition, for massive amount of HS, normal SEM review won't be able to review all HS due to throughput reasons. To address the HS marginality issue, a methodology using one single high speed e-Beam system, D2DB HS metrospection combined with process window metrology (PWM) has been developed. This methodology can offer a significant new defense line against the marginal patterning HS issues. In addition, it detecting HS much faster will shorten the product qualification time to release to HVM, which is especially important for a foundry with many varieties of products at the same time.**

Keywords—hot spot, e-beam metrospection, massive metrology, die to database (D2DB), process window metrology (PWM)

I. INTRODUCTION

In modern advanced foundry fabs, the sources of hot spots are from multiple channels[1,2], as Table.1 shown, i.e., OPC HS based on simulations and design rule check; Design For Manufacture (DFM) simulations; design house Design For Test (DFT) patterns, such as scan chain, ATPG (Auto Test Pattern Generation) and MBIST (Memory Build in Self Test); yield engineering defect inspections and inline inspections; from Failure Analysis (FA) at PDE (Product Development Engineering); and from various modules, such as Litho, etch, film; and from test key results of Process Integration Engineering (PIE), etc. These methods can be complementary to each other and to cover different aspects of the HS sources. Among them, the HS source from OPC is frequently used in fab routine basis for mask qualifications.

TABLE I. HOT SPOT SOURCES AT ADVANCED FABS

Hot spot sources	Methods
OPC / Litho	Design rule check / Marginal pattern
DFM	Topography simulation
Design house/ design service	DFT pattern (scan chain, ATPG, MBIST…)
YE	Inline inspection
PDE	FA analysis
Module	Process limitation issue
PIE/3rd	Test-key

For the verification of the HS from OPC simulations, e-Beam tools are normally employed because the e-Beam technology has much higher resolution and much better sensitivity over optical bright field inspections, as Fig.1 shown [2]. The ITRS has derived defect defection sensitivity ~0.5 times of the design rule. When the technology nodes scale down, the bright field inspection (BFI) sensitivity becomes lower than the required, while eBeam inspection (EBI) has kept consistent sensitivity, thus the sensitivity gap between BFI and EBI becomes bigger and bigger. With design rule shrinkage continues, the HS defect sizes become smaller. Thus, it requires more sensitive defect inspection technology to capture smaller defects.

To be able to detect, measure and analyze marginality HS defects with e-Beam tools, SEM image quality is a key factor. There are two typical methods to improve image quality [3,4]. The first method is to acquire the images several times then make an average of them. This method however takes longer tool time. The other method is by image post processing, which consumes little tool time and have negligible throughput impact in most cases. The image quality is made up of three elements: sharpness, noise and contrast. The three elements can be tuned together in order to achieve an optimal image per application layer, as seen in Fig.2. One can observe that in the IQE2 and IQE3 methods, the pattern edges are significantly enhanced compared with original image. This can enhance HS pattern metrospection accuracy where pattern dimensions are measured as a defect matrix

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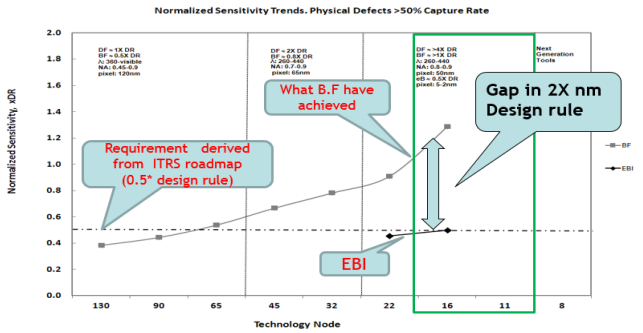

Fig. 1. normalized sensitivity vs technology nodes (B.F and BF: bright field inspection. DF: dark field inspection. EBI: eBeam inspection)

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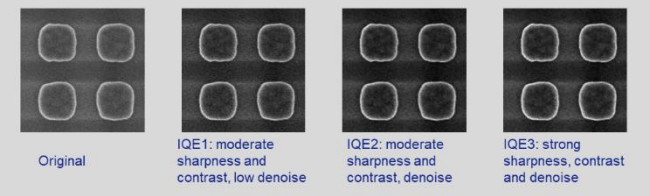

Fig. 2. image quality enhancement with different methods

In the advanced processing, some critical layers are more defects constrained, such as metal layers. In this situation, defect inspection and metrospection can provide effective verifications while CD based analysis such as process window metrology can assist the analysis to conclude. Some other layers are more CD constrained, i.e., gate layer. In this situation, the CD based analysis, process window analysis thus shall be a dominant method to quantify and verify the HS over defect analysis methods.

Process window analysis based on FEM (focus-energy matrix) [5,6] wafers has been fundamental for setting up and optimization of imaging conditions for an optimal lithography process, as well as for OPC model setup and verification for past many years. The process window normally has been analyzed by process engineers manually, while it is not bearable and error prone if the number of features up to 20+. For the patterning HS verification use case, there are a few hundred, thousands or even up to 10,000 of HS. The manual process window analysis is not long efficient. While for the advanced logic foundry, the need to analyze the massive amount of HS is increasing with technology nodes shrinkage. So, an automatic and high efficiency process window analysis tool is required to process massive HS. In this paper, a new process window metrology (PWM) tool is utilized to analyze process window for HS in hundreds, and up to 10,000 HS. This PWM analysis tool relates to ASML latest generation eBeam metrology tool, eP5, and D2DB GDS for analysis. It has the following characteristics.

1. With a button click, PWM directly loads CD results and images from eP5+D2DB, and obtains target CD from GDS-CD
2. PWM capable to analyze HS FEM data up to 10,000+
3. Process window linkage to image is established, which can be used for data cleaning

II. EXPERIMENTAL SETUP AND ANALYSIS

In this paper, we've selected 28nm node layers, one FEOL gate layer, one MEOL Contact Hole layer (CT), and one BEOL M1 layer. The process stage is after lithographic process. To enhance the HS marginality defects detection, an FEM wafer is utilized to stress the HS defects possibility at non BE/BF (best energy, best focus) conditions. CDU wafers are not used since they have lower chance for HS to form a real detect. The FEM wafers layout is shown in Fig.3. The right part of the wafer has higher exposure dose, while the left has lower dose. Toward upside, the focus is reduced. Toward downside, the focus is increased. The focus step is 10nm per step, and energy step is with ~3% of nominal energy.

The HS verification block diagram is described in Fig.4. The 1st step is HS generation. In the layers studied in this paper, the HS are generated by OPC simulations based on process windows analysis. The HS with limited process windows is selected for HS verification. Then binning the predicted HS is performed by pattern geometry and proximity, etc.. This is followed by HS metrospection which consists of both defect inspection based on die to database (D2DB), and pattern CD metrology where the data is further analyzed by PWM. Combined both defect inspection and metrospection, and PWM analysis, HS are verified based on defects and process window. Thus, the goal of patterning HS verification can be achieved to qualify masks.

eP5, ASML latest generation high speed e-Beam metrology and inspection (metrospection) tool with integrated D2DB, 1nm resolution, is used to inspect HS physical defect and measure CD simultaneously. Software setup and analytics have been developed to compare inspected image to GDS designed patterns, as shown in Fig.5. The measured CD of each HS in FEM is fed into PWM tool to generate process window for each HS in a few buttons clicks. PWM is built upon eP5 software analytics. The amount of inspection and measurement locations are in level of 50K for CT layer, and in level of 1.8M for M1, over the die/field per wafer. eP5 high speed can handle this massive metrology with throughput >10K HS/hour in 1nm pixel size, 1um field of view, ~5-30 times quicker than conventional CD-SEM tools.

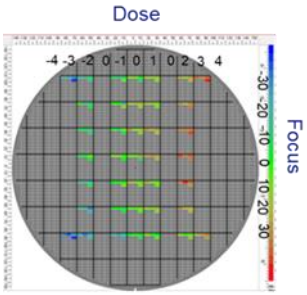

Fig. 3. FEM matrix

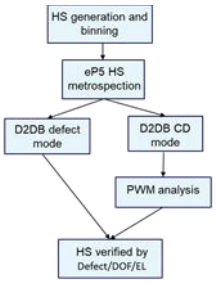

Fig. 4. Block diagram of HS verification

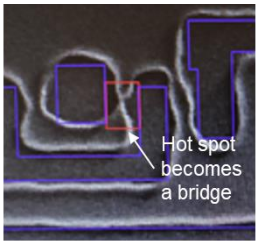

Fig. 5. HS image aligned to GDS for defect inspection (blue: GDS. Red: indicating potential defect

A. Contact hole patterning HS verification

The number of HS input at CT layer is 111, based on OPC simulation. The die layout is 3x8 in one field, as Fig.6. shown, and this is an FEM wafer. As shown in Fig.6., there are 20 dies/field measured, where the grey color means no measurements in these dies. At different dies, different number of HS are measured. For example, 19, 21, 15 etc., indicate there are 19 HS, 21 HS, 15 HS measured in this die. For each number of HS, such as 19, there are two dies are measured. So, there is a repetition which can compare to each other.

There are four types methodologies that are used to verify the contact hole layer HS, i.e., measurement map count analysis, D2DB CDU (CD uniformity) tailing analysis, D2DB defect inspection and PWM, shown in table 1.

TABLE II. SUMMARY OF CONTACT HOLE LAYER HS ANALYSIS METHODOLOGY

Method types	Analysis method descriptions	Priority layers	Remark
1	Measurement map count analysis	Hole layers	Effective for hole blind/missing
2	D2DB CDU tailing analysis	Hole layers	Effective for hole missing, hole size abnormal
3	D2DB defect inspection	All layers	Defect threshold separates true and false defects
4	PWM	All layers	HS ranking based on process window size

The measurement map count can visualize blind or missing holes, as shown in Fig.6. Both the color and defect counts shown in the graph indicate the number of holes measured. For example, the number 12 at green color die means there are 12 holes measured, in both dies. In this case, the uniform color and identical measurements counts indicate the same number of holes got measured at both dies. At the example with 12, given there are 12 HS input, this suggest there are no blind holes, nor missing holes.

According to the hole CD sizes, these 111 HS are separated into Group-a till Group-d, as indicated in Figure 4.2. D2DB CDU tailing can measure hole size abnormal, too big to neck to neighboring holes, or too small to get nearly closed. In this CT layer with 4 groups, Group-a till Group-d, as Fig.7. shown, the CDU tailing is analyzed. In the CD histogram, toward left the CD gets smaller, which indicating hole might be closed. Toward right the CD gets bigger indicating the hole might be connected to its neighboring holes and causing necking. The smaller holes take place at lower exposure dose areas in the FEM wafer, and bigger holes happen at higher exposure dose area, as top-left figure in Fig4.2 shown. Reviewing the HS images at CDU tailings can indicate missing holes and hole size abnormal. At CT layer, 5% of left tail and right tail images are reviewed and compared with GDS designed CD size. The images don't show the HS hole size different than its neighboring holes. The HS hole size and its neighboring holes size are the same. Thus, to conclude that no HS with abnormal hole size in this layer. At this regard, D2DB defect inspection method can be skipped.

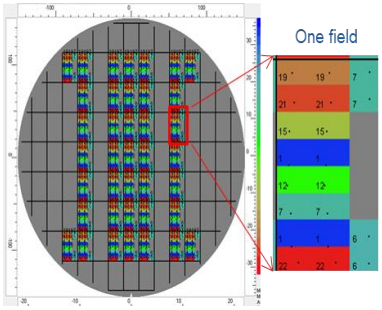

Fig. 6. Measurement map count analysis (waferlevel, left), (field level, right). The number indicatesthe # of measurements.If a hole is missed, the # will be 1 smaller

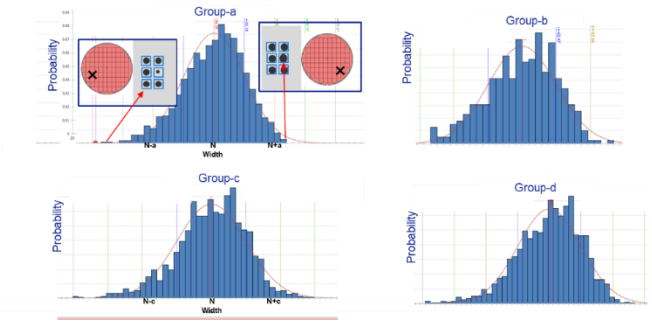

Fig. 7. Baesd on CD ranges, all the CT HS are separated into 4 groups, Group-a(top-left), b(top-right), c(bottom-left), and d(bottom right), CDU talling analysis in both N- and N+ directions. Blue box: GDS design

PWM analyzes HS process window with GDS designed CD as target CD. All the 111 CT HS process window is plotted in Fig.8. One can observe that there is a reasonable overlapping process window from all these HS.

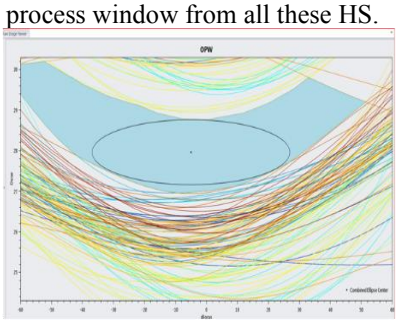

Fig. 8. PWM analysis and ranking of HS based onexposure latitude (EL).DoF (depth of focus)and area (EL and DoF confined area)

TABLE III. HS PATTERN ID IN DOF/EL RANKING AND CORRESPONDENT GDS COORDINATES

Pattern ID	DoF (nm)	EL (100%)	GDS P X	GDS P Y	Pattern ID	DoF (nm)	EL (100%)	GDS P X	GDS P Y
39	82.5	0.148196	2076246	355026	53	97	0.127311	1861902	360372
95	89.5	0.132427	6543347	2451247	96	97	0.107094	6477561	819935
97	90	0.125995	568512	461166	100	97	0.137836	1667554	885006
140	90	0.090126	3974103	2075385	104	97	0.119503	5020920	1632898
103	92.5	0.120079	477162	1022963	138	97	0.104016	1110407	3557449
107	92.5	0.15069	1666928	885006	142	97	0.114132	5133137	1529063
144	92.5	0.090293	5235377	3602501	150	97	0.103035	5458631	2810862
128	93.25	0.094169	1181853	248792	30	97.5	0.12	6414827	1573315
36	94.5	0.14874	1755333	756542	108	97.5	0.107942	1748997	875065
43	94.5	0.134667	3990321	2668258	112	97.5	0.11694	887263	474170
94	94.5	0.136905	6464286	826235	41	99.5	0.157221	1313723	667562
143	94.5	0.095045	1666303	885006	115	99.5	0.106175	879815	473819
91	95	0.113853	6126633	1046847	137	99.5	0.094717	1969022	878940
114	95	0.132347	6249965	1706021	146	99.5	0.095032	1969022	879926
145	95	0.113889	352975	2636768					

The process window size specification is set as: DoF>=100nm, and EL >=8%. With the spec, the 111 HS are ranked. Out of all the HS, there are 29 HS are process window constrained, as shown in Table 2. These HS process window DoF are smaller than 100nm. The corresponding GDS coordinates of these process window constrained HS are reported, as shown in Table 2. These HS will be further investigated for root causes. They can be either fixed by mask producing process to improve mask quality or fixed by OPC model optimization according to different root causes. The root cause investigation is not included in this paper.

B. Gate layer patterning HS verification

As the gate layer defines the device performance in 28nm node, the HS verification of gate layer thus must be CD based, with defects to assist for verification. The number of HS in gate layer is 201, based on OPC simulation. Based on the pattern types, we've separated them into Line group with 181 HS, and Space group with 20 HS. Generally, the OPC is more aggressive toward line end than middle of the regular line at dense line arrays. To closely monitor the line end performance, there are 10+ line end defined as HS. These lines end HS is merged into the line group, as shown in Fig.9.

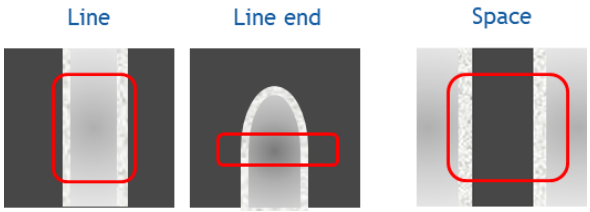

Fig. 9. HS types in gate layer, line and line-end in one group, and space in the second group

The CDU histogram and tailing are analyzed, the same as CT layer. All the 201 HS CD at FEM conditions is plotted in Figure 4.5. At the tail of the CDU, 5% of the images are reviewed. On the contrast to hole patterns, toward the left the smaller CD side, the exposure energy is higher. Toward the right the bigger the CD, the exposure energy is lower. At left tail, the HS is typically line end types. The CD tends to become smaller which is normal for a line end structure at over exposure condition. At right tail, the bigger CD is from array type at under exposure condition. Randomly review 1% of the CDU histogram at left tail and right tail, there is no defects like bridge or line broken. This suggests the bridging lines or broken line defects are not pronounced in this gate layer.

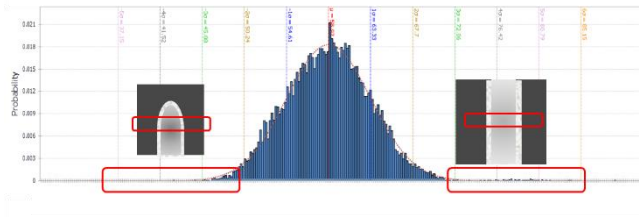

Fig. 10. CD histogram for 201 HS including line, line end and space HS patterns at FEM condition

To further study the gate layer HS performance, the delta CD between measured CD vs GDS CD at nominal energy and focus condition is used, as Fig.11 shown. This step is to identify the HS which is far from design target. The hot spots which are about 1% away from the target CD are mainly line end. Apparently, both OPC over correction and under correction have been applied in some line end locations. Less hot spots in array types have CD difference more than 1% of target CD. In this case, the data indicate all the 181 line type HS delta CD are in control limit.

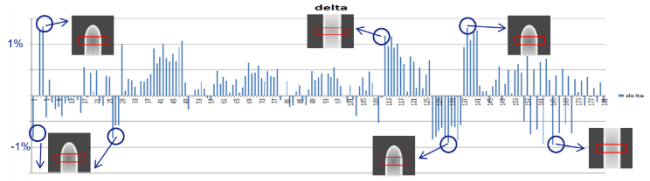

Fig. 11. Delta CD between measured CD vs GDS CD at nominal energy and focus condition, for line and line-end HS patters

In the process window analysis, the DoF for the line and line end HS patterns is plotted in Fig.12. One can observe that, for line end type, the DoF is smaller, and in 90nm level. For regular array lines, the DoF is bigger, 120nm. This is in line with line end and dense array lithographic performance. The dense array lines normally have higher DoF, and line end has smaller DoF.

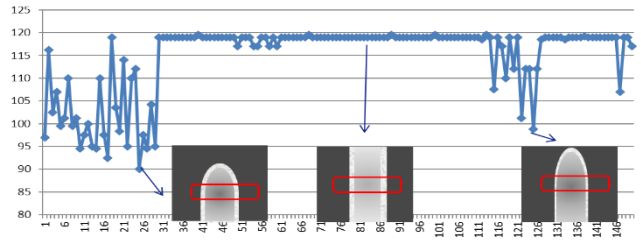

Fig. 12. Depth of Focus (DoF) analysis of line type and line end type

Overlapping process window (OPW) of these 181 line type HS is analyzed, as Fig.13. shown. As can be seen, based on 10% target CD, the EL is >10%, and minimal DoF is 90nm.

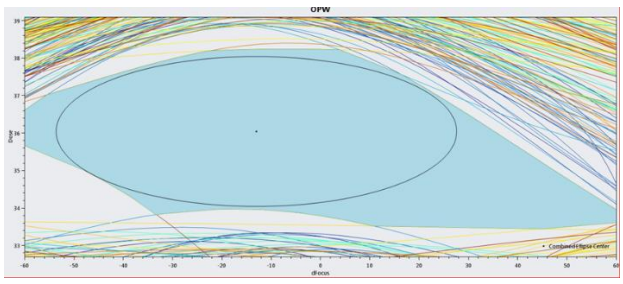

Fig. 13. overlapping process window of 181 line patterns HS

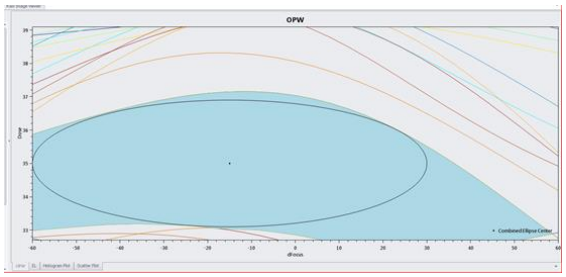

Fig. 14. overlapping process window of 21 space patterns HS

Overlapping process window analysis is applied to 21 space HS patterns, as Fig.14. shown. The minimal DoF of the 21 space HS is 101nm, and EL is 8%.

Based on the comprehensive anslysis of defect, CDU histogram, delta CD, and process window analysis, for gate layer with 201 HS, they are verified as none HS. No further mask or OPC fix is required.

C. Metal-1 layer patterning HS verification

There are close to 90547 HS to be verified in M1 layer, with critical HS as various broken defects, as Fig.16. shown. The normal pattern should be straight as GDS red lines shown. When line CD at some position becomes much narrow than GDS design, it is defined as a broken defect. Broken defects can impact yield [7,8], therefore it is the focus on this layer. Other defects types are not critical. The metrology of the broken HS is performed, which is known as metrospection.

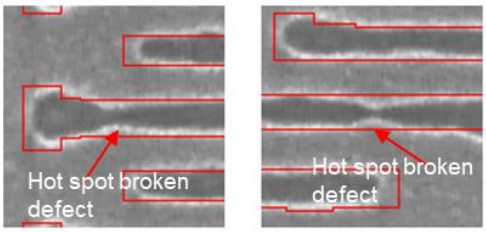

Fig. 15. typical defects in M1, broken defects

An image quality enhancement (IQE) is performed to enhance image quality thus to improve defect inspection and metrospection accuracy. There are multiple enhancement methods, as shown in Fig4.11. In this Figure, the Default is the raw image with correction, and Method_1 till Method_9 is to use different combination of noise reduction, sharpness and contrast enhancement to improve image quality. One can observe the image quality difference through these Methods, where noise, edge sharpness or contrast enhancement are varied. Per application layer, a unique combination of noise reduction, sharpness and contrast enhancement shall be applied. In this M1 layer, Method_9 is used to enhance edge sharpness and reduced background noise [9].

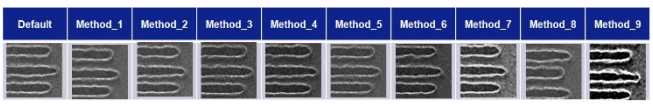

Fig. 16. Nine different image quality enhancement methods and their images' appearance

In addition to enhance the image quality, Automatic Defect Classification (ADC) is applied. About 10% of the total HS 90547 are reviewed and trained for ADC. The classifier is the HS CD measured based on the metrospection,

as shown in Fig.17. Among them, 8047 broken defects are separated from other types with 99.4% of accuracy and 98.12% purity, as shown in Table 3.

We've found that if the raw images has been enhanced with IQE, the accuracy and purity are much lower than the results after IQE. Very importantly, the IQE has enhanced image quality thus enhanced measurement accuracy of the broken HS. This indicates one can either optimize the e-Beam image acquisition conditions, and build up best known method per applications, or use IQE to further enhance the images after raw image acquisition is performed

Like other layers, the broken HS after ADC are delivered to mask manufacturing and OPC team for further root causes analysis and fix. This part is not included in this paper.

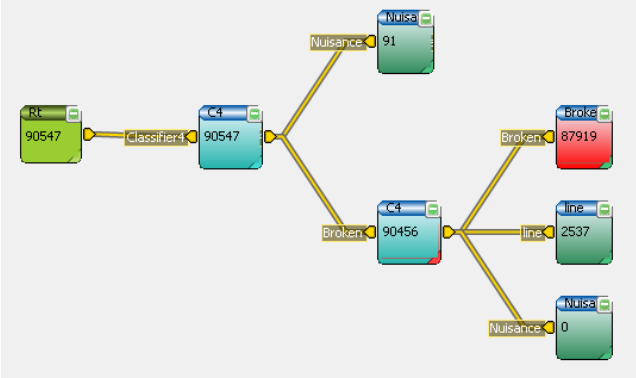

Fig. 17. Automatic defect classification of 90547 HS at M1 layer

TABLE IV. ADC RESULTS, FOCUSING ON BROKEN DEFECTS

Review\ADC	Nuisance	Broken	line	Total	Accuracy(%)
Nuisance	4	0	0	4	100
Broken	0	7999	48	8047	99.4
line	0	153	850	1003	84.75
Total	4	8152	898	9054	
Purity(%)	100	98.12	94.65		97.78

III. SUMMARY

For patterning HS verifications, two categories of methods, namely, defect inspection/metrospection and CD metrology, have been developed. For layers such as hole layer, line and space layer, and irregular 2D patterns, both categories can be used but with different weighting. For hole layers and line/space layers, such as contact hole, via, and gate layers, CD based methods, D2DB CDU tailing, delta CD to GDS CD, and process window metrology, have higher weighting over defect method. For irregular 2D patterns such as metal layers, defect inspection, metrospection have higher weighting over CD metrology. IQE and ADC have been applied to improve the efficiency in inspection and metrospection. These methods have become the POR methods to quality masks and monitor mask quality.

As an outlook, HS pattern search can be applied to extend the patterning HS verification and mask qualification. The HS input from OPC simulation can be limited. To do a pattern search [9,10] can extend the HS list to discover unknown weak points. Pattern Search processes full GDS with pre-defined patterns. For example, as Fig.18. indicates, the HS is identified as top-left SEM images. Pattern search would use the defined pattern to search through the full chip GDS, to identify patterns identical to the pre-defined one, and/or rotated and/or mirrored images, as the other images in Fig.18. shown. These four patterns are identical from imaging point of view except that they are rotated or mirrored as first order estimation. After performing the pattern search through full chip GDS, all images' locations with these four patterns will be delivered for HS verification.

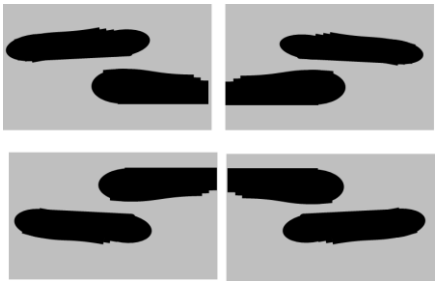

Fig. 18. yield limiting hot spot (top left), rotated and mirrored (others) through pattern search

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