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Massive metrology of 2D logic patterns on BEOL EUVL

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ABSTRACT

At sub10nm nodes of Backend of Line (BEOL) using Extreme Ultraviolet Lithography (EUVL), the requirements of the process window of patterning are extremely tight for parameters such as Critical Dimension (CD) and Overlay which are traditionally managed for the semiconductor process. In addition to these parameters, because the latest BEOL pattern consists of a variety of space patterns, Edge Placement Error (EPE) of the tip feature of space pattern is the most critical to secure the contact between metal layer and contact or via layer. Because tip EPE is assumed to be affected by multiple factors such as pattern layout, the accuracy of Optical Proximity Correction (OPC), mask pattern, scanner tool conditions, and etching process conditions etc., the characterization of the patterning process and the establishing analysis method to find the root cause of EPE is of utmost importance before starting a high-volume manufacturing. However, general CD-SEM metrology is only utilized to collect the limited number of data from several features which are predicted by simulation or searched by optical inspection tool. This implies the possibility of further process optimization is still covered inside of various 2D feature in BEOL. In this paper, we apply Die to Database(D2DB) EPE and show the necessity of massive data-based methodology to identify local process variability of 2D feature using e-beam metrology.

Keywords: CD, EPE, D2DB, OPC, SEM, EUVL, metrology

1. INTRODUCTION

As Extreme Ultraviolet Lithography (EUVL) tools are reaching high-volume manufacturing capabilities, products with EUV processed layers will be commercially available soon. Currently, huge efforts are being dedicated to the development of novel process node for each layer in Frontend of Line (FEOL) and Backend of Line (BEOL). Utilizing single exposure EUV is regarded as the best option in terms of cost and process simplicity but tight control of pattern fidelity is still challenging issue under the influence of 3D mask effect and stochastic defect as nature of EUVL [1]. BEOL metal layer with 2D layout is one of the candidates to implement single exposure EUV in sub 10nm process node. However, EUV lithography tool still requires critical patterning control because it is directly connected to electrical failure. Figure 1 shows the target-design of a representative example pattern from a logic Metal layer(blue) and the Via layer (red) in bottom. As illustrated in the Figure 1, line-end pull-back will increase the risk for missing connection with lower patterns.

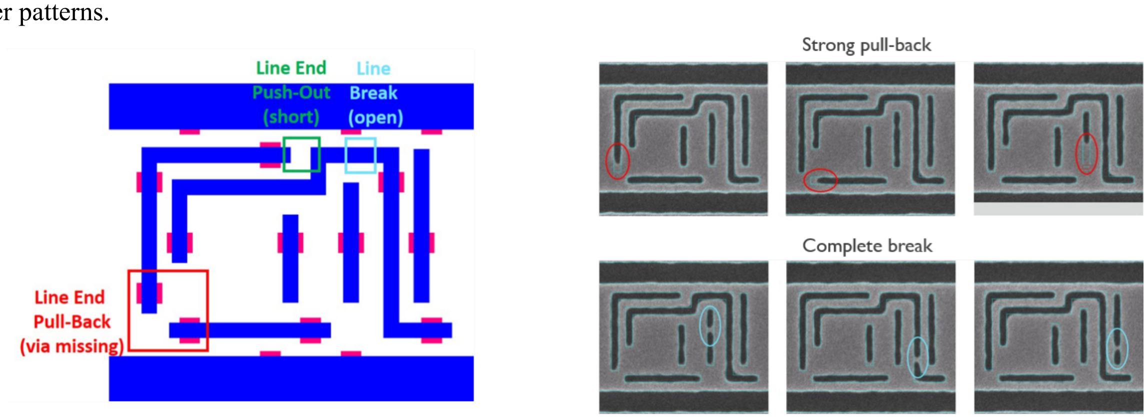

Figure 1. Example of different types of defects

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On the other hand, line-end push-out increases the risk of shorts within the metal layer (red box). Moreover, at tighter pitches (iN7 and below) the trenches itself suffer from random bridging and necking defects, also causing shorts or missing connections respectively. Thus, maintaining pattern fidelity to the target-design has become a critical topic when using EUV based processes.

Furthermore, each unique 2D pattern inside of the 2D layout needs individual optical proximity correction (OPC) under 3D mask effect to satisfy acceptable printability. This will make OPC and mask making process more challenging compare to 1D layout. In general, CD-SEM is used to collect data for process control and OPC. However, CD-SEM metrology is typically applied to the very local area including the insufficient number of measured features due to lack of flexibility. This implies there is still missing information that could be valuable for OPC and process engineer.

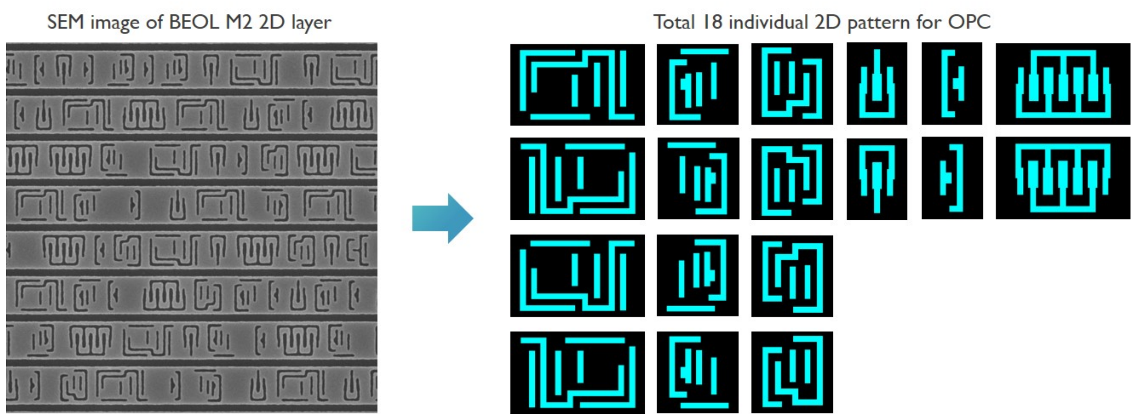

Figure 2. Example of a variety of pattern in 2D logic layer

Figure 2 shows an example of the abovementioned. Inside of the scanning electron microscopy (SEM) image in Figure 2, a total of 18 individual 2D pattern are existing. In other words, 18 individual 2D patterns required to be optimized during OPC phase. Therefore, a more realistic approach for OPC and process optimization is to use large areas covered massive metrology to collect enough information from each individual 2D pattern. In our previous work, several results are already presented to show the necessity of massive e-beam metrology based on the measurement of Die to Database (D2DB) edge placement error (EPE) [2]. This paper continues our effort to reveal EPE characteristics of the EUVL printed 2D metal layer by identifying local variability and evidence of systematic error using massive e-beam metrology.

2. TEST VEHICLE FABRICATION

The metrology was done on wafer that underwent a short loop of fabrication steps utilizing the IMEC 10nm design rule (iN10). For this study, the focus is on EUVL printed metal layer with a nominal pitch of 48nm and a nominal trench width of 24nm. The target patterns consist of 2D logic type structures which are arbitrarily routed on large areas within the field, thus enabling this layout to detect process variations both intra-field and inter-field. The imec iN10 single patterning (SE) EUV flow consists of trench patterns which are directly transferred by etching the TiN hard-mask layer right after the single exposure EUV. For this metal layer, a quadrupole MP4 45 source was used and exposures on ASML NXE:3300 EUV system was done at Imec. The process flow is described below in Figure 3.

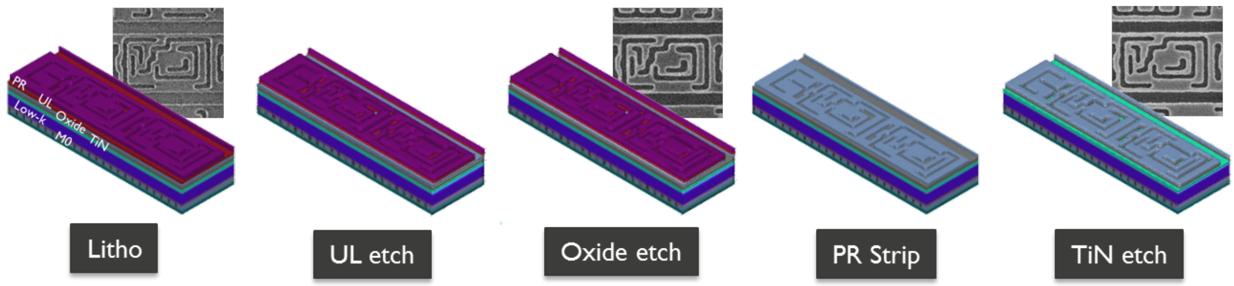

Figure 3. iN10 EUV SE process flow to transfer pattern on hard-mask layer

3. EXPERIMENTAL SETUP

3.1 Metrology tool and definition of D2DB EPE

The overall configuration of the metrology system for this work is illustrated in Figure 4. The D2DB system of NGR3500 tool provides high-throughput capability by parallel data process during e-beam scanning in real-time. With over the ten of cluster processors and high-speed network connections, a massive amount of data can be processed in the most effective way. During continuous SEM image collection, acquired SEM images are aligned to clipped layout data using D2DB and pattern contour of SEM image is extracted [3]. To minimize alignment error between clipped layout and pattern contour of SEM image, multiple rules are automatically applied during the alignment step and best position is decided after negligible error is identified. After that, CD values are measured as the distance between the edges of pattern contours. EPE value is calculated as the distance between the contour edge of the pattern and target layout edge which is named as D2DB EPE as shown in Figure 5 [4].

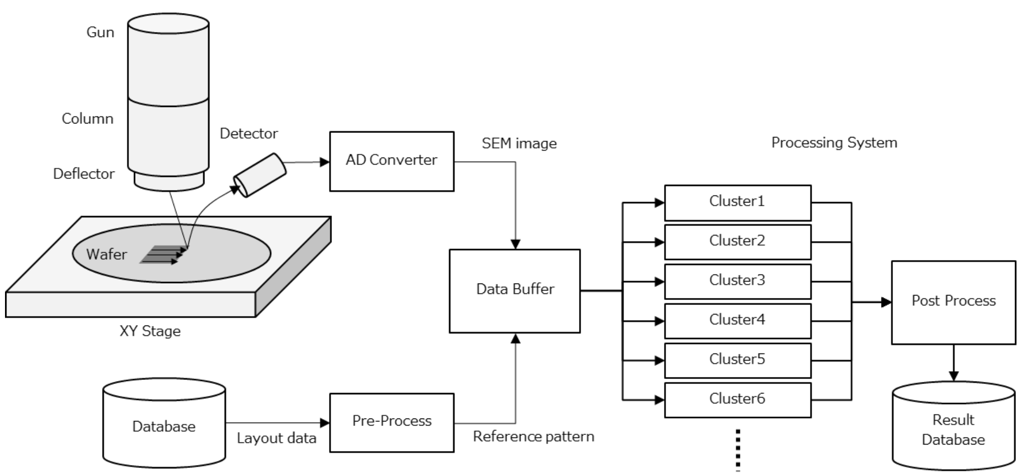

Figure 4. Schematic of the e-beam metrology tool

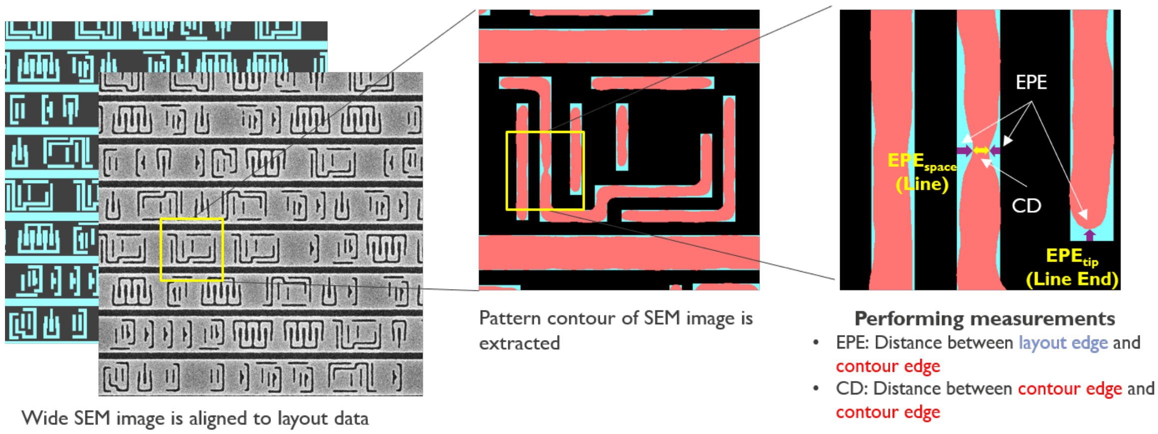

Figure 5. Definition of D2DB EPE

3.2 Selection of pattern of interest from 2D layout

Before describing the recipe setup for metrology, it is important to explain the concept of the pattern of interest (POI) which will be used in the rest of the section. In this work, we select the specific pattern to identify local variability and systematic trend inside of 2D feature in an effective way. Figure 6 shows the design layout of the POI. The chosen POI consists of both 1D, 2D feature and also a total of 4 kinds of symmetry are existing. As already mentioned, the wafer for this study is a single parameter processed. To identify process variability with this wafer, it is required to analyze the same measurement point within POI across a field. By labeling each measurable point as described in Figure 7, quantitative analysis at the geometrically same location is available regardless of the symmetry condition.

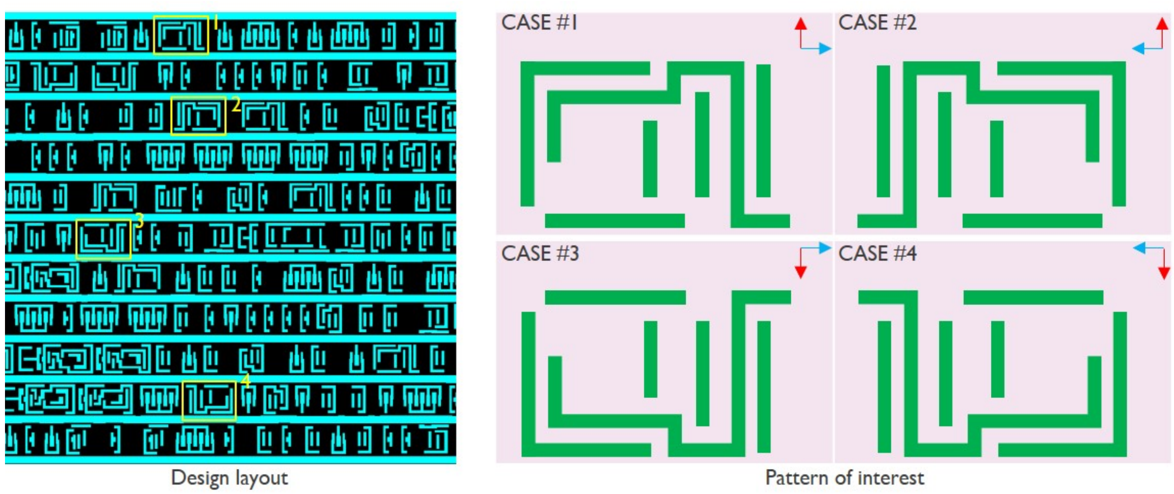

Figure 6. Selection of POI from the original layout

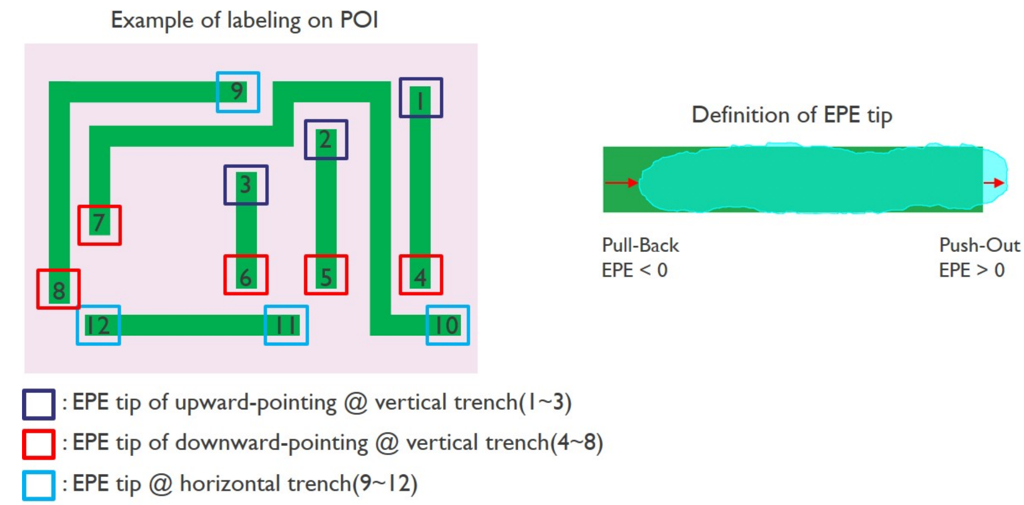

Figure 7. Labeling on POI (left) and definition for pull-back, push-out of EPE_{tip} (right)

After acquiring massive data, POI will be exclusively analyzed to show the necessity of massive data analysis in 2D layout. One thing to note is that the selection of this POI was done in the step of data analysis as the last part to demonstrate the necessity of this approach. Any 2D pattern inside of the original layout can be targeted and analyzed as the same method which will be introduced in this work.

3.3 Recipe setup for data collection

To collect the meaningful number of massive data across a field within acceptable throughput, the sampling plan is adopted. Figure 8 shows the example of the sampling scheme inside of a single die. A total of 20 logic clips are selected to cover entire area of die and 12 SEM images are collected per each logic clip. The locations for 12 SEM images are uniformly distributed to include the variability within a clip. A point to be considered in the 2D logic layout is the number of each unique 2D pattern is not equal in a logic clip. Therefore, 8μm by 8μm Large FOV is utilized to collect the significant number of each different 2D pattern. With this sampling plan, 323,406 of EPE_{tip} features can be measured in 35 minutes. As already mentioned, data from POI will be exclusively utilized for analysis. Within raw data, approximately 96,000 EPE_{tip} values from POI are existing and this data will be used for the following analysis.

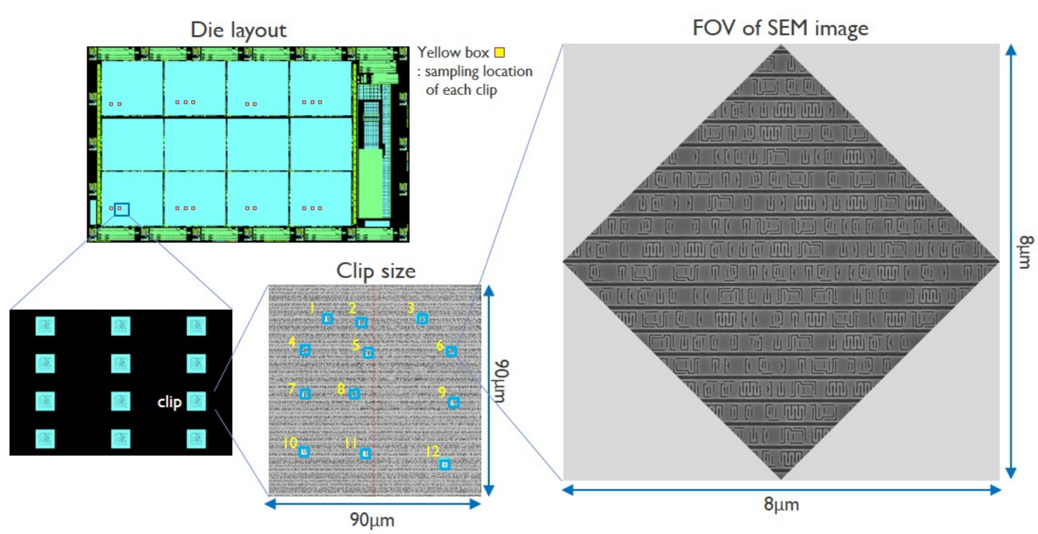

Figure 8. Schematic of the sampling plan for massive metrology

4. MEASUREMENT RESULT AND ANALYSIS

4.1 Analysis of EPE_{tip}

Figure 9 shows the distribution of EPE_{tip} from all labels in Case 1. As observed in the histogram, all labels except Label 1 have minus offset which means pull-back at the end of the line. A more obvious fact is that a clear difference of offset and variability are existing within POI. The biggest and smallest variability are found from label 5 and 1 respectively. Label 5 have 6nm higher value in terms of 3σ compare to Label 1. This difference indicates Label 5 show more stochastic behavior within all labels. Another noticeable observation is only Label 12 shows the different distribution and offset among EPE_{tip} at the horizontal trench(Label 9~12). This could be due to imbalanced OPC on the pattern of Label 12.

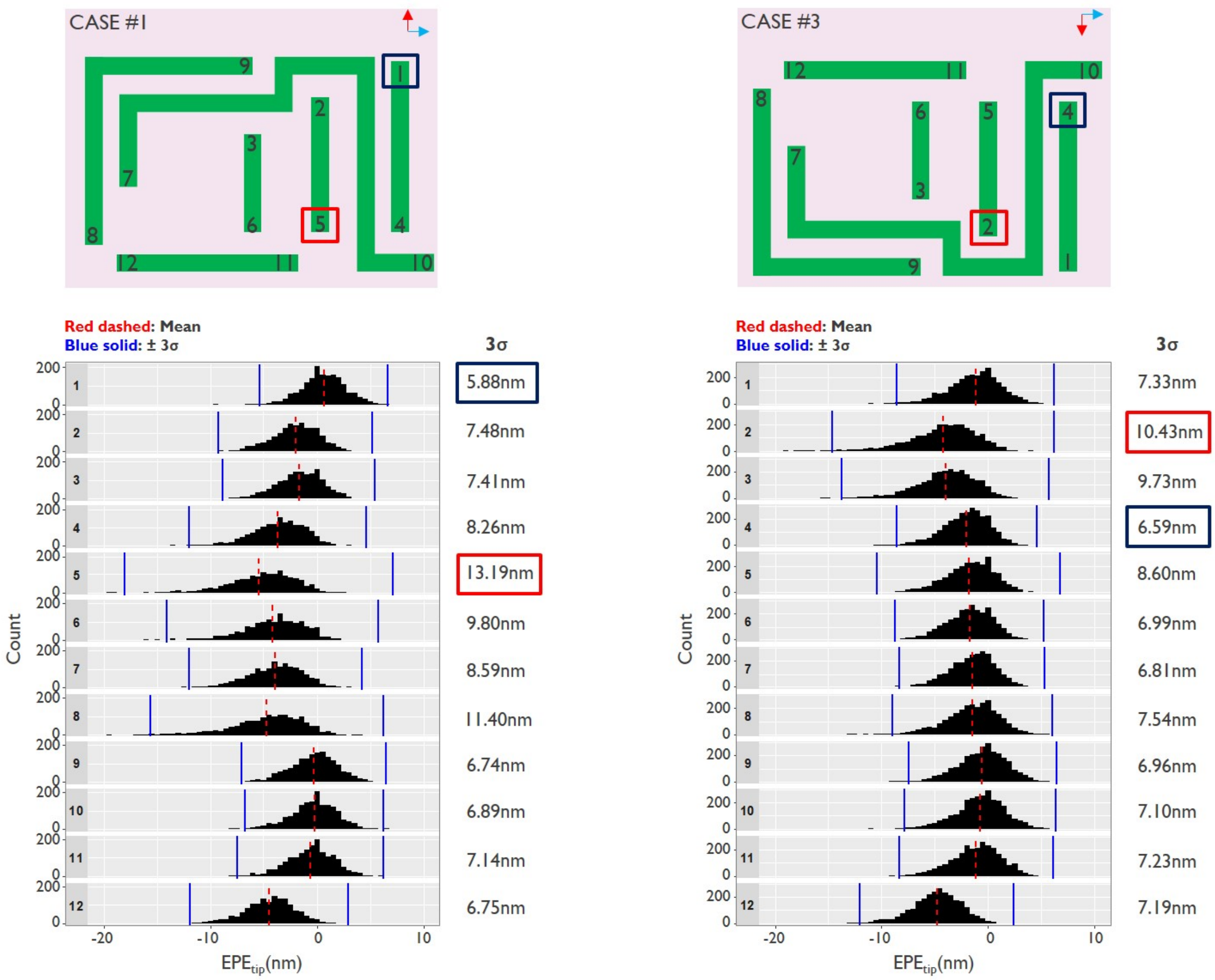

Figure 9. Histogram of EPE_{tip} from each label in Case 1(left) and Case 3(right)

In the same manner, Case 3 is also analyzed. Unlike the trend of Case 1, the distribution of each label show different trend. In the case of Case 3, Label 2 and 4 have the biggest and smallest variability as shown in the histogram of Figure 9 respectively. However, Label 12 still shows the same trend as Case 1. To understand our observation result between each symmetry case, we combined all data of 4 symmetry cases as one bar plot. Figure 10 shows the average and 3σ value from each label in every case. Several results can be summarized from Figure 10 as below.

(1) Clear local variability is existing among 12 labels in terms of average and 3σ

(2) Clear local variability is existing among 4 symmetry case in terms of average and 3σ

(3) Obvious different level of average and 3σ EPE between Case 1,2 and Case 3,4(maximum Δ3.78nm)
This trend is only observed from EPE_{tip} at the vertical trench (Label 1 to 8)

(4) Relatively similar level of average and 3σ EPE between all cases (maximum Δ0.73nm)
This trend is only observed from EPE_{tip} at the horizontal trench (Label 9 to 12)

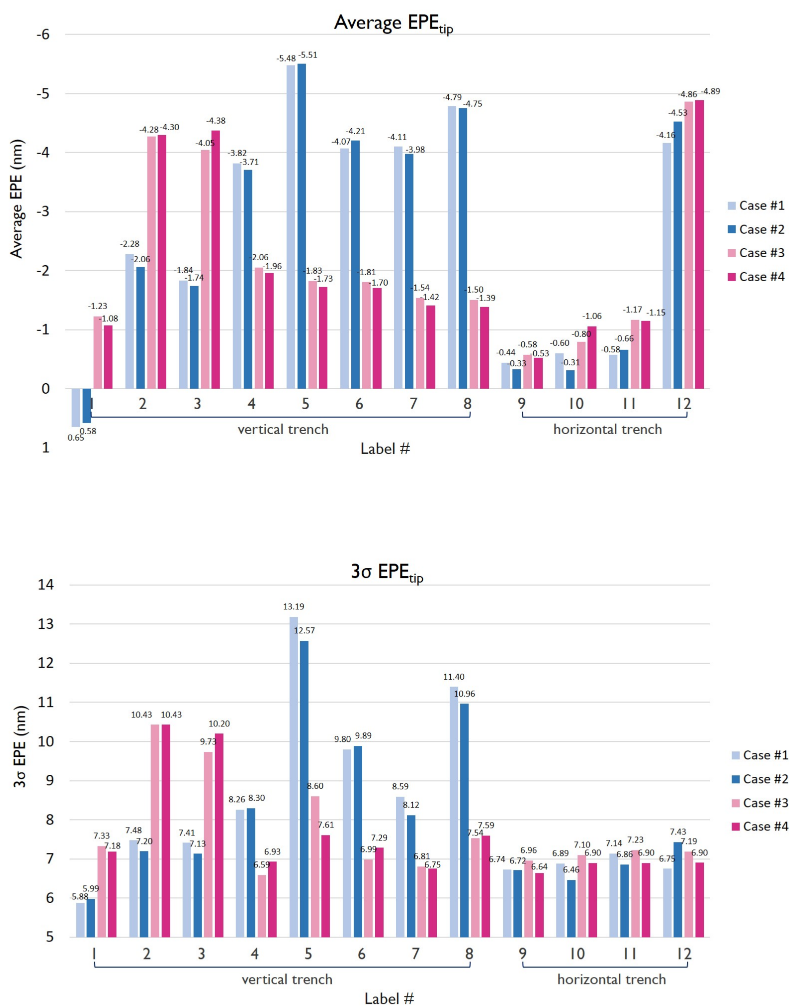

Figure 10. Average(upper) and 3σ(lower) of measured EPE_{tip} from all case

Result (1), (2) and Figure 10 indicates clear evidence of local variability and suspicious hot spot position, also provide information to judge which position shows more stochastic behavior in terms of variability. Moreover, with the result (3) and (4), the signature of orientation dependency can be apparently found. From the result (3), the difference between Case 1,2 and Case 3,4 is the vertical flip of the pattern as shown in Figure 6 from the earlier section. In other words, printability of EPE_{tip} showed different sensitivity by direction at the end of the pattern. Different trend between the result (3) and (4) is also directly related to horizontal and vertical trench which means orientation. Figure 11 shows the wafer map of all labels. The color variation between different cases can be easily recognized from Label 1 to 8 in the wafer map. The outcome from Label 9 to 12 is also same as the result (4) in above. This observation result from the wafer map suggests systematic error related to orientation dependency is included in the printing result. A plot in Figure 12 also shows variability within 4 symmetry case. As we expected from the result (3) and (4), EPE range(Maximum average EPE_{tip} – Minimum average EPE_{tip}) from vertical trench has a higher range than the horizontal trench. Currently, we can't insist this difference is a critical issue in OPC or process control but it could be valuable feedback to related engineers for further optimization.

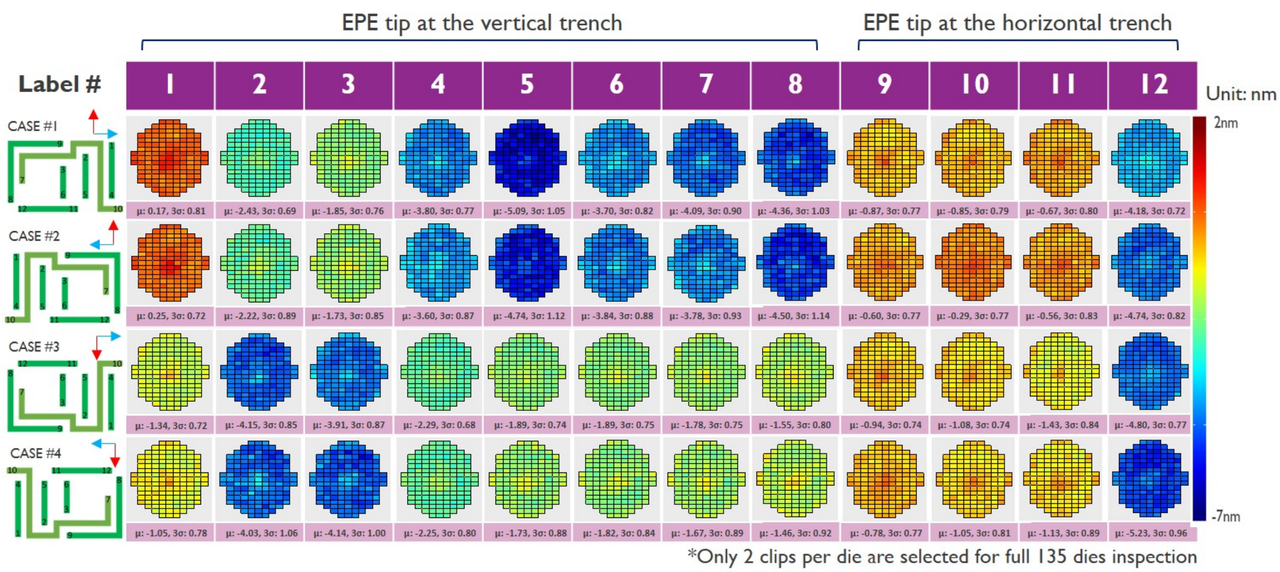

Figure 11. Wafer map of average EPE_{tip} from all case(average EPE_{tip} is calculated per die and displayed as the color at each die coordinates)

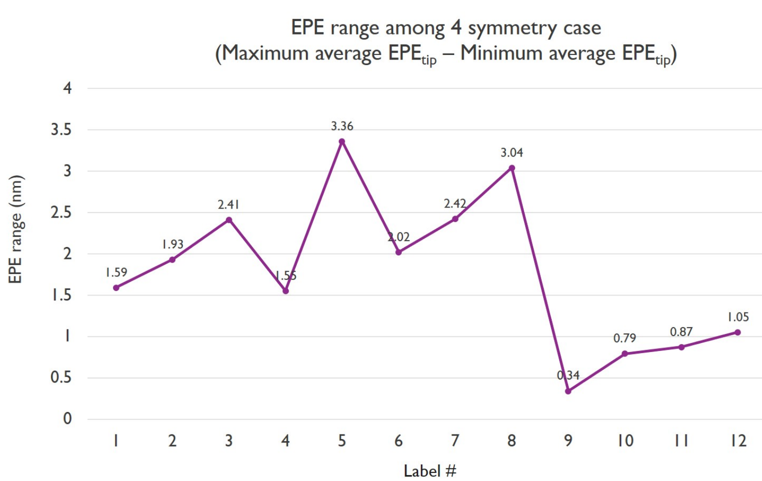

Figure 12. Variation of average EPE_{tip} within 4 symmetry case

4.2 Additional analysis with contour

To provide a more intuitive form of result, we utilized contour-based analysis using SEM images already acquired. Figure 13 explains the simple process of contour extraction and overlapping to generate stacked contours. The basic process before contour extraction is exactly identical as explained in the earlier page.(Section 3.2) After completed alignment and measurement between SEM image and layout data, individual contour is extracted from edge detection result on each pattern. Figure 14 shows the result of stacked contours overlapped with via Graphic Database System (GDS). Red circled area indicates several locations where can be easily identified by strong pull-back and line shrink. While stacked contours can provide an intuitive and clear vision of the process range as we observed in Figure 14, judging hot spot could be a difficult job in case of less catastrophic defects are shown. For quantitative analysis, we combined via GDS and metal contour from POI to calculate the overlapping area. Every single contour extracted from POI is used to calculate the effective overlap area between metal contour and via GDS. Because overlap area calculation is performed using via GDS, we assume as 100% overlap value when two rectangle areas overlap perfectly as shown in Figure 15.

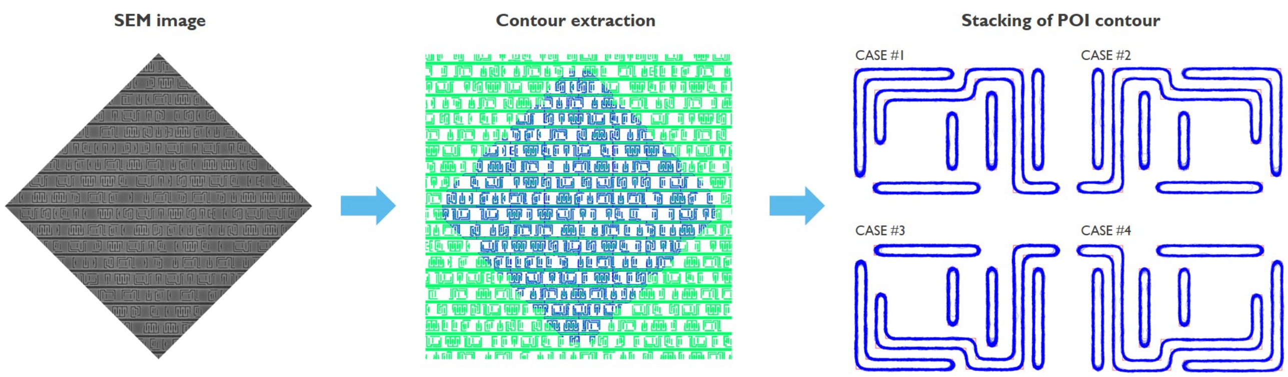

Figure 13. Workflow to generate stacked contours

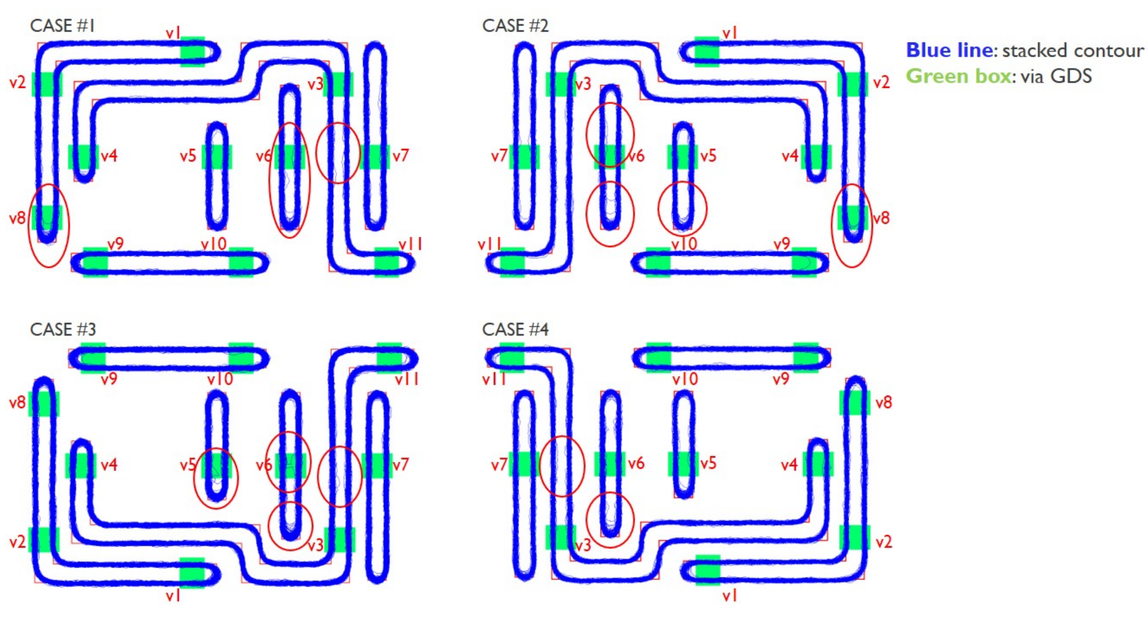

Figure 14. Result of stacked contours

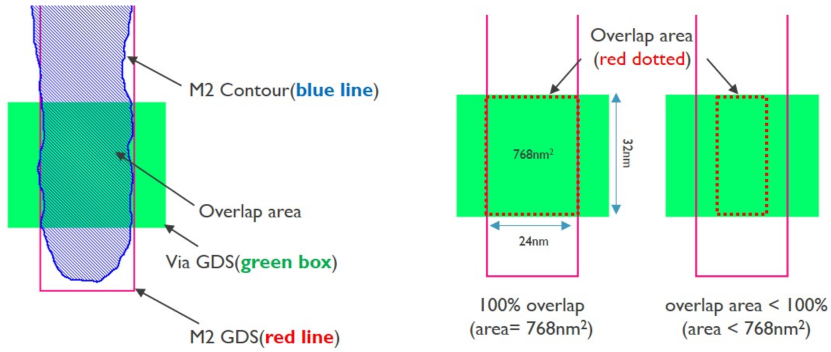

Figure 15. Definition of overlap area between Metal layer and Via (left), description for area coverage (right)

The calculation result is represented in Figure 16. A noticeable difference is distinguished by each overlap area value. Via 6 shows clearly the lowest overlap area among 11 vias. Moreover, via 8 shows a good example of orientation dependency again as the different level of overlap area between Case 1, 2 and Case 3, 4. If we take a look at each location of via 6 and 8, the difference between this two via is recognized easily. Via 6 is located in the middle of the vertical trench so the reason for the relatively small overlap area should be due to line shrink. On the other hand, via 8 is located near to the end of the line and exposed to the possibility of missing via from by pull-back. These results prove the necessity of massive data acquired from multiple and different locations again. Without guided inspection based on simulation or optical inspection, finding this kind of phenomenon will be a difficult job with typical metrology. Figure 17 shows a more specific example of variability as the outlier. Three outliers are observed below the line of 60% overlap. One example from via 6 shows a line break case before being a catastrophic defect. By analyzing overlap area calculation, the risky position of missing via can be detected easily as well as provide quantitative value for judgment. If we increase the sampling area to a larger area, it is expected to identify the relationship between defectivity and variability. This task will have remained as future work.

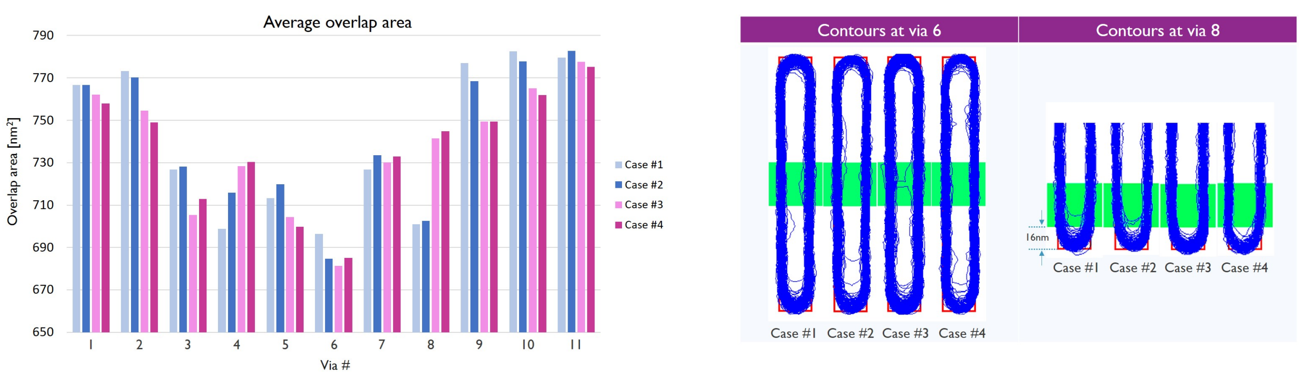

Figure 16. Calculated overlapping area at each via location (left) and an example of stacked contour at the specific via location (right)

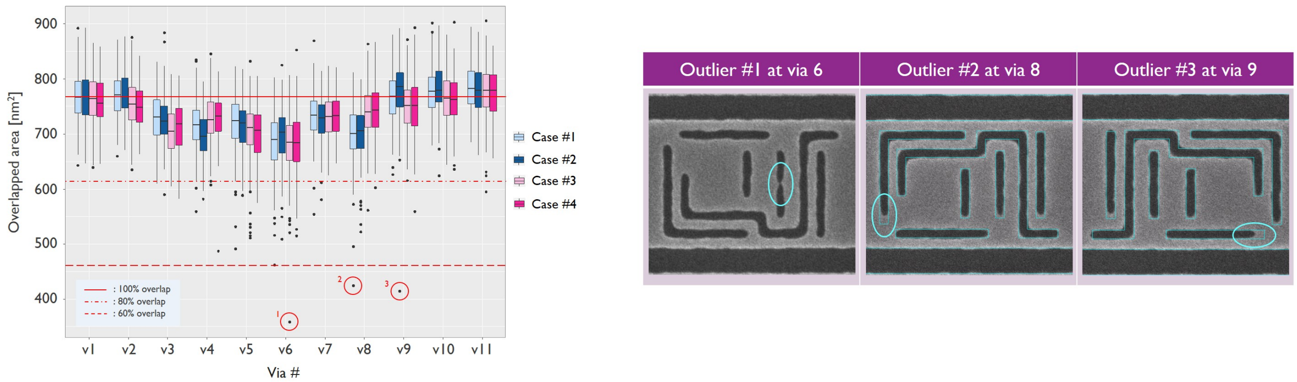

Figure 17. Overlap area comparison with reference line (upper) and SEM images of outlier (lower)

5. CONCLUSION

This study started by the necessity of massive data analysis in IMEC iN10 BEOL 2D layer. To analyze true local variability within the random 2D logic pattern, the meaningful number of D2DB EPE data is collected from multiple locations across field and wafer using NGR3500 tool.

By utilizing a large amount of data acquired from massive e-beam metrology tool, clear local variability and suspicious hot spot point inside of specific 2D pattern was identified by statistical value. This result proves massive measurement of the entire geometry of various 2D pattern is necessary to optimize printability correctly.

As the byproduct of our analysis approach, the orientation-dependent systematic error which could be connected to 3D mask effect was proved by D2DB EPE analysis with 4 kinds of symmetry patterns. Furthermore, EPE augmented with the overlap area calculation based on contour from D2DB EPE revealed suspicious hot spot exposed to the risk of missing via in a quantitative way.

The result and methodology in this study can be utilized for deep analysis to understand the root cause of local variability which is affected by the nature of EUV characteristics as well as providing feedback for process optimization. As the following work, a thorough analysis of different random 2D logic patterns including all D2DB EPE features (tip, space, corner) has remained as the task.

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