Pattern Centric Yield Management Approach with Machine Learning to Detect and Track Defects with Full Chip Coverage

Yu Zhang, Shirui Yu, Jiaqi Liu, Renyang Meng, Yin Long, Kai Wang, Kun Cai, Xingdi Zhang, Xinghua Song, Jiadong Ren, Shanghai Huali Integrated Circuit Corporation, No. 6 Liangteng Rd., Pudong New Area, Shanghai, China 201314

Abhishek Vikram[‡], Changlian Yan, Guojie Cheng, Hui Wang, Qing Zhang, Wenkui Liao Anchor Semiconductor Inc., 668 East Beijing Road, East Building 19B, Shanghai, China 200001
[‡]3235 Kifer Rd, Suite 200, Santa Clara, CA 95051

ABSTRACT

The importance of pattern-based defect study has grown with more complex processes in advanced semiconductor manufacturing. The pattern is the heart of the DPTCO Design Process Technology Co-Optimization approach. But the definition of pattern has been limited by the design rules that can be setup by an individual. Moreover, the huge volume of data points generated by any DRC Design Rule Check type of search forces user to sort and filter out most of them and keep only a manageable count. This effectively reduces the sample space of pattern-based learning. In this work we have employed a new approach of PCYM Pattern Centric Yield Manager where the high count of unique patterns and all its instances in full chip design is retained. It is a fundamental pillar of computational system for semiconductor fabrication where pattern-centric learning can be deployed to study any related process [1-4].

Keywords: pattern centric yield manager, full chip pattern decomposition, pattern signature, pattern grouping, care area generation, defect sampling, machine learning.

1. INTRODUCTION

Pattern study has been a domain for CAD (computer Aided Design) community. The process modeling and simulation highly depends on accurate and early detection of pattern failures [5-8]. The metrology on wafer during key process steps is another checkpoint to detect any anomaly in the wafer [9, 10]. But they suffer from low throughput with limited wafer coverage. Optical wafer inspection is the workhorse of defect monitoring for past several technology nodes. With the advent of Deep Ultra-Violet (DUV) and Extreme Ultra Violet (EUV) regime the feature size on wafer has gone far below the resolution limit of any optical wafer inspection tool. In light of this challenge the burden of defect discovery is now shared by the high-resolution electron beam inspection. Still, this does not lower the steam for the optical inspection technique owing to its potential for full chip coverage. There have been several design guided methodologies adopted to direct the inspection tool to high-risk regions

[‡]Corresponding author contact: abhishek@anchorsemi.com

in the chip [11-15]. KLA's Nanopoint® allows such design guided definition of care areas for wafer inspection [16]. We have employed the PCYM to guide the Nanopoint® wafer inspection and the confirmed defect learning after SEM Scanning Electron Microscope review is fed back precisely to the impacted pattern in the PCYM database.

In this work we report the following with real case study–

(i) Full chip pattern decomposition into PCYM database

(ii) PCYM database driving intelligent defect inspection

(iii) Determining pattern risk with the feedback from confirmed wafer SEM Review

As shown in *Figure 1*, pattern based full chip design decomposition is done by creating PCYM map index. Pattern grouping is performed to establish inter correlation of patterns with full chip coverage. Some pre-defined pattern signatures are extracted and saved as attributes of pattern in the PCYM database. An intelligent machine learning based signature extraction is done on the full chip indexed patterns. This provides the specific feature vectors which have dominant impact on pattern centric variation on the wafer. This dynamic learning drives pattern sampling for wafer inspection care area setup. The wafer confirmation after SEM review is fed back to the PCYM database for improving the pattern learning. This PCYM based methodology captures the pattern behavior on a full chip scale with easy tracking capability.

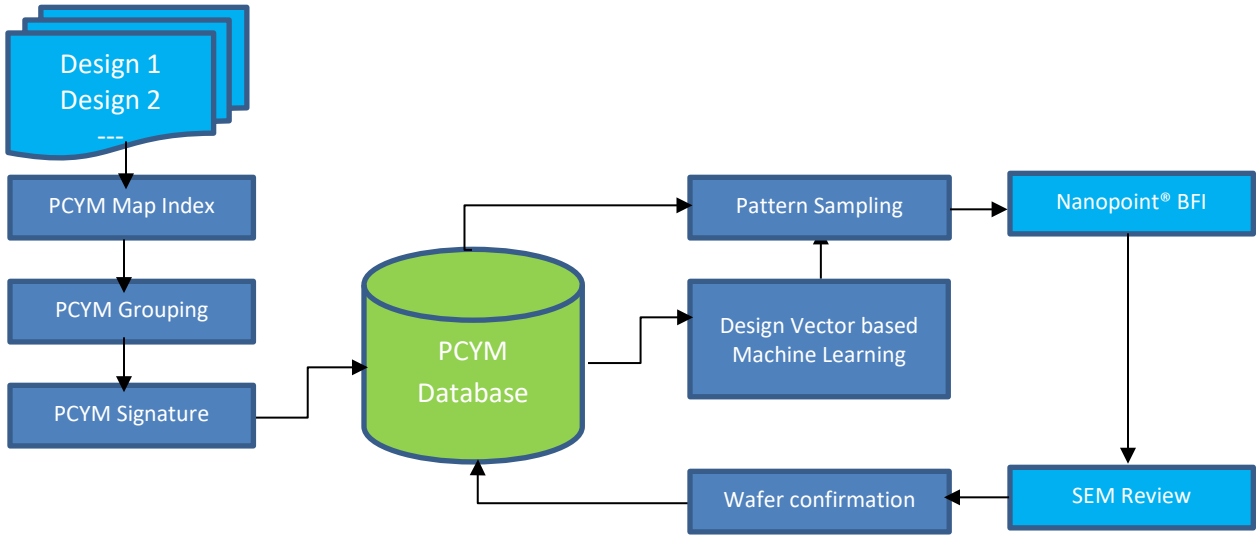

Figure 1 Data Flow for pattern centric inspection setup and wafer learning feedback

2. CASE STUDY

In this real case study sub-28nm technology device, optical wafer inspection monitor on a Mx layer was found to exhibit break and pinch defects at random locations, as shown in *Figure 2*. Visually they did not appear to be systematic issue and these locations were not captured by prior design verifications like DRC and OPC. Simple correlation of defects with physical parameters could not identify any specific root cause. Even after visual correlation of the defect SEM images with the associated current design layer clip did not indicate any obvious pattern issue.

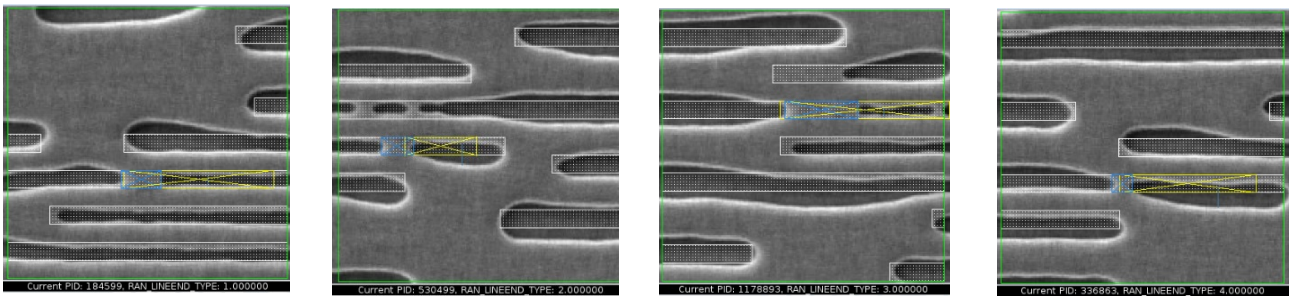

Figure 2 Examples of pinching and break defects found in Mx layer

We then utilized the automated SEM image-to-design alignment tool to see the overlaid image, as shown in *Figure 2*. An observation was made with further design analysis with upper and lower Via polygons, as shown in in *Figure 3*. There were four different types of patterns found based on relative locations of metal and Via polygons. It indicated that these defects were occurring mostly on long metal lines that were surrounded by other line ends along with upper and lower Via polygons. We utilized this observation to build multiple-layer PCYM rules to do full chip design decomposition. It is a unique capability where multiple design layer interaction can be used to decompose a full chip design. As shown in *Figure 1*, it first creates a map index of the target rule. There are multiple instances (sites) of the same design features. So, a pattern-based grouping reduces it to unique pattern groups, while keeping the information of all the instances of each unique pattern in the full chip design.

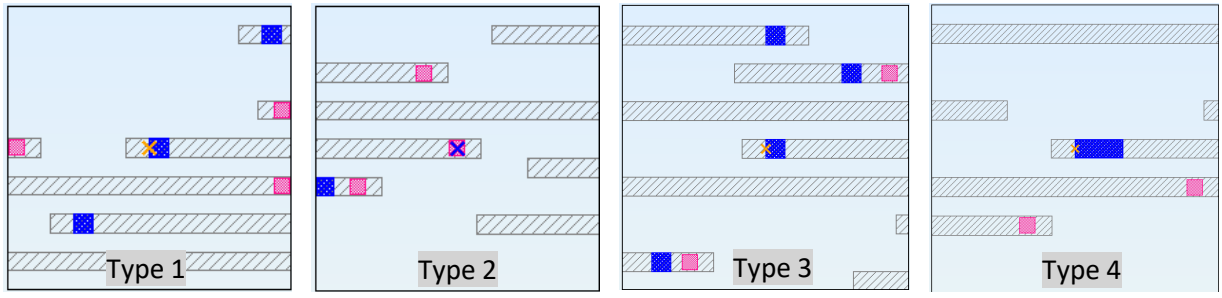

Figure 3 Corresponding design clip of Mx layer with upper and lower Via

Pattern signatures such as distance and relative location to the adjoining metal line, line-end and VIA polygons, are extracted for each of the pattern locations thus captured in the PCYM Database. Over 20 design vectors are extracted around the defect locations. Feature-to-feature correlation of 15 such signatures are shown as a matrix in *Figure 4*. None of the correlations were sufficiently significant to match with the pattern behavior on the wafer. Anchor's PCML Pattern Centric Machine Learning I was utilized to study all possible combinations of design vectors and rank them by importance, as shown in *Figure 5*.

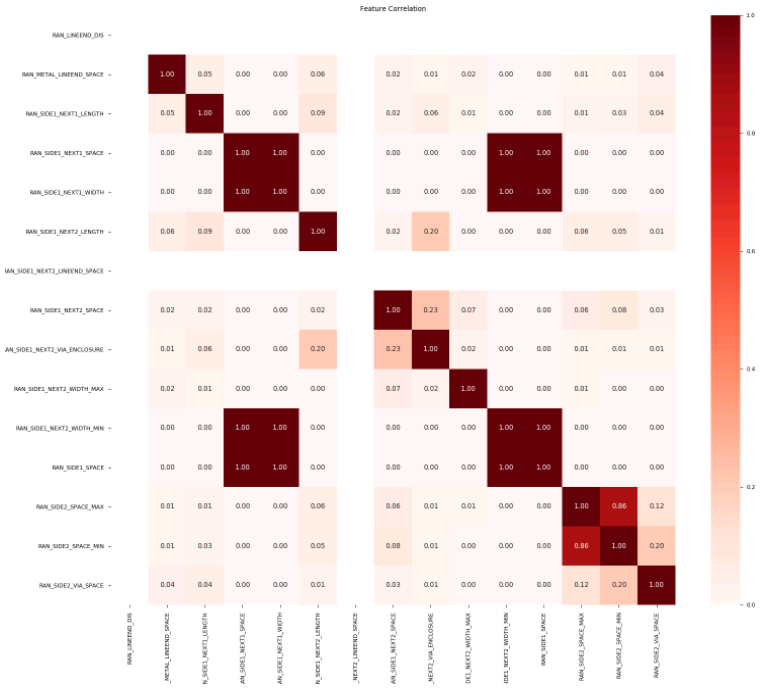

Figure 4 Design vector feature correlation

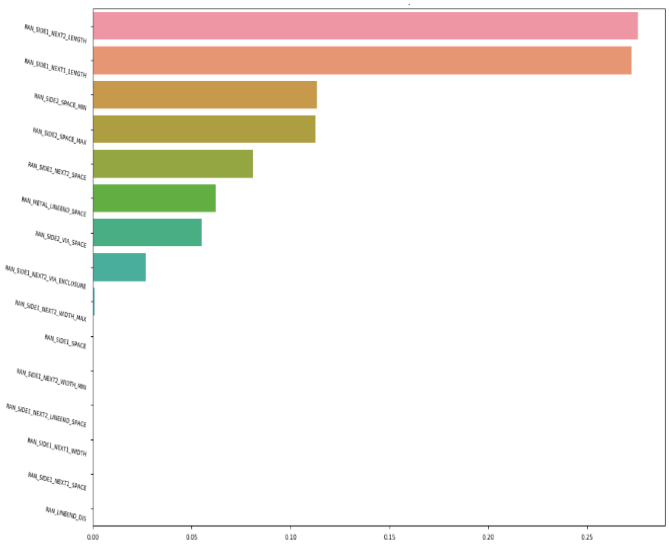

Figure 5 Feature importance ranked by PCML I

This is followed by the PCML II special application after binning the patterns by defect types. For each pattern type different features are considered to build the model. So, a machine learning model is calibrated for each pattern type. All the models are then used in tandem to assess the complete pattern data set. The patterns are scored with every model. These scores act like a new feature vector for further analysis. The patterns classified for high risk are given preference when performing pattern sampling, as shown in *Figure 6*. The sampling criteria is customized based on the application for doing full chip inspection or for targeted imaging. In this use case we performed classified sampling for generating care areas to feed into optical inspection.

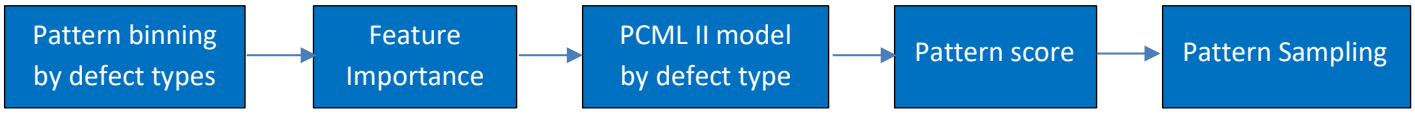

Figure 6 Scoring of patterns by defect type

3. RESULTS AND DISCUSSION

Pattern sampling is done by implementing user's preference as weights of several feature vectors to generate care area for KLA Nanopoint® wafer inspection setup. The *Table 1* shows the summary of findings for each type of pattern.

Table 1. Pattern Centric Yield Manager Case study summary with back end of line design layer

Pattern Type	*Count of Signature combination*	*Count sampled for inspection*	*Count SEM Reviewed*	*Sites measured in the SEM images*	*Sites measured had Pinch defect*
Type 1	1026169	29452	4854	70404	15137
Type 2	51259	17203		6155	615
Type 3	46588	16400		4085	855
Type 4	84039	30104		4991	353

The inline sampling from the inspection collected 4854 SEM review images. Multiple sites on each image were measured by the automated Die-to-Database offline engine at the targeted locations as was initially defined by the design vectors. It thus provides wafer measurement values for each design signature values. The amount of feature variation in wafer is captured by a Box Plot and it indicates the weakness of a particular design pattern. The *Figure 7* shows design measurements for one such design vector, distance between two lineends in the neighborhood, on the X-axis with histogram count of hard defects on the Y-axis. The secondary Y-axis shows the wafer measurement values at the same locations. The high counts of hard defect at any location can be correlated by the weakness captured in the associated wafer measurement, as reflected by large range of associated Box Plot and highlighted by red box in *Figure 7*. The real wafer measurement values serve as vital input for PCML III model building, as shown in the flow of *Figure 8*. It is then utilized to predict the weakness in the rest of the unseen patterns in PCYM DB that did not have SEM images collected.

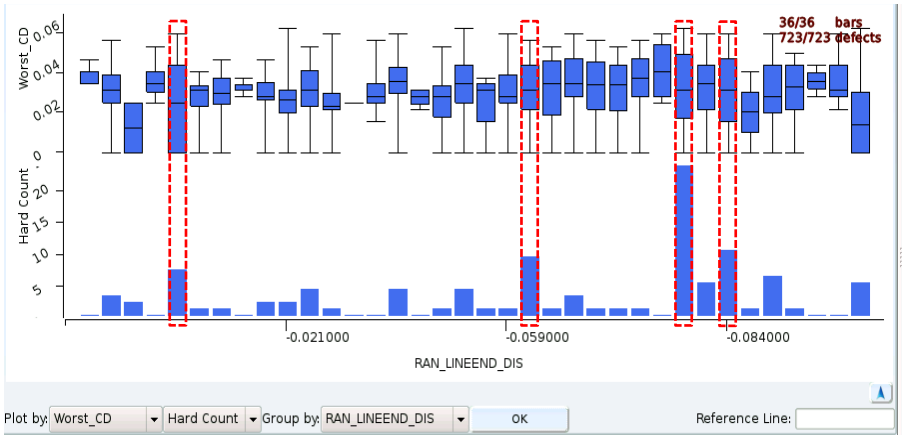

Figure 7 Lineend-to-lineend distance as measured in Design vs. Wafer with hard defect count

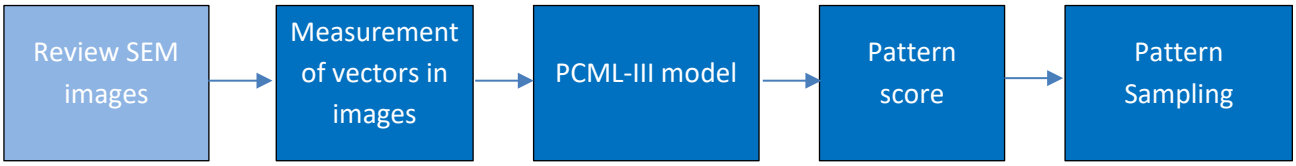

Figure 8 Using wafer measurements for pattern scoring

Several more locations that were sampled by the model were confirmed on wafer, as shown in *Figure 9*. In another case where sufficient defect detection was not found in first round, a second round of pattern sampling from PCML III guided the optical wafer inspection and confirmed the learning.

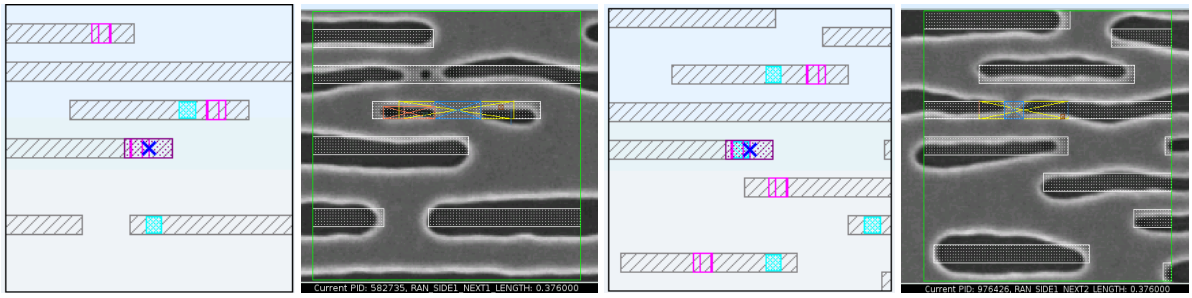

Figure 9 More risk locations that were confirmed on wafer

4. CONCLUSION

The Pattern Centric Yield Manager facilitated translation of defect observation to a pattern-centric platform. Multiple layer interactions (V_{x-1}-M_x-V_x) were captured even though the defect impact on wafer was visible only on a single layer M_x. A full chip design decomposition is achieved with preservation of every single instance of all unique patterns in the PCYM Database. The complete pattern information is mapped, indexed and available for analytics along with other design vectors extracted from around each pattern. The PCML-I engine helped to identify meaningful design vector combinations that factored in the defect mechanism. Further PCML-II special application by targeted defect types helped to improve the purity of pattern binning. Targeted pattern sampling then feeds the wafer inspection and review strategy. After SEM review images were available an automated image measurement and comparison to design was done to process millions of pattern data from thousands of SEM images to produce actionable results. The wafer measurements guided the standard PCML-III modeling to predict weakness in the rest of the unseen patterns in PCYM Database. The complete detail of every pattern is available throughout the flow for analysis to help in quick decision making. As a result of this exercise the team was able to find the root cause of a multiple layer process issue. We were able to communicate the relevant information to the OPC team who compensated to fix the issue in the revised mask. It helped us to build a reliable and complete pattern database for full chip

pattern management for each product design and track their multiple versions from the perspective of risk pattern coverage. The PCYM DB infrastructure along with the capability to integrate with the wafer image measurements has reduced the turnaround time in root cause analysis by at least four times. Once the full chip pattern database is in place then all pattern related analytics and wafer data correlation is trivial for the Yield Engineering module.

REFERENCES

[1] Khurram Zafar, Chenmin Hu, Ye Chen, Yue Ma, Chingyun Hsiang, Justin Chen, Raymond Xu, Abhishek Vikram, Ping Zhang, "Pattern weakness and strength detection and tracking during a semiconductor device fabrication process", US Patents #9,846,934 (2017), #10,062,160 (2018).

[2] Khurram Zafar, Chenmin Hu, Ye Chen, Yue Ma, Chingyun Hsiang, Justin Chen, Raymond Xu, Abhishek Vikram, Ping Zhang, "Pattern weakness and strength detection and tracking during a semiconductor device fabrication process", Taiwan Patents #I608427(2017), #I634485 (2018).

[3] Chenmin Hu, Khurram Zafar, Chen Ye, Ma Yue, Lv Rong, Justin Chen, Abhishek Vikram, Yuan Xu, Ping Zhang, "Pattern Centric Process Control", US Patent 10,546,085 (2020).

[4] Chenmin Hu, Khurram Zafar, Abhishek Vikram, Geoffrey Ying, “Pattern-Centric Computational System for Logic and Memory Manufacturing and Process Technology Development”, Journal of Microelectronics Manufacturing, Vol 3 (4): 20030410, 2020.

[5] Li-Fu Chang, Chang-Il Choi, Guojie Cheng, Abhishek Vikram, Gary Zhang, and Bo Su, "Detection of OPC conflict edges through MEEF analysis", Proc. SPIE 7641, Design for Manufacturability through Design-Process Integration IV, 764111, 2010.

[6] Eric Guo, Shirley Zhao, Skin Zhang, Sandy Qian, Guojie Cheng, Abhishek Vikram, Ling Li, Ye Chen, Chingyun Hsiang, Gary Zhang, and Bo Su, "Simulation based mask defect repair verification and disposition”, Proc. SPIE 7488, Photomask Technology 2009, 74880G, 2009.

[7] Eric Guo, Irene Shi, Blade Gao, Nancy Fan, Guojie Cheng, Li Ling, Ke Zhou, Gary Zhang, Ye Chen, Chingyun Hsiang, and Bo Su, "Simulation based mask defect printability verification and disposition, part II", Proc. SPIE 8166, Photomask Technology 2011, 81662D, 2011.

[8] Gyun Yoo, Jungchan Kim, Taehyeong Lee, Areum Jung, Hyunjo Yang, Donggyu Yim, Sungki Park, Kotaro Maruyama, Masahiro Yamamoto, Abhishek Vikram, Sangho Park, "OPC verification and hotspot management for yield enhancement through layout analysis", Metrology, Inspection, and Process Control for Microlithography XXV, Proc. of SPIE Vol. 7971, 79710H, 2011.

[9] Taehyeong Lee, Hyunjo Yang, Jungchan Kim, Areum Jung, Gyun Yoo, Donggyu Yim, Sungki Park, Akio Ishikawa, Masahiro Yamamoto, Abhishek Vikram, "Hot spot management through design-based metrology: measurement and filtering", Proc. SPIE. Vol. 7520, 75201U, 2009.

[10] Sicong Wang, Jian Mi, Abhishek Vikram, Gao Xu, Guojie Cheng, Liming Zhang, Pan Liu, "Novel pattern-centric solution for high performance 3D NAND VIA dishing metrology", Design-Process-Technology Co-optimization for Manufacturability XIII, SPIE Vol. 10962, 1096217, 2019.

[11] Jing Zhang, Qingxiu Xu, Xin Zhang, Xing Zhao, Jay Ning, Guojie Cheng, Shijie Chen, Gary Zhang, Abhishek Vikram, Bo Su, "Yield impacting systematic defects search and management", Design for Manufacturability through Design-Process Integration VI, Proc. of SPIE Vol. 8327, 832716, 2012.

[12] Qian Xie, Panneerselvam Venkatachalam, Julie Lee, Zhijin Chen, Khurram Zafar, "Design guided data analysis for summarizing systematic pattern defects and process window", Proc. SPIE. 9778, Metrology, Inspection, and Process Control for Microlithography XXX Proceedings Article, 2016.

[13] Qian Xie, Panneerselvam Venkatachalam, Julie Lee, Zhijin Chen, Khurram Zafar, "Precise design-based defect characterization and root cause analysis", Proc. SPIE. 10145, Metrology, Inspection, and Process Control for Microlithography XXXI Proceedings Article, 2017.

[14] Ming Tian, Yu Zhang, Tiapeng Guan, Jianghua Leng, Baojun Zhao, Lei Yan, Wei Hua, Abhishek Vikram, Guojie Chen, Hui Wang, Gary Zhang, Wenkui Liao, "Critical Defect Detection, Monitoring and Fix through Process Integration Engineering by Using D2DB Pattern Monitor Solution", Design-Process-Technology Co-optimization for Manufacturability XIII, SPIE Vol. 10962, 109620L, 2019.

[15] Lijun Chen, Jun Zhu, Xuedong Fan, Haichang Zheng, Xiaolong Wang, Yancong Ge, Yu Zhang, Abhishek Vikram, Guojie Cheng, Hui Wang, Qing Zhang, Wenkui Liao, "An Advanced and Efficient Methodology for Process Setup and Monitoring by Using Process Stability Diagnosis in Computational Lithography", Design-Process-Technology Co-optimization for Manufacturability XIV, Proc. SPIE. 11328, 2020.

[16] Abhishek Vikram, Kuan Lin, Janay Camp, Sumanth Kini, Frank Jin, Vinod Venkatesan, “Inspection of high-aspect ratio layers at sub 20nm node”, Metrology, Inspection, and Process Control for Microlithography XXVII, Proc. of SPIE Vol. 8681, 86811Q, 2013.