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EE272
Cover Groups Assignment

Tests

dashboard | hierarchy | modlist | groups | tests | asserts

Assertions are 100% covered

Total Coverage Summary

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	GROUP
98.55	97.73	100.00	95.00		100.00	100.00

100% coverage on both cover groups

Total tests in report: 1

Data from the following tests was used to generate this report
simv/test1

dashboard | hierarchy | modlist | groups | tests | asserts

Dashboard

dashboard | hierarchy | modlist | groups | tests | asserts

Date: Mon Nov 13 20:43:57 2017
User: 010754159
Version: I-2014.03-2
Command line: urg -dir ./simv.vdb -format both

Total Coverage Summary

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	GROUP
98.55	97.73	100.00	95.00		100.00	100.00

Total Coverage of 98.5% Aseertions and groups are 100% co

Hierarchical coverage data for top-level instances

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	NAME
98.18	97.73	100.00	95.00		100.00	testbench

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Assertions

Assertions by Category

	ASSERT	PROPERTIES	SEQUENCES
Total	13	0	0
Category 0	13	0	0

Assertions by Severity

	ASSERT	PROPERTIES	SEQUENCES
Total	13	0	0
Severity 0	13	0	0

Summary for Assertions

	NUMBER	PERCENT
Total Number	13	100.00
Not Covered	0	0.00
At Least 1 Real Success	13	100.00
At Least 1 Failure	11	84.62
At Least 1 Incomplete	1	7.69
Without Attempts	0	0.00

Detail Report for Assertions

Assertions At Least 1 Real Success:

ASSERTIONS	CATEGORY	SEVERITY	ATTEMPTS	REAL SUCCESSES	FAILURES	INCOMPLETE
testbench.d.unnamed$$_1	0	0	4010	10	0	0
testbench.d.unnamed$$_10	0	0	4010	175	131	0
testbench.d.unnamed$$_11	0	0	4010	91	0	0
testbench.d.unnamed$$_12	0	0	4010	16	31	0
testbench.d.unnamed$$_13	0	0	4010	10	16	0
testbench.d.unnamed$$_2	0	0	4010	118	99	0

Name	Attempts	Real Successes	Failures	Incomplete
unnamed$$_1	4010	10	0	0
unnamed$$_10	4010	175	131	0
unnamed$$_11	4010	91	0	0
unnamed$$_12	4010	16	31	0
unnamed$$_13	4010	10	16	0
unnamed$$_2	4010	118	99	0
unnamed$$_3	4010	240	303	0
unnamed$$_4	4010	241	313	0
unnamed$$_5	4010	225	227	1
unnamed$$_6	4010	244	250	0
unnamed$$_7	4010	201	262	0
unnamed$$_8	4010	193	227	0
unnamed$$_9	4010	189	197	0

Due to bugged in testbench, we see failures here

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Module Instance : testbench.d

Instance :

SCORE	LINE	COND	TOGGLE	FSM	ASSERT
100.00	100.00				100.00

Instance's subtree :

SCORE	LINE	COND	TOGGLE	FSM	ASSERT
100.00	100.00				100.00

Module :

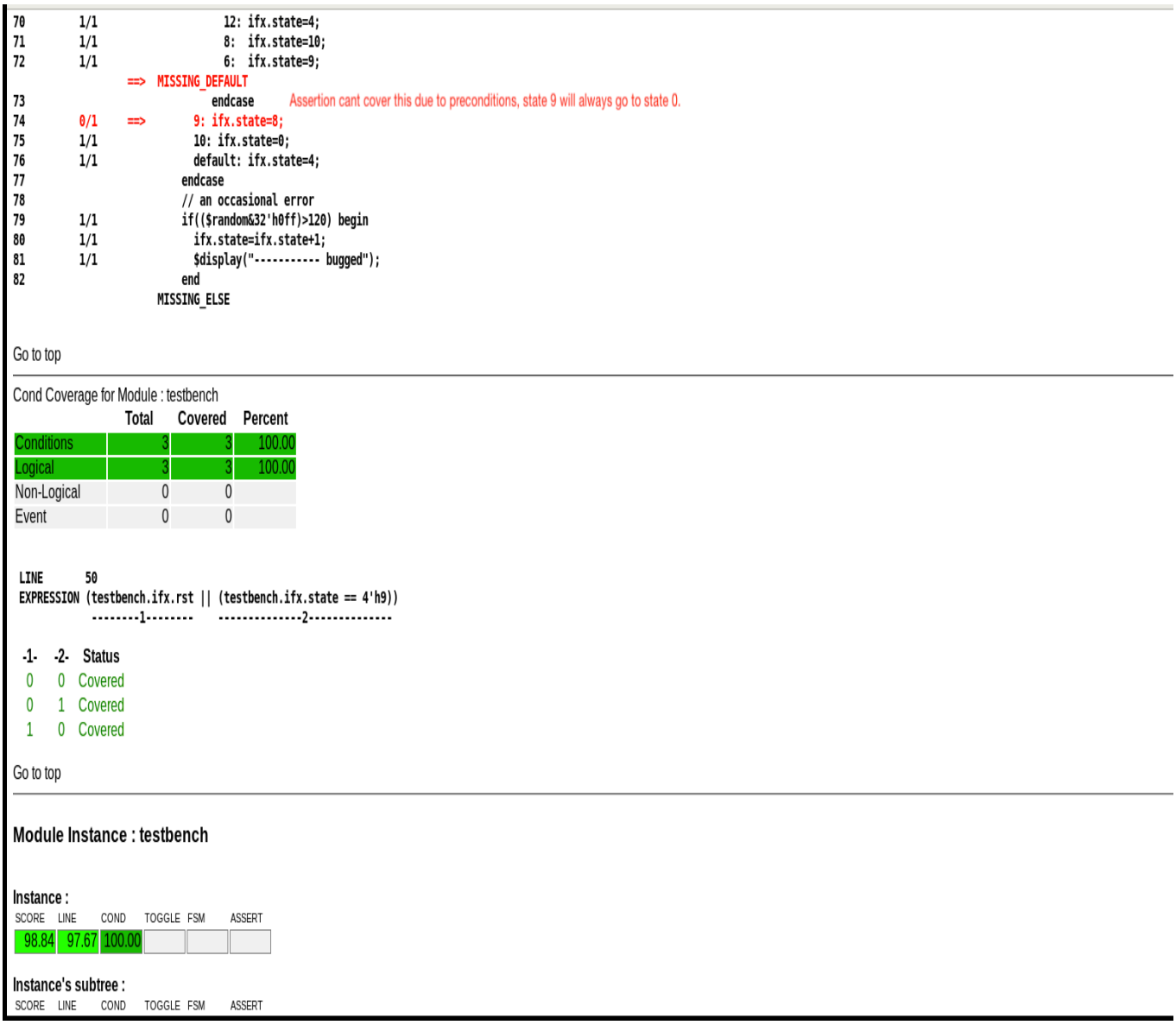
SCORE	LINE	COND	TOGGLE	FSM	ASSERT	NAME
100.00	100.00				100.00	dut

Parent :

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	NAME
98.84	97.67	100.00				testbench

Subtrees :

no children



```
70        1/1                  12: ifx.state=4;
71        1/1                  8:  ifx.state=10;
72        1/1                  6:  ifx.state=9;
                 ==>  MISSING_DEFAULT
73                             endcase      Assertion cant cover this due to preconditions, state 9 will always go to state 0.
74        0/1      ==>       9: ifx.state=8;
75        1/1                 10: ifx.state=0;
76        1/1                 default: ifx.state=4;
77                          endcase
78                          // an occasional error
79        1/1               if(($random&32'h0ff)>120) begin
80        1/1                 ifx.state=ifx.state+1;
81        1/1                 $display("---------- bugged");
82                          end
                       MISSING_ELSE
```

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Cond Coverage for Module : testbench

	Total	Covered	Percent
Conditions	3	3	100.00
Logical	3	3	100.00
Non-Logical	0	0	
Event	0	0	

```
LINE       50
EXPRESSION (testbench.ifx.rst || (testbench.ifx.state == 4'h9))
            --------1--------    -------------2-------------
```

-1-	-2-	Status
0	0	Covered
0	1	Covered
1	0	Covered

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Module Instance : testbench

Instance :

SCORE	LINE	COND	TOGGLE	FSM	ASSERT
98.84	97.67	100.00			

Instance's subtree :

SCORE	LINE	COND	TOGGLE	FSM	ASSERT

Assertions cannot cover the missing default because state 9 never goes to state 8.

Two Cover groups to cover states and reset.

Testbench Group List

Total Groups Coverage Summary

SCORE	WEIGHT
100.00	1

Total groups in report: 2

SCORE	WEIGHT	GOAL	AT LEAST	PER INSTANCE	AUTO BIN MAX	PRINT MISSING	COMMENT	NAME
100.00	1	100	1	0	64	64		testbench.d::dutcg
100.00	1	100	1	0	64	64		testbench.d::cgr

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Group : testbench.d::dutcg

SCORE	WEIGHT	GOAL	AT LEAST	PER INSTANCE	AUTO BIN MAX	PRINT MISSING	COMMENT
100.00	1	100	1	0	64	64	

Summary for Group testbench.d::dutcg

CATEGORY	EXPECTED	UNCOVERED	COVERED	PERCENT
Variables	12	0	12	100.00

Variables for Group testbench.d::dutcg

VARIABLE	EXPECTED	UNCOVERED	COVERED	PERCENT	GOAL	WEIGHT	AT LEAST	AUTO BIN MAX	COMMENT
state_coverage	12	0	12	100.00	100	1	1	0	

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Summary for Variable state_coverage

CATEGORY	EXPECTED	UNCOVERED	COVERED	PERCENT
User Defined Bins	12	0	12	100.00

User Defined Bins for state_coverage

Bins

NAME	COUNT	AT LEAST
s12	10	1
s11	16	1
s10	91	1
s9	175	1
s8	189	1
s7	193	1
s6	201	1
s5	244	1
s4	225	1
s3	241	1
s2	240	1
s1	128	1

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There are 12 bins for the 12 expected test cases an all of them are met.

Design Module List

Total Module Definition Coverage Summary

SCORE	LINE	COND	TOGGLE	FSM	ASSERT
98.18	97.73	100.00	95.00		100.00

Total modules in report: 3

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	NAME
95.00			95.00			intf
98.84	97.67	100.00				testbench
100.00	100.00				100.00	dut

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Module : testbench

SCORE	LINE	COND	TOGGLE	FSM	ASSERT
98.84	97.67	100.00			

Source File(s) :
/home/010754159@SJSUAD.SJSU.EDU/EECE272/assertions/assertions/tbsm.sv

Module self-instances :

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	NAME
98.84	97.67	100.00				testbench

Line Coverage for Module : testbench

	Line No.	Total	Covered	Percent
TOTAL		43	42	97.67
INITIAL	28	9	9	100.00
INITIAL	41	7	7	100.00
ALWAYS	49	27	26	96.30

Can never be 100% due to bugged

```
27                      initial begin
28          1/1           ifx.state=0;
29          1/1           ifx.clk=0;
30          1/1           ifx.rst=1;
31          1/1           ##10;
32          1/1           ifx.rst=0;
33                      //  while(cv2.cp2.get_coverage()<25) ##5;
34          1/1           ##4000;
35          1/1           $display("\n\n\nAt the end of the run\n\n\n");
36          1/1           $display("Time is ",$time);
37          1/1           $finish;
38                      end
39
40                      initial begin
41          1/1           ifx.clk=0;
42          2/2           forever #5 begin
43          1/1             ifx.clk=~ifx.clk;
44          3/3             if(ifx.clk==1) #1 -> fun;
                        MISSING_ELSE
45                        end
46                      end
47
48                      always @(fun) begin
49          1/1           ifx.old_state=ifx.state;
```

Design Hierarchy

SCORE	LINE	COND	TOGGLE	FSM	ASSERT	
98.18	97.73	100.00	95.00		100.00	testbench
SCORE	LINE	COND	TOGGLE	FSM	ASSERT	
100.00	100.00				100.00	d
95.00			95.00			ifx

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```
covergroup dutcg @(posedge ix.clk);

     state_coverage: coverpoint ix.state
     {

      bins s1 = (0 => 1,0);
      bins s2 = (1 => 2,4);
      bins s3 = (2 => 3);
      bins s4 = (3 => 5,1);
      bins s5 = (4 => 5);
      bins s6 = (5 => 1,6);
      bins s7 = (6 => 7);
      bins s8 = (7 => 0,8);
      bins s9 = (8 => 2,4,10,9);
      bins s10 = (9 => 0,8);
      bins s11 = (10 => 0);
      bins s12 = (11 => 4);

     }

endgroup

dutcg cg= new();

covergroup cgr @(posedge ix.clk);
reset_coverage: coverpoint ix.rst
{
bins r0 =  (1 => 0);
//bins r1 = (0 => 1);
}
endgroup

cgr cg2 = new();

endmodule
```