Giovanni Funchal Ph.D student -- STMicro/Verimag (2008 - 2011)



- General topic: Definition of the notions of <u>component</u> and <u>abstraction-level</u> for TLM
 - How to write models that are correct by construction?
 - How to avoid common modeling errors?
 - How to integrate models so that they "work" together?

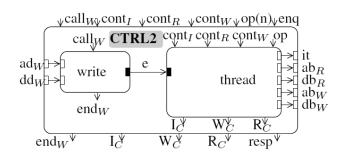
Theoretical and fundamental modeling issues

Simulator implementation-dependent issues

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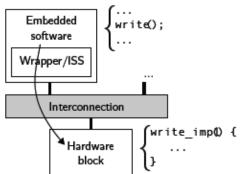
Theoretical and fundamental modeling issues

Formal and Executable Contracts for TLM in SystemC (EMSOFT'09)



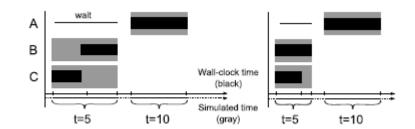
- Connection between formal approach and SystemC
- Enables reasoning about composition even if only part of the platform is implemented

- Faithfulness Considerations for Virtual Prototyping of Systems-on-Chip (RAPIDO'11)
 - Some micro-architectural features (caches, fifos, reordering pipelines, prefetch buffers) can impact the behavior of software in a virtual prototype

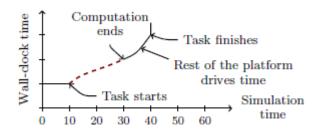


Simulator implementation-dependent issues

- jTLM: an Experimentation Framework for the Simulation of TL Models (DATE'11)
 - A framework for research on issues that originate or depend on a particular simulator implementation choice



- e.g. wait(SC_ZERO_TIME)
- Cooperative/preemptive, sequential/parallel
- Modeling of Time in Discrete-Event Simulation of Systems-on-Chip (submitted to MEMOCODE'11)



- Propose new semantics and primitives for modeling time
- Tasks with a known or unknown duration (SystemC has only instantaneous tasks and delays)