Design Rules Verification Report

Filename : W:\GreenfieldTechSolutions\Projects\Ontwerpen\Project_234_BAS\PCB\BAS_Tower1\Tower1.PcbDoc

Warnings 0
Rule Violations 0
Waived Violations 2

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.15mm) (InNet('NetC104_1')),(All)	0
Clearance Constraint (Gap=0.1mm) (All),(All)	0
Clearance Constraint (Gap=0mm) (All),(All)	0
Clearance Constraint (Gap=0.1mm) ((InDifferentialPairClass('All Differential Pairs'))),(All)	0
Clearance Constraint (Gap=0.175mm) (InNet('VPWR') or InNet('Vin') or InNet('PWR')),(All)	0
Clearance Constraint (Gap=0.2mm) (InNet('+12V') or InNet('+5V')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=20mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.125mm) (Max=5mm) (Preferred=1mm) (InNet('VIN'))	0
Width Constraint (Min=0.75mm) (Max=2mm) (Preferred=1mm) (InNet('+12V'))	0
Width Constraint (Min=0.2mm) (Max=2mm) (Preferred=0.7mm) (InNet('VPWR'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.1mm) (All)	0
Hole Size Constraint (Min=0.095mm) (Max=20mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (OnLayer('Top Overlay') or OnLayer('Bottom Overlay'))	0
Board Clearance Constraint (Gap=0mm) (All)	0
Matched Lengths(Tolerance=12.6mm) (InDifferentialPair ('USBF0') Or (InDifferentialPair('USBF0_RX')and	0
Matched Lengths(Tolerance=12.6mm) (InDifferentialPair ('USBF1') Or (InDifferentialPair('USBF1_RX')and	0
Matched Lengths(Tolerance=12.6mm) (InDifferentialPair ('USBG') Or (InDifferentialPair('USBG_RX')and	0
Matched Lengths(Tolerance=12.6mm) (InDifferentialPair ('USB0') Or InDifferentialPair ('USB0_RX') Or	0
Matched Lengths(Tolerance=12.6mm) (InDifferentialPair('USBG_TX2') or InDifferentialPair('USBG_RX2'))	0
Matched Lengths(Tolerance=12.6mm) (InDifferentialPair('USBG_TX1') or InDifferentialPair('USBG_RX1'))	0
Matched Lengths(Tolerance=1.27mm) (InNetClass('SD'))	0
Matched Lengths(Tolerance=0.127mm) (InDifferentialPairClass('USB3'))	0
Matched Lengths(Tolerance=12mm) (InDifferentialPairClass('HDMI'))	0
Matched Lengths(Tolerance=0.127mm) (InDifferentialPairClass('PCIE'))	0
Matched Lengths(Tolerance=1.27mm) (InDifferentialPair('USBG') or InDifferentialPair('USB0') or	0
Matched Lengths(Tolerance=12mm) (InDifferentialPair ('PCIE_CLK') or InDifferentialPair ('PCIE_RX') or	0
Matched Lengths(Tolerance=0.127mm) (InDifferentialPairClass('HDMI'))	0
Height Constraint (Min=0mm) (Max=100mm) (Prefered=12.7mm) (All)	0
Total	0

Waived Violations	
Board Clearance Constraint (Gap=0mm) (All)	2
Total	2

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Pad CO102-H(88mm,53mm) on Multi-Layer Waived by Jonathan
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Pad CO1-H(251.25mm,75mm) on Multi-Layer Waived by