Design Rules Verification Report

Filename : W:\GreenfieldTechSolutions\Projects\Ontwerpen\Project_234_BAS\PCB\BAS_DevKIT\DevKIT.PcbDoc

Warnings 0
Rule Violations 2
Waived Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.1mm) (All),(OnLayer('Top Layer') or OnLayer('Bottom Layer'))	0
Clearance Constraint (Gap=0.475mm) (InNet('VPWR') or InNet('VIN') or InNet('PWR')),(All)	0
Clearance Constraint (Gap=0.125mm) ((InDifferentialPairClass('All Differential Pairs'))),(All)	0
Clearance Constraint (Gap=0.125mm) (All),(All)	0
Clearance Constraint (Gap=0.15mm) (InNet('NetC104_1') or InNet('1V8_OUT')),(All)	0
Clearance Constraint (Gap=0mm) (All),(All)	0
Clearance Constraint (Gap=0.1mm) ((InDifferentialPairClass('All Differential Pairs'))),(OnLayer('Top Layer') or	0
Clearance Constraint (Gap=0.3mm) (InNet('+12V') or InNet('+5V') or InNet('+5VR')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	1
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.75mm) (Max=2mm) (Preferred=1mm) (InNet('VIN'))	0
Width Constraint (Min=0.125mm) (Max=20mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.75mm) (Max=2mm) (Preferred=1mm) (InNet('+12V'))	0
Width Constraint (Min=0.5mm) (Max=2mm) (Preferred=0.7mm) (InNet('VPWR'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.124mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=20mm) (All)	0
Hole To Hole Clearance (Gap=0.125mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	1
Board Clearance Constraint (Gap=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (OnLayer('Top Overlay') or OnLayer('Bottom Overlay'))	0
Matched Lengths(Tolerance=1.27mm) (InDifferentialPairClass('HDMI'))	0
Matched Lengths(Tolerance=5mm) (InNetClass('SD'))	0
Matched Lengths(Tolerance=12mm) (InDifferentialPair ('USBF1') Or InDifferentialPair ('USBF1_RX') Or	0
Matched Lengths(Tolerance=0.127mm) (InNetClass('SDASCL'))	0
Matched Lengths(Tolerance=0.127mm) (InNetClass('I2C'))	0
Matched Lengths(Tolerance=0.127mm) (InNetClass('SPI'))	0
Matched Lengths(Tolerance=12mm) (InDifferentialPair ('USBF2') Or InDifferentialPair ('USBF2_RX') Or	0
Matched Lengths(Tolerance=0.127mm) (InDifferentialPairClass('HDMI'))	0
Matched Lengths(Tolerance=0.127mm) (InDifferentialPairClass('USB3'))	0
Matched Lengths(Tolerance=12mm) (InDifferentialPair ('USBF0') Or InDifferentialPair ('USBF0_RX') Or	0
Height Constraint (Min=0mm) (Max=100mm) (Prefered=12.7mm) (All)	0
Total	2

Waived Violations	
Board Clearance Constraint (Gap=0mm) (All)	1
Total	1

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net +3V3 Between Track (113.275mm,50.5mm)(114.95mm,48.825mm) on Bottom Layer And Track

Net Antennae (Tolerance=0mm) (All)
Net Antennae: Track (113.275mm,50.5mm)(114.95mm,48.825mm) on Bottom Layer

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Pad CO501-H(152mm,130mm) on Multi-Layer Waived by