Design Rules Verification Report

Filename : W:\GreenfieldTechSolutions\Projects\Ontwerpen\Project_234_BAS\PCB\BAS_Dev

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.1mm) (All),(OnLayer('Top Layer') or OnLayer('Bottom Layer'))	0
Clearance Constraint (Gap=0.1mm) ((InDifferentialPairClass('All Differential Pairs'))),(OnLayer('Top Layer') or	0
Clearance Constraint (Gap=0.3mm) (InNet('+12V') or InNet('+5V')),(All)	0
Clearance Constraint (Gap=0mm) (All),(All)	0
Clearance Constraint (Gap=0.15mm) (InNet('NetC104_1')),(All)	0
Clearance Constraint (Gap=0.475mm) (InNet('VPWR') or InNet('VIN') or InNet('PWR')),(All)	0
Clearance Constraint (Gap=0.125mm) (All),(All)	0
Clearance Constraint (Gap=0.125mm) ((InDifferentialPairClass('All Differential Pairs'))),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.5mm) (Max=2mm) (Preferred=0.7mm) (InNet('VPWR'))	0
Width Constraint (Min=0.75mm) (Max=2mm) (Preferred=1mm) (InNet('VIN'))	0
Width Constraint (Min=0.125mm) (Max=20mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.75mm) (Max=2mm) (Preferred=1mm) (InNet('+12V'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.124mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=20mm) (All)	0
Hole To Hole Clearance (Gap=0.125mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (OnLayer('Top Overlay') or OnLayer('Bottom Overlay'))	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=100mm) (Prefered=12.7mm) (All)	0
Total	0