Design Rules Verification Report

Filename : W:\GreenfieldTechSolutions\Projects\Ontwerpen\Project_234_BAS\PCB\BAS_T

Warnings 0
Rule Violations 130

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.15mm) (InNet('NetC104_1')),(All)	0
Clearance Constraint (Gap=0.2mm) (InNet('+12V') or InNet('+5V')),(All)	0
Clearance Constraint (Gap=0mm) (All),(All)	0
Clearance Constraint (Gap=0.105mm) (All),(All)	6
Clearance Constraint (Gap=0.105mm) ((InDifferentialPairClass('All Differential Pairs'))),(All)	74
Clearance Constraint (Gap=0.2mm) (InNet('VPWR') or InNet('Vin') or InNet('PWR')),(All)	24
Short-Circuit Constraint (Allowed=No) (All),(All)	6
Un-Routed Net Constraint ((All))	2
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=20mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.5mm) (Max=2mm) (Preferred=0.7mm) (InNet('VPWR'))	0
Width Constraint (Min=0.75mm) (Max=2mm) (Preferred=1mm) (InNet('+12V'))	0
Width Constraint (Min=0.125mm) (Max=5mm) (Preferred=1mm) (InNet('VIN'))	0
Minimum Annular Ring (Minimum=0.124mm) (All)	12
Hole Size Constraint (Min=0.025mm) (Max=20mm) (All)	0
Hole To Hole Clearance (Gap=0.125mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (OnLayer('Top Overlay') or OnLayer('Bottom Overlay'))	0
Board Clearance Constraint (Gap=0mm) (All)	6
Height Constraint (Min=0mm) (Max=100mm) (Prefered=12.7mm) (All)	0
Total	130

Clearance Constraint (Gap=0.105mm) (All),(All)
Clearance Constraint: (0.102mm < 0.105mm) Between Track (156.5mm,94.6mm)(157mm,94.1mm) on Top Layer And Via (157.033mm,94.6mm) from Top
Clearance Constraint: (0.05mm < 0.105mm) Between Via (166.6mm,89.693mm) from Top Layer to Bottom Layer And Via (167mm,89.693mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (234.4mm,89.6mm) from Top Layer to Bottom Layer And Via (234.4mm,90mm) from Top Layer to
Clearance Constraint: (0.1mm < 0.105mm) Between Via (234.4mm,90mm) from Top Layer to Bottom Layer And Via (234.8mm,90mm) from Top Layer to
Clearance Constraint: (0.1mm < 0.105mm) Between Via (234.8mm,90.4mm) from Top Layer to Bottom Layer And Via (234.8mm,90mm) from Top Layer to
Clearance Constraint: (0.1mm < 0.105mm) Between Via (234.8mm,90.4mm) from Top Layer to Bottom Layer And Via (235.2mm,90.4mm) from Top Layer

Clearance Constraint (Gap=0.105mm) ((InDifferentialPairClass('All Differential Pairs'))),(All)
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-11(122.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-11(122.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-11(122.75mm,59.6mm) on Top Layer And Track
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Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-11(122.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-11(122.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-2(127.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-2(127.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-2(127.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-2(127.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-2(127.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-2(127.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-5(125.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-5(125.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-5(125.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-5(125.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-5(125.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-5(125.75mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-8(124.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-8(124.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-8(124.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO103-8(124.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-8(124.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.104mm < 0.105mm) Between Pad CO103-8(124.25mm,59.6mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO301-0(108mm,71.25mm) on Multi-Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO301-0(108mm,71.25mm) on Multi-Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO301-0(108mm,71.25mm) on Multi-Layer And Track
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Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO301-0(108mm,71.25mm) on Multi-Layer And Track
Clearance Constraint: (0.103mm < 0.105mm) Between Pad CO301-21(107.17mm,72.25mm) on Top Layer And Track
Clearance Constraint: (0.103mm < 0.105mm) Between Pad CO301-22(107.17mm,72.75mm) on Top Layer And Track
Clearance Constraint: (0.103mm < 0.105mm) Between Pad CO301-22(107.17mm,72.75mm) on Top Layer And Track
Clearance Constraint: (0.101mm < 0.105mm) Between Pad CO301-3(108.83mm,76.75mm) on Top Layer And Track
Clearance Constraint: (0.101mm < 0.105mm) Between Pad CO301-3(108.83mm,76.75mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO301-SH(106.865mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO301-SH(106.865mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO301-SH(109.135mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO301-SH(109.135mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO301-SH(110.15mm,77.4mm) on Multi-Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO302-0(125mm,71.25mm) on Multi-Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO302-0(125mm,71.25mm) on Multi-Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO302-0(125mm,71.25mm) on Multi-Layer And Track
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Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO302-0(125mm,71.25mm) on Multi-Layer And Track
Clearance Constraint: (0.103mm < 0.105mm) Between Pad CO302-21(124.17mm,72.25mm) on Top Layer And Track
Clearance Constraint: (0.103mm < 0.105mm) Between Pad CO302-22(124.17mm,72.75mm) on Top Layer And Track
Clearance Constraint: (0.103mm < 0.105mm) Between Pad CO302-22(124.17mm,72.75mm) on Top Layer And Track
Clearance Constraint: (0.101mm < 0.105mm) Between Pad CO302-3(125.83mm,76.75mm) on Top Layer And Track
Clearance Constraint: (0.101mm < 0.105mm) Between Pad CO302-3(125.83mm,76.75mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO302-SH(123.865mm,71.12mm) on Top Layer And Track

Clearance Constraint (Gap=0.105mm) ((InDifferentialPairClass('All Differential Pairs'))),(All)
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO302-SH(123.865mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO302-SH(126.135mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.102mm < 0.105mm) Between Pad CO302-SH(126.135mm,71.12mm) on Top Layer And Track
Clearance Constraint: (0.1mm < 0.105mm) Between Pad CO302-SH(127.15mm,77.4mm) on Multi-Layer And Track
Clearance Constraint: (0.051mm < 0.105mm) Between Polygon Region (276 hole(s)) Layer 2 And Track (233.395mm,75.314mm)(233.395mm,76.199mm)
Clearance Constraint: (0.054mm < 0.105mm) Between Polygon Region (276 hole(s)) Layer 2 And Track (233.395mm,75.314mm)(233.944mm,74.765mm)
Clearance Constraint: (0.051mm < 0.105mm) Between Polygon Region (276 hole(s)) Layer 2 And Track (233.395mm,76.199mm)(233.621mm,76.425mm)
Clearance Constraint: (0.076mm < 0.105mm) Between Polygon Region (276 hole(s)) Layer 2 And Track (233.621mm,76.425mm)(234.588mm,76.425mm)
Clearance Constraint: (0.1mm < 0.105mm) Between Via (107.422mm,75.235mm) from Top Layer to Bottom Layer And Via (107.42mm,74.785mm) from
Clearance Constraint: (0.1mm < 0.105mm) Between Via (108.875mm,74.777mm) from Top Layer to Bottom Layer And Via (108.875mm,75.228mm) from
Clearance Constraint: (0.1mm < 0.105mm) Between Via (124.422mm,75.235mm) from Top Layer to Bottom Layer And Via (124.42mm,74.785mm) from
Clearance Constraint: (0.1mm < 0.105mm) Between Via (125.875mm,74.777mm) from Top Layer to Bottom Layer And Via (125.875mm,75.228mm) from
Clearance Constraint: (0.1mm < 0.105mm) Between Via (138.235mm,65.6mm) from Top Layer to Bottom Layer And Via (138.685mm,65.6mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (140.435mm,65.6mm) from Top Layer to Bottom Layer And Via (140.885mm,65.6mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (142.435mm,65.6mm) from Top Layer to Bottom Layer And Via (142.885mm,65.6mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (152.6mm,63.935mm) from Top Layer to Bottom Layer And Via (152.6mm,64.385mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (152.6mm,65.035mm) from Top Layer to Bottom Layer And Via (152.6mm,65.485mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (152.6mm,66.235mm) from Top Layer to Bottom Layer And Via (152.6mm,66.685mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (219mm,79.915mm) from Top Layer to Bottom Layer And Via (219mm,80.365mm) from Top Layer
Clearance Constraint: (0.1mm < 0.105mm) Between Via (219mm,83.55mm) from Top Layer to Bottom Layer And Via (219mm,84mm) from Top Layer to
Clearance Constraint: (0.1mm < 0.105mm) Between Via (234.527mm,73.97mm) from Top Layer to Bottom Layer And Via (234.978mm,73.97mm) from Top
Clearance Constraint: (0.1mm < 0.105mm) Between Via (234.535mm,75.425mm) from Top Layer to Bottom Layer And Via (234.985mm,75.423mm) from

Clearance Constraint (Gap=0.2mm) (InNet('VPWR') or InNet('Vin') or InNet('PWR')),(All)
Clearance Constraint: (0.1mm < 0.2mm) Between Pad CO1-4(247.5mm,77mm) on Top Layer And Pad CO1-H(251.25mm,78.25mm) on Multi-Layer
Clearance Constraint: (0.1mm < 0.2mm) Between Pad CO1-9(247.5mm,79.5mm) on Top Layer And Pad CO1-H(251.25mm,78.25mm) on Multi-Layer
Clearance Constraint: (0.16mm < 0.2mm) Between Pad COG1-23(233mm,75.675mm) on Bottom Layer And Track
Clearance Constraint: (0.185mm < 0.2mm) Between Pad COG1-24(233.5mm,75.675mm) on Bottom Layer And Via (234mm,75.675mm) from Top Layer to
Clearance Constraint: (0.16mm < 0.2mm) Between Pad COG1-25(234mm,75.675mm) on Bottom Layer And Track
Clearance Constraint: (0.16mm < 0.2mm) Between Pad COG1-28(235.5mm,75.675mm) on Bottom Layer And Track
Clearance Constraint: (0.16mm < 0.2mm) Between Pad COG1-30(236.5mm,75.675mm) on Bottom Layer And Track
Clearance Constraint: (0.185mm < 0.2mm) Between Pad COG1-4(236mm,73.825mm) on Bottom Layer And Via (235.5mm,73.825mm) from Top Layer to
Clearance Constraint: (0.15mm < 0.2mm) Between Pad IC1-E2(234.8mm,90mm) on Top Layer And Via (235.2mm,90mm) from Top Layer to Bottom Layer
Clearance Constraint: (0.15mm < 0.2mm) Between Pad IC1-F1(235.2mm,89.6mm) on Top Layer And Via (235.2mm,90mm) from Top Layer to Bottom
Clearance Constraint: (0.15mm < 0.2mm) Between Pad IC1-F2(235.2mm,90mm) on Top Layer And Via (234.8mm,90mm) from Top Layer to Bottom Layer
Clearance Constraint: (0.15mm < 0.2mm) Between Pad IC1-F2(235.2mm,90mm) on Top Layer And Via (235.2mm,90.4mm) from Top Layer to Bottom
Clearance Constraint: (0.15mm < 0.2mm) Between Pad IC1-F3(235.2mm,90.4mm) on Top Layer And Via (235.2mm,90mm) from Top Layer to Bottom
Clearance Constraint: (Collision < 0.2mm) Between Track (120.625mm,62.075mm)(142.025mm,83.475mm) on Layer 5 And Via (132.9mm,75mm) from Top
Clearance Constraint: (0.175mm < 0.2mm) Between Track (233.5mm,74.75mm)(233.5mm,75.675mm) on Bottom Layer And Via (234mm,75.675mm) from
Clearance Constraint: (0.125mm < 0.2mm) Between Track (233.5mm,75.675mm)(233.5mm,76.65mm) on Bottom Layer And Via (234mm,75.675mm) from
Clearance Constraint: (0.187mm < 0.2mm) Between Track (234.8mm,89.5mm)(234.8mm,90mm) on Layer 2 And Via (235.2mm,90mm) from Top Layer to
Clearance Constraint: (0.187mm < 0.2mm) Between Track (235.2mm,89.6mm)(235.913mm,88.887mm) on Top Layer And Via (235.2mm,90mm) from Top
Clearance Constraint: (0.186mm < 0.2mm) Between Track (235.2mm,90.4mm)(235.411mm,90.4mm) on Layer 2 And Via (235.2mm,90mm) from Top Layer
Clearance Constraint: (0.175mm < 0.2mm) Between Track (235.2mm,90mm)(237.2mm,90mm) on Bottom Layer And Via (234.8mm,90mm) from Top Layer
Clearance Constraint: (0.175mm < 0.2mm) Between Track (235.2mm,90mm)(237.2mm,90mm) on Bottom Layer And Via (235.2mm,90.4mm) from Top
Clearance Constraint: (0.175mm < 0.2mm) Between Track (236mm,73.825mm)(236mm,74.75mm) on Bottom Layer And Via (235.5mm,73.825mm) from
Clearance Constraint: (0.1mm < 0.2mm) Between Via (234.8mm,90mm) from Top Layer to Bottom Layer And Via (235.2mm,90mm) from Top Layer to
Clearance Constraint: (0.1mm < 0.2mm) Between Via (235.2mm,90.4mm) from Top Layer to Bottom Layer And Via (235.2mm,90mm) from Top Layer to

Short-Circuit Constraint (Allowed=No) (All),(All)
Short-Circuit Constraint: Between Pad H5-1(250.5mm,93.5mm) on Multi-Layer And Text "3 = for" (248.679mm,94.548mm) on Bottom Layer Location : [X =
Short-Circuit Constraint: Between Polygon Region (276 hole(s)) Layer 2 And Text "1 = Easter" (167.859mm,92.54mm) on Layer 2 Location : [X = 0mm][Y =
Short-Circuit Constraint: Between Polygon Region (309 hole(s)) Layer 5 And Text "2 = egg" (97.004mm,51.54mm) on Layer 5 Location : [X = 0mm][Y =
Short-Circuit Constraint: Between Polygon Region (418 hole(s)) Top Layer And Text "4 = Carson" (64.077mm,86.779mm) on Top Layer Location : [X =
Short-Circuit Constraint: Between Polygon Region (47 hole(s)) Bottom Layer And Text "3 = for" (248.679mm,94.548mm) on Bottom Layer Location : [X =
Short-Circuit Constraint: Between Track (120.625mm,62.075mm)(142.025mm,83.475mm) on Layer 5 And Via (132.9mm,75mm) from Top Layer to Bottom

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net USB0_TX_N Between Track (205.757mm,80.268mm)(218.843mm,80.268mm) on Layer 5 And Via (219mm,80.365mm) from
Un-Routed Net Constraint: Net USB0_TX_P Between Track (205.863mm,80.013mm)(218.843mm,80.013mm) on Layer 5 And Via (219mm,79.915mm) from

Minimum Annular Ring (Minimum=0.124mm) (All)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (233.6mm,90.8mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234.4mm,89.6mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234.4mm,90.8mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234.4mm,90mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234.4mm,91.6mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234.8mm,90.4mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234.8mm,90mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234mm,90.4mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (234mm,91.2mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (235.2mm,90.4mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (235.2mm,90mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)
Minimum Annular Ring: (0.1mm < 0.124mm) Via (235.2mm,91.6mm) from Top Layer to Bottom Layer (Annular Ring=0.1mm) On (Top Layer)

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Pad CO102-H(88mm,53mm) on Multi-Layer
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Pad CO1-H(251.25mm,78.25mm) on Multi-Layer
Board Outline Clearance(Outline Edge): (0.119mm < 0.254mm) Between Board Edge And Via (221.635mm,96.381mm) from Top Layer to Bottom Layer
Board Outline Clearance(Outline Edge): (0.134mm < 0.254mm) Between Board Edge And Via (222.905mm,96.366mm) from Top Layer to Bottom Layer
Board Outline Clearance(Outline Edge): (0.139mm < 0.254mm) Between Board Edge And Via (225.965mm,96.361mm) from Top Layer to Bottom Layer
Board Outline Clearance(Outline Edge): (0.119mm < 0.254mm) Between Board Edge And Via (227.235mm,96.381mm) from Top Layer to Bottom Layer