

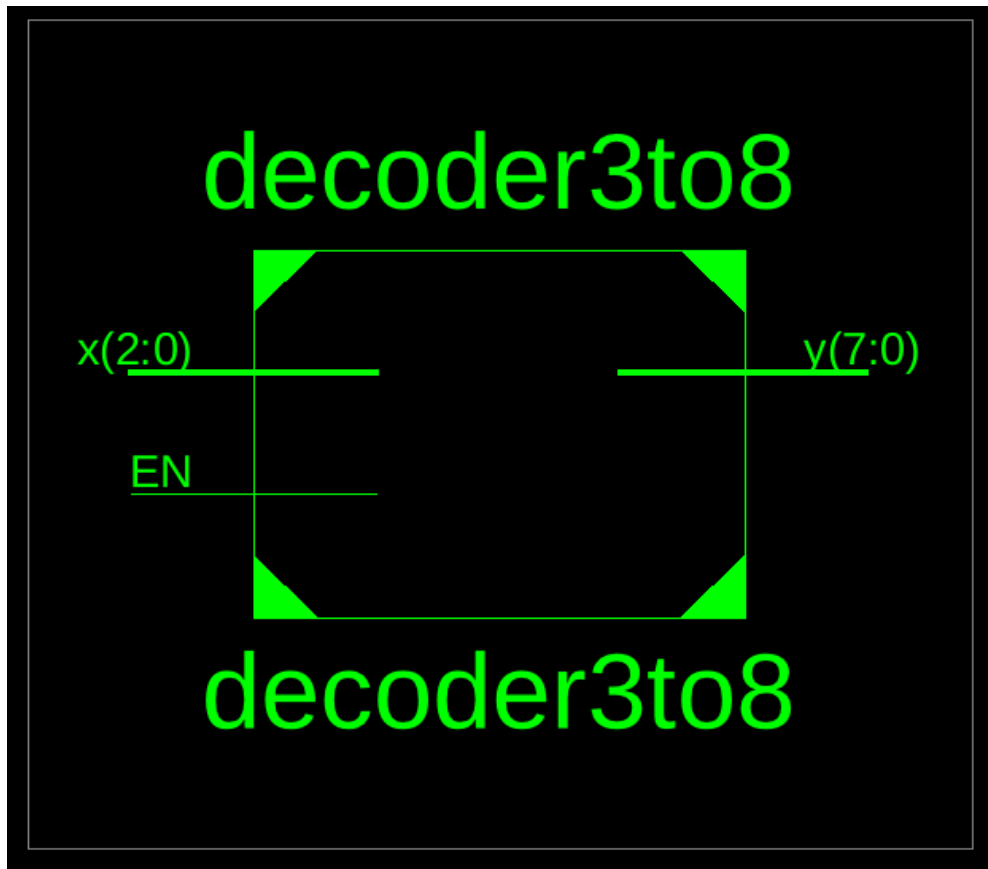
**İSTANBUL ÜNİVERSİTESİ**  
**BİLGİSAYAR MÜHENDİSLİĞİ**

**Bilgisayar Organizasyonu ve Tasarımı**  
**Laboratuvarı**

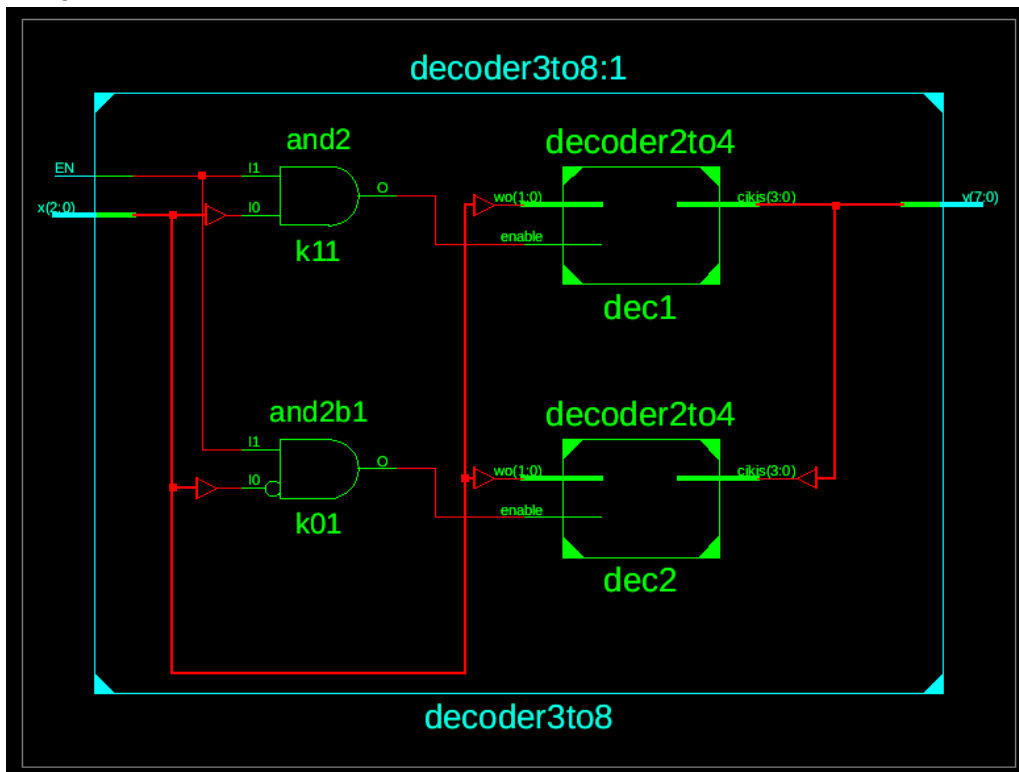
**Uygulama 2 :**

2 adet 2-4 Kod Çözücü Kullanılarak 3-8 Kod Çözücü  
Oluşturulması

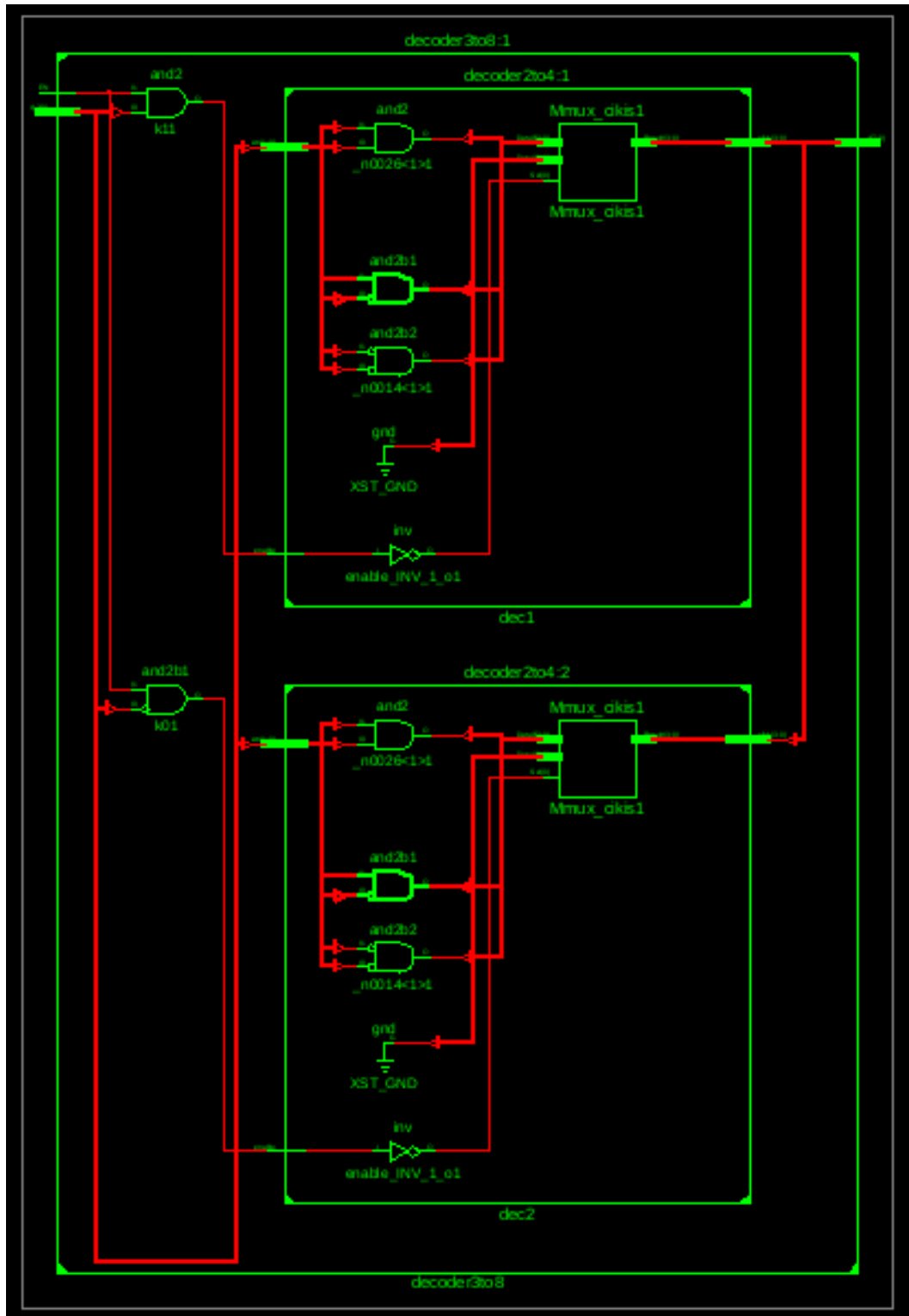
## 1- Devre:



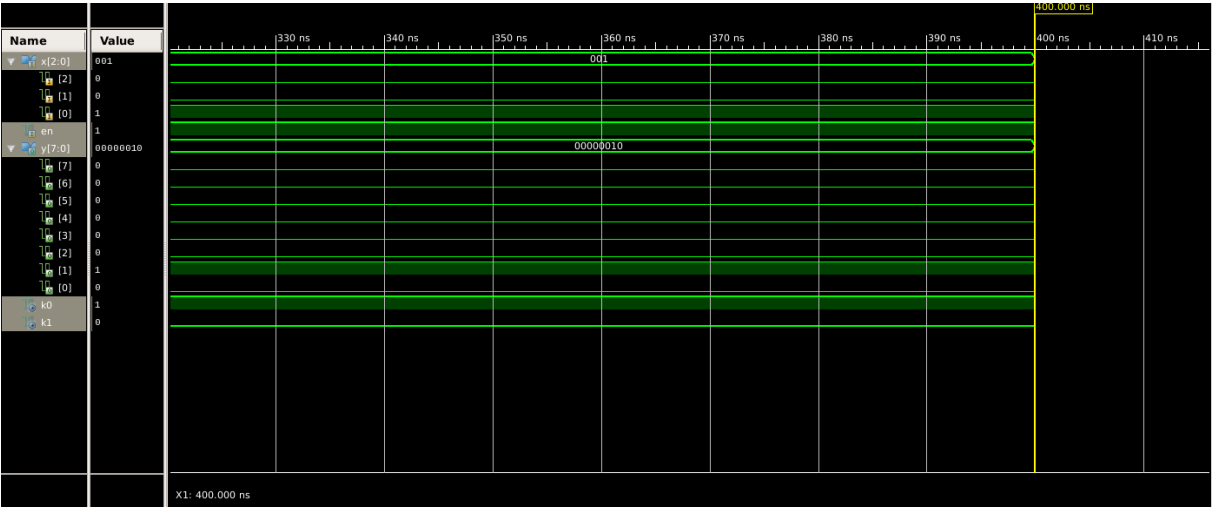
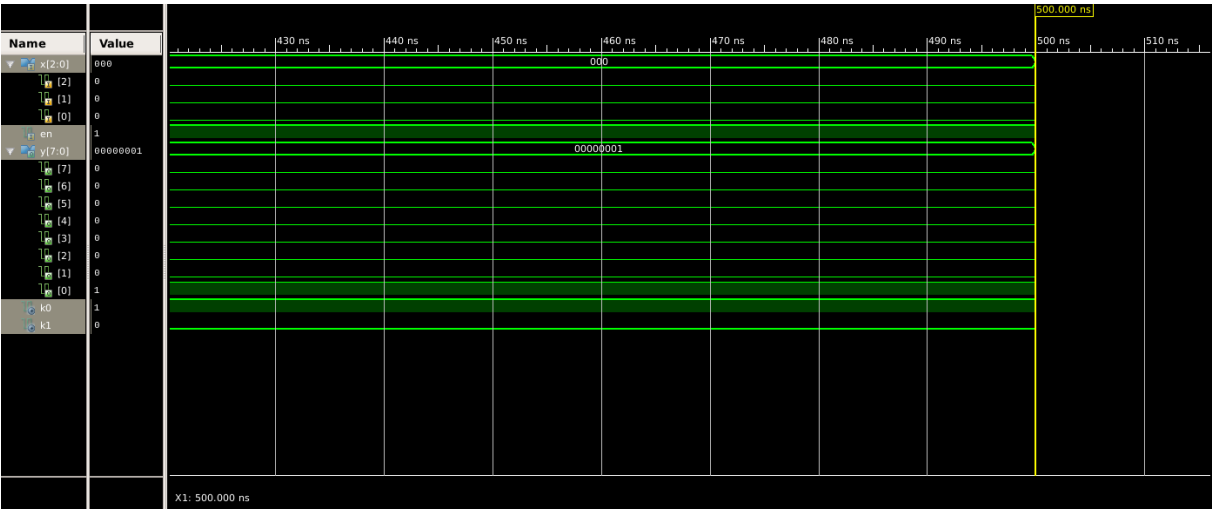
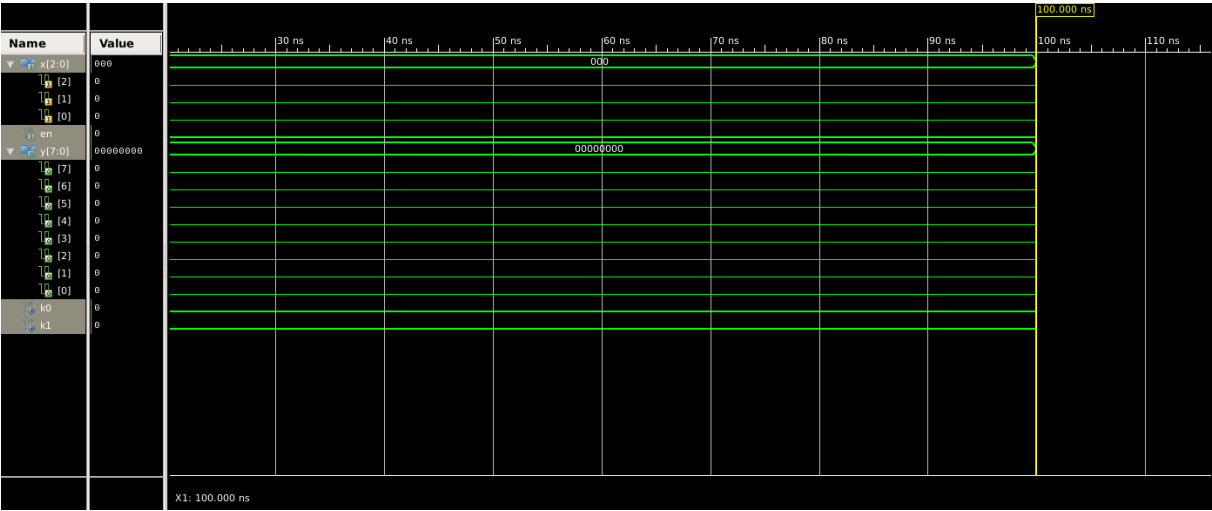
## 2.1- Şematik:

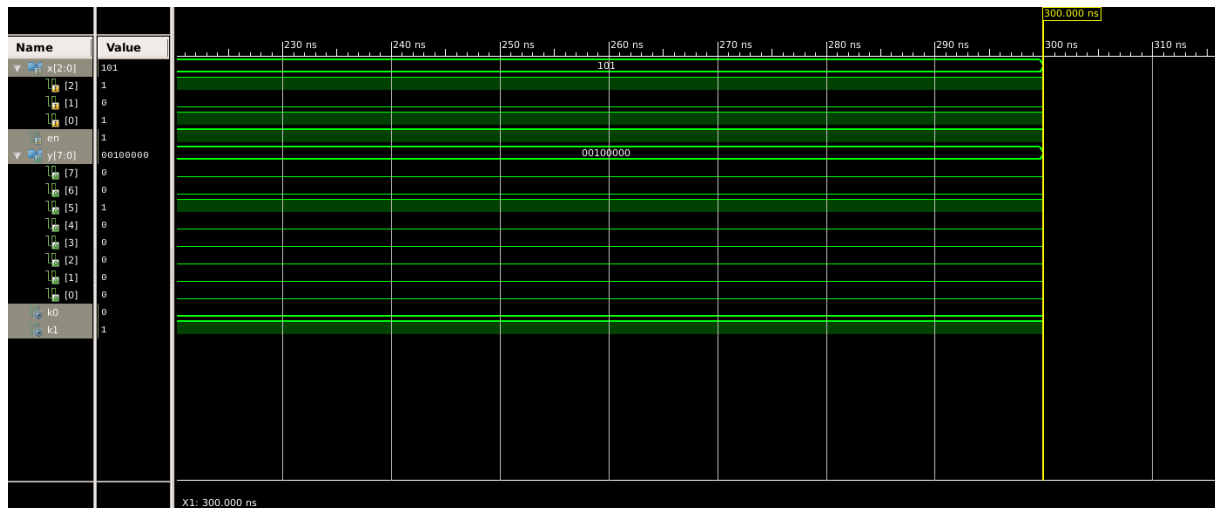
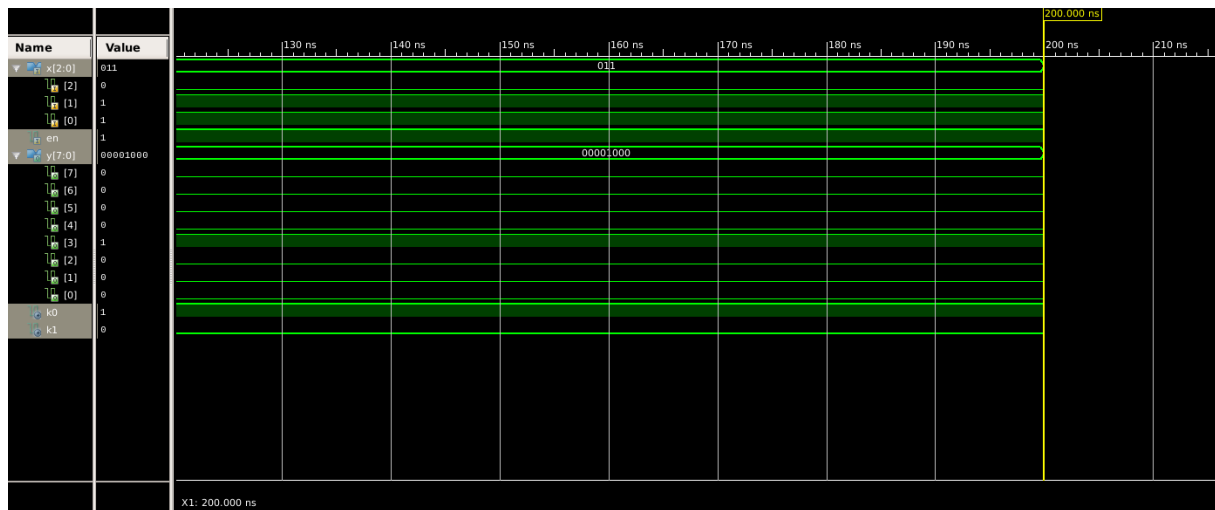


## 2.2- Detaylı Şematik:



3- Simülasyonlar:





#### 4- Kodlar:

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--3to8 decoder kodumuz

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity decoder3to8 is
```

```
port (
    x  : in STD_LOGIC_VECTOR (2 downto 0);    --giris bitleri
    EN : in STD_LOGIC;                        --enable biti
    y  : out STD_LOGIC_VECTOR (7 downto 0));   --cikis bitleri
end decoder3to8;
```

```
architecture Behavioral of decoder3to8 is
```

```

component decoder2to4 is
port (
    enable : in STD_LOGIC;
    wo     : in STD_LOGIC_VECTOR (1 downto 0);
    cikis  : out STD_LOGIC_VECTOR(3 downto 0));
end component;

signal k0: STD_LOGIC;
signal k1: STD_LOGIC;

begin
    dec1: decoder2to4 port map(k1,x(1 downto 0),y(7 downto 4));
    dec2: decoder2to4 port map(k0,x(1 downto 0),y(3 downto 0));
    k0 <= NOT x(2) AND EN;
    k1 <= x(2) AND EN;

```

```

end Behavioral;

```

-----

```

--2to4 decoder kodumuz

```

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

```

```

entity decoder2to4 is
port (
    enable : in STD_LOGIC;
    wo     : in STD_LOGIC_VECTOR (1 downto 0);
    cikis  : out STD_LOGIC_VECTOR (3 downto 0));
end decoder2to4;

```

```

architecture Behavioral of decoder2to4 is

```

```

begin
    cikis <= "0000" when enable='0' else
        "0001" when wo="00" else
        "0010" when wo="01" else
        "0100" when wo="10" else
        "1000";

```

```

end Behavioral;

```