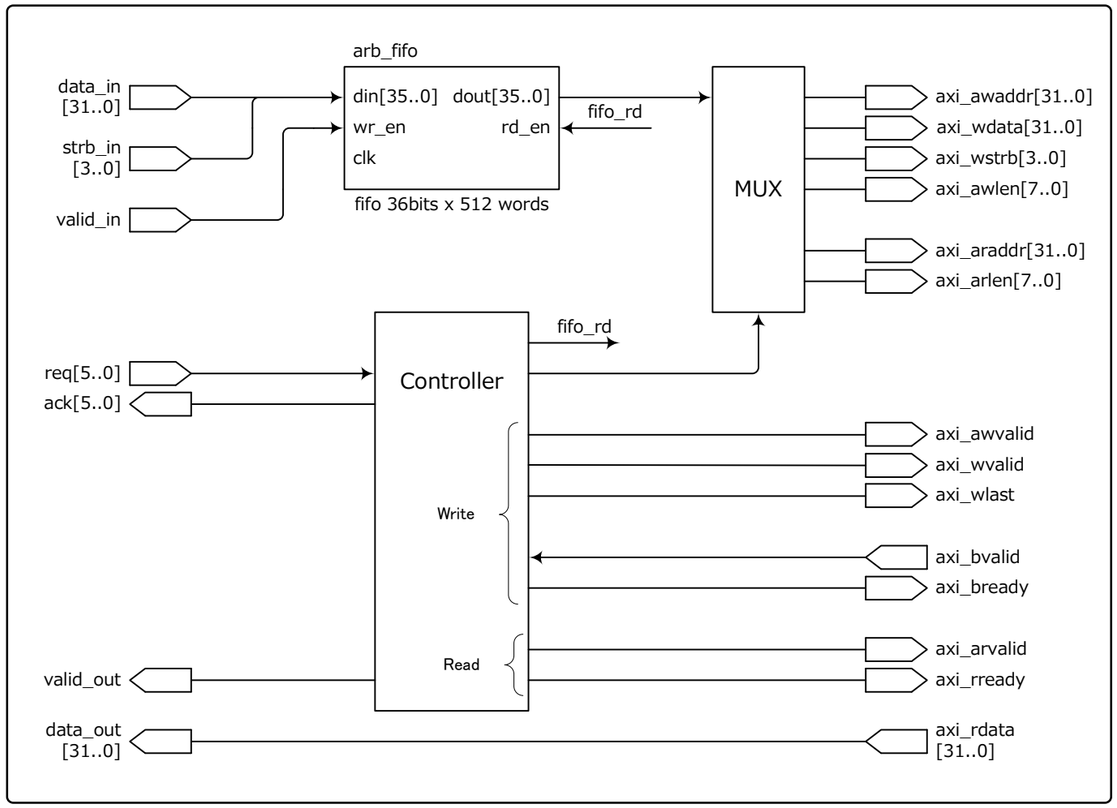
arb

DDR Arbiter
This module arbitrates various write/read requests to/from DDR.

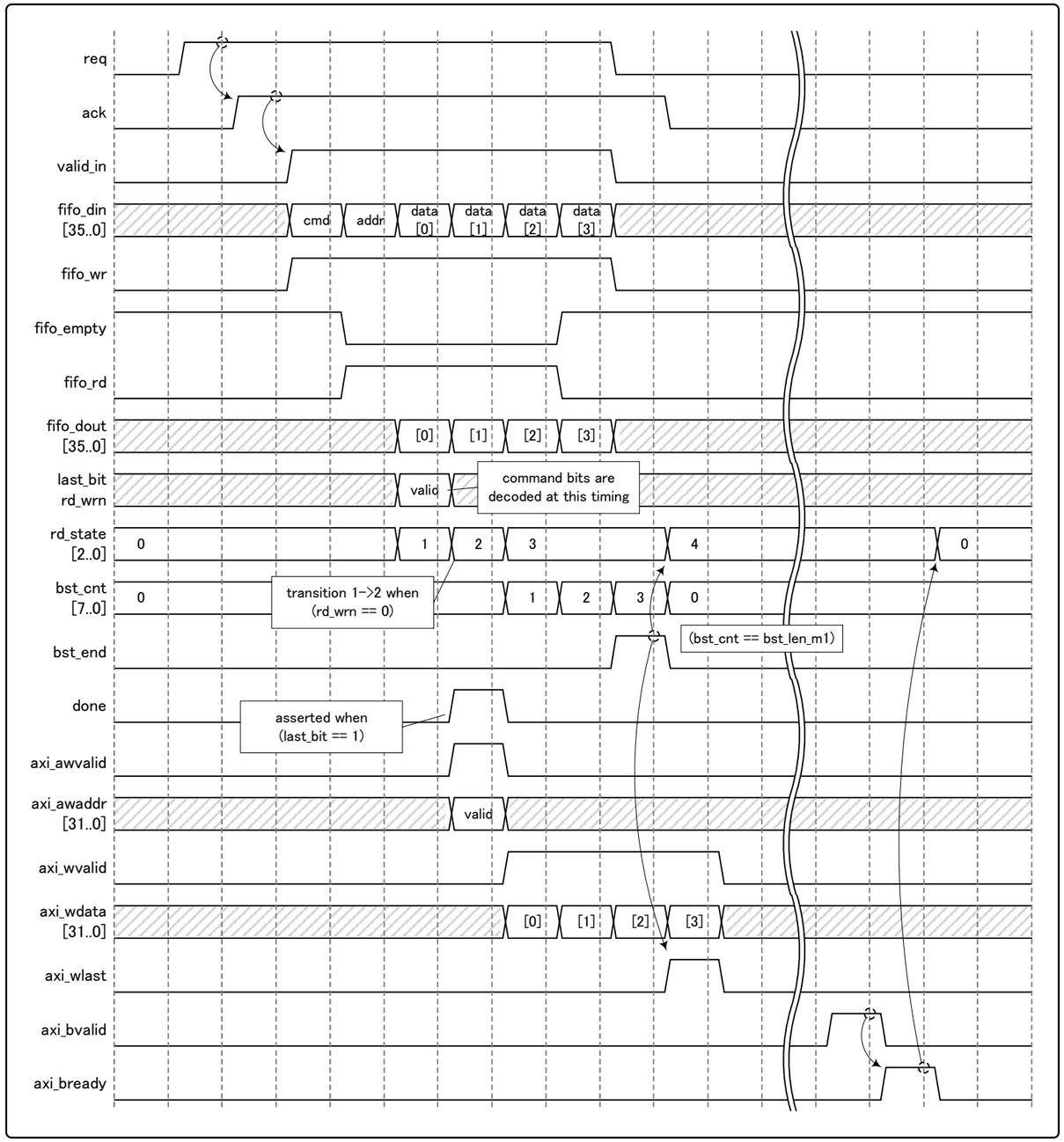
Nov.23.2020

Block diagram




```
// AXI I/F
input           axi_aclk;
output  [31:0]  axi_awaddr;
output  [7:0]   axi_awlen;
output          axi_awvalid;
input           axi_awready;
output  [31:0]  axi_wdata;
output          axi_wlast;
output          axi_wvalid;
input           axi_wready;
input           axi_bvalid;
output          axi_bready;
```

DDR Write (where burst length is 4)



CMD
[31..10]: reserved
[9]: last
[8]: rd_wrn
[7.. 0]: bst_len_m1

rd_state
0 -> 1: ~empty & awready & wready & arready
1 -> 2: ~rd_wrn
1 -> 5: rd_wrn
2 -> 3: unconditional
3 -> 4: wlast & wready
4 -> 0: bready
5 -> 0: rlast

DDR Read (where burst length is 4)