Create project “dvp”

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1. Preface

This document describes a procedure to create “dvp” project. There are two methods to create this project. One of them is to use a script to automatically create the project. Such a script is included in the repository. The other is to create a project from scratch. This method is presented here in case the above script somehow won’t work.

2. Create “dvp” project from script

Launch Vivado, type the following commands in “Tcl Console”.

```
cd [Project Directory]/U96-SVM/vivado
source create_project_dvp.tcl
```

* board files for ultra96v2 must be installed.

3. Create “dvp” project from scratch

3.1. Create a new project

Create the following working directory.

[Project Directory]/U96-SVM/vivado

Launch Vivado, create a new project with the following properties.

[Project Name]

Project name: dvp

Project location: [Project Directory]/U96-SVM/vivado

Create project subdirectory: Checked

[Project Type]

RTL Project: Selected

Do not specify sources at this time: Checked

[Default Part]

Boards->Display Name: Ultra96v2 Single Board Computer

* board files for ultra96v2 must be installed.

3.2. Adding RTL sources

Click “Add Sources” in the Flow Navigator to open “Add Sources” dialog.

Proceed with the following settings.

[Add Sources]

Add or create design sources: Selected

[Add or Create Design Sources]

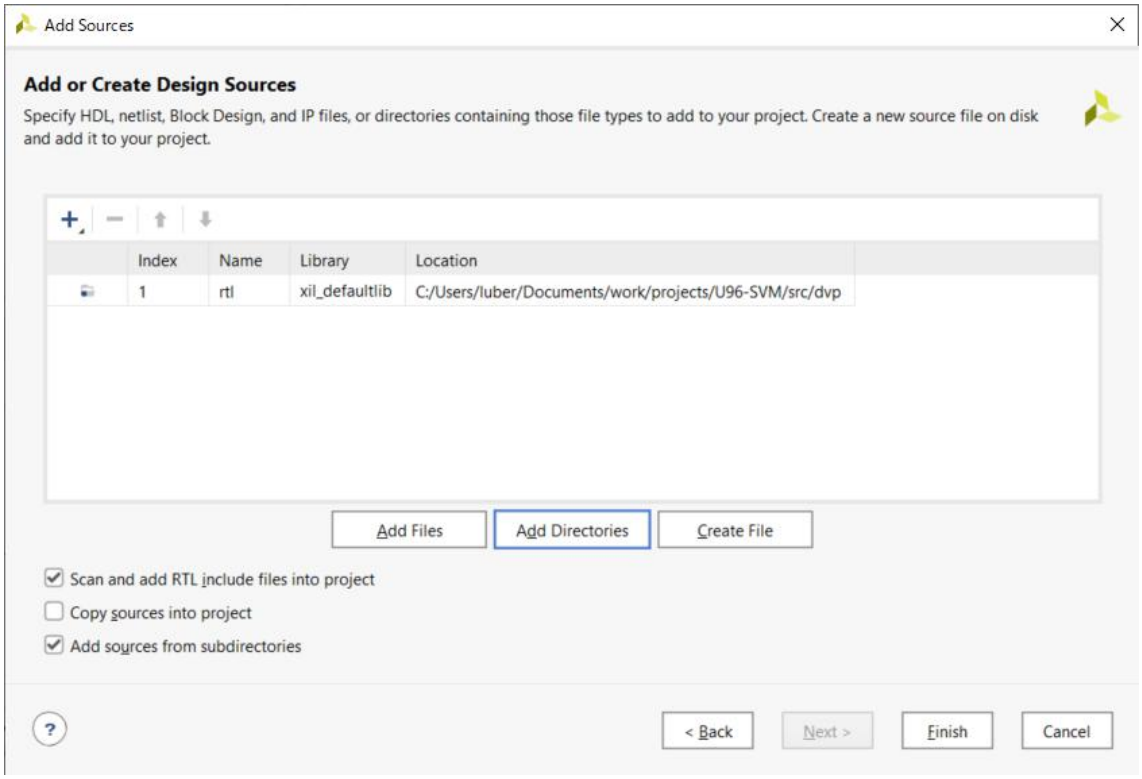
Click “Add Directories” to add the following directory.

[Project Directory]/U96-SVM/src/dvp/rtl

Scan and add RTL include files into project: Checked

Copy sources into project: Not checked

Add sources from subdirectories: Checked



3.3. Adding Simulation sources

Click “Add Sources” in the Flow Navigator to open “Add Sources” dialog.
Proceed with the following settings.

[Add Sources]

Add or create simulation sources: Selected

[Add or Create Design Sources]

Click “Add Directories” to add the following directory.

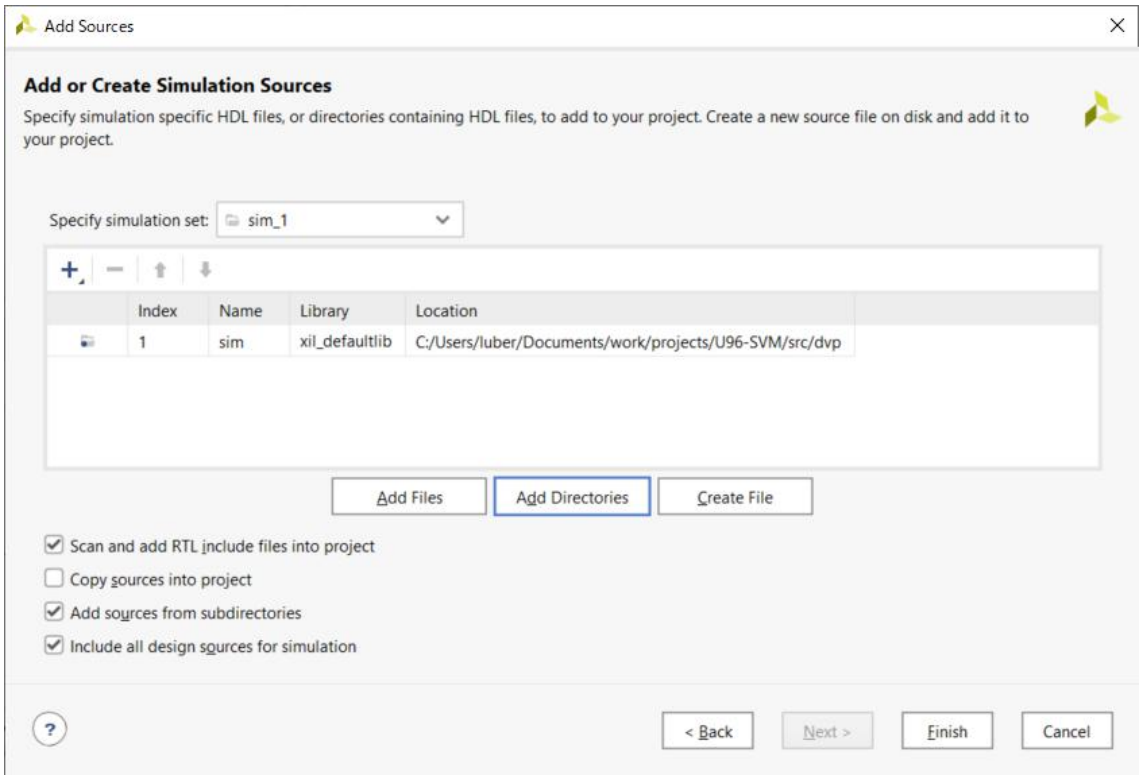
[Project Directory]/U96-SVM/src/dvp/sim

Scan and add RTL include files into project: Checked

Copy sources into project: Not checked

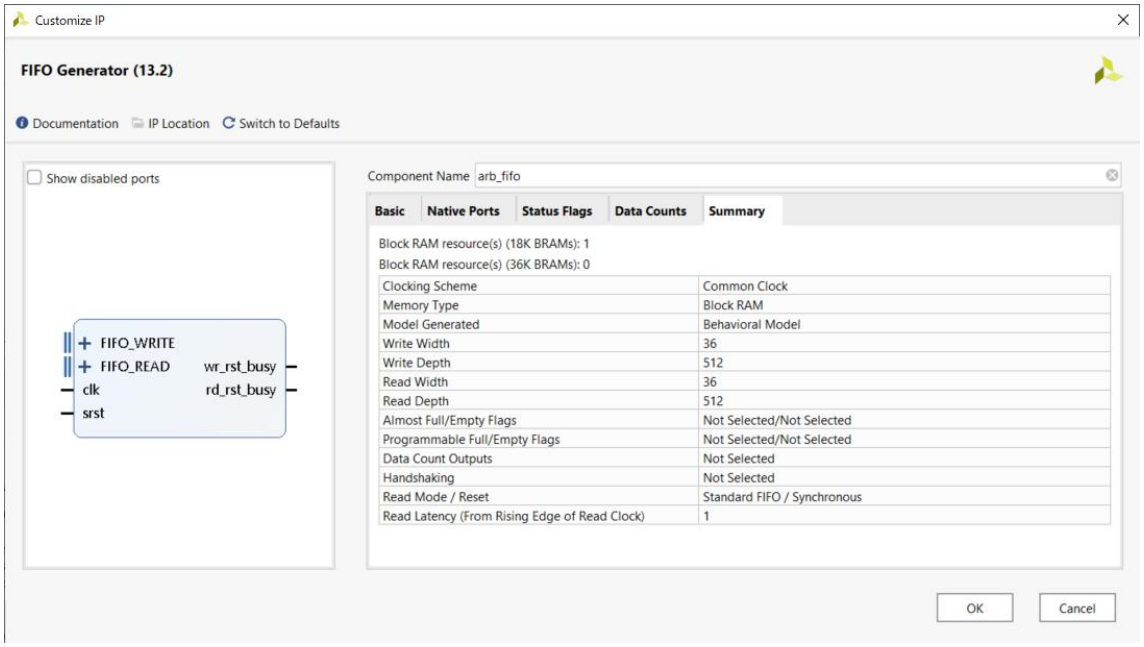
Add sources from subdirectories: Checked

Include all design sources for simulation: Checked



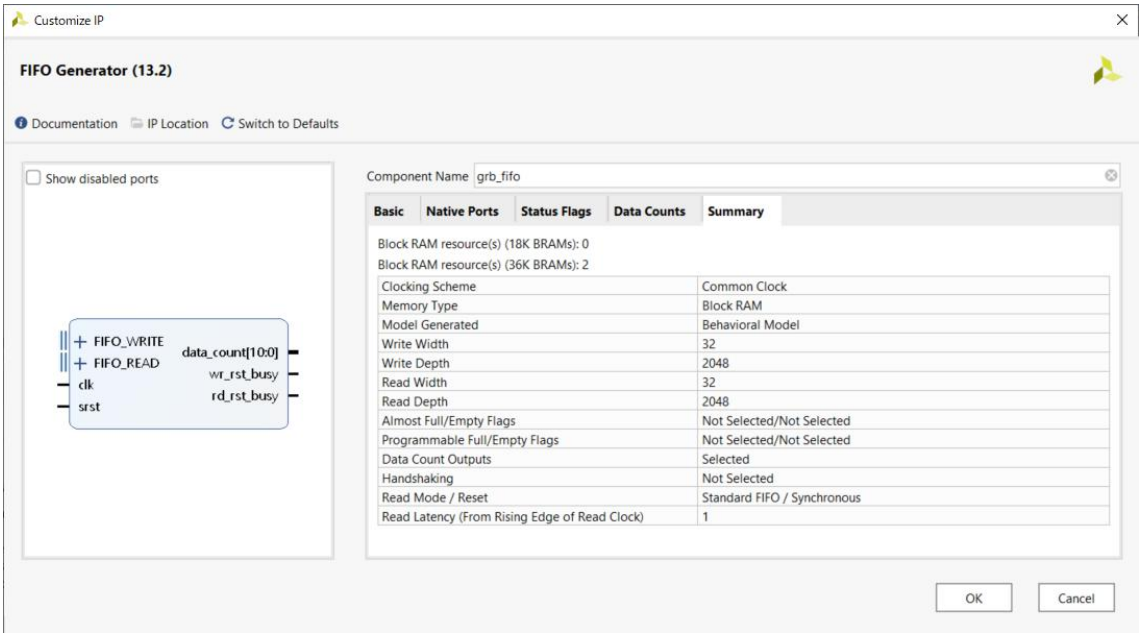
3.4. “arb_fifo”

Click “IP Catalog” in the Flow Navigator.
Select “FIFO Generator” and create an IP with the following settings.
Component Name: arb_fifo
[Basic]
Fifo Implementation: Common Clock Block RAM
[Native Ports]
Data Port Parameters
Write Width: 36
Write Depth: 512
ECC, Output Register and Power Gating Options
Output Registers: Not checked
*Only the settings different from default are shown.
“Generate Output Products” dialog will open.
Click “Skip” for now. This is to reduce the number files that are put into git-controlled directory in the later step.



3.5. “grb_fifo”

Click “IP Catalog” in the Flow Navigator.
Select “FIFO Generator” and create an IP with the following settings.
Component Name: grb_fifo
[Basic]
Fifo Implementation: Common Clock Block RAM
[Native Ports]
Data Port Parameters
Write Width: 32
Write Depth: 2048
ECC, Output Register and Power Gating Options
Output Registers: Not checked
[Data Counts]
Data Count: Checked
*Only the settings different from default are shown.
“Generate Output Products” dialog will open.
Click “Skip” for now. This is to reduce the number files that are put into git-controlled directory in the later step.



3.6. Moving IP sources

This process will move IP sources to git-controlled directory.

Copy “arb_fifo directory as follows.
Move from:
    [Project Directory]/U96-SVM/vivado/dvp/dvp.srcs/sources_1/ip/arb_fifo
Move to:
    [Project Directory]/U96-SVM/src/dvp/ip/arb_fifo

Right click “arb_fifo” in “Sources” pane in PROJECT MANAGER.
Select “Remove File from Project...”.
Check “Also delete the projet local file/directory from disk”.
Click OK.

Click “Add Sources” in the Flow Navigator to open “Add Sources” dialog.
Proceed with the following settings.
[Add Sources]
    Add or create design sources: Selected
[Add or Create Design Sources]
    Clock “Add Files” to add the following file.
        [Project Directorh]/U96-SVM/src/dvp/ip/arb_fifo/arb_fifo.xci
    Scan and add RTL include files into project: Checked
    Copy sources into project: Not checked

Do the same operation with “grb_fifo”.

3.7. Create a script

This process will make a script that automatically creates this project.
Click “Window->Tcl Console”.
In the command line in the Tcl Console, type the following commands.

```
cd [Project Directory]/U96-SVM/vivado
write_project_tcl create_project_dvp.tcl
```

“create_project_dvp.tcl” will be created in the specified directory.

4. Export IP

Click “Run Synthesis” in the Flow Navigator to see there aren’t any errors.
Click “Tools->Create and Package New IP...” to open “Create and Package New IP” dialog.
Proceed with the following settings.
[Create Peripheral, Package IP or Package a Block Design]
Packaging Options
Package your current project: Selected
[Package Your Current Project]
IP location: [Project Directory]/U96-SVM/src/ip_repo/dvp

When prompted, choose to overwrite the existing files.
Click “Finish”.
“Package IP - dvp” will appear.
Select “Review and Package”, click “Package IP”.
IP sources for “dvp” are exported under “ip_repo/dvp” directory.