Create project “project_1”

Dec.10.2020

1. Preface

This document describes a procedure to create “project_1” project. There are two methods to create this project. One of them is to use a script to automatically create the project. Such a script is included in the repository. The other is to create a project from scratch. This method is presented here in case the above script somehow won’t work.

2. Create “project_1” from script

Launch Vivado, type the following commands in “Tcl Console”.

```
cd [Project Directory]/U96-SVM/vivado
source create_project_1.tcl
```

* board files for ultra96v2 must be installed.

3. Create “project_1” from scratch

3.1. Create a new project

If not, create the following working directory.

[Project Directory]/U96-SVM/vivado

Launch Vivado, create a new project with the following properties.

[Project Name]

Project name: project_1

Project location: [Project Directory]/U96-SVM/vivado

Create project subdirectory: Checked

[Project Type]

RTL Project: Selected

Do not specify sources at this time: Checked

[Default Part]

Boards: Ultra96v2 Single Board Computer

* board files for ultra96v2 must be installed.

3.2. Adding a block design

Click “Create Block Design” in the Flow Navigator to open “Create Block Design” dialog.
Proceed with the following settings.

Design name: design_1

Directory: [Project Directory]/U96-SVM/src

Specify source set: Design Sources

Click “+” icon in “BLOCK DESIGN->Diagram” to add an IP.
Select “Zynq UltraScale+ MPSoC”.
Click “Run Block Automation” and click “OK” with the default options.

Make the following connections.

Source	Destination
pl_clk0	maxihpm0_fpd_aclk
pl_clk0	maxihpm1_fpd_aclk

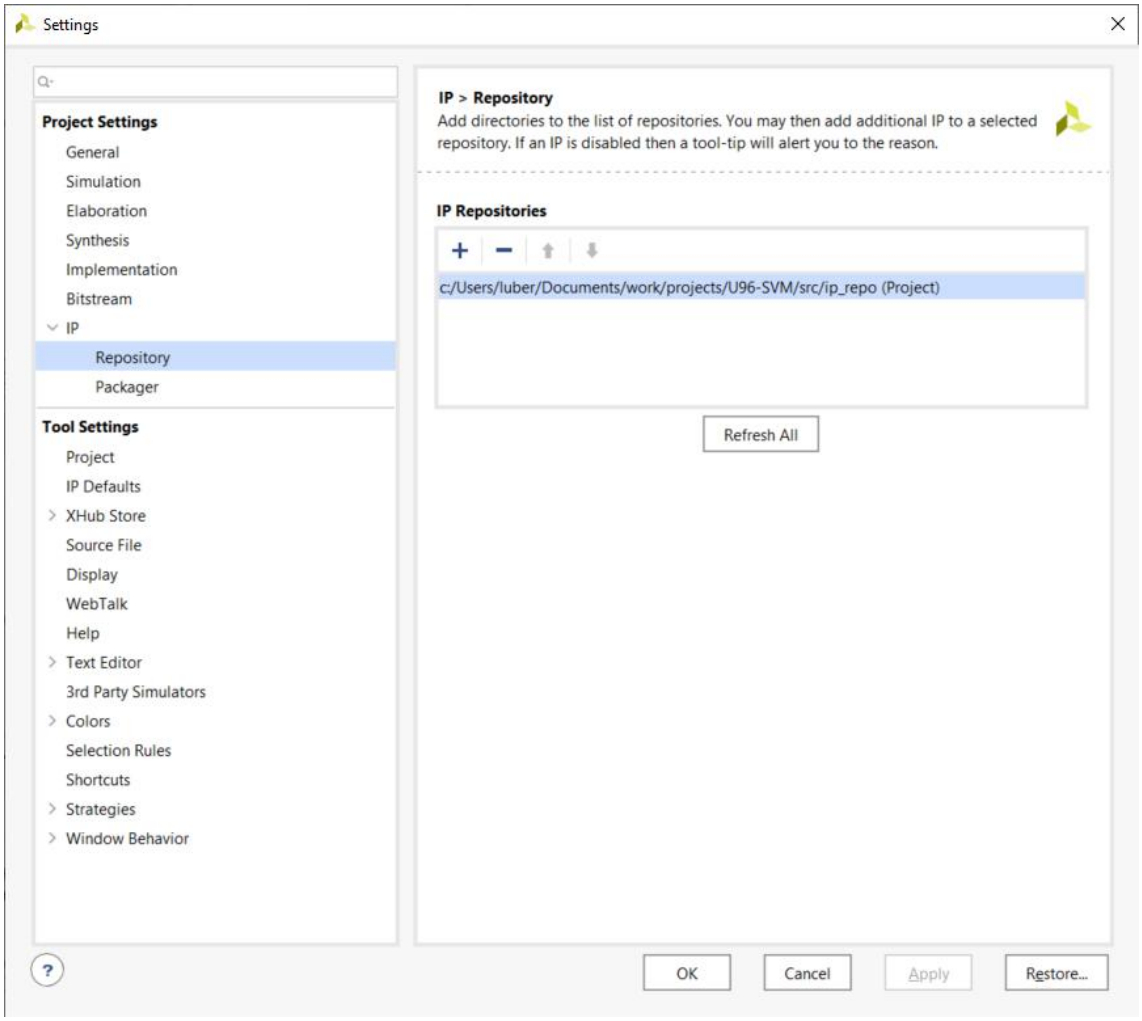
3.3. Adding IPs

Click “Tools->Settings...” to open “Settings” dialog.

Select “Project Settings->IP->Repository”. Add the following path to “IP Repositories”.

[Projecct Directory]/U96-SVM/src/ip_repo

*IP sources for “dvp” module must be exported under “ip_repo/dvp” directory.



Double click “zynq_ultra_ps_e_0” in the BLOCK DESIGN.
Select “PS-PL Configuration->PS-PL Interfaces->Slave Interfaces->AXI HP”
Check “AXI HP0 FPD”.

Add the following IPs by clicking “+” icon in “BLOCK DESIGN->Diagram”

- IP Name: “dvp_v1_0”.

- IP Name: MIPI CSI-2 Rx Subsystem

Component Name: mipi_csi2_rx_subsyst_0
Configuration-> Sybsystem Options-> Pixel Format: YUV422 8bit
Serial Data Lanes: 2
DPHY Options->D-PHY Register Interface: Checked
Shared Logic->Shared Logic->Include Shared Logic in core: Selected
Pin Assigment-> Clock Lane->Pin Loc: N2
Data Lane0->Pin Loc: N5

Data Lane1->Pin Loc: M2

❖ IP Name: MIPI CSI-2 Rx Subsystem

Component Name: mipi_csi2_rx_subsyst_1

Configuration-> Sybsystem Options-> Pixel Format: YUV422 8bit

Serial Data Lanes: 2

DPHY Options->D-PHY Register Interface: Checked

Shared Logic->Shared Logic->Include Shared Logic in example design: Selected

Pin Assigment-> Clock Lane->Pin Loc: T3

Data Lane0->Pin Loc: P3

Data Lane1->Pin Loc: U2

❖ IP Name: Clocking Wizard

Component Name: clk_wiz_0

Output Clocks->clk_out1->Output Freq->Requested: 200

❖ IP Name: Clocking Wizard

Component Name: clk_wiz_1

Output Clocks->clk_out1->Output Freq->Requested: 24

Set the following port to “external” by right click the port then select “Make External”.

Module	Signal
dvp_0	gpio_in[1:0]
dvp_0	led[1:0]
mipi_csi2_rx_subsyst_0	mipi_phy_if
mipi_csi2_rx_subsyst_1	mipi_phy_if
clk_wiz_1	clk_out1

Connect the following signals.

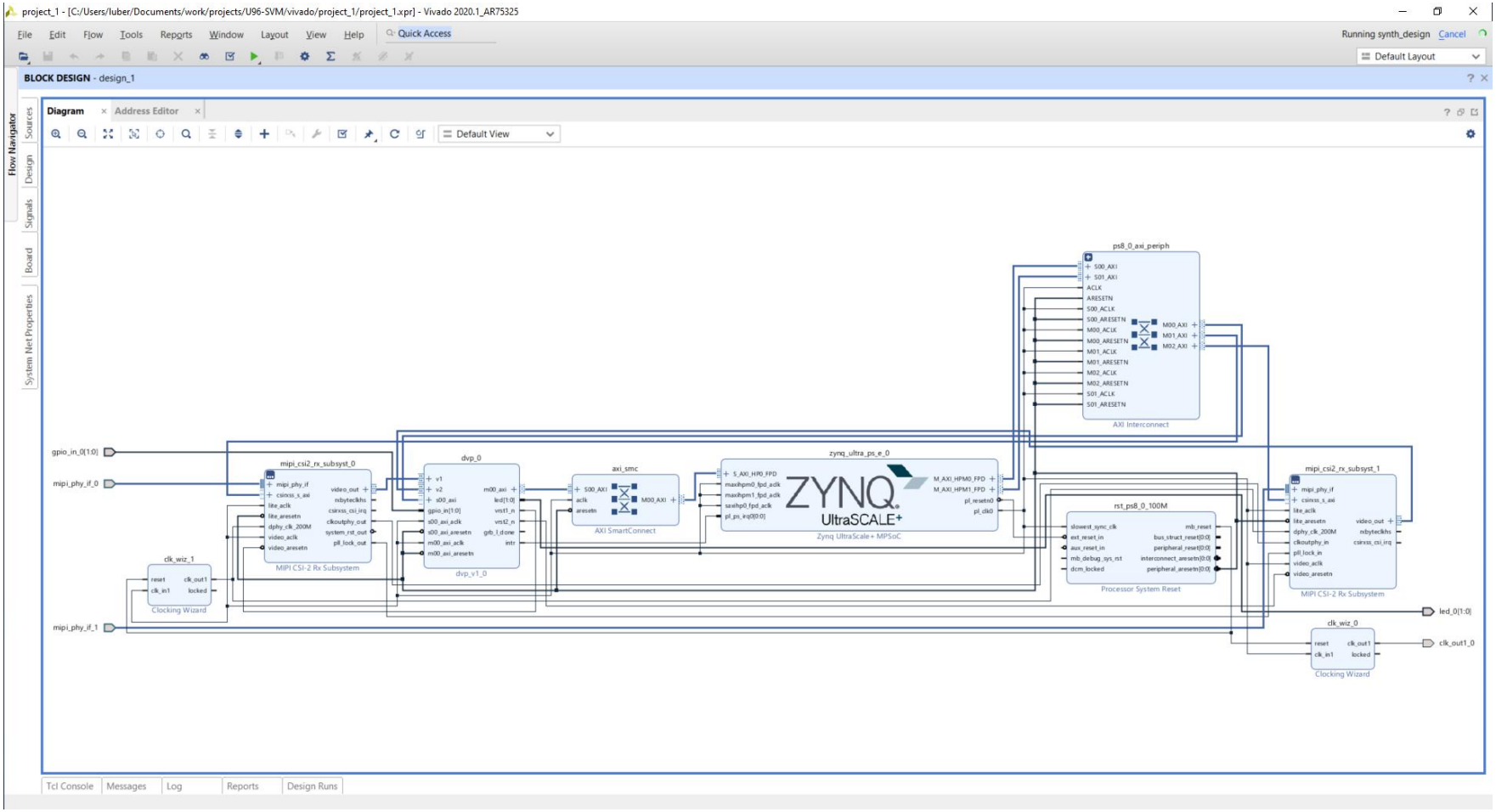
Source		Destination	
Module	Signal	Module	Signal
dvp_0	vrst1_n	mipi_csi2_rx_subsyst_0	video_aresetn
dvp_0	vrst2_n	mipi_csi2_rx_subsyst_1	video_aresetn
dvp_0	intr	zynq_ultra_ps_e_0	pl_ps_irq0[0:0]
mipi_csi2_rx_subsyst_0	video_out	dvp_0	v1
mipi_csi2_rx_subsyst_1	video_out	dvp_0	v2
mipi_csi2_rx_subsyst_0	clkoutphy_out	mipi_csi2_rx_subsyst_1	clkoutphy_in
mipi_csi2_rx_subsyst_0	pll_lock_out	mipi_csi2_rx_subsyst_1	pll_lock_in
clk_wiz_0	clk_out1	mipi_csi2_rx_subsyst_0	dphy_clk_200M
clk_wiz_0	clk_out1	mipi_csi2_rx_subsyst_1	dphy_clk_200M

Click “Run Connection Automation” twice with the default parameters.

Delete “reset_rtl” and “reset_rtl_0” input pins and connect to the following ports instead.

Source		Destination	
Module	Signal	Module	Signal
clk_wiz_0	reset	rst_ps8_0_100M	mb_reset
clk_wiz_1	reset	rst_ps8_0_100M	mb_reset

Right click somewhere on the “Diagram” the click “Regenerate Layout”.
“design_1” block design should look like this.


project_1 - [C:/Users/luber/Documents/work/projects/U96-SVM/vivado/project_1/project_1.xpr] - Vivado 2020.1_AR75325
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Running synth_design Cancel
Default Layout
BLOCK DESIGN - design_1
Diagram
Address Editor
Default View
Flow Navigator
Sources
Design
Signals
Board
System Net Properties
ps8_0_axi_periph
AXI Interconnect
gpio_in_0[1:0]
mipi_phy_if_0
mipi_phy_if_1
mipi_csi2_rx_subsyst_0
MIPI CSI-2 Rx Subsystem
dvp_0
dvp_v1_0
axi_smc
AXI SmartConnect
zynq_ultra_ps_e_0
Zynq UltraScale+ MPSoC
rst_ps8_0_100M
Processor System Reset
clk_wiz_1
Clocking Wizard
mipi_csi2_rx_subsyst_1
MIPI CSI-2 Rx Subsystem
led_0[1:0]
clk_wiz_0
Clocking Wizard
clk_out1_0
Tcl Console
Messages
Log
Reports
Design Runs

3.4. Create wrapper HDL

Right click “BLOCK DESIGN->Sources->Design Sources->design_1”.
Click “Create HDL Wrapper...” in the menu to open “Create HDL Wrapper” dialog.
Select “Let Vivado manage wrapper and auto-update” and click “OK”.

3.5. Pin assignment

Click “Run Synthesis” in the Flow Navigator.
“Synthesis Completed” dialog will appear.
Select “Open Synthesized Design” and click “OK”.

Select “Window->I/O Ports”.
“I/O Ports” tab will appear in the SYNTHESIZED DESIGN.
Set the following pin location and I/O standard for each signal.

Name	Package Pin	I/O Std
clk_out1_0	E8	LVCMOS18
gpio_in_0[1]	C5	LVCMOS18
gpio_in_0[0]	G6	LVCMOS18
led_0[1]	B9	LVCMOS18
led_0[0]	A9	LVCMOS18

Click “File->Constraints->Save As...” to open “Save Constraints” dialog.
Proceed with the following settings.

Create a new file: Selected
File type: XDC
File name: constr_1
File location: [Project Directory]/U96-SVM/src

3.7. Create a script

This process will make a script to automatically create this project.
Click “Window->Tcl Console”.
In the command line in the Tcl Console, type the following command.

```
cd [Project Directory]/U96-SVM/vivado
write_project_tcl create_project_1.tcl
```

“create_project_1.tcl” will be created in the specified directory.

4. Export Hardware

Click “Generate Bitstream” in the Flow Navigator.
Click “File->Export->Export Hardware” to open “Export Hardware Platform” dialog.
Proceed with the following settings.
[Export Hardware Platform]

Platform type: Fixed

[Output]

Include bitstream: Selected

[Files]

XSA file name: design_1_wrapper

Export to: [Project Directory]/U96-SVM/vivado

“design_1_wrapper.xsa” will be created in the specified directory.