

***Inter-Chip USB Supplement to the
USB 2.0 Specification***

Revision 1.0

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1 Introduction

1.1 General

The core specification [USB] defines mechanical, electrical and protocol interfaces between products interconnected with cables. The mechanical part of the interface includes definitions for receptacles and plugs.

USB requires a power-supply voltage V_{BUS} , at 5.0 Volt nominal, which provides the energy to supply bus-powered peripherals, and a voltage source supporting 3.3 Volt nominal signaling. These voltages are generally higher than would normally be used to support communication between peripheral subsystems, such as ICs manufactured with deep submicron technology.

In mobile products, where subsystems are in close proximity, there is value in communicating with USB data transfer protocols. Bringing USB capability to a multi-chip assembly improves embedded communication performances. These inter-subsystem mechanical interfaces do not include standard USB connectors, nor do they necessarily use 3.3 Volt nominal signaling.

The resulting configuration between ICs communicating with USB data transfer protocols is defined as Inter-Chip USB (IC_USB). Short physical distances between ICs do not require twisted-pair cable. Differing from standard USB, the same voltage level is used in signaling as is provided to power the interface and logic circuits within the IC_USB peripheral.

By nature, IC_USB links are constrained to be between a root port and a peripheral, tier 1 to tier 2 within a product's box. Products making use of IC_USB shall only provide external USB interfaces through standard USB connectors and cables. IC_USB connections shall not be made available externally on the product. While this does not require that all connections using IC_USB be fixed, any changes shall only be done when power to the peripheral is turned off. Therefore, the "plug and play" features of USB do not apply to IC_USB.

Compliance rules regarding IC_USB products are not established at the time of this writing and should be checked with the USB-IF compliance committee (see <http://www.usb.org/>).

1.2 Objective of This Supplement

The purpose of this document is to define a minimal set of changes to USB, such that IC_USB applications are enabled. This document addresses the IC_USB electrical characteristics derived from those listed in Chapter 7 of the core specification [USB].

This document is not a stand-alone document. It is a supplement to the core specification, and any aspects of USB not specifically changed by this specification are governed by the core specification.

1.3 Intended Audience

This specification is intended for developers of links using USB software protocol where the distance between an IC_USB host port and an IC_USB peripheral is less than 10 cm.

1.4 Relevant Documents

Reference	Title	Location
[USB]	<p>In the context of this document, this specifically refers to the following parts of the USB 2.0 Specification package, "usb_20_02212005.zip":</p> <ul style="list-style-type: none"> • The original USB 2.0 specification released on April 27, 2000 • Errata to the USB 2.0 specification as of December 7, 2000 • Pull-up/pull-down Resistors Engineering Change Notice to the USB 2.0 specification • Errata to the USB 2.0 specification as of May 28, 2002 • Interface Association Descriptor Engineering Change Notice to the USB 2.0 specification • Unicode Engineering Change Notice to the USB 2.0 specification as of February 21, 2005 	www.usb.org/
[JESD8-B]	INTERFACE STANDARD for Nominal 3 Volt / 3.3 Volt Supply Digital Integrated Circuits	www.jedec.org/
[JESD8-7]	ADDENDUM No. 7 to JESD8 1.8 Volt +/- 0.15 Volt (Normal Range) and 1.2 Volt – 1.95 Volt (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits	
[JESD8-11]	ADDENDUM No. 11 to JESD8 1.5 Volt +/- 0.1 Volt (Normal Range) and 0.9 Volt – 1.6 Volt (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits	
[JESD8-12]	1.2 Volt +/- 0.1 Volt (Normal Range) and 0.8 Volt – 1.3 Volt (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits	
[JESD8-14]	1.0 Volt +/- 0.1 Volt (Normal Range) and 0.7 Volt – 1.1 Volt (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits	

1.5 Acronyms and Terms

Term	Definition
Core specification	Refers to the complete set of documents listed in [USB].
Family	A Family of host and removable peripherals is defined as a set of hosts and peripherals having matching mechanical interfaces. Also, within the Family, any choice of host and peripheral are able to communicate.
FS	USB operation at 12 Mb/s. See also LS.
IC_DM	Inter-Chip USB D- Data line
IC_DP	Inter-Chip USB D+ Data line
IC_USB	Inter-Chip USB
IC_USB Bus Interface	Host hardware that supports IC_USB
IC_VDD	Inter-Chip VDD, power-supply voltage
LS	USB operation at 1.5 Mb/s. See also FS.
RPDH	Host-side Pull-Down resistor as defined in § 5.4
RPDP	Peripheral-side Pull-Down resistor as defined in § 5.4
RPU1	Peripheral-side first Pull-Up resistor as defined in § 5.4
RPU2	Peripheral-side second Pull-Up resistor as defined in § 5.4
VMIN	<p>Voltage Minimum</p> <p>When the voltage across a peripheral is above VMIN and before Δt_{p1} expires, the peripheral shall set data line status to prevent false connect (see § 6).</p> <p>VMIN is defined for all voltage classes, 1.0 Volt and above, as 0.72 Volt.</p>
Voltage Class	A specified range of voltage for IC_VDD
VOP	<p>Voltage Operative</p> <p>VOP is defined for each voltage class as $VOP = 0.8 * IC_VDD$ minimum.</p> <p>When the voltage across a peripheral is below VOP the peripheral shall not attach (see § 6 and § 11.1).</p>

Other acronyms and terms used in this specification are defined in the core specification [USB].

2 Significant Features

This chapter identifies the significant features of the IC_USB supplement. The purpose of this chapter is not to present all the technical details associated with each major feature, but rather to highlight its existence.

2.1 Compliance with the Core Specification [USB]

Any product with IC_USB characteristics is a USB product, host or peripheral, that uses USB compliant software.

The core specification contents of Chapter 6, Mechanical, does not apply to IC_USB. This is replaced by the Family definition as specified in § 11.1 of this document.

The core specification contents of Chapter 7, Electrical, is significantly modified by this specification.

2.2 Bus Idle Bias Current

Any peripheral with IC_USB characteristics does not draw any current from the power supply to bias the bus during idle.

2.3 Physical Implementation

Standard USB connectors are not used.

The length of the physical link is limited to 10 cm. The IC_USB Bus Interface does not require an analog transceiver.

2.4 Voltage Classes

Any peripheral with IC_USB characteristics may be supplied by one power-supply voltage selected from five voltage classes, ranging from 1.0 Volt to 3.0 Volt.

The IC_USB Bus Interface is in charge of managing the voltage class negotiation sequence.

2.5 Family

Interoperable IC_USB peripherals and IC_USB hosts constitute a Family.

Mechanical interlock for electrical contacts and specific electrical behaviors characterize a Family.

2.6 Speeds

All IC_USB hosts shall support Full-speed (FS).

The Family specifies if Low-speed (LS) support is required on the host and allowed on the peripheral.

High-speed (HS) is reserved for future study.

3 Inter-Chip USB

3.1 Topology

IC_USB is a point-to-point connection between a Root Hub port and a non-hub peripheral. IC_USB does not offer a tiered star topology.

Figure 3-1 depicts valid Root Hub configurations.

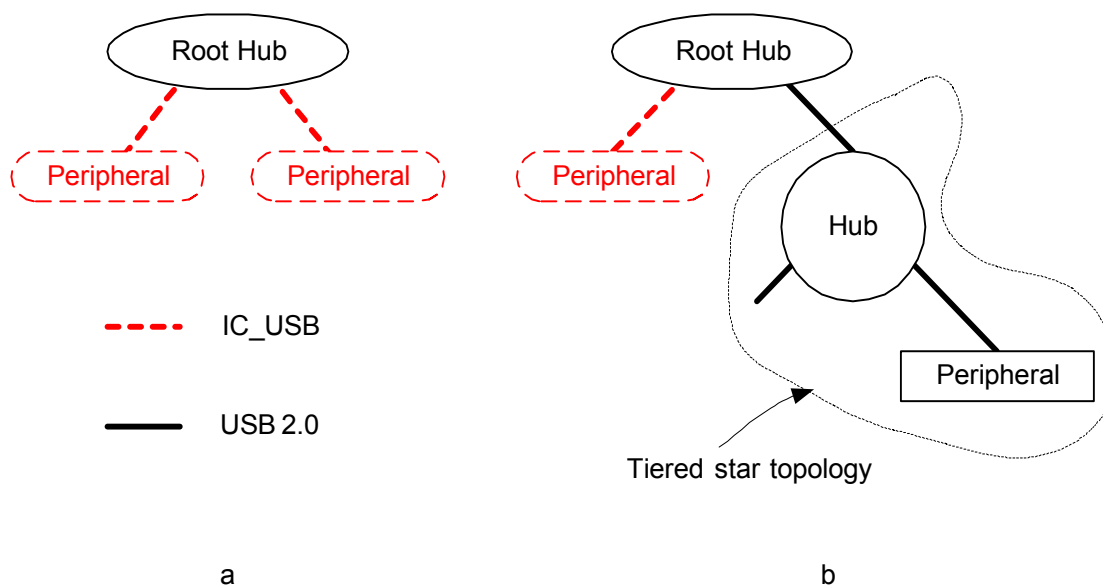


Figure 3-1 Valid Root Hub configurations supporting IC_USB

Figure 3-1 a represents two IC_USB downward-facing ports. The root ports support IC_USB.

Figure 3-1 b represents one IC_USB downward-facing port and one downward-facing port as defined in the core specification [USB]. Only the downward-facing port supports a tiered star topology.

A Root Hub supporting multiple IC_USB ports for removable peripherals, possibly belonging to different Families (see § 11.1) with different voltage classes (see § 5), shall be able to handle a voltage class negotiation sequence (see § 11.2) independently on each of its IC_USB interfaces.

3.2 Signals

Table 3-1 defines how the IC_USB signals, IC_VDD, GND, IC_DP and IC_DM, correspond to the USB signals.

IC_USB Signals	Description
IC_VDD	Used in the manner of USB VBUS
GND	Used in the manner of USB GND
IC_DP	Used in the manner of USB D+
IC_DM	Used in the manner of USB D-

Table 3-1 IC_USB signals

4 Power

4.1 Power Distribution

Peripherals may be self- or bus-powered.

The root port's interface and the peripheral's interface shall have the same nominal value IC_VDD.

Product design shall ensure that a removable peripheral may be assembled or removed from the system only when the power-supply voltage IC_VDD is turned off. As a consequence, there is no switch contact bouncing at make or break on IC_VDD during the power-up sequence.

The peripheral's connection sequence to IC_USB starts when IC_VDD is applied to the upstream port of the peripheral (see § 6).

A peripheral shall never source a measurable current on the IC_VDD line.

4.2 Power Management

In battery-powered peripherals, all subsystems have to minimize power consumption. The IC_USB idle state biasing current is minimized by design.

An IC_USB peripheral shall consume less than a specified IC_VDD current, ICC_init, from initial power-up until a USB configuration is set. The value of ICC_init is specified in Table 7-1 and applies to all peripherals.

When the peripheral is configured, the peripheral power consumption shall remain within the limit defined for its Family.

4.3 Configuration Descriptor *bMaxPower* Field

IC_USB peripherals do not use 5 Volt and do not connect to VBUS. All issues of appropriate power levels, both what is supplied by the host and what is required by the peripheral are handled in the IC_USB Family definition (see § 11.1). For this reason IC_USB redefines the meaning of the *bMaxPower* field in the Configuration Descriptor. To simplify operation of IC_USB peripherals with existing USB software stacks, all IC_USB peripherals shall place a value of 4 or less in the *bMaxPower* field. This does not indicate that the IC_USB peripheral actually draws 8 mA or less current -- the IC_USB family specifies peripheral power. This value of 4 or less in *bMaxPower* is sufficiently low that no host stack will refuse to configure the peripheral believing that the port has insufficient power.

5 Electrical Interfaces

The root port and the peripheral interfaces comply with the same electrical interface specification. The DC levels defined in Figure 5-1 apply to IC_DP and IC_DM data lines.

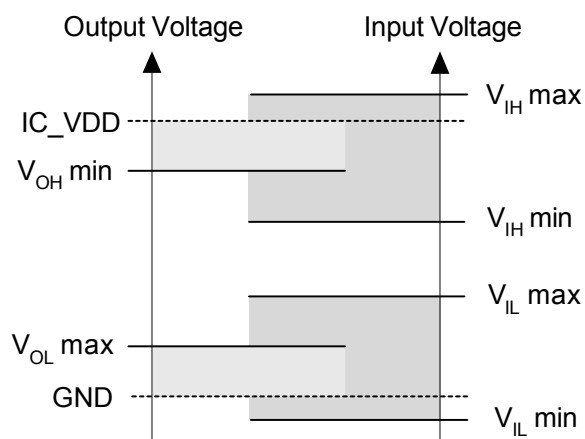


Figure 5-1 Voltage definitions for Inter-Chip USB

V_{IH} and V_{IL} are defined relatively to the actual IC_VDD level of the receiving interface.
 V_{OH} and V_{OL} are defined relatively to the actual IC_VDD level of the sending interface.

Where applicable, class-specific voltage levels are derived from those in the corresponding JEDEC standards [JESD8-B] and addenda for lower voltages [JESD8-7], [JESD8-11], [JESD8-12], and [JESD8-14].

5.1 Operating Voltage Classes

To promote interoperability, the interface of a root port and the interface of the peripheral shall each comply with a common voltage class and its DC electrical characteristics. To suit the needs of different industries and technologies, IC_USB allows a choice among five different voltage classes.

The interface of a given host or peripheral may support one or more voltage classes. In all cases, the voltage classes supported are indicated in the family specification. When voltage classes are supported, they shall be chosen according to § 11.1.2. The voltage class negotiation sequence shall be initiated by the IC_USB Bus Interface (see § 11.2).

5.1.1 Voltage Class 1.0 Volt

This class is derived from [JESD8-14].

Symbol	Parameter	Test conditions	Minimum	Maximum	Unit
IC_VDD	Supply Voltage		0.9	1.1	Volt
V_{IH}	Input High Voltage	$V_{OH} \geq V_{OH\ min}$	$0.65\ IC_VDD$	$IC_VDD + 0.2$	Volt
V_{IL}	Input Low Voltage	$V_{OH} \leq V_{OL\ max}$	-0.2	$0.35\ IC_VDD$	Volt
V_{OH}	Output High Voltage	$I_{OH} = -2mA$	$0.75\ IC_VDD$		Volt
V_{OL}	Output Low Voltage	$I_{OL} = 2mA$		$0.25\ IC_VDD$	Volt

Table 5-1 Voltage Class 1.0 Volt, DC electrical characteristics

5.1.2 Voltage Class 1.2 Volt

This class is derived from [JESD8-12].

Symbol	Parameter	Test conditions	Minimum	Maximum	Unit
IC_VDD	Supply Voltage		1.1	1.3	Volt
V _{IH}	Input High Voltage	V _{OH} ≥ V _{OH} min	0.65 IC_VDD	IC_VDD + 0.3	Volt
V _{IL}	Input Low Voltage	V _{OH} ≤ V _{OL} max	-0.3	0.35 IC_VDD	Volt
V _{OH}	Output High Voltage	I _{OH} = - 2mA	0.75 IC_VDD		Volt
V _{OL}	Output Low Voltage	I _{OL} = 2mA		0.25 IC_VDD	Volt

Table 5-2 Voltage Class 1.2 Volt, DC electrical characteristics

5.1.3 Voltage Class 1.5 Volt

This class is derived from [JESD8-11].

Symbol	Parameter	Test conditions	Minimum	Maximum	Unit
IC_VDD	Supply Voltage		1.4	1.6	Volt
V _{IH}	Input High Voltage	V _{OH} ≥ V _{OH} min	0.65 IC_VDD	IC_VDD + 0.3	Volt
V _{IL}	Input Low Voltage	V _{OH} ≤ V _{OL} max	-0.3	0.35 IC_VDD	Volt
V _{OH}	Output High Voltage	I _{OH} = - 2mA	0.75 IC_VDD		Volt
V _{OL}	Output Low Voltage	I _{OL} = 2mA		0.25 IC_VDD	Volt

Table 5-3 Voltage Class 1.5 Volt, DC electrical characteristics

5.1.4 Voltage Class 1.8 Volt

This class is derived from [JESD8-7].

Symbol	Parameter	Test conditions	Minimum	Maximum	Unit
IC_VDD	Supply Voltage		1.65	1.95	Volt
V _{IH}	Input High Voltage	V _{OH} ≥ V _{OH} min	0.65 IC_VDD	IC_VDD + 0.3	Volt
V _{IL}	Input Low Voltage	V _{OH} ≤ V _{OL} max	-0.3	0.35 IC_VDD	Volt
V _{OH}	Output High Voltage	I _{OH} = - 2mA	IC_VDD - 0.45		Volt
V _{OL}	Output Low Voltage	I _{OL} = 2mA		0.45	Volt

Table 5-4 Voltage Class 1.8 Volt, DC electrical characteristics

5.1.5 Voltage Class 3.0 Volt

This class is adapted from [JESD8-B].

Symbol	Parameter	Test conditions	Minimum	Maximum	Unit
IC_VDD	Supply Voltage		2.7	3.6	Volt
V _{IH}	Input High Voltage	V _{OH} ≥ V _{OH} min	2	IC_VDD + 0.3	Volt
V _{IL}	Input Low Voltage	V _{OH} ≤ V _{OL} max	-0.3	0.8	Volt
V _{OH}	Output High Voltage	I _{OH} = - 2mA	IC_VDD - 0.45		Volt
V _{OL}	Output Low Voltage	I _{OL} = 2mA		0.45	Volt

Table 5-5 Voltage Class 3.0 Volt, DC electrical characteristics

5.2 Downstream Port

Figure 5-2 shows a typical downstream-facing port when no peripheral is connected. Output buffers are connected in parallel to the input pins. Each pull-down RPDH is in series with a switch.

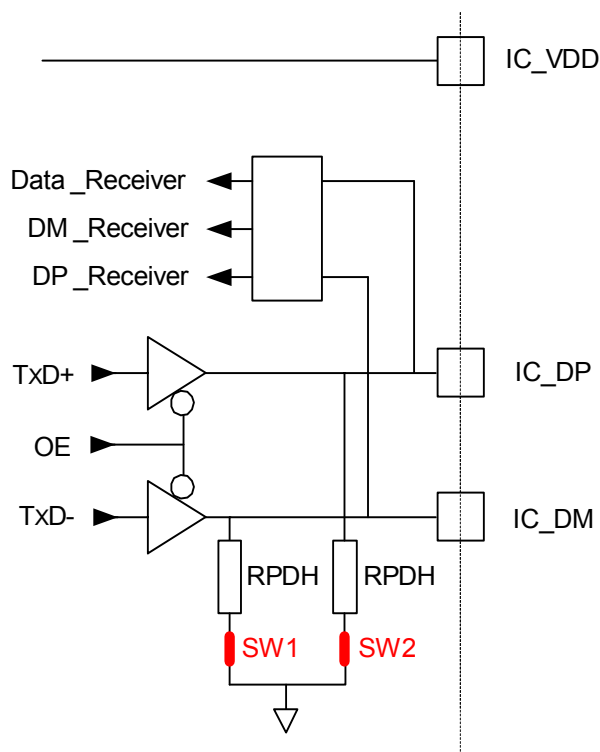


Figure 5-2 Downstream-facing port

5.2.1 Downstream-Facing Port Connected to a Fixed Peripheral

For a downstream-facing port connected to a fixed peripheral, RPDHs need not be present. The data lines are biased by the peripheral RPDHs.

5.2.2 Downstream-Facing Port Connected to a Removable Peripheral

For a downstream-facing port connected to a removable peripheral, RPDHs shall be connected to GND through SW1 and SW2.

Once the IC_USB Bus Interface has detected a peripheral and before Reset signaling ends (see § 6), the IC_USB Bus Interface has the responsibility for opening SW1 and SW2.

5.3 Upstream Port

Figure 5-3 shows a typical FS or LS upstream-facing port with settled switches after the voltage across the peripheral is above VMIN and before the peripheral connects to IC_USB. While the switch SW5 is open, the status of SW6 is unspecified.

The pull-up, either SW5 in series with RPU1 and SW6 or SW5 in series with RPU1 and RPU2, shall be connected to IC_DP for a FS peripheral or to IC_DM for a LS peripheral.

Output buffers are connected in parallel to the input pins.

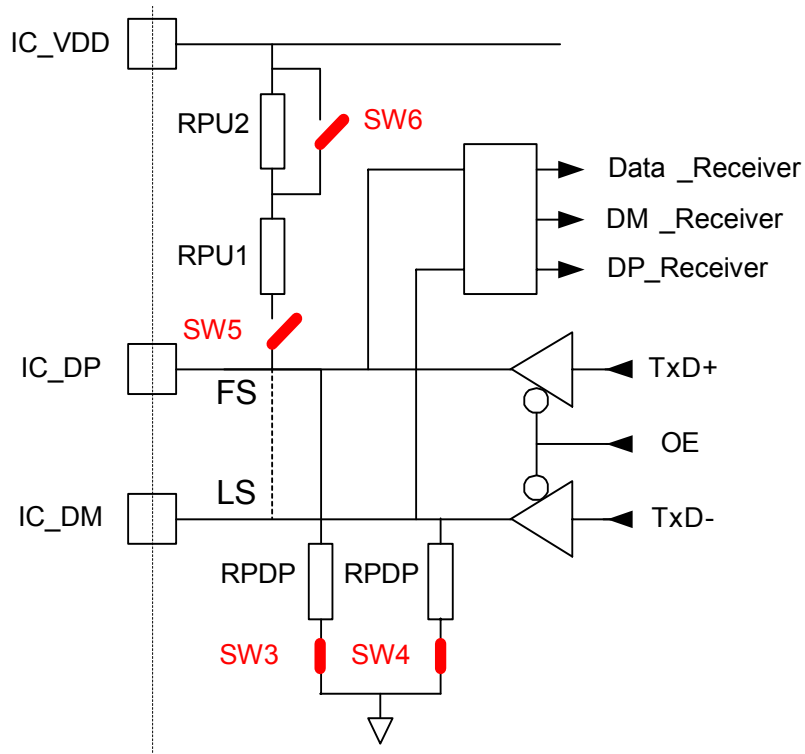


Figure 5-3 Upstream-facing port before attachment

When the root port supplies IC_VDD to the peripheral, the voltage across the peripheral rises to its stable value. During the transient phase, the peripheral shall behave according to the following rules:

1. When the voltage across the peripheral is below or at VMIN, SW3, SW4, SW5 and SW6 positions may not be guaranteed. As a consequence, the voltage on each data line is undefined.
2. When the voltage across the peripheral is above VMIN, SW3, SW4, SW5 and SW6 positions shall be guaranteed.
3. When the voltage across the peripheral is above VOP, stable and before Δt_{p1} expires, the peripheral shall connect to the bus.

Peripheral behaviors are detailed in § 6.

5.4 Pull-Up and Pull-Down Definitions

This section defines RPDH, RPDP, RPU1 and RPU2.

When the peripheral is removable, RPU1 and RPU2 contribute to the pull-up of one data line. They are used in two different circumstances:

1. RPU1 only pulls up the voltage on IC_DP or IC_DM beyond V_{IH} min even when RPDHs are pulling down.
2. RPU1 in series with RPU2 pulls up the voltage on IC_DP or IC_DM beyond V_{IH} min when RPDHs are not pulling down.

Ideally, pull-up and pull-down equivalent resistive values are related together as shown in the following theoretical relationships:

$$RPDH + (SW1 \text{ or } SW2) = RPDP + (SW3 \text{ or } SW4) = RPU1 + SW5 + RPU2 \quad (1)$$

$$(RPU1 + SW5) \text{ max} = [RPDH + (SW1 \text{ or } SW2)] \text{ min} / 10 \quad (2)$$

The allowed practical values, derived from (1) and (2), are listed in Table 7-1. Each resulting voltage divider sources a voltage compliant with interfaces voltage class DC electrical characteristics.

When the peripheral is fixed, there may be no pull-down RPDH on the host side, and the upstream-facing port configuration, shown in Figure 5-3, may be simplified. The pull-up may include only SW5 in series with a single pull-up equivalent to $RPU1 + RPU2$, and SW6 may not be present. The respective load to GND and to IC_VDD can be made equal.

$$RPDP + (SW3 \text{ or } SW4) = RPU1 + SW5 + RPU2 \quad (3)$$

6 Connection to IC_USB

IC_USB peripherals shall not be hot-plugged (see § 4.1). As a consequence, when the IC_USB Bus Interface provides power to the peripheral, it applies IC_VDD across a mechanically and electrically connected peripheral.

Within a Family, both the IC_USB Bus Interface and the peripheral may support more than one voltage class.

If the IC_USB Bus Interface supports more than one voltage class, the IC_USB Bus Interface starts the voltage class negotiation by supplying the IC_VDD level of the lowest voltage class, while the IC_USB data lines are connected to GND via RPDHs, if any. In the case of a removable peripheral compatible port, when no peripheral is present on a root port, IC_DP and IC_DM indicate a single-ended zero (SE0).

The following cases highlight the IC_USB Bus Interface port, the peripheral and the host behaviors when:

1. The Family supports one voltage class or multiple voltage classes while no peripheral is present.
2. The Family supports one voltage class and a peripheral is present.

These cases are documented in § 6.1, § 6.2 and § 6.3.

Sections 6.3.1 and 6.3.2 describe, respectively, LS and FS downstream and upstream port configurations.

6.1 One Voltage Class and No Peripheral Present

Figure 6-1 depicts the root port behavior when the IC_USB Bus Interface supports only one voltage class on that port and no peripheral is present.

The root port supplies IC_VDD as defined in the voltage class supported by the Family. When $\Delta th1$ expires, the IC_USB Bus Interface detects that no peripheral is attached. Optionally, the root port is powered off before $\Delta thoff$ expires to minimize power consumption.

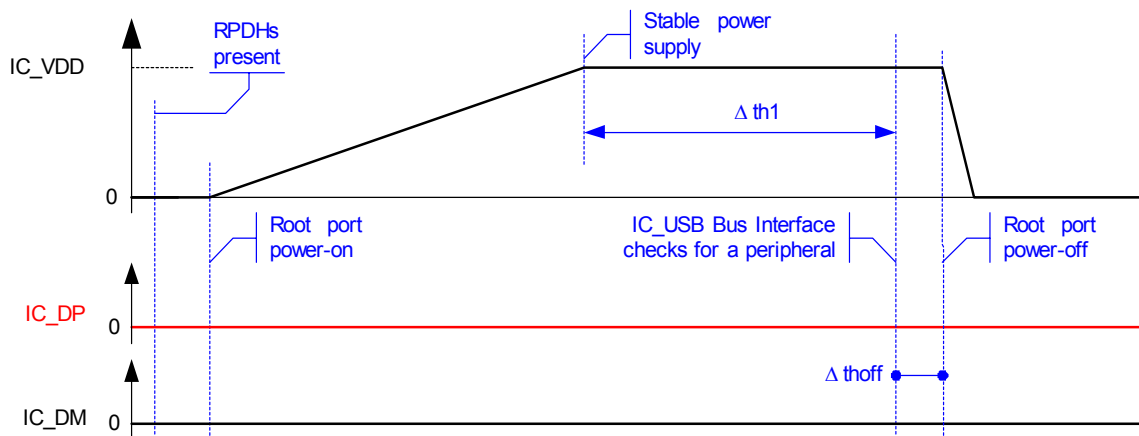


Figure 6-1 One voltage class supported, no peripheral present

6.2 Multiple Voltage Classes and No Peripheral Present

Figure 6-2 depicts the root port behavior when the IC_USB Bus Interface supports two voltage classes on that port and no peripheral is present. The same behavior shall apply to other multiple voltage classes.

The root port supplies IC_VDD as defined in the lowest voltage class supported by the Family. When $\Delta th1$ expires, the IC_USB Bus Interface detects that no peripheral is attached. The root port supplies IC_VDD as defined in the next voltage class required by the Family definition. During $\Delta thnew$, the IC_USB Bus Interface switches the power-supply voltage from the current voltage class to the next. A drop in the voltage might occur during that period of time. When $\Delta th1$ expires again, the IC_USB Bus Interface detects whether a peripheral is connected. If not, optionally, the root port may be powered off before $\Delta thoff$ expires to minimize power consumption.

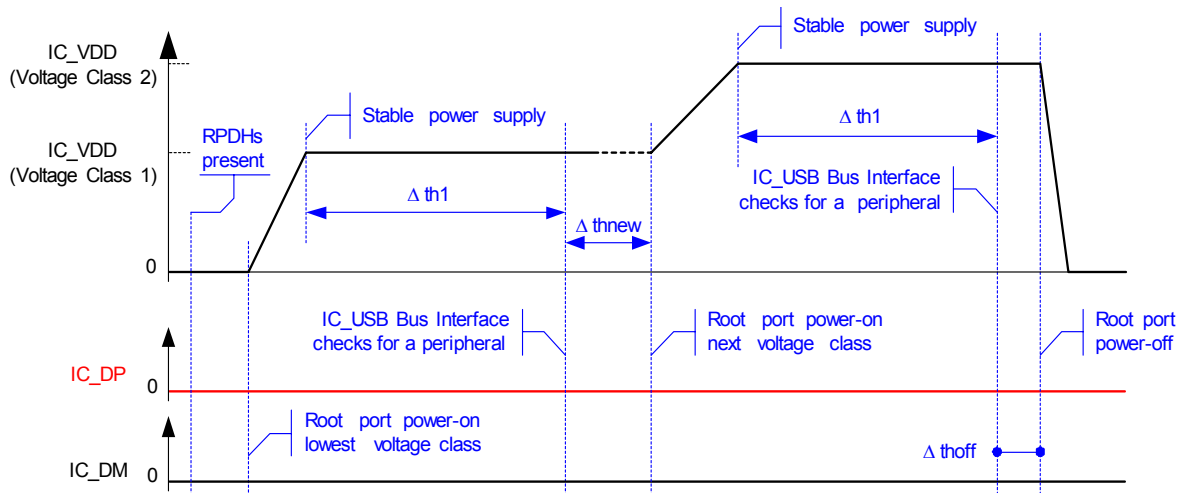


Figure 6-2 Two voltage classes supported, no peripheral present

6.3 Peripheral Present

Figure 6-3 depicts the root port behavior when the IC_USB Bus Interface supports one or more voltage classes and a peripheral is present on that port. The root port supplies IC_VDD as defined in the voltage class supported by the Family: During the power up sequence the following rules shall apply:

1. When IC_VDD is below or at VMIN, the state of IC_DP and IC_DM is undefined.
2. When IC_VDD is above VMIN, and prior to the expiration of Δt_{p1} , the data line status shall be settled.
3. When IC_VDD is below or at VOP the peripheral shall not attach.
4. When IC_VDD is valid and prior to the expiration of Δt_{p1} , the peripheral shall be attached.

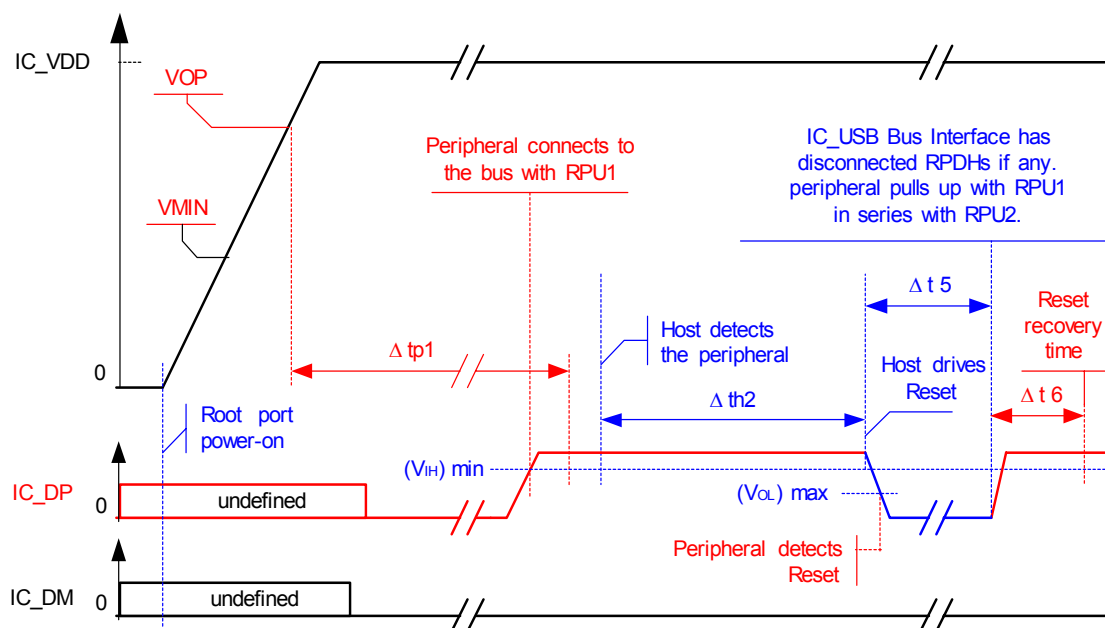


Figure 6-3 FS peripheral connection to the IC_USB

Table 6-1 defines timings used during the connection phase.

Parameter	Symbol	Min	Max	Units
Host timings	Δt_{h1}	20		ms
	Δt_{h2}		10	ms
	Δt_5	20*		ms
Peripheral timings	Δt_{p1}		20	ms
	Δt_6		10*	ms

Table 6-1 Timings during connection

* Host reset minimum timing and Peripheral reset recovery timing are defined in the core specification [USB].

For scenarios in Figure 6-1, Figure 6-2 and Figure 6-3, the following timing definitions apply.

 Δt_{h1} :

This is the minimum period of time allocated by the IC_USB Bus Interface before it checks for a peripheral.

 Δt_{p1} :

This is the maximum period of time allocated to a peripheral to settle its conditions on the IC_DP and IC_DM data lines.

If the voltage class of the peripheral matches the voltage class of the root port, before Δt_{p1} expires, the peripheral shall pull up one of the IC_DP and IC_DM data lines with RPU1 only. SW5 and SW6 are closed, and either SW3 or SW4 is open.

Also, in the case of a fixed peripheral, before Δt_{p1} expires, the IC_DP and IC_DM data lines are polarized by RPDs, even though there is no pull-down RPDH.

 Δt_{h2} :

This timing starts when the host has detected the peripheral and ends when the host drives Reset.

 Δt_5 (TDRST):

Before Δt_5 ends, the root port has disconnected RPDHs, if any, and the peripheral has inserted RPU2 in series with RPU1. After Δt_5 has expired, the IC_USB data lines are driven by terminations on the peripheral side only. The IC_USB is idle.

 Δt_6 (TRSTRCY):

The peripheral has less than Δt_6 to get ready to receive a first SETUP packet.

6.3.1 Low-speed Peripheral

A power-supply voltage compatible with a supported voltage class by a LS peripheral has been applied across that peripheral. The voltage on IC_VDD is stable and the voltages on IC_DP and IC_DM are defined. The electrical schematic of an IC_USB port with a LS removable peripheral connected is shown in Figure 6-4.

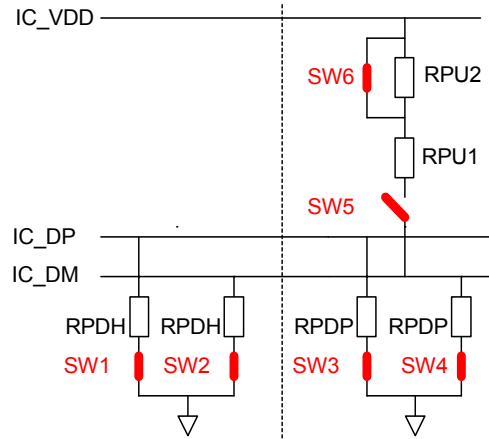


Figure 6-4 IC_USB port with LS peripheral, data lines pulled down by RPDs

Figure 6-5, Figure 6-6, and Figure 6-7 depict the IC_USB port with a LS removable peripheral connected during the attachment sequence.

Events 1 to 4 characterize the attachment sequence after a root port power-on, as follows:

1. When the peripheral connects to the IC_USB, it closes SW5 and breaks SW4 to pull up the IC_DM data line toward IC_VDD. With SW5 closing before SW4 breaks, the data line IC_DM does not float when there is no RPDH. The IC_USB Bus Interface recognizes that a LS peripheral is connected to IC_USB by detecting a voltage on IC_DM greater than V_{IH} before Δt_{p1} expires, as shown in Figure 6-5. After the peripheral is connected to the IC_USB, there is a bias current in the voltage divider RPU1, RPDH.

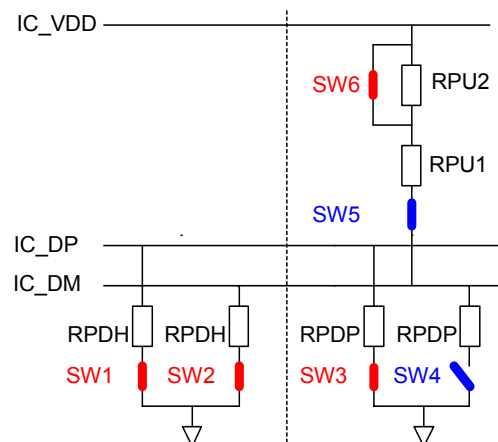


Figure 6-5 LS peripheral connection to IC_USB before Δt_{p1} expires

2. The host detects the peripheral and will drive Reset before Δt_{h2} expires.

- The IC_USB Bus Interface shall disconnect RPDHs, if present, when Reset is driven to reduce to zero the biasing current in Event 1. Figure 6-6 represents the LS IC_USB after the IC_USB Bus Interface has disconnected the RPDHs.

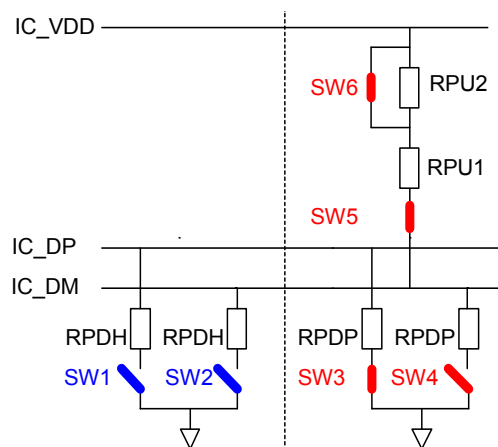


Figure 6-6 LS IC_USB, IC_USB Bus Interface disconnects RPDHs

- The peripheral shall break SW6 before Δt_5 expires to increase the load on the IC_DM data line. Figure 6-7 depicts the LS IC_USB beyond Δt_5 during idle.

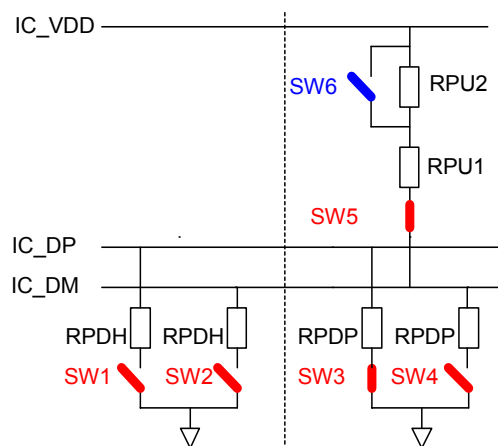


Figure 6-7 IC_USB port with LS peripheral during idle

Events 5 and 6 characterize a detach-attach sequence driven by the peripheral:

5. When the peripheral wants to detach from the IC_USB, it forces a SE0 by closing SW4 before breaking SW5, as shown in Figure 6-8. The peripheral keeps receiving power from the IC_USB after disconnecting.

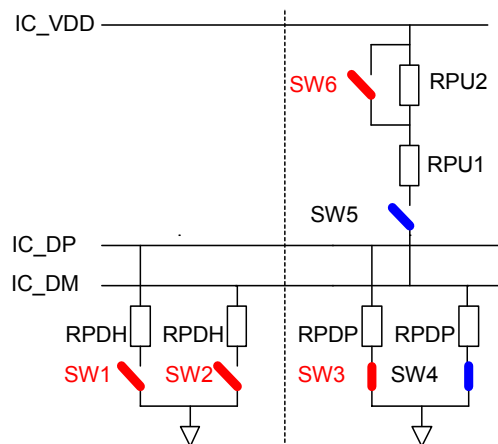


Figure 6-8 LS peripheral drives SE0

6. At any time, the peripheral may then decide to attach to the bus by closing SW5 before breaking SW4, as shown in Figure 6-9.

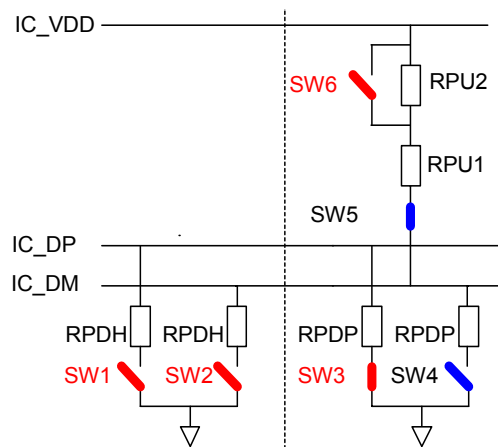


Figure 6-9 LS peripheral attaches to the bus

6.3.2 Full-speed Peripheral

A power-supply voltage compatible with a supported voltage class by a FS peripheral has been applied across that peripheral. The voltage on IC_VDD is stable, and the voltages on IC_DP and IC_DM are defined. The electrical schematic of an IC_USB port with a FS removable peripheral connected is shown in Figure 6-10.

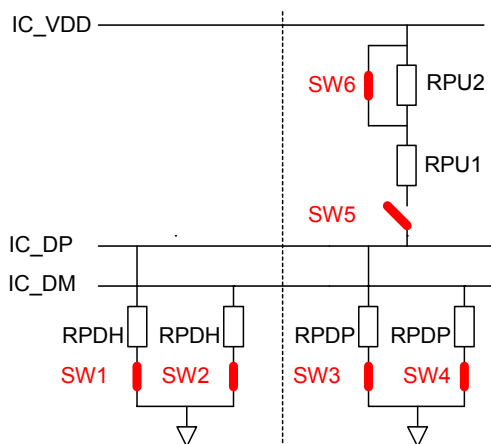


Figure 6-10 IC_USB port with FS peripheral, data lines pulled down by RPDPs

Figure 6-11, Figure 6-12, and Figure 6-13 depict the IC_USB port with a FS removable peripheral connected during the attachment sequence.

Events 1 to 4 characterize the attachment sequence after a root port power on, as follows:

1. When the peripheral connects to the IC_USB, it closes SW5 and breaks SW3 to pull up the IC_DP data line toward IC_VDD. With SW5 closing before SW3 breaks, the data line IC_DP does not float when there is no RPDH. The IC_USB Bus Interface recognizes that a FS peripheral is connected to IC_USB by detecting a voltage on IC_DP greater than V_{IH} before Δt_{p1} expires, as shown in Figure 6-11. After the peripheral is connected to the IC_USB, there is a bias current in the voltage divider RPU1, RPDH.

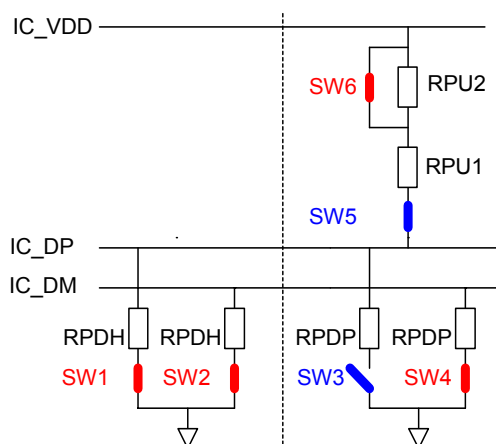


Figure 6-11 FS peripheral connection to IC_USB before Δt_{p1} expires

2. The host detects the peripheral and will drive Reset before Δt_{h2} expires.

- The IC_USB Bus Interface shall disconnect RPDHs, if present, when Reset is driven to reduce to zero the biasing current in Event 1. Figure 6-12 represents the FS IC_USB after the IC_USB Bus Interface has disconnected the RPDHs.

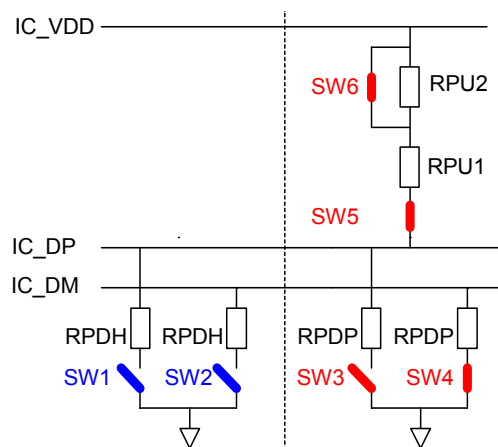


Figure 6-12 FS IC_USB, IC_USB Bus Interface disconnects RPDHs

- The peripheral shall break SW6 before Δt_5 expires to increase the load on IC_DP data line. Figure 6-13 depicts the FS IC_USB beyond Δt_5 during idle.

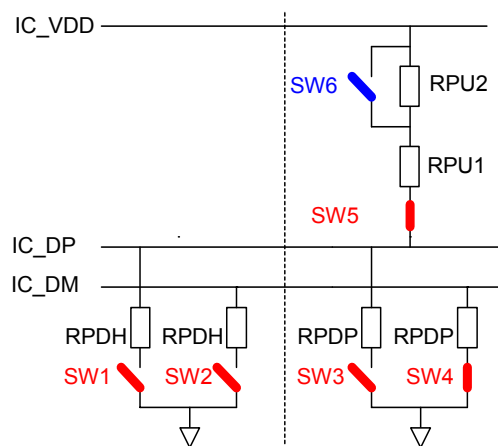


Figure 6-13 IC_USB port with FS peripheral during idle

Events 5 and 6 characterize a detach-attach sequence driven by the peripheral:

- When the peripheral wants to detach from the IC_USB, it forces a SE0 by closing SW3 before breaking SW5, as shown in Figure 6-14. The peripheral keeps receiving power from the IC_USB after disconnecting.

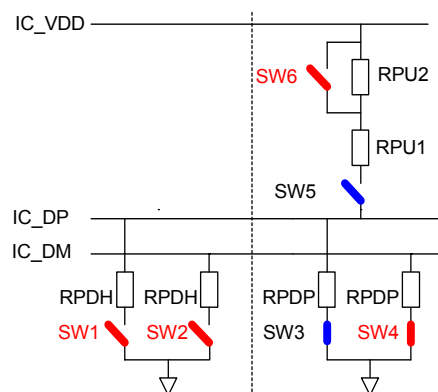


Figure 6-14 FS peripheral drives SE0

6. At any time, the peripheral may then decide to connect back to the bus by closing SW5 before breaking SW3, as shown in Figure 6-15.

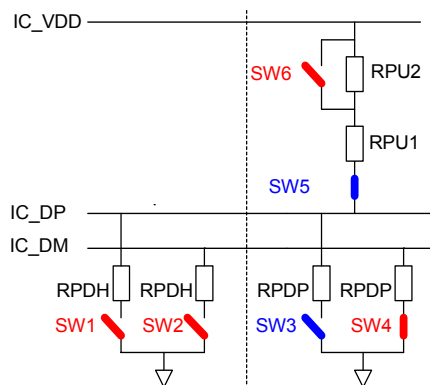


Figure 6-15 FS peripheral attaches to the bus

6.3.3 Connect and Disconnect Timings

A disconnect condition, as specified in the core specification [USB], shall be detected by the host when a SE0, forced either by the RPDHs or RPDPs, persists on a downstream port for more than 2.5 μ s.

The connect condition is as specified in the core specification.

6.3.4 Data Line Loads During Traffic Signaling

The switches controlling connection/disconnection of the pull-up and pull-down resistors shall be managed at the hardware level. This management shall be independent from the USB software stack.

IC_USB minimizes the current consumption in idle state.

Each family shall specify one of the following behaviors during signaling:

1. No change during traffic signaling -- pull-down and pull-up resistors remain in the same state as in idle.
2. To save power during traffic signaling, the peripheral shall isolate the remaining pull-down and pull-up resistors from the circuit by opening the serial switches. This allows the buffers to drive only the capacitive loads on IC_DM and IC_DP and further reduce the power consumption. The switches shall change state during the SOP and while the bus is driven to J State at the end of EOP (see Figure 9-2).

7 Electrical Characteristics

Table 7-1 summarizes the IC_USB's electrical characteristics.

Parameter	Symbol	Conditions	Min	Max	Units
Capacitive loads:					
Input equivalent load	Cinput	Note 1		7	pF
Input loads mismatch		Note 2	-1	+1	pF
Output load	CL	Note 3		18	pF
Output loads mismatch		Note 4	-2	+2	pF
Terminations:					
Upstream port first Pull-up resistor	RPU1	Note 5	1	3	kΩ
Upstream port second Pull-up resistor	RPU3	Note 6	30	150	kΩ
Upstream port Pull-down resistor	RPDP	Note 7	30	150	kΩ
Downstream port Pull-down resistor	RPDH	Note 8	30	150	kΩ
Pull-down resistors matching Ratio (Downstream and Upstream)	RPDRatio	Note 9	0.7	1.3	
Currents:					
Input Current	I _{in}	§ 8	-2	+2	μA
IC_VDD power provider		§ 4	8		mA
Maximum peripheral power consumption during enumeration	ICC_init	§ 4.2		8	mA
Maximum peripheral power consumption during Suspend	ICC_suspend	§ 12.1		150	μA

Table 7-1 Electrical characteristics

Note 1: The Input equivalent load is the resulting capacitor for IC_DP and IC_DM pins when receiving.

Note 2: The Input loads mismatch is the difference between the resulting capacitors of IC_DP and IC_DM pins when receiving.

Note 3: The Output load is the capacitive load driven by IC_DP and IC_DM pins when transmitting.

Note 4: The Output loads mismatch is the difference between the capacitive loads driven by IC_DP and IC_DM pins when transmitting.

Note 5: RPU1 is used by the peripheral to force the voltage above V_{IH} min on one data line when a pull-down is on the host port. The resistor value includes the switches SW5 and SW6 in series (see § 5.4).

Measurement method: The peripheral is powered by an IC_VDD level compliant with each supported voltage class, the switches are closed, a voltage source V_{pin} is applied to the tested data line with $0 \leq V_{pin} < IC_VDD$ and the current I_{pin} is measured:

$$RPU1 = (IC_VDD - V_{pin}) / I_{pin}$$

Note 6: RPU3 is used by the peripheral to bias one data line when no pull-down is on that data line. The resistor value includes SW5, RPU1 and RPU2 (see § 5.4).

Measurement method: The peripheral is powered by an IC_VDD level compliant with each supported voltage class, the switch SW5 is closed, a voltage source V_{pin} is applied to the tested data line with $0 \leq V_{pin} < IC_VDD$ and the current I_{pin} is measured:

$$RPU3 = (IC_VDD - V_{pin}) / I_{pin}$$

Note 7: The peripheral pull-down resistors are between IC_DP and GND and IC_DM and GND.

Each resistor value includes RPDP and the resistance of the switch, SW3 or SW4, in series.

Measurement method: The peripheral is powered by an IC_VDD level compliant with each supported voltage class, the switch is closed, a voltage source Vpin is applied to the tested data line with $0 < V_{pin} \leq IC_VDD$ and the current Ipin is measured:

$$RPDP = V_{pin} / I_{pin}$$

Note 8: The root port pull-down resistors are between IC_DP and GND, and IC_DM and GND.

The root port pull-down resistors may not be present when a peripheral is always connected on that port.

Each resistor value includes RPDH and the resistance of the switch, SW1 or SW2, in series.

Measurement method: The root port is powered by an IC_VDD level compliant with each supported voltage class, the switch is closed, a voltage source Vpin is applied to the tested data line with $0 < V_{pin} \leq IC_VDD$ and the current Ipin is measured.

$$RPDH = V_{pin} / I_{pin}$$

Note 9: This applies to both root port and peripheral. The ratio is determined for each tested Vin across the range of applied voltage levels by dividing the pull-down resistor measured on the IC_DM data line by the pull-down resistor measured on the IC_DP data line as described in Note 7 and Note 8.

8 Input Characteristics

8.1 Host Chip

When the host is operational, with disconnected pull-down resistors and in receiving mode, the input characteristics of an IC_USB port shall be such that, when submitted to input voltages GND or IC_VDD on IC_DP and IC_DM, the input currents (I_{in}) are within the range indicated in Table 7-1.

8.2 Peripheral Chip

When the peripheral is operational, with disconnected pull-up resistor and in receiving mode, the input characteristics of the peripheral shall be such that, when submitted to input voltages GND or IC_VDD on IC_DP and IC_DM, the input currents (I_{in}) are within the range indicated in Table 7-1.

9 Signaling

Figure 9-1 represents an example of an IC_USB electrical link between a root port and a FS removable peripheral during idle or during signaling. The capacitors (CL) represent the equivalent capacitive loads seen by the buffers.

During idle, SW1, SW2, SW3 and SW6 are open, SW4 and SW5 are closed, RPU1 is in series with RPU2, and together they pull up the IC_DP signal line while RPDP pulls down the IC_DM data line.

The IC_USB Bus Interface has disconnected its RPDHs, and the peripheral pulls up the IC_DP line and pulls down the IC_DM line. The bias current is null.

During signaling, by family option (see § 6.3.4), the peripheral is either required to present the same terminations to GND and to IC_VDD that it presents during idle, or to open SW4 and SW5 during downstream or upstream traffic, leaving no load on the IC_USB beside capacitive loads.

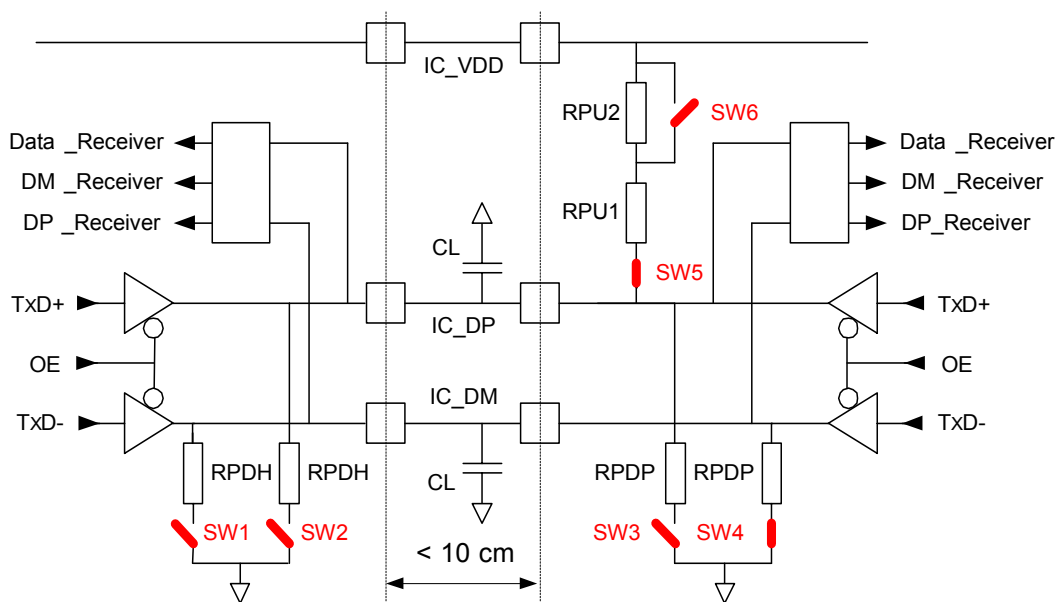


Figure 9-1 Root port and a FS removable peripheral during idle

Table 9-1 defines the IC_USB logical states.

IC_DP	IC_DM	Description
0	0	Single Ended Zero (SE0)
0	1	Differential "Zero"
1	0	Differential "One"
1	1	Single Ended One (SE1)

Table 9-1 IC_USB logical states

9.1 Data Signaling

Four periods characterize data signaling in a packet: Idle, Start of Packet (SOP), Data transmission and End of Packet (EOP). Figure 9-2 depicts the different periods in a packet.

Data transmission within a packet uses differential signals with the following specifics:

1. IC_DP and IC_DM DC voltages V_{OH} and V_{OL} shall comply with the Voltage Class DC characteristics as defined in § 5.1.
2. Data signals rise and fall times shall comply with § 9.2.2.
3. J-to-K and K-to-J transitions shall comply with § 9.2.3. Skew between IC_DP and IC_DM signals may induce spurious SE1 and SE0 during J-to-K and K-to-J transitions; receiver designs shall ignore them.

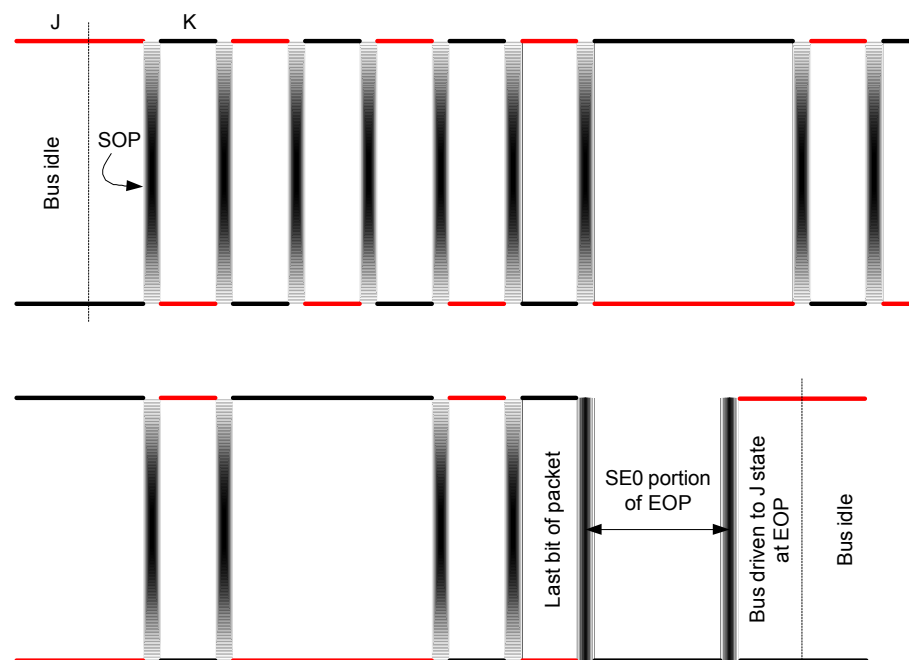


Figure 9-2 Data signaling

9.2 Buffer Characteristics

The IC_USB uses two output buffers to drive data signals onto the connections between two ICs. In a transitory situation, a pull-down termination to GND and a pull-up termination to IC_VDD may load a buffer.

The static output swing of the buffer in its low state shall be below V_{OL} max while sinking the current associated with the pull-up termination, and in its high state shall be above V_{OH} min while sourcing the current associated with the pull-down termination.

The buffer is not required to accept a permanent short circuit between its output and any combination of the signals IC_DP or IC_DM, IC_VDD and GND. To assure reliability in the field, Families of removable peripherals may set additional requirements.

9.2.1 Tests Setup

The tests setup for measuring buffer performances is shown in Figure 9-3.

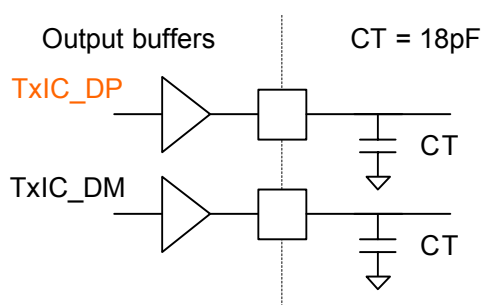


Figure 9-3 Tests setup

9.2.2 Data Signal Rise and Fall

The output rise and fall times are measured between 10% and 90% of the actual signal swing ($V_{OH}-V_{OL}$) above V_{OL} (see Figure 9-4) on the tests set up as shown in Figure 9-3 and on each data line. Rise and fall time requirements (see Table 9-2) apply to J-to-K and K-to-J transitions as well as to single-ended transitions.

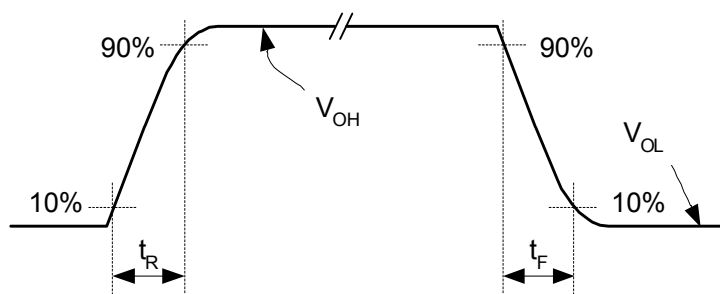


Figure 9-4 Data signals IC_DP and IC_DM rise and fall times

Parameter	Symbol	Conditions	Max	Units
Data Signal Rise and Fall characteristics:				
Signal Rise time	t_R	§ 9.2.1	10	ns
Signal Fall time	t_F	§ 9.2.1	10	ns

Table 9-2 LS and FS Data Signals IC_DP and IC_DM rise and fall times

9.2.3 J-to-K and K-to-J Transitions

This section specifies J-to-K and K-to-J transitions.

Figure 9-5 and Figure 9-6 depict IC_DP and IC_DM transitions in worst-case conditions. They illustrate skew resulting from data-signal routings, buffers and capacitive loads.

The rising signal is in advance in (a) or is late in (b). Timings td1 through td4 specify the maximum values listed in Table 9-3. These timings characterize signals on IC_DP and IC_DM when J and K states are indeterminate.

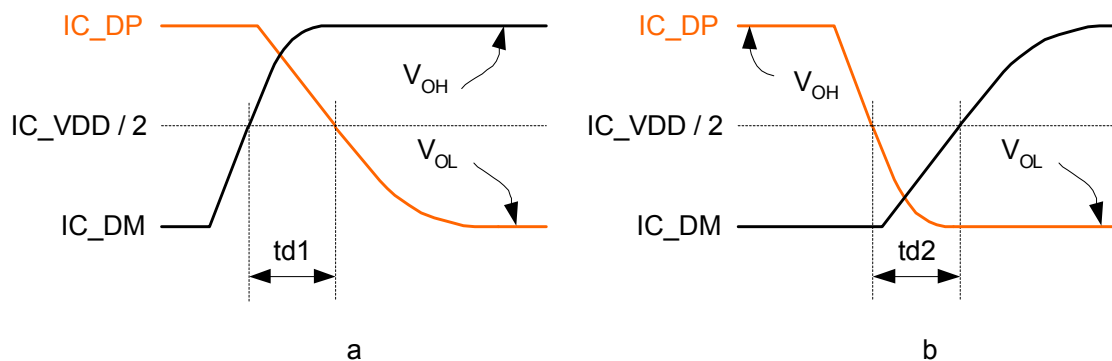


Figure 9-5 IC_DP V_{OH} to V_{OL} and IC_DM V_{OL} to V_{OH} transitions

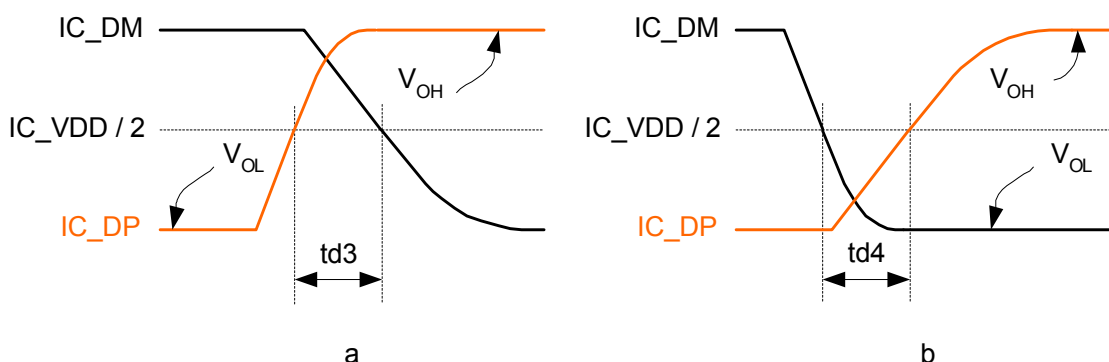


Figure 9-6 IC_DM V_{OH} to V_{OL} and IC_DP V_{OL} to V_{OH} transitions

Parameter	Symbol	Conditions	Max	Units
J-to-K and K-to-J transitions:				
IC_DM goes high before IC_DP goes low	td1	§ 9.2.1	5	ns
IC_DP goes low before IC_DM goes high	td2	§ 9.2.1	5	ns
IC_DP goes high before IC_DM goes low	td3	§ 9.2.1	5	ns
IC_DM goes low before IC_DP goes high	td4	§ 9.2.1	5	ns

Table 9-3 J-to-K and K-to-J transitions

9.2.4 Data Source Jitter

The source of data can have some variation (jitter) in the timing of edges of the data transmitted. The time between any set of data transitions is $N * T_{\text{PERIOD}} \pm \text{jitter time}$, where N is the number of bits between the transitions and T_{PERIOD} is the actual period of the data rate. The data jitter on the data lines is measured with the loads as defined in § 9.2.1 and at the $IC_VDD/2$ level, as shown in Figure 9-7.

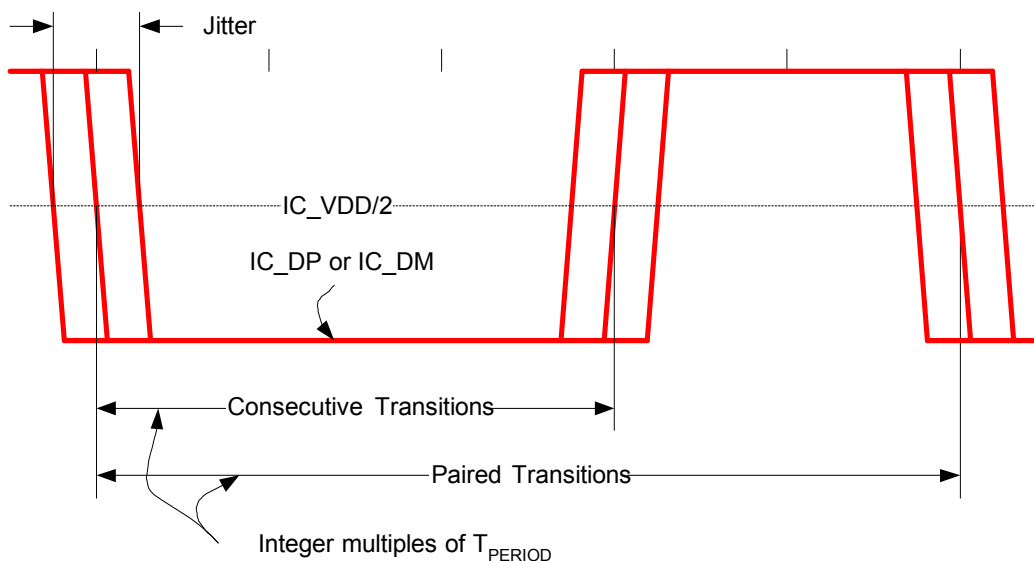


Figure 9-7 Data Jitter

- For FS transmissions, the jitter time for any consecutive data transitions must be within ± 2 ns and within ± 1 ns for any set of paired data transitions.
- For LS transmissions, the jitter time for any consecutive data transitions must be within ± 25 ns and within ± 10 ns for any set of paired data transitions.

9.3 Receiver Characteristics

The receiver shall correctly interpret IC_USB signals. The receiver shall ignore spurious SE1 of less than 8 ns and SE0 of less than 14 ns.

10 Fixed Peripheral

A peripheral is fixed when the system design ensures that it is permanently connected to its host. It may be, for example, a separate chip that is soldered on the system printed circuit board.

In the case of a fixed peripheral, the system designer selects a Voltage Class from the specified Voltage Classes and selects components compatible with this voltage class (see § 5.1). Both the IC_USB Bus Interface and the peripheral electrical interfaces shall comply with the same Voltage Class DC electrical characteristics.

Components used in a fixed configuration do not need to support voltage class negotiation, as they only need to support one common voltage class.

The host shall provide the power required by a fixed peripheral.

This does not preclude the use of host and peripheral components designed to support removable peripherals (see § 11). Mechanical interlocks required by removable peripheral systems do not apply to fixed peripheral designs.

11 Removable Peripheral

The system design shall ensure that, when a peripheral is added to or removed from the system, the power IC_VDD supplied by the IC_USB Bus Interface to the peripheral has been turned off. The system begins powering up the peripheral after the physical assembly has been completed.

To connect the IC_USB Bus Interface's IC_VDD, GND, IC_DP and IC_DM to the removable peripheral's counterparts, an electrical connector has to be used. Most applications may need to define a custom electrical connector to match such characteristics as the peripheral's volume and accessibility. A mechanical interlock defines a Family. Members of a Family of peripherals have common characteristics as specified in § 11.1.

For interoperability, the peripheral interface power supply must match the IC_USB Bus Interface's power supply. Section 11.2 defines the voltage class negotiation sequence implemented by IC_USB Bus Interfaces supporting multiple voltage classes.

11.1 Family

A Family of hosts and removable peripherals is defined as a set of hosts and peripherals having matching mechanical interfaces. The mechanical interface shall include a mechanical interlock, to ensure that the peripheral connector matches only with the IC_USB host port connector dedicated to that Family.

The definition of a Family shall also ensure the following characteristics:

1. Within the Family, any choice of host and peripheral supports at least one common voltage class.
2. All hosts support full-speed. If any peripheral within the Family supports low-speed, the host shall support low-speed.
3. Within the Family, every host shall be able to provide the power required by any peripheral in the Family.
4. The Family shall specify the option of data line loads during traffic signaling (see § 6.3.4).

Peripherals of a given Family may bring different functions to the user, for example, through the support of different USB device classes. Families shall comply with all the requirements of the present document, and may also be subject to specific requirements not covered by this specification.

11.1.1 One Voltage Class

A Family may support only one voltage class from those defined in § 5.1, in which case, support for this voltage class is mandatory on both the IC_USB host and the peripheral sides.

The IC_USB Bus Interface does not need to support the voltage class negotiation sequence defined in § 11.2. It may of course remove power when no peripheral is present.

The peripheral may or may not ensure that it will attach to the IC_USB only if the voltage applied to its interface is above VOP (see § 6.3). This requirement may be useful to allow further evolution, as such behavior is necessary for the peripheral to support the voltage class negotiation sequence with an IC_USB Bus Interface supporting multiple voltage classes.

11.1.2 Multiple Voltage Classes

A Family may support multiple voltage classes. To optimize the negotiation process, IC_USB Bus Interfaces and removable peripherals shall make use only of the following voltage classes defined in § 5.1:

- 1.0 Volt
- 1.8 Volt
- 3.0 Volt

Support of multiple voltage classes facilitates migration to foreseen higher-density IC technologies. An IC_USB Bus Interface supporting two or more voltage classes shall support the voltage class negotiation sequence defined in § 11.2.

The peripherals shall support VOP detection prior to attachment, regardless of whether they are capable of working at different voltage classes.

11.1.3 Family Definition Template

Industry-specific working groups, aware of particular constraints, may define a Family using the template in Table 11-1.

Family Requirements	Description	Comments
Mechanical interface	Exhaustive definition of the connecting mechanism used by the Family, including dimensions, contacts definition and locations, etc.	This is out of scope of the present document. The definition may, for example, point to an existing industry standard.
Family voltage classes	<ol style="list-style-type: none"> 1. IC_USB Bus Interface requirements for voltage classes support. 2. Peripheral requirements for voltage classes support and VOP detection. 3. Maximum peripheral power consumption from IC_VDD. 	<p>This shall remain compliant with the present document.</p> <p>The voltage class support requirements shall ensure that any combination of IC_USB Interface and peripheral belonging to the family will be able to establish communication using a common voltage class.</p>

Table 11-1 Family definition template

Different strategies are possible to share the constraints between hosts and peripherals, for example:

- Require all the voltage classes to be supported on one side (host or peripheral), allowing the other side to support any allowed voltage class.
- Require each side to support a combination of two voltage classes, when three classes are allowed.

The following sections 11.1.4, 11.1.5, and 11.1.6 provide three detailed examples of Families. The mechanical interface of each Family is unique. One sketch is depicted for each example. The host's mechanical interface matches with the peripheral's mechanical interface. The mechanical interface further provides four electrical contacts to support IC_USB.

The electrical interfaces are defined for each example. The definition includes the voltage classes that are supported on the host side and on the peripheral side. Also, some possible combinations are shown.

11.1.4 Example 1

This example depicts a Family designed to support only one voltage class.

- Mechanical interface:

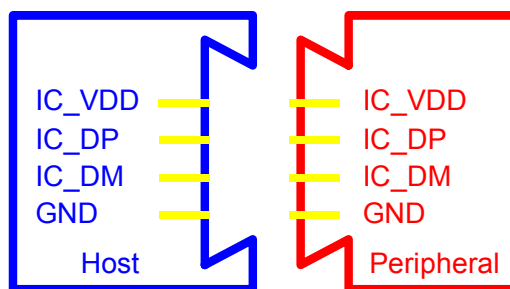


Figure 11-1 Example 1, Mechanical interface

- Electrical interface:

Voltage class supported by the host	Voltage class supported by the peripheral	Comments
3.0 Volt	3.0 Volt Attachment is possible when the power-supply voltage is above VMIN.	The interfaces are powered by 3.0 Volt.

Table 11-2 Example 1, Electrical interface

Only one voltage class, 3.0 Volt, is allowed on both the host and the peripheral sides.

The host supports the 3.0 Volt voltage class and does not implement the voltage class negotiation sequence.

IC_VDD shall be turned off if no peripheral is detected.

The peripheral supports the 3.0 Volt voltage class.

The peripheral may attach to the IC_USB for any power-supply voltage above VMIN.

The system relies on the timing introduced by the host after it powers up a port and before it checks for a peripheral. This timing allows the power-supply voltage across the peripheral to reach a stable and final value within the voltage class range. At that time, the peripheral is ready to receive a Reset signal and to bring functions to the user.

11.1.5 Example 2

This example depicts a Family designed to support possible future evolution driven by new silicon technologies.

- Mechanical interface:

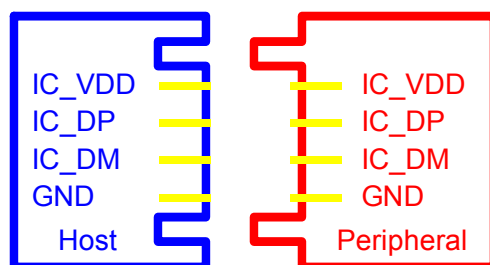


Figure 11-2 Example 2, Mechanical interface

- Electrical interface:

Voltage classes supported by the host	Voltage classes supported by the peripheral	Comments
1.0 Volt and 1.8 Volt	1.0 Volt Attachment is possible when the power-supply voltage is above VMIN.	The interfaces are powered by 1.0 Volt.
	1.8 Volt Attachment is possible only when the power-supply voltage is at or above VOP.	The interfaces are powered by 1.8 Volt. Voltage detection is implemented. Voltage-dependent functions are possible.

Table 11-3 Example 2, Electrical interface

The Family supports 1.0 Volt and 1.8 Volt voltage classes. The Host is required to support both, and it implements the voltage class negotiation sequence by first supplying 1.0 Volt.

Each peripheral supports only one voltage class.

A peripheral supporting the 1.0 Volt voltage class may attach to the IC_USB for any power-supply voltage above VMIN. The system relies on the timing introduced by the host after it powers up a port and before it checks for a peripheral. This timing allows the power-supply voltage across the peripheral to reach a stable and final value within the voltage class range. At that time, the peripheral is ready to receive a Reset signal and to bring functions to the user.

A peripheral supporting the 1.8 Volt voltage class can attach to the IC_USB only when the power-supply voltage is at or above VOP. This kind of peripheral relies on a voltage detection mechanism to attach.

11.1.6 Example 3

This example depicts a Family where some peripherals require more energy, and therefore a higher power-supply voltage, to bring a specific function to the user.

Also, some other peripherals may require higher-density silicon technologies to increase, for example, the memory size possibly integrated into the peripheral. There, a lower power-supply voltage is needed.

- Mechanical interface:

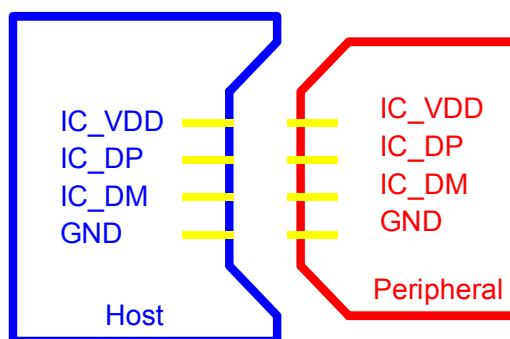


Figure 11-3 Example 3, Mechanical interface

- Electrical interface:

Voltage classes supported by the host	Voltage classes supported by the peripheral	Comments
3.0 Volt	3.0 Volt Attachment is possible only when the power-supply voltage is at or above VOP of that voltage class.	The interfaces are powered by 3.0 Volt. Voltage detection is implemented. Voltage-dependent functions are possible.
	1.8 Volt and 3.0 Volt Attachment is possible when the power-supply voltage is above VMIN.	The interfaces are powered by 3.0 Volt.
1.8 Volt and 3.0 Volt	3.0 Volt Attachment is possible only when the power-supply voltage is at or above VOP of that voltage class.	The interfaces are powered by 3.0 Volt. Voltage detection is implemented. Voltage-dependent functions are possible.
	1.8 Volt and 3.0 Volt Attachment is possible when the power-supply voltage is above VMIN.	The interfaces are powered by 1.8 Volt.

Table 11-4 Example 3, Electrical interface

The Family supports the 1.8 Volt and 3.0 Volt voltage classes.

Some Hosts support the 3.0 Volt voltage class only.

Some other Hosts support both the 1.8 Volt and 3.0 Volt voltage classes and then will initiate the voltage class negotiation sequence starting with the 1.8 Volt voltage class.

Some peripherals support the 3.0 Volt voltage class only. They attach to the IC_USB only when the power-supply voltage is at or above the VOP of that voltage class. This kind of peripheral relies also on a voltage-detection mechanism to attach.

Some peripherals support both the 1.8 Volt and 3.0 Volt voltage classes. A 3.0 Volt to lower-voltage converter may be embedded in the IC peripheral to allow internal circuits to work under the lower voltage. Despite this extra footprint, the IC peripheral, with more functions, is still smaller than the one with fewer functions and no DC-to-DC voltage converter.

This sort of peripheral may attach to the IC_USB for any power-supply voltage above VMIN. The system relies on the timing introduced by the host after it powers up a port and before it checks for a peripheral. This timing allows the power-supply voltage across the peripheral to reach a stable and final value within the voltage class range. At that time, the peripheral is ready to receive a Reset signal and to bring functions to the user.

11.2 Voltage Class Negotiation Sequence

When a Family specification allows more than one voltage class, the IC_USB Bus Interface and peripheral shall negotiate a common voltage class for their electrical interface before communicating, according to the procedure described below.

A voltage class negotiation sequence, as depicted in Figure 11-4, is initiated between the root port and the peripheral during the power-up sequence of the peripheral.

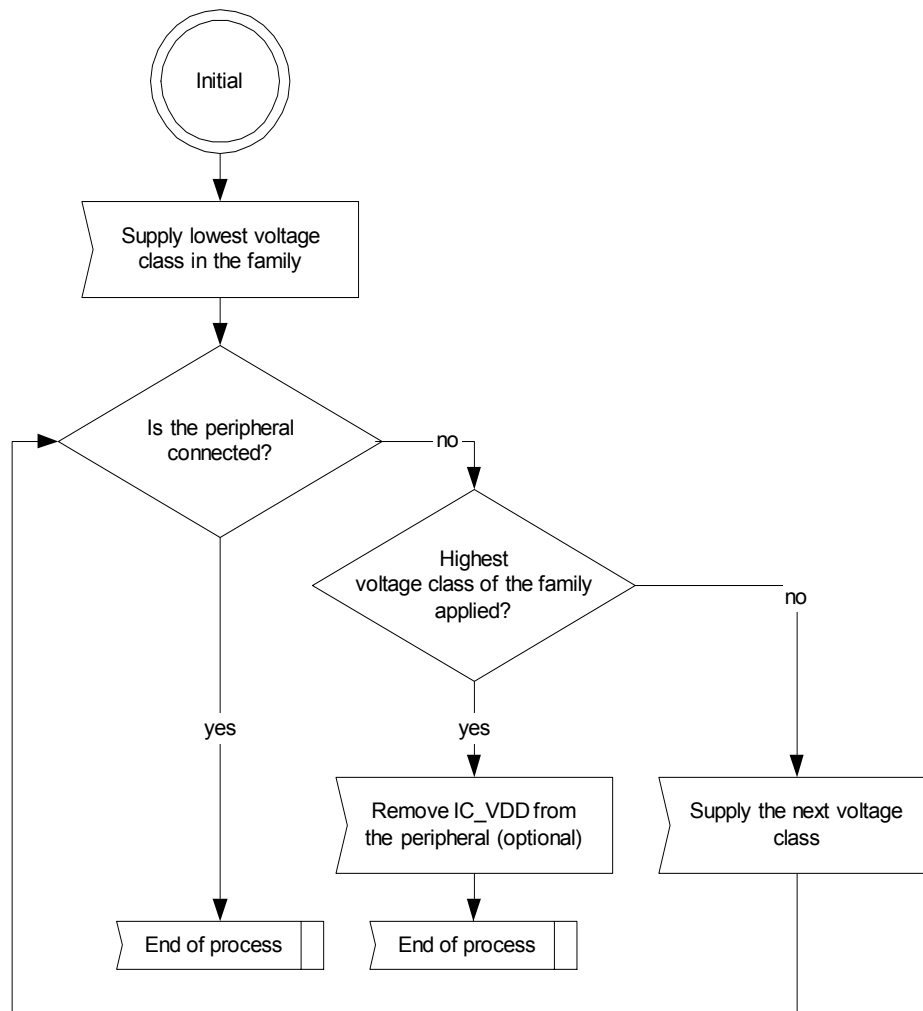


Figure 11-4 Voltage class negotiation sequence

11.2.1 IC_USB Bus Interface Responsibilities

The IC_USB Bus Interface is responsible for selecting the appropriate voltage class required by the peripheral. When more than one voltage class is supported, the IC_USB Bus Interface shall start the power-up sequence of the peripheral by supplying the peripheral with the lowest power-supply voltage available on the IC_USB Bus Interface side. The IC_USB Bus Interface shall always start with the voltage class featuring the lowest nominal voltage and proceed sequentially toward higher voltages. The voltage class negotiation mechanism applies only once during the power-up phase.

If the peripheral does not connect to the bus before Δt_{h1} expires (see § 6), the IC_USB Bus Interface is responsible for supplying the next power-supply voltage available. This sequence is repeated until the peripheral connects to the bus. The process stops when the last voltage class supported by the host is reached and there is no connection to the bus.

When a peripheral disconnects itself from the IC_USB by forcing a SE0 and then connects itself again to the IC_USB bus, the IC_VDD voltage shall not be affected. The IC_VDD voltage always remains unchanged until the power is removed from the system.

11.2.2 Peripheral Responsibilities

The peripheral is responsible for connecting to the IC_USB when it detects that the voltage on IC_VDD is compatible with the voltage range covered by its voltage class.

A peripheral shall not be damaged when powered at the highest voltage class specified for a host of its Family, even if it only supports operation at lower voltages.

12 Suspend, Resume and Remote Wakeup

12.1 Suspend

Suspend mode applies to IC_USB as defined in the core specification [USB]. However, in IC_USB, no DC bias current is dedicated to the VTERM (3.3 Volt) generator, nor is there any IC_USB bias current. Therefore, the IC_USB suspend current is minimized. The suspend current value is specified in § 7, and it applies to all voltage classes. The biasing conditions of the bus as defined in § 6.3.1 and § 6.3.2 during Suspend and upon Resume remain the same as before entering the Suspend mode.

12.2 Resume

Resume mode applies to IC_USB as defined in the core specification [USB].

12.3 Remote Wakeup

Remote Wakeup applies to IC_USB as defined in the core specification [USB].

