High-Speed Inter-Chip USB Electrical Specification

Version 1.0

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Revision History

The 1.0 revision of the specification is intended for product design. Every attempt has been made to ensure a consistent and implementable specification. Implementations should ensure compliance with this revision.

Revision	Issue Date	Comments
1.0	18 September 2007	Initial Release

Please send comments via electronic mail to techsup@usb.org
For industry information, refer to the USB Implementers Forum web page at http://www.usb.org

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1 Introduction

1.1 General

USB is the ubiquitous peripherals interconnect of choice for a large number of computing and consumer applications. Many systems provide a comprehensive set of drivers to support all commonly available USB peripherals. This enables consumers to purchase and use USB peripherals without having to install a new driver, thus strengthening the popularity of USB. In addition, there are a large number of suppliers of USB silicon, so costs are normally very low for product manufacturers of USB hosts and peripherals.

As a result of this popularity, it is becoming increasingly attractive to use USB as a chip-to-chip interconnect within a product (without use of external cables or connectors). However, because USB was designed to enable hot-plugging and unplugging of peripherals over cables up to 5 meters in length, there are certain power and implementation issues that are not attractive for many chip-to-chip interconnect solutions.

To better meet the needs of a USB chip-to-chip interconnect, this specification defines a High-Speed Inter-Chip USB supplement to the USB2.0 specification. HSIC accomplishes this by removing the analog transceivers, thus reducing complexity, cost, and manufacturing risk.

1.2 Objective of This Supplement

This supplement provides all of the technical information required to implement a High-Speed Inter-Chip USB solution when used in conjunction with the USB 2.0 Specification.

1.3 Intended Audience

Developers and Systems Architects of High-Speed Inter-Chip interfaces that have a maximum circuit trace length of 10cm are the intended audience for this document.

1.4 Relevant Documents

Reference	Title	Location
[USB]	In the context of this document, this specifically refers to the following parts of the USB 2.0 Specification package: • The original USB 2.0 specification released on April 27, 2000 • Errata to the USB 2.0 specification as of December 7, 2000 • Pull-up/pull-down Resistors Engineering Change Notice to the USB 2.0 specification • Errata to the USB 2.0 specification as of May 28, 2002 • Interface Association Descriptor Engineering Change Notice to the USB 2.0 specification • Unicode Engineering Change Notice to the USB 2.0 specification as of February 21, 2005	www.usb.org/
[JESD76-2]	Standard Description of 1.2 V CMOS Logic Devices (Normal Range Operations)	www.jedec.org/

1.5 Acronyms and Terms

Term	Definition
DDR	Double Data Rate: Describes a signaling technique where data is transferred on both the rising and falling edges of a reference clock (STROBE for HSIC).
HSIC	High Speed Inter-Chip: Used in reference to the 2-signal data/strobe signals defined by this specification
LVCMOS	Standard Description of 1.2V CMOS Logic Devices (Normal Range of Operations), as described in JESD76-2
Strobe-period	The unit of time from a STROBE rising edge until the next periodic STROBE rising edge (or falling edge to falling edge).

Other acronyms and terms used in this specification are defined in the core specification [USB].

2 Significant Features

HSIC is a 2-signal (strobe, data) source synchronous serial interface which uses 240MHz DDR signaling to provide High-Speed 480Mbps USB transfers which are 100% host driver compatible with traditional USB cable-connected topologies. Full-Speed (FS) and Low-Speed (LS) USB transfers are not directly supported by the HSIC interface (a HSIC enabled hub can provide FS and LS support, as well as IC_USB support)

Major feature and performance highlights are as follows:

- High-Speed 480Mbps data rate only
- Source-synchronous serial interface
- No power consumed unless a transfer is in progress
- Maximum trace length of 10cm
- No hot Plug-n-Play support, no hot removal/attach
- Signals driven at 1.2V standard LVCMOS levels
- Designed for low-power applications
- No high-speed chirp protocol, the HSIC interface is always operated at high-speed

2.1 HSIC & Standard USB comparison:

HSIC is an interface that has been designed to replace a standard USB PHY and USB Cable with an interface that is optimized for circuit board layouts. Figure 1 shows a standard USB implementation of a USB Host and a USB peripheral, Figure 2 shows a similar implementation with an HSIC interface.

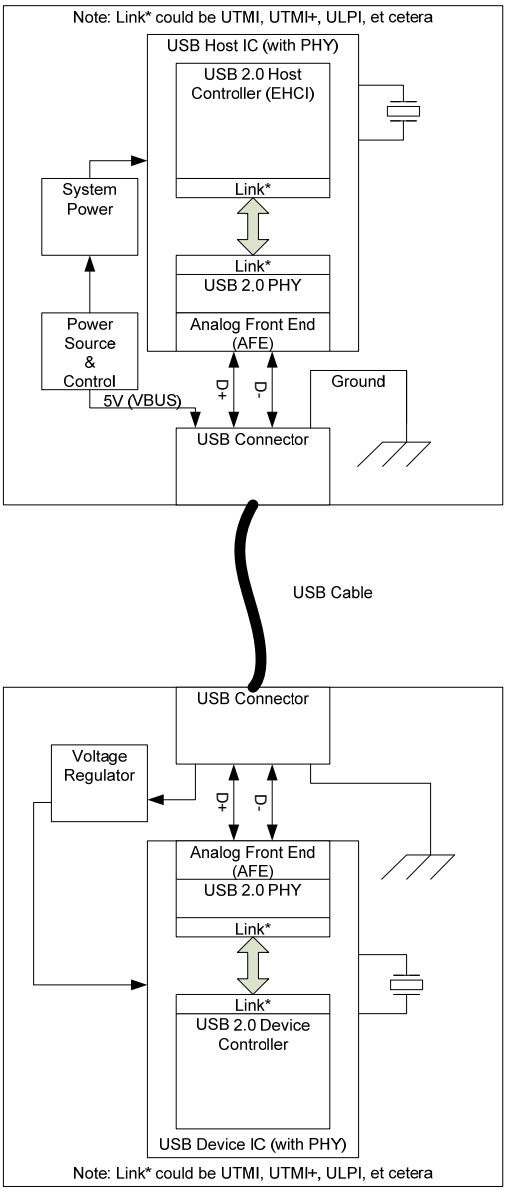

Figure 1 - Standard USB Host & Peripheral Example

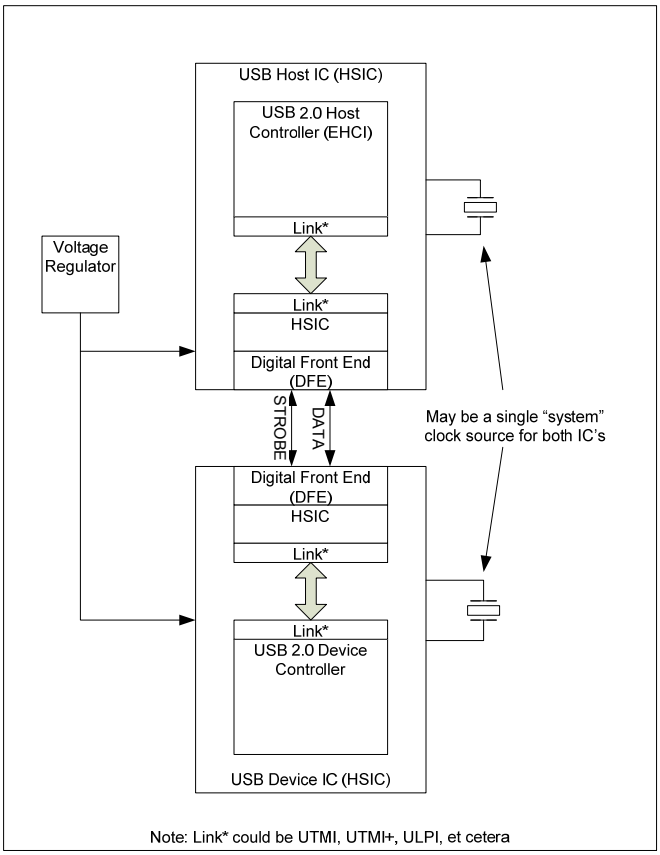

Figure 2 - HSIC USB Host & Peripheral Example

3 HSIC USB Signaling & Operation:

An HSIC interface consists of two signals, a bi-directional data strobe signal (STROBE) and a bi-directional DDR data signal (DATA) that is synchronous to the (STROBE) signal of the transmitter. HSIC utilizes the tiered star topology of the USB 2.0 specification; therefore the interface is a point to point connection between a downstream facing host/hub port and an upstream facing peripheral port. The data that is transferred includes sync, bit stuffing, EOP and NRZI encoding to ensure that the packet lengths, turn around times, interpacket gaps, etc… are as identical as possible between HSIC and standard USB 2.0 signaling. This enables a single host to drive standard USB and HSIC USB interfaces without any modifications to the internal logic structure of the host.

There are several different types of HSIC signaling; bus state signaling and data signaling are used for standard USB data and control signaling. The peripheral discovery signaling occurs after power has been applied and is utilized for determining peripheral and host availability.

3.1 Discovery:

In order to support various IC power sequences, the HSIC interface is structured so that a host or a peripheral can be powered in any order.

3.1.1 Power state is OFF:

USB host, hub and peripherals must be constructed in such a way to ensure that the STROBE and DATA signals do not float to an undetermined value, or a false connect may be detected. An example implementation to prevent this floating condition from occurring is to incorporate a clamping diode on both STROBE and DATA.

3.1.2 Power state is ON, but HSIC is not enabled.

- Downstream facing host or hub HSIC interface:
  - Must assert bus keepers on both STROBE and DATA to provide a logic ‘0’ state
- Upstream facing peripheral or hub HSIC interface:
  - Will not assert any signaling (passive or active).

3.1.3 Power state is ON, and HSIC is enabled.

- Downstream facing host or hub HSIC interface:
  - Must present a USB IDLE bus state, and will monitor the STROBE and DATA lines for a CONNECT bus state.

- Upstream facing peripheral or hub HSIC interface:
  - Peripheral will monitor the STROBE and DATA lines for an IDLE bus state.

3.1.4 Power state is ON, HSIC is enabled, and Peripheral signals a CONNECT.

- Upstream facing peripheral or hub HSIC interface:
  - Upon detection of an IDLE bus state, must assert a CONNECT bus state.
- Downstream facing host or hub HSIC interface:
  - Upon detection of a CONNECT bus state, standard USB enumeration will commence.

3.2 Speed detection:

There are no provisions for a speed detection/selection mechanism in HSIC, the interface defaults to USB 2.0 High-Speed operation.

3.3 Bus State Signaling

The STROBE and DATA lines signal the bus states shown in Table 3-1 when there are no active data transfers in progress.

Table 3-1: Bus State Signaling

	STROBE	DATA	Description
IDLE	Hi	Lo	1 or more Strobe-periods
CONNECT	Lo	Hi	2 Strobe-periods
RESUME	Lo	Hi	For time periods per USB 2.0 SPEC
SUSPEND	Hi	Lo	Per USB 2.0 SPEC
RESET	Lo	Lo	Per USB 2.0 SPEC

IDLE

(STROBE line high, DATA line low) for 1 or more Strobe-periods. Note: when transitioning from any non-IDLE bus state to an IDLE bus state, the transmitter must drive IDLE for 2 Strobe-periods.

CONNECT

(STROBE line low, DATA line high) for 2 Strobe-periods. Note: this is an event that only occurs after a peripheral detects an IDLE bus state for the first time, usually after power on reset (POR). At the end of signaling a CONNECT, the transmitter must drive IDLE for 2 Strobe-periods.

RESUME

(STROBE line low, DATA line high) to match current USB specification. Note: RESUME can be signaled by either a host or a peripheral, i.e. remote wake up.

SUSPEND

Identical to idle state, but the time period matches current USB specification.

RESET

(STROBE line low, DATA line low) to match current USB specification requirements.

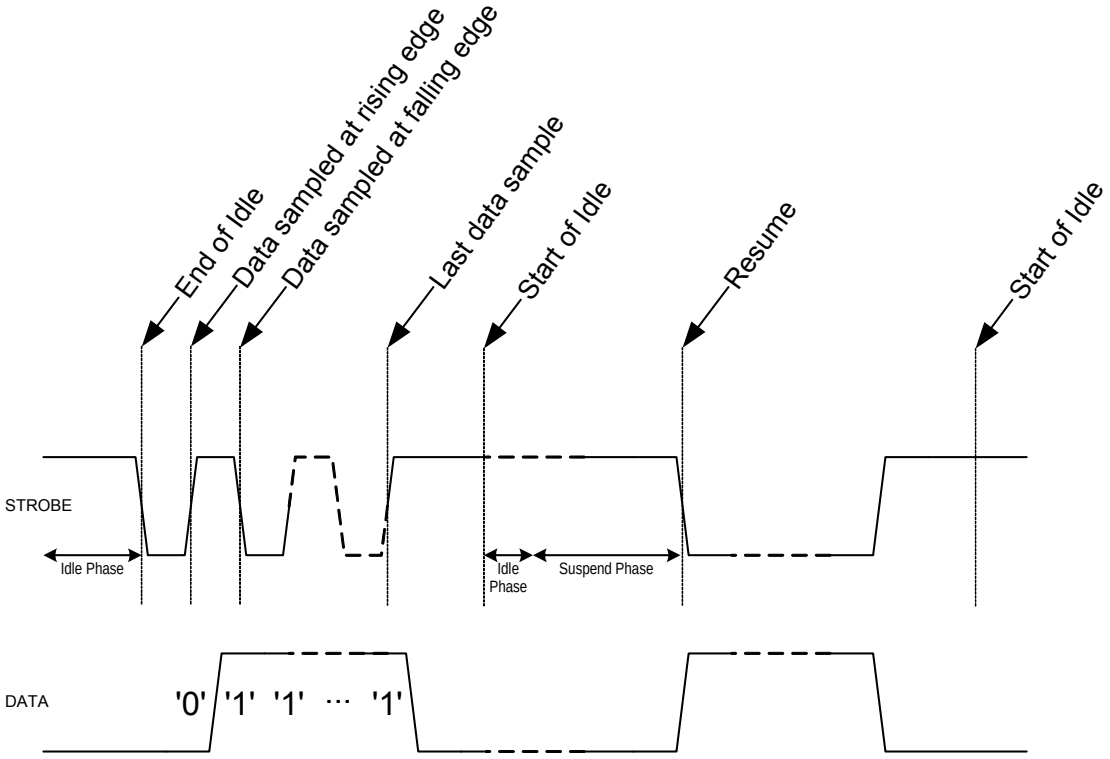

Figure 3: Mixed Bus State and Data Transfer Signaling

3.4 Data Signaling:

Data is transferred when the STROBE and DATA lines transition from IDLE to END-OF-IDLE, which is defined as STROBE switching from high to low, while DATA is low. Data is transferred for the next strobe transition and all subsequent transitions of the STROBE line, until IDLE is again signaled.

3.5 Bus Keepers in IDLE bus state:

Bus keepers will be asserted by the downstream facing Host or Hub interface on the STROBE and DATA lines to maintain the bus IDLE state. These keepers must be disabled 1 Strobe-period after any non-IDLE bus state is detected, and must be enabled 1 Strobe-period after IDLE is detected.

3.6 Hub Support and Mixed Interface Systems:

HSIC interfaces can be combined with standard analog USB interfaces and Inter-Chip 1.0 interfaces. The figures below show several examples.

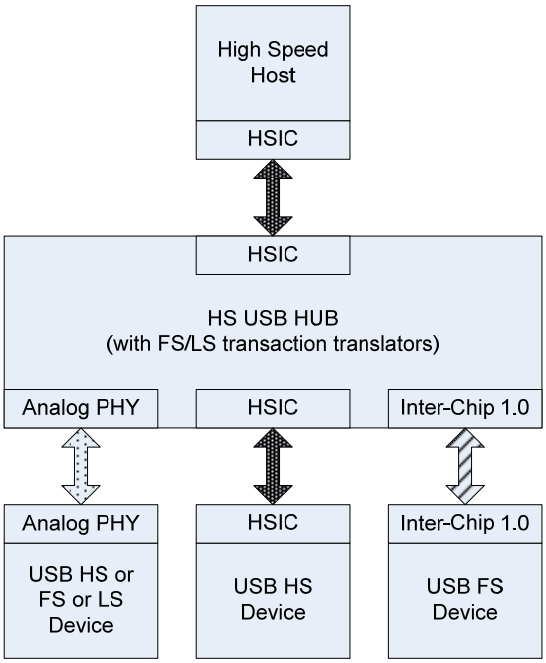

Figure 4 - HSIC Host & Mixed Interface Hub

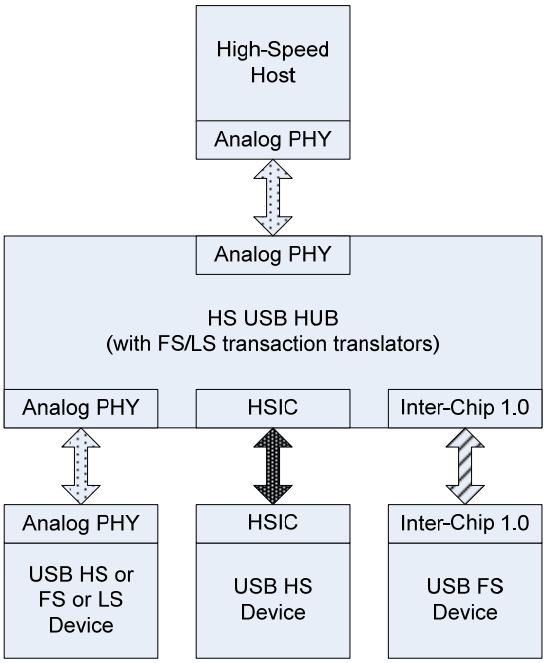

Figure 5 - Analog Host & Mixed Interface Hub

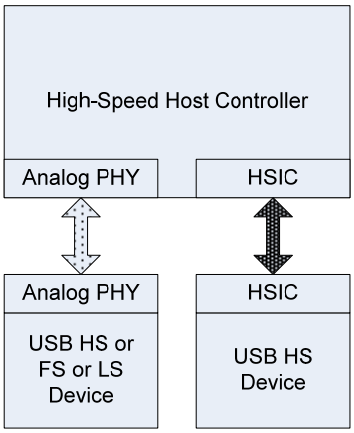

Figure 6 - Host with Analog & HSIC interfaces

4 Electrical Specification:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
HSIC signaling Voltage	V_{DD}	1.1	1.2	1.3	V	
I/O Voltage input low	V_{IL}	-0.3		0.35 * V_{DD}	V	
I/O Voltage input high	V_{IH}	0.65 * V_{DD}		V_{DD} + 0.3	V	
I/O Voltage output low	V_{OL}			0.25 * V_{DD}	V	
I/O Voltage output high	V_{OH}	0.75 * V_{DD}			V	
I/O Pad Drive Strength	O_D	40		60	Ω	Controlled output impedance driver
I/O Weak keepers	I_L	20		70	µA	
I/O Input Impedance	Z_i	100			kΩ	
Total Capacitive load	C_L	3		14	pF	Note 1
Characteristic Trace Impedance	T_I	45	50	55	Ω	
Circuit Board Trace Length	T_L			10	cm	
Circuit Board Trace propogation skew	T_S			15	ps	Note 3
STROBE Frequency	F_{STROBE}	239.988	240	240.012	MHz	±500ppm Note 2
Slew Rate (rise and fall) STROBE & DATA	T_{slew}	0.60 * V_{DD}	1.0	1.2	V/ns	Averaged from 30% - 70% points Note 2
Receiver DATA Setup time (with respect to STROBE)	T_s	300			ps	Measured at the 50% point Note 2
Receiver DATA Hold time (with respect to STROBE)	T_h	300			ps	Measured at the 50% point Note 2

Note 1) Total Capacitive Load, C_L, includes device Input/Output capacitance, and capacitance of a 50ohm PCB trace with a length of 10cm.

Note 2) Jitter and duty cycle are not separately specified parameters, they are incorporated into the values in the table above.

Note 3) Maximum propagation delay skew in STROBE or DATA with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that the signal timing is within specification limits at the receiver.