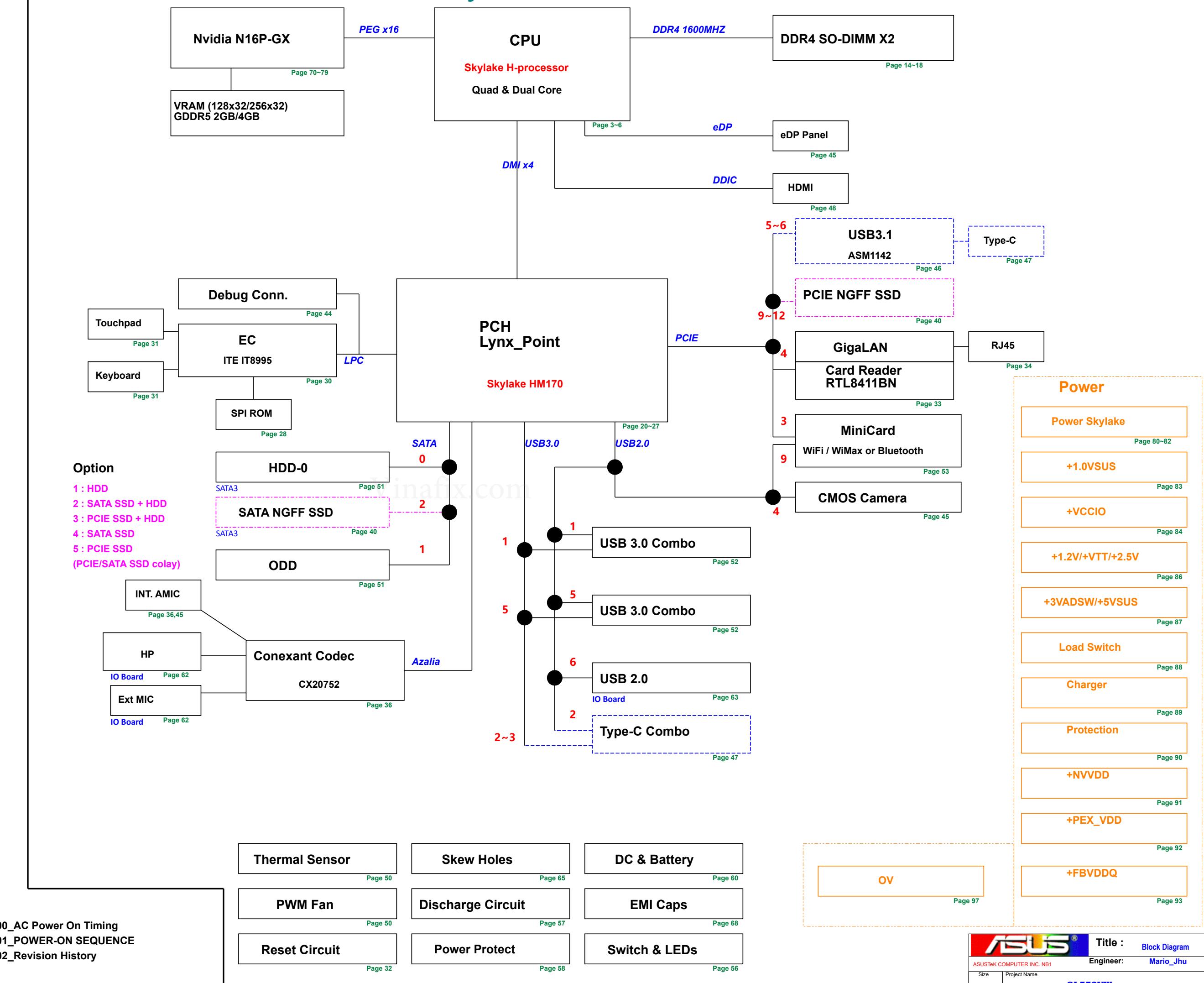


001_Block Diagram
 002_System Setting
 003_CPU_DMI,PEG,eDP,DDI
 004_CPU_DDR4
 005_CPU_GND
 006_CPU_CFG,RSVD
 007_CPU_XDP
 008_CPU_PWR
 009_CPU_PWR
 010_CPU_POWER_CAP
 016_DIM_DDR4 SO-DIMM A(0) TOP
 017_DIM_DDR4 SO-DIMM B(0) TOP
 018_DIM_CA/DQ Voltage
 019.Silego_Green_CLK_Gen
 020_PCH_HDA,SMBUS,SYS PWR,JTAG
 021_PCH-CPT(2)_PCIE,USB2,MISC
 022_PCH-CPT(3)_CLK,LPC,USB3
 023_PCH-CPT(4)_eDP,PCI,DP
 024_PCH-CPT(5)_SPI
 025_PCH-CPT(6)_GPIO
 026_PCH-CPT(7)_POWER,GND
 027_PCH-CPT(8)_POWER,GND
 028_PCH-SPI ROM,OTH
 029_PCH-XDP
 030_KBC_IT8995
 031_KBC_KB & TP
 032_RST_Reset Circuit
 033_LAN_CR_RTL8411BN
 034_LAN RJ45
 036-AUD-CX20752
 037-AUD-AMP
 038_AUD-SPEAKER Connector
 040_NGFF_SSD
 044_DEBUG_LPC
 045_CRT_eDP
 046_USB 3.1 ASM1142
 047_USB 3.1 MB Type-C
 048_HDMI
 050_FAN_Thermal Sensor & Fan
 051_HDD & ODD CON
 052_USB_Port
 053_WiFi/WiMax
 055_Lid_SW_BD
 056_LED
 057_DSG_Discharge
 058_Power Protect
 059_MB_to_I/O_CONN.
 060_DC & BAT IN
 062->>>/I/O board(1)_MIC/HP
 063->>>/I/O board(2)_USB
 065_ME_NUT
 069_OTH_EMI
 070_VGA_PCI-EXPRESS(1)
 071_GPU_FB-IF_GDDR5(2)
 072_FRAME BUFFER-A(3)
 073_FRAME BUFFER-B(4)
 074_VGA_CRT/LVDS(5)
 075_VGA_GPIO/DVI/DP(6)
 076_VGA_XTAL/STRAPPING(7)
 077_VGA_PWG/GND(8)
 078_VRAM Cap
 080_PW_SKYLAKE (1)
 081_PW_SKYLAKE (2)
 083_PW_+1.0VSUS
 084_PW_+VCCIO
 086_PW_1.2V+VTT/2.5V
 087_PW_+3VADSW/+5VSUS
 088_PW_LOAD SWITCH
 089_PW_CHARGER
 090_PW_PROTECTION
 091_PW_+NVVDD
 092_PW_+PEX_VDD
 093_PW_+FBVDDQ
 099_PW_FLOW CHART

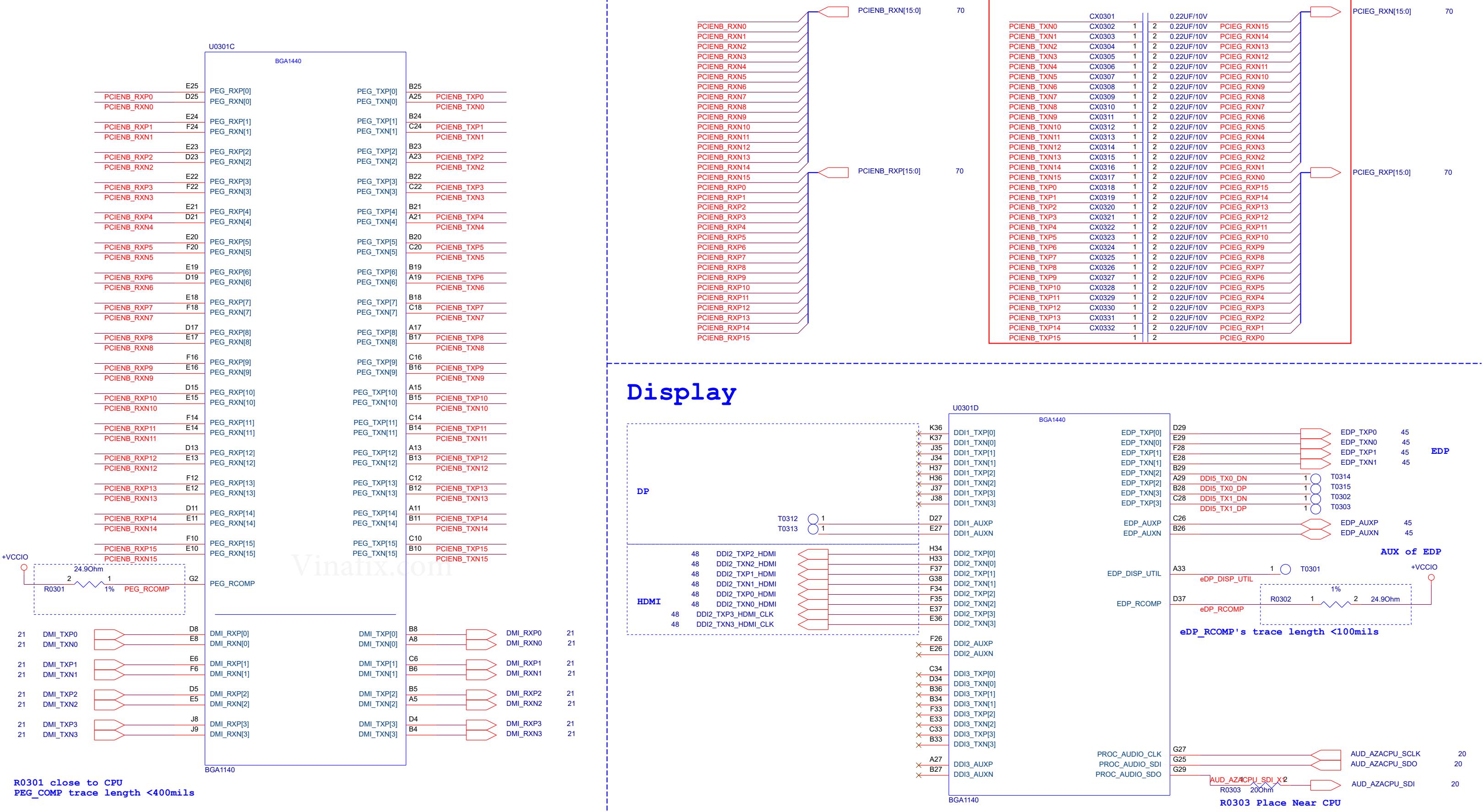
Asus GL552VW Block Diagram

Skylake Platform



Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power	
GPP_A0	RCIN#	Native	RC_IN#	PU 10K	+3VS	
GPP_A1	LAD0	Native	LPC_ADO			
GPP_A2	LAD1	Native	LPC_ADI			
GPP_A3	LAD2	Native	LPC_ADO2			
GPP_A4	LAD3	Native	LPC_ADO3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ	PU 10K	+3VS	
GPP_A7	PIRQA#	Native	PCI_INTA#	PU 10K	+3VS	
GPP_A8		Native	PM_CLKRUN#	PU 8.2K	+3VS	
GPP_A9	CLKOUT_LPC0	Native	CLK_KBPC1_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEB00_X1			
GPP_A11	PME#	GPO	PCI_PME#			
GPP_A12	GPO	GPO	PCI_GPP_A12			
GPP_A13	SUSMANN#	Native	ME_SusPwDnAck	PU 10K	+3VSUS	
GPP_A14	SUS_STAT#	Native	PCI_SUS_STAT#			
GPP_A15	SUS_ACIR#	Native	PM_SUSACIR#			
GPP_A16	Native/GPI	GPO	GPP_A16			
GPP_A17	GPO	GPO	PCI_GPP_A17			
GPP_A18	GPO	GPO	PCI_GPP_A18			
GPP_A19	GPO	GPO	PCI_GPP_A19			
GPP_A20	GPO	GPO	PCI_GPP_A20			
GPP_A21	GPO	GPO	PCI_GPP_A21			
GPP_A22	GPO	GPO	PCI_GPP_A22			
GPP_A23	GPO	GPO	PCI_GPP_A23			
	Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power
GPP_B0	GPO	GPO	(N.C.)			
GPP_B1	GPO	GPO	(N.C.)			
GPP_B2	GPI	GPO	(N.C.)			
GPP_B3	GPI	GPO	(N.C.)			
GPP_B4	GPI	GPO	(N.C.)			
GPP_B5	Native	CLP_PEGA_REQQ#_X1		PU 10K	+3VSUS	
GPP_B6	Native	CLP_REQQ#		PU 10K	+3VSUS	
GPP_B7	Native	CLP_RQ2#		PU 10K	+3VSUS	
GPP_B8	Native	CLPREQ3_WLAN#_X1		PU 10K	+3VSUS	
GPP_B9	Native	CLPREQ4_GLAN#_X1		PU 10K	+3VSUS	
GPP_B10	Native	CLPREQ5_USB#_X1		PU 10K	+3VSUS	
GPP_B11	GPO	GPO	MPHI_PWRDN	PU 10K	+3VSUS	
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTAS#	Native	PLTAS#			
GPP_B14	Strap	Native	PCI_GPP014	PD		
GPP_B15	GPO	GPO	SDIO_C0#			
GPP_B16	GPO	GPO	SDIO_CLK			
GPP_B17	GPO	GPO	SDIO_MISO			
GPP_B18	GPO	Strap	PCI_GPP018	PD		
GPP_B19	GPO	PCI_GPP019/PF_C0_PCH		PU 10K(8)		
GPP_B20	GPO	PCI_GPP020/NV_GPU_EVENT#		PU 10K(8)	+3VS	
GPP_B21	GPO	PCI_GPP021/NV_GCE_F0_EN		PU 10K(8)	+3VS	
GPP_B22	GPO	Strap	PCI_GPP022	PD		
GPP_B23	GPO	SM1ALERT#		PD	PU 150K	+3VSUS
	Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power
GPP_C0	SMCLK	Native	SM2_CLK	PU 2.2K	+3VSUS	
GPP_C1	SMBDATA	Native	SM2_SDA	PU 2.2K	+3VSUS	
GPP_C2	GPO	Strap	PCI_GPPC2			
GPP_C3	SMDCLK	Native	SM2_CLK	PU 2.2K	+3VSUS	
GPP_C4	SMLODATA	Native	SM2_DAT	PU 2.2K	+3VSUS	
GPP_C5	GPO	Strap	PCI_GPPC5	PD		
GPP_C6	GPI	Native	SM2_CLK	PU 2.2K	+3VSUS	
GPP_C7	GPI	Native	SM2_SAT	PU 2.2K	+3VSUS	
GPP_C8	GPI	Native	SM2_SDQS			
GPP_C9	GPO	PCI_GPPC9				
GPP_C10	GPO	PCI_GPPC10				
GPP_C11	GPO	PCI_GPPC11				
GPP_C12	GPI	DDIMM_SEL0		PD 10K		
GPP_C13	GPI	DDIMM_SEL1		PD 10K		
GPP_C14	GPI	DDIMM_SEL2		PD 10K		
GPP_C15	GPI	Strap	NPC_ID	PU 10K	+3VSUS	
GPP_C16	GPO	ACM_GPLIANED		PU 10K(8)	+3VSUS	
GPP_C17	GPO	PCI_GPPC17		PU 10K(8)	+3VS	
GPP_C18	GPI	Native	I2C1_SDA	PU 4.7K	+3VS	
GPP_C19	GPI	Native	I2C1_SCL	PU 4.7K	+3VS	
GPP_C20	GPI	PCI_GPPC20/DPGPU_PWR0K				
GPP_C21	GPO	PCI_GPPC21/GPU_RST#		PD 10K		
GPP_C22	GPO	PCI_GPPC22/DPGPU_PWR_EN#		PU 10K	+3VS	
GPP_C23	GPI	CPAD INT#		PU 10K	+3VS	
	Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power
GPP_D0	GPO	PCI_PLUG_EVENT				
GPP_D1	GPO	PCI_PME#_FORCE_PWR				
GPP_D2	GPO	EXT_SMI#		PU 10K	+3VS	
GPP_D3	GPI	EXT_SCI#		PU 10K	+3VS	
GPP_D4	GPI	(N.C.)				
GPP_D5	GPO	(N.C.)				
GPP_D6	GPI	(N.C.)				
GPP_D7	GPO	WLAN_GN#		PD 10K(8)		
GPP_D8	GPO	(N.C.)				
GPP_D9	GPO	Strap	PCI_I00			
GPP_D10	GPO	PCI_ISI		PD 10K		
GPP_D11	GPO	PCI_ISI2		PD 10K		
GPP_D12	GPO	Strap	TOUCHPAD_ID			
GPP_D13	GPO	Strap	TOUCH_PANEL_ID			
GPP_D14	GPO	PCI_GPP_D14/WLAN_LED		PD 10K(8)	+3VSUS	
GPP_D15	GPO	PCI_GPP_D15/WLAN_BT_LED				
GPP_D16	GPI	(N.C.)				
GPP_D17	GPI	(N.C.)				
GPP_D18	GPI	(N.C.)				
GPP_D19	GPI	(N.C.)				
GPP_D20	GPO	(N.C.)				
GPP_D21	GPO	LED_Record				
GPP_D22	GPO	(N.C.)				
GPP_D23	GPO	(N.C.)				
GPP_D24	GPO	(N.C.)				
GPP_D25	GPO	(N.C.)				
GPP_D26	GPO	(N.C.)				
GPP_D27	GPO	(N.C.)				
GPP_D28	GPO	(N.C.)				
GPP_D29	GPO	(N.C.)				
GPP_D30	GPO	(N.C.)				
GPP_D31	GPO	(N.C.)				
GPP_D32	GPO	(N.C.)				
GPP_D33	GPO	(N.C.)				
GPP_D34	GPO	(N.C.)				
GPP_D35	GPO	(N.C.)				
GPP_D36	GPO	(N.C.)				
GPP_D37	GPO	(N.C.)				
GPP_D38	GPO	(N.C.)				
GPP_D39	GPO	(N.C.)				
GPP_D40	GPO	(N.C.)				
GPP_D41	GPO	(N.C.)				
GPP_D42	GPO	(N.C.)				
GPP_D43	GPO	(N.C.)				
GPP_D44	GPO	(N.C.)				
GPP_D45	GPO	(N.C.)				
GPP_D46	GPO	(N.C.)				
GPP_D47	GPO	(N.C.)				
GPP_D48	GPO	(N.C.)				
GPP_D49	GPO	(N.C.)				
GPP_D50	GPO	(N.C.)				
GPP_D51	GPO	(N.C.)				
GPP_D52	GPO	(N.C.)				
GPP_D53	GPO	(N.C.)				
GPP_D54	GPO	(N.C.)				
GPP_D55	GPO	(N.C.)				
GPP_D56	GPO	(N.C.)				
GPP_D57	GPO	(N.C.)				
GPP_D58	GPO	(N.C.)				
GPP_D59	GPO	(N.C.)				
GPP_D60	GPO	(N.C.)				
GPP_D61	GPO	(N.C.)				
GPP_D62	GPO	(N.C.)				
GPP_D63	GPO	(N.C.)				
GPP_D64	GPO	(N.C.)				
GPP_D65	GPO	(N.C.)				
GPP_D66	GPO	(N.C.)				
GPP_D67	GPO	(N.C.)				
GPP_D68	GPO	(N.C.)				
GPP_D69	GPO	(N.C.)				
GPP_D70	GPO	(N.C.)				
GPP_D71	GPO	(N.C.)				
GPP_D72	GPO	(N.C.)				
GPP_D73	GPO	(N.C.)				
GPP_D74	GPO	(N.C.)				
GPP_D75	GPO	(N.C.)				
GPP_D76	GPO	(N.C.)				
GPP_D77	GPO	(N.C.)				
GPP_D78	GPO	(N.C.)				
GPP_D79	GPO	(N.C.)				
GPP_D80	GPO	(N.C.)				
GPP_D81	GPO	(N.C.)				
GPP_D82	GPO	(N.C.)				
GPP_D83</						

PCIEG



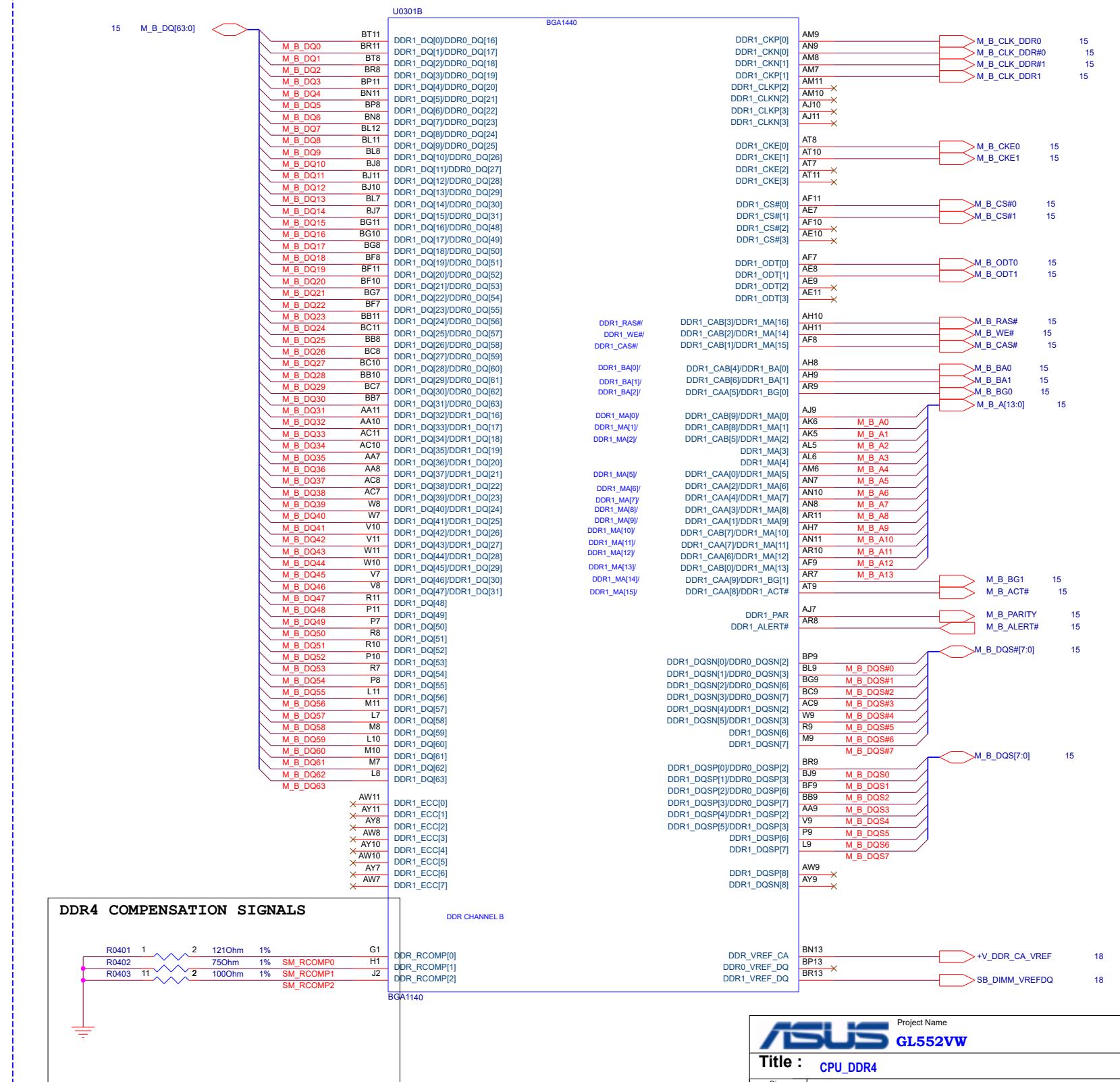
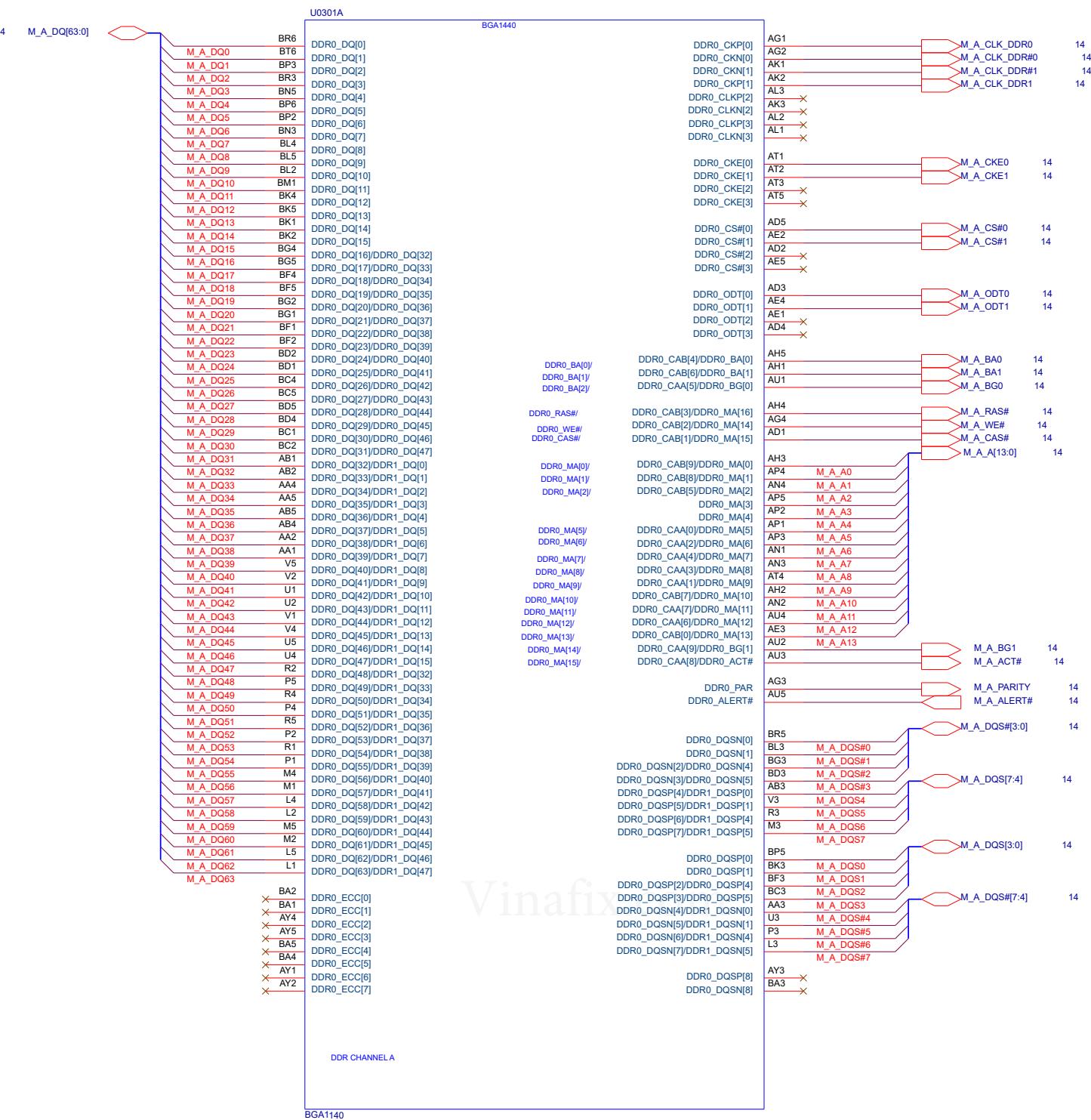
Intel CPU	ASUS P/N	規格
Quad Core (QS)	01001-01150500	I7-6700HQ 2.8G/8M QJJR 45W BGA
Dual Core (QS)	01001-01150400	I5-6300HQ 2.3G/6M QJJQ 45W BGA

Project Name		Rev
ASUS GL552VW		2.0
Title :	CPU_DMI,PEG,FDI,eDP,DDI	
Size B	Dept.:	ASUSTeK COMPUTER INC. Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet	3 of 103

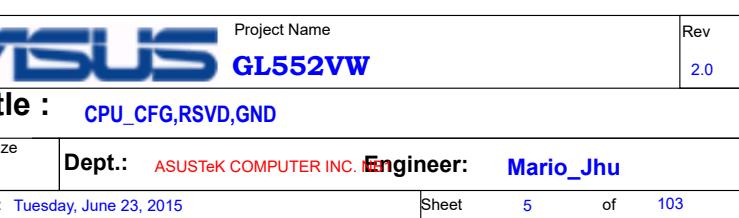
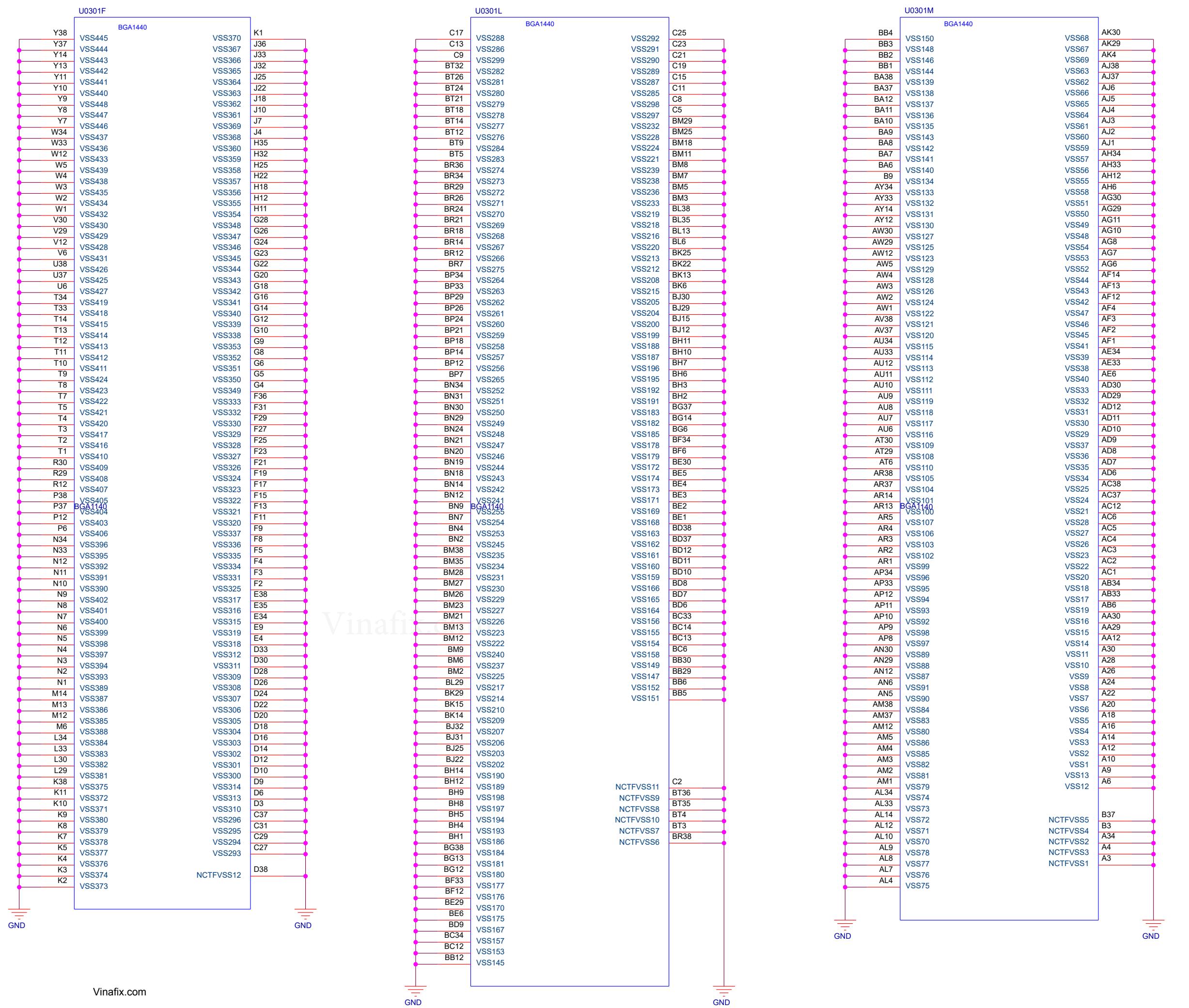
Main Board

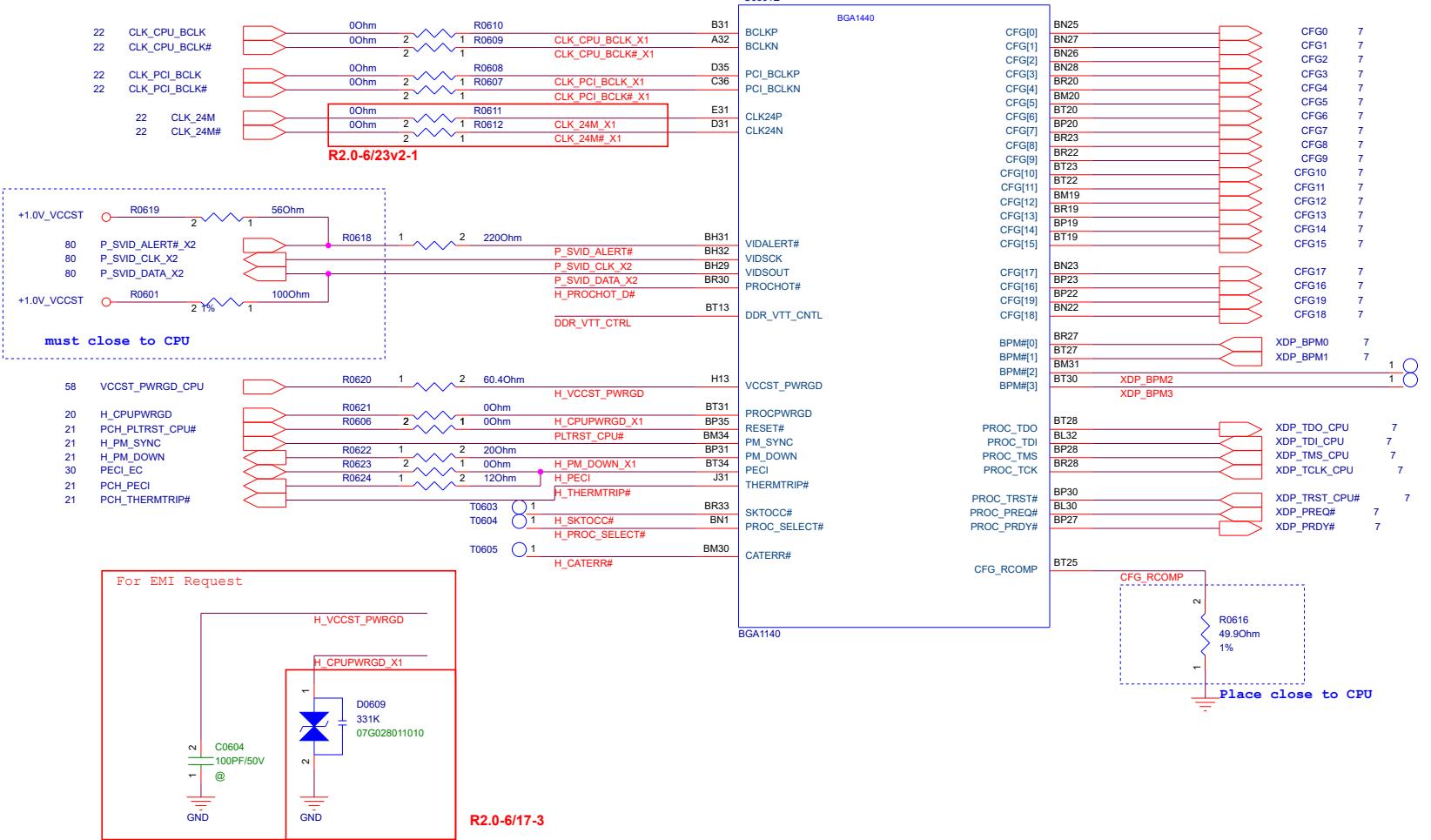
Memory Channel B

Memory Channel A

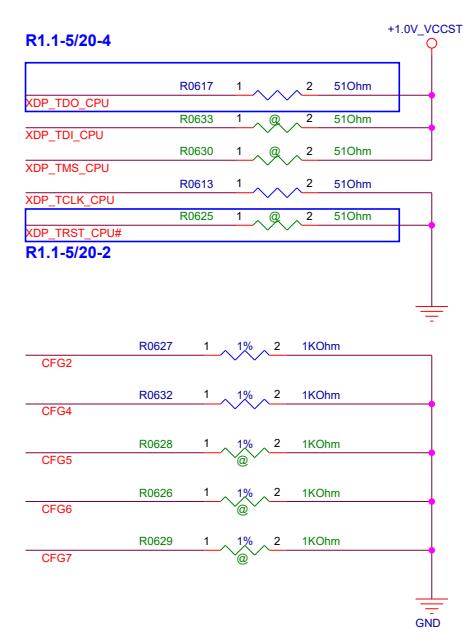


Main Board





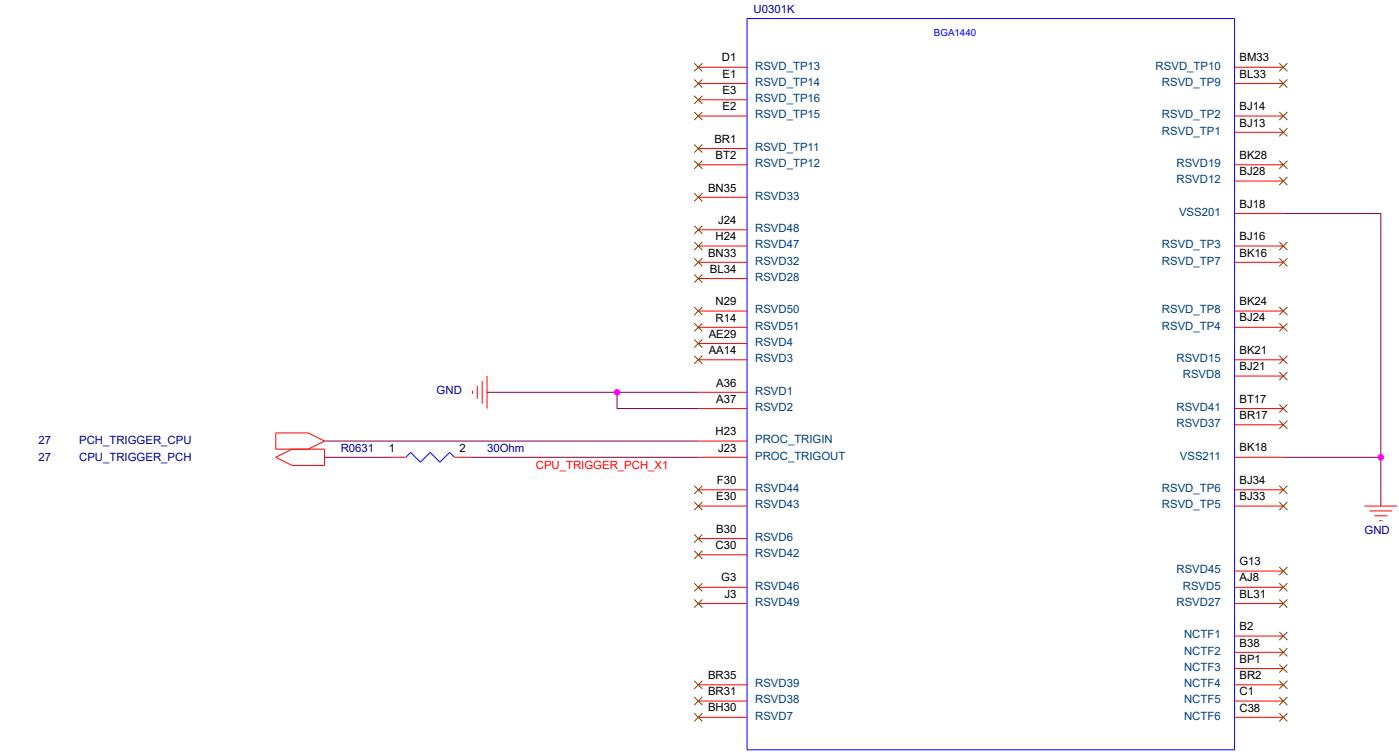
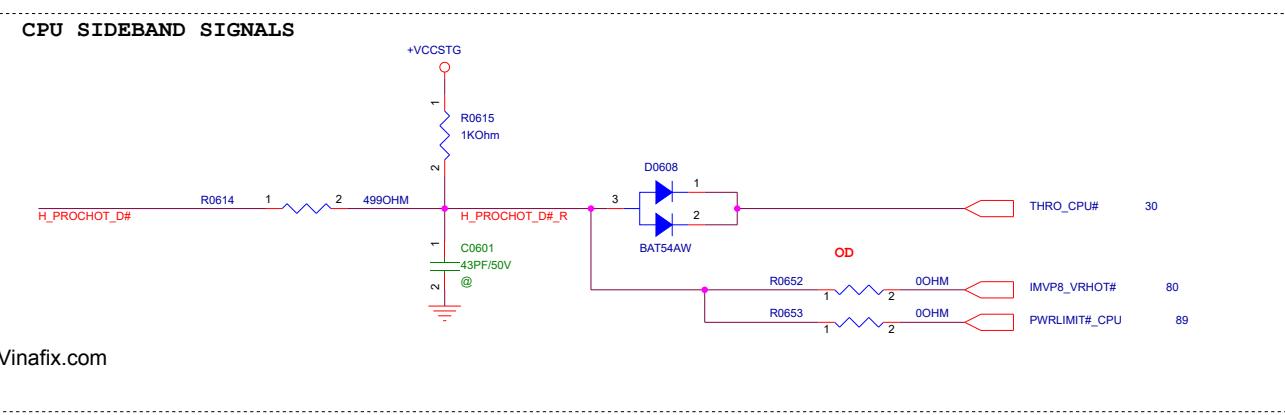
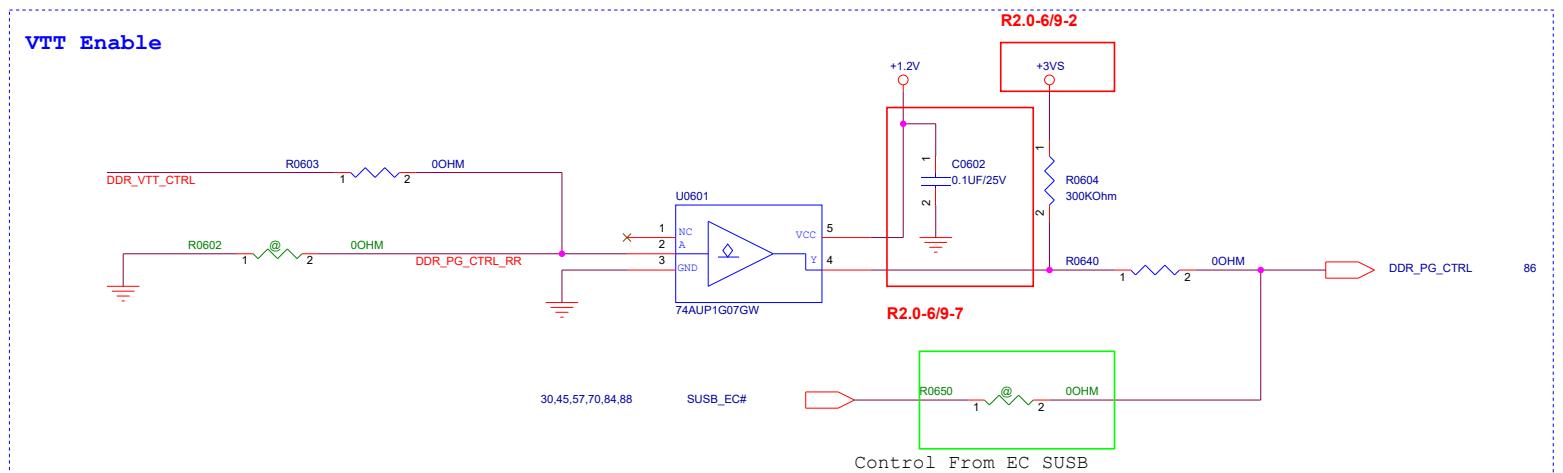
CFG Straps



CFG Straps for Processor	
ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9_P.121	
CFG[0]	: Stall reset sequence after PCU PLL lock until de-asserted - 1 : (Default) Normal Operation; No stall - 0 : Stall
CFG[1] : Reserved Configuration Lane	
	Reserved Configuration Lane
CFG[2] : PCI Express® Static x16 Lane Numbering Reversal	
	- 1 : (Default) Normal Operation - 0 : Lane Numbers Reversed
CFG[3] : Reserved configuration lanes	
	Reserved Configuration Lane
CFG[4] : eDP Enable	
	- 1 : Disabled - 0 : Enabled
CFG[6:5] : PCI Express® Bifurcation	
	- 00 : 1 x8 , 2 x4 PCI Express® - 01 : Reserved - 10 : 2 x8 PCI Express® - 11 : 1 x16 PCI Express®
CFG[7] : PEG Training	
	- 1 : (Default) PEG Train Immediately Following RESET# de-assertion - 0 : PEG Wait for BIOS for Training
CFG[19:8] : Reserved Configuration Lanes	
	Reserved Configuration Lanes

Intel 544924_Skylake_EDS_Vol_1_Rev0.9_P.121
Richard 2014I209

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

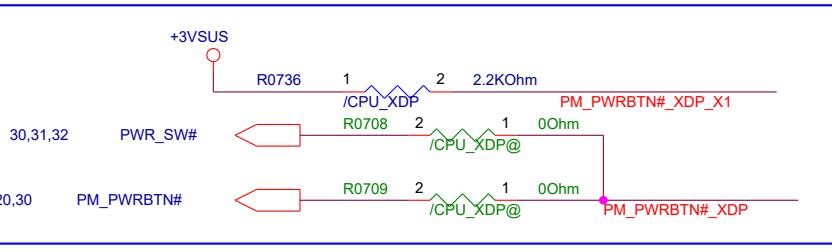


CPU XDP connector

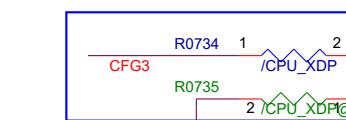
R1.1-4/13-1



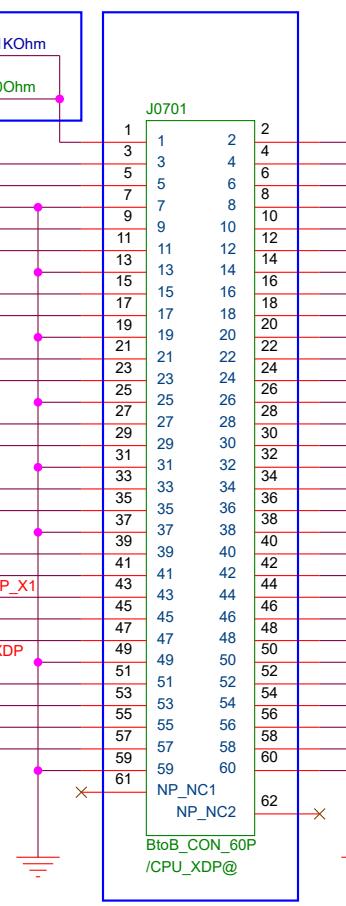
R1.1-5/8-1



R1.1-5/8-1



R1.1-5/12-10



/CPU_XDP

0Ohm

RN0701B

RN0701A

CLK_ITP_BCLK_PCH#

CLK_ITP_BCLK_PCH

22

/CPU_XDP

0Ohm

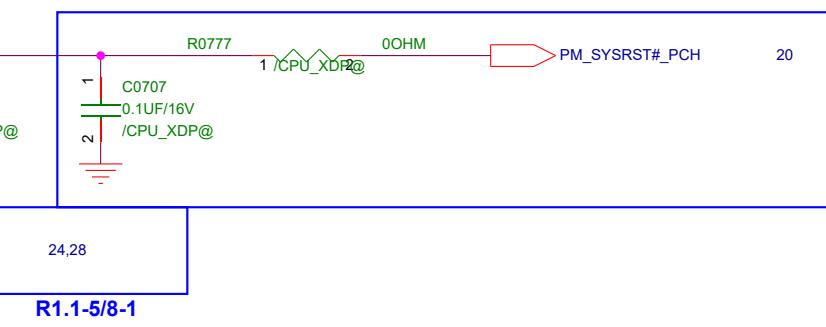
RN0701A

CLK_ITP_BCLK_PCH#

CLK_ITP_BCLK_PCH

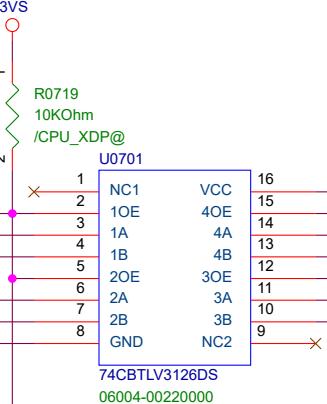
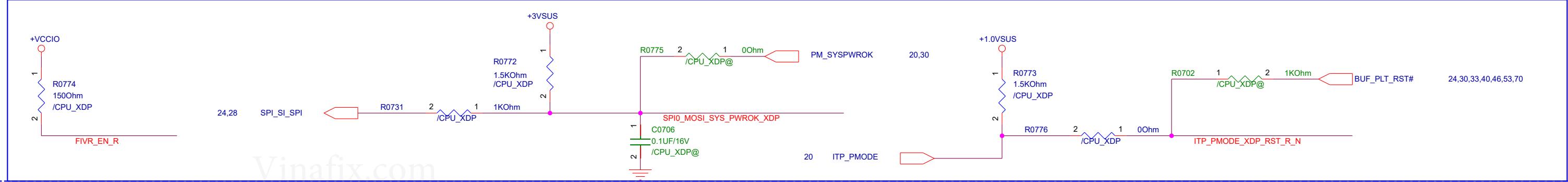
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R1.1-5/20-2 & 3



R1.1-5/8-1

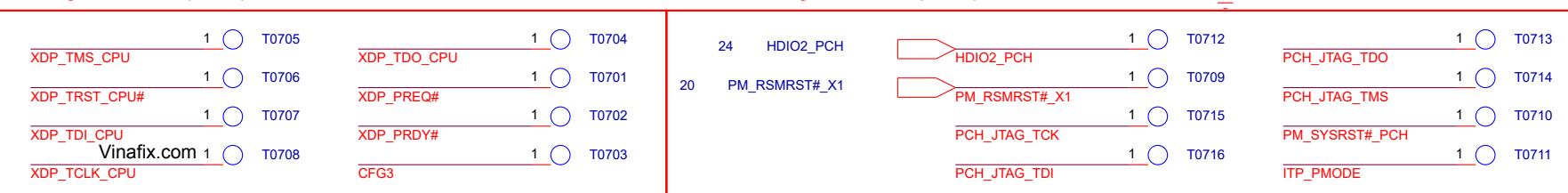
R1.1-5/8-1



Boundary Scan TP (CPU)

R1.1-5/11-10

Boundary Scan TP (PCH)



BOM



Title : CPU_XDP

Engineer: Mario_Jhu

ASUSTeK COMPUTER INC. NB1

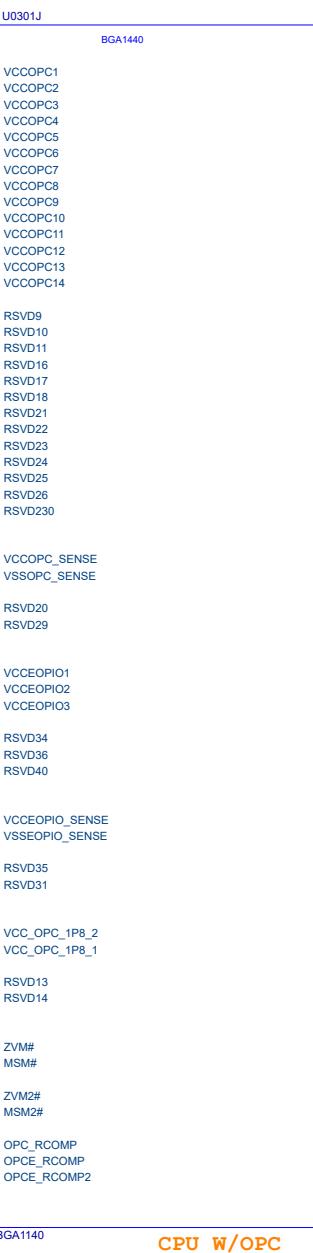
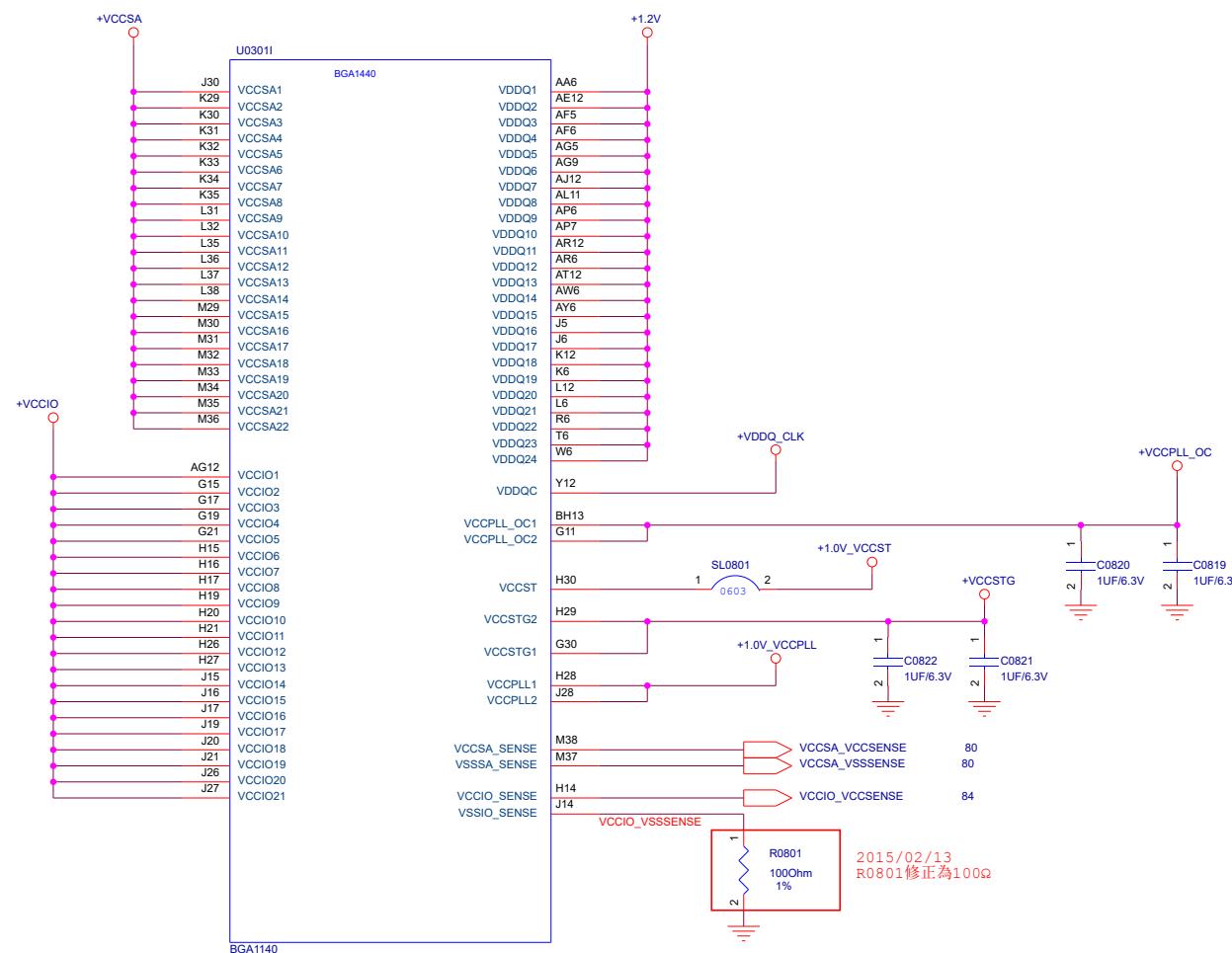
Size Project Name

B

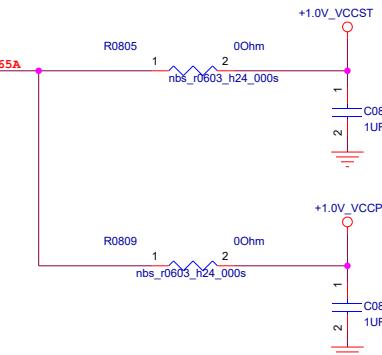
Rev 2.0

GL552VW

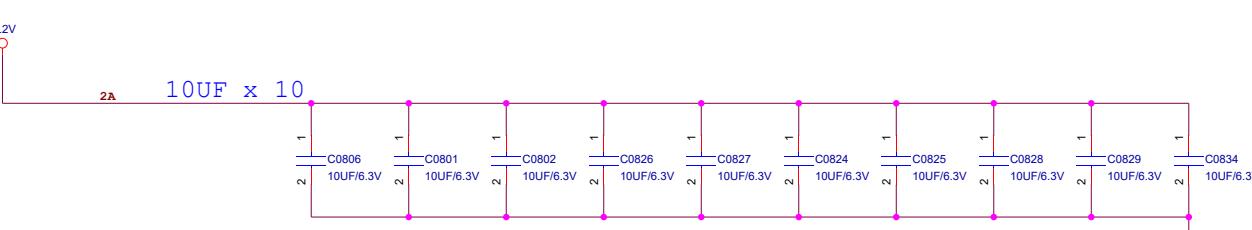
OPC Power Rails



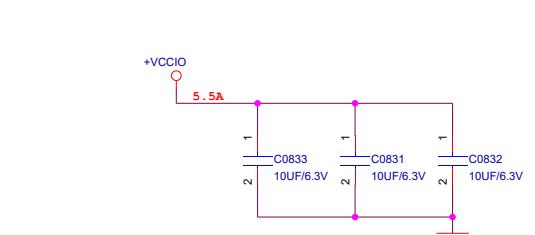
Vinafix.com

+1.0V_VCCST/+1.0V_VCCPLL
DECAPS Place Back Side (TOP)

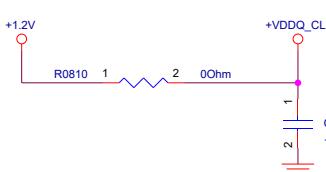
+VDDQ DECAPS Place Back Side (TOP)



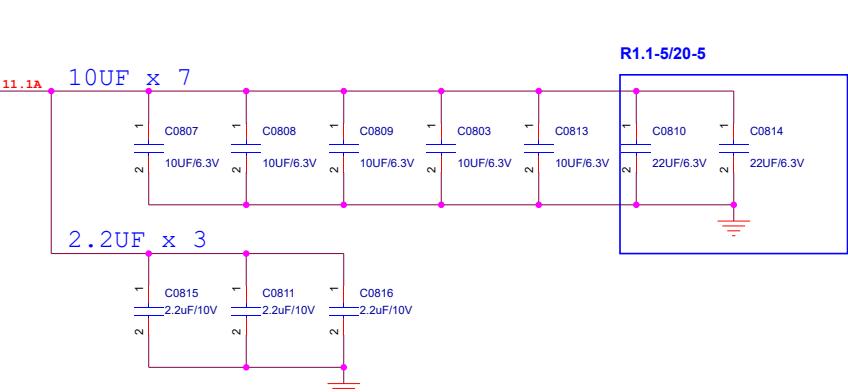
+VCCIO DECAPS Place Back Side (TOP)



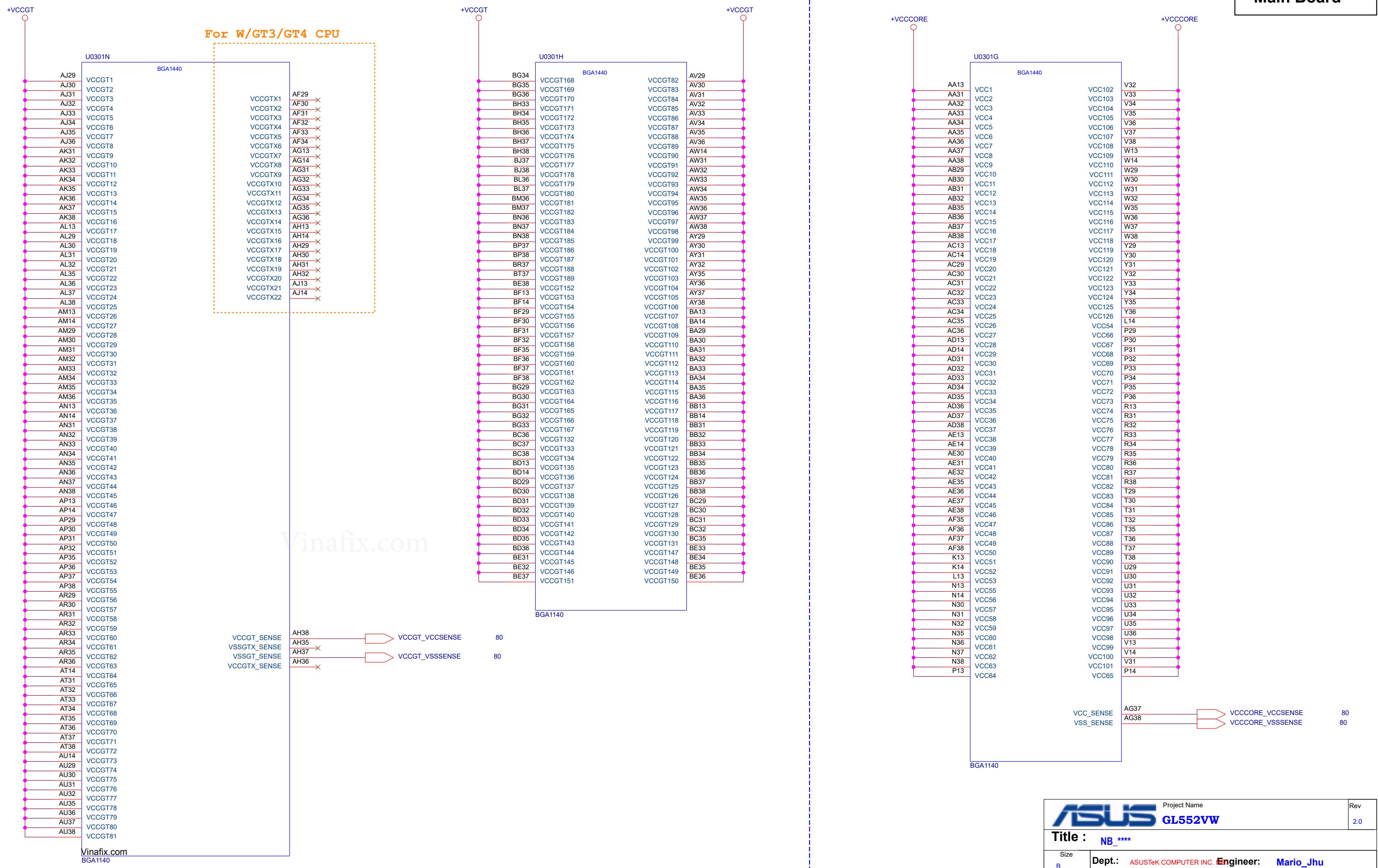
+VDDQ_CLK DECAPS Place Back Side (TOP)



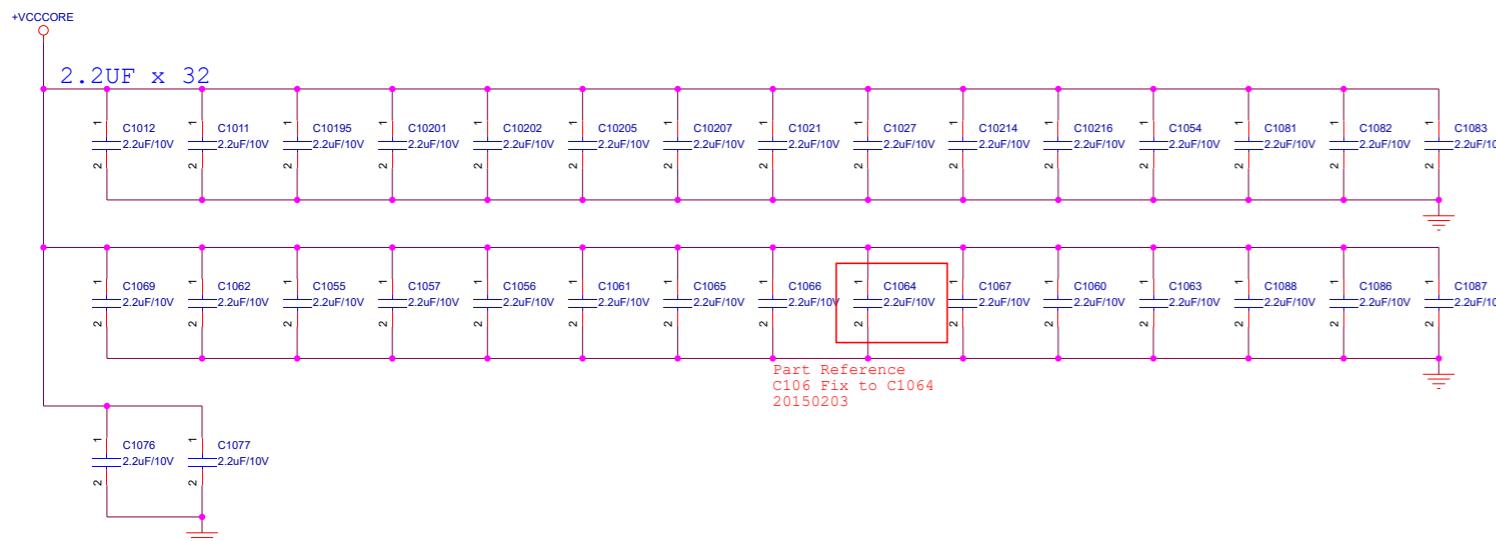
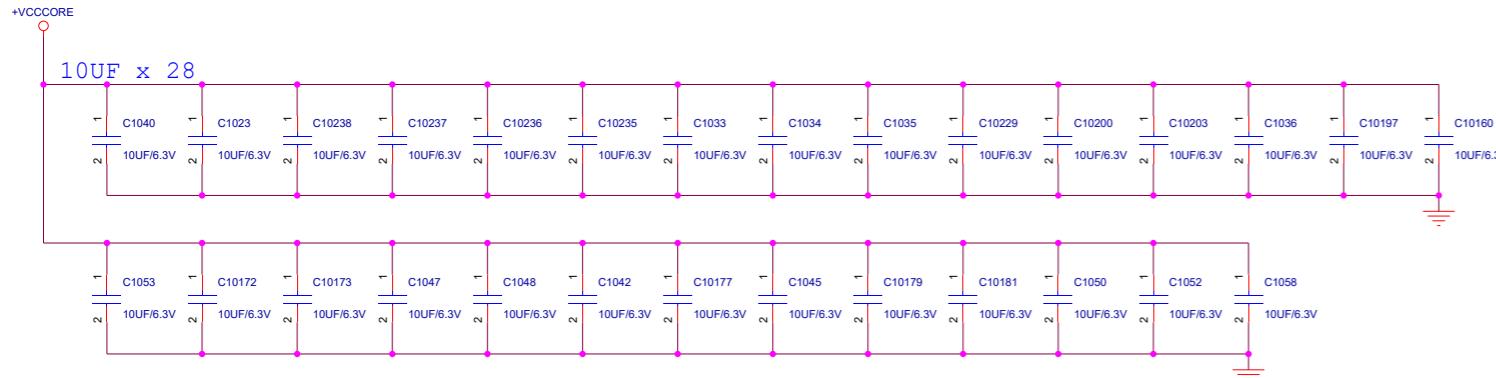
+VCCSA DECAPS Place Back Side (TOP)



Vinafix.com

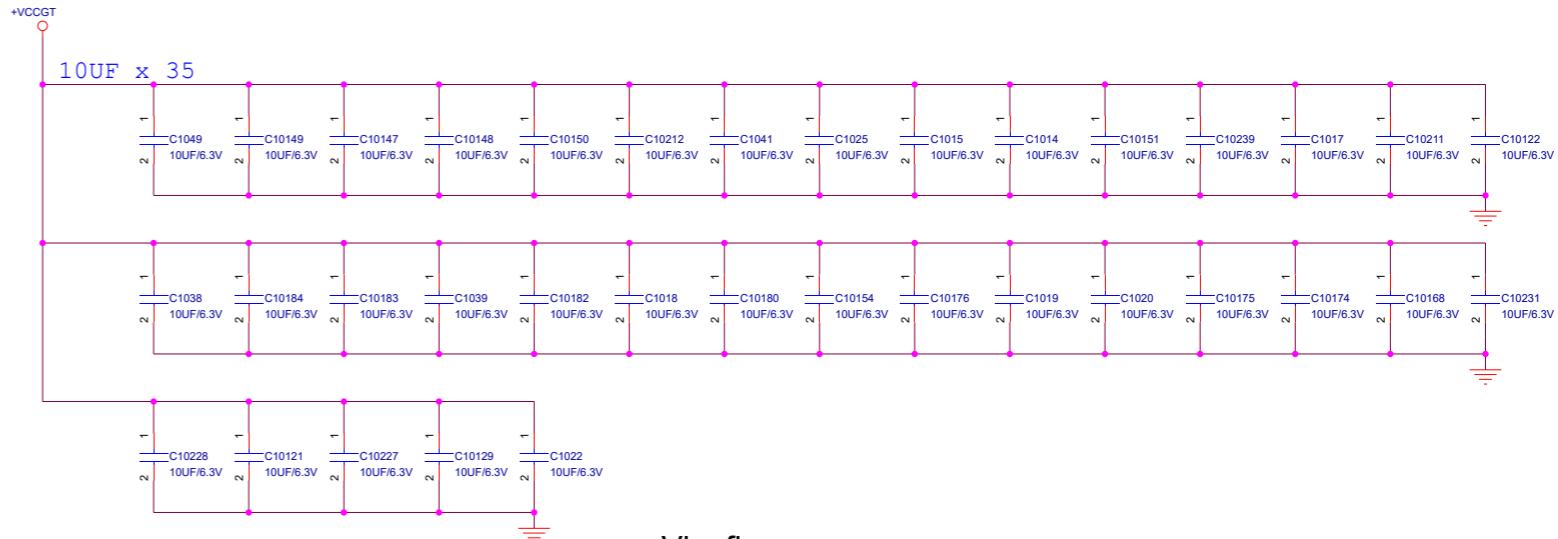


+VCCCORE DECAPS Place Back Side (TOP)

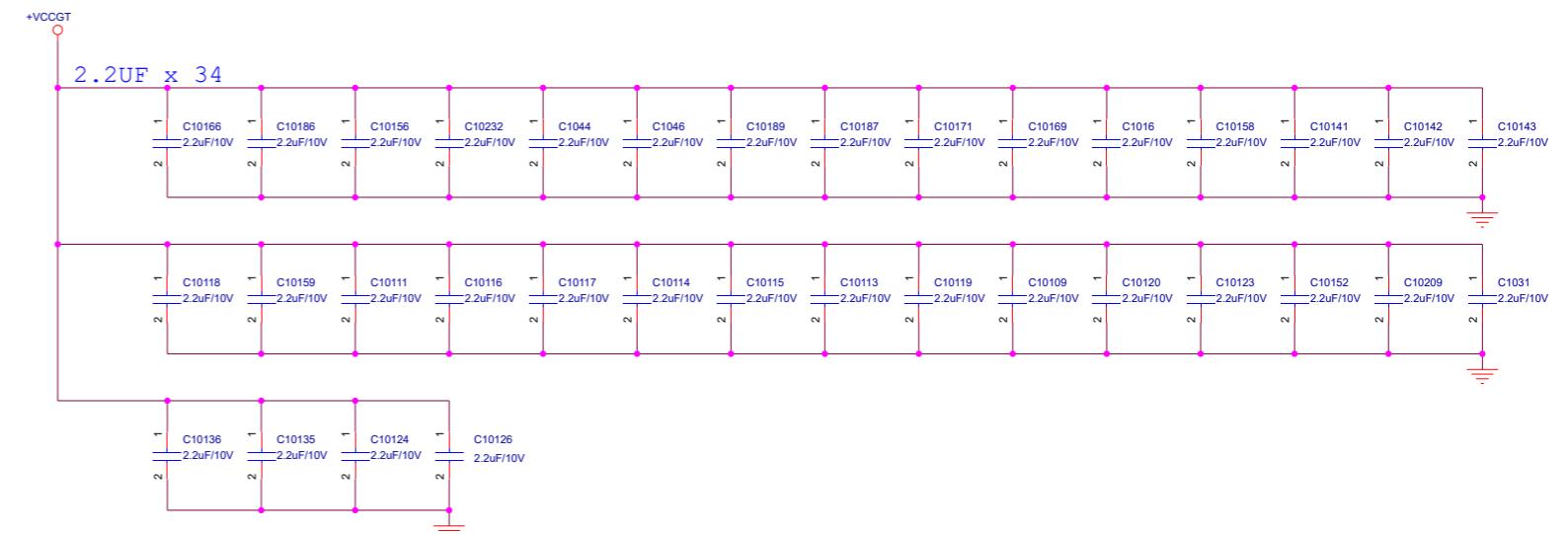


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+VCCGT DECAPS Place Back Side (TOP)



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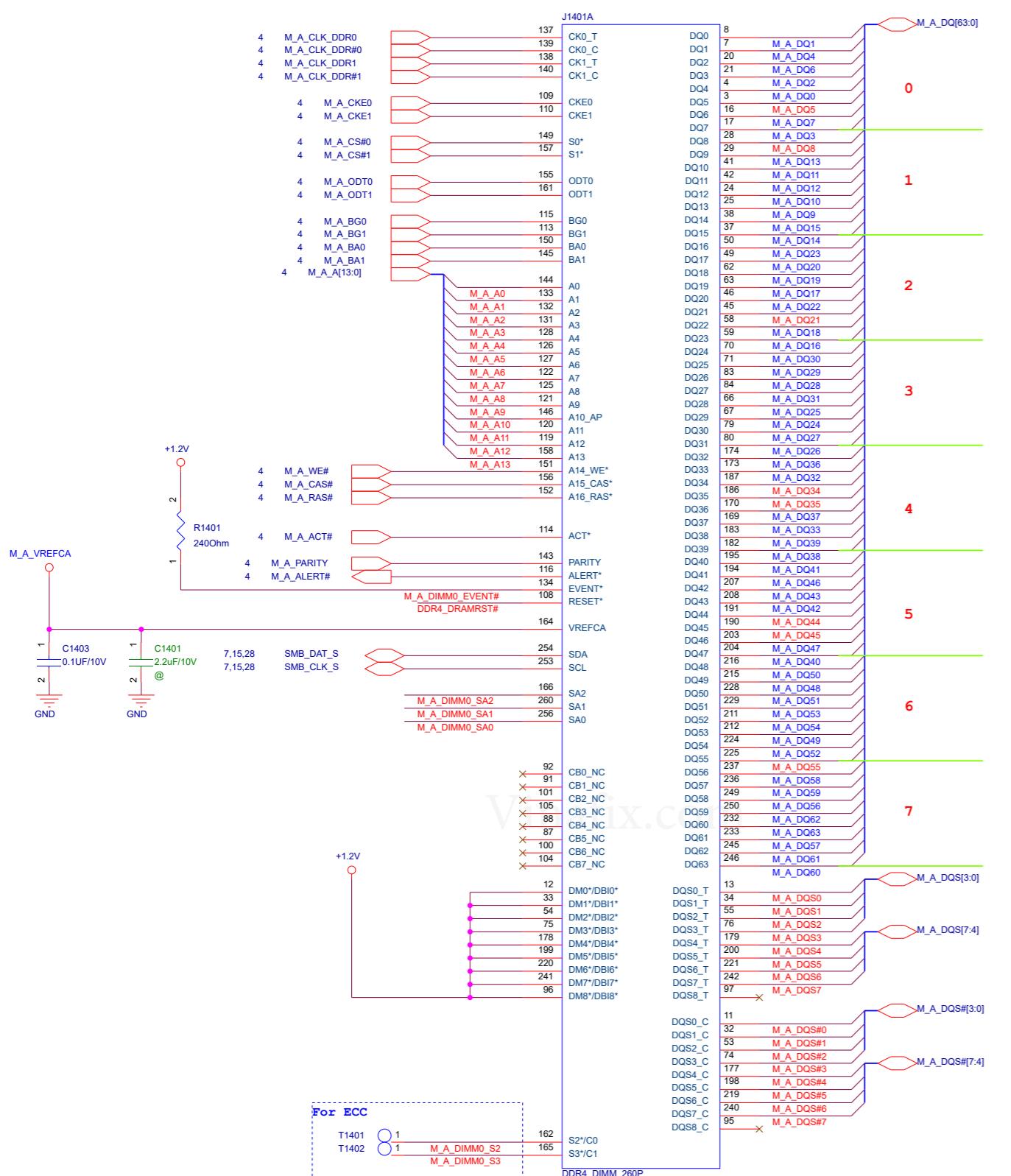


Vinafix.com

SODIMM CHA-DIMM0

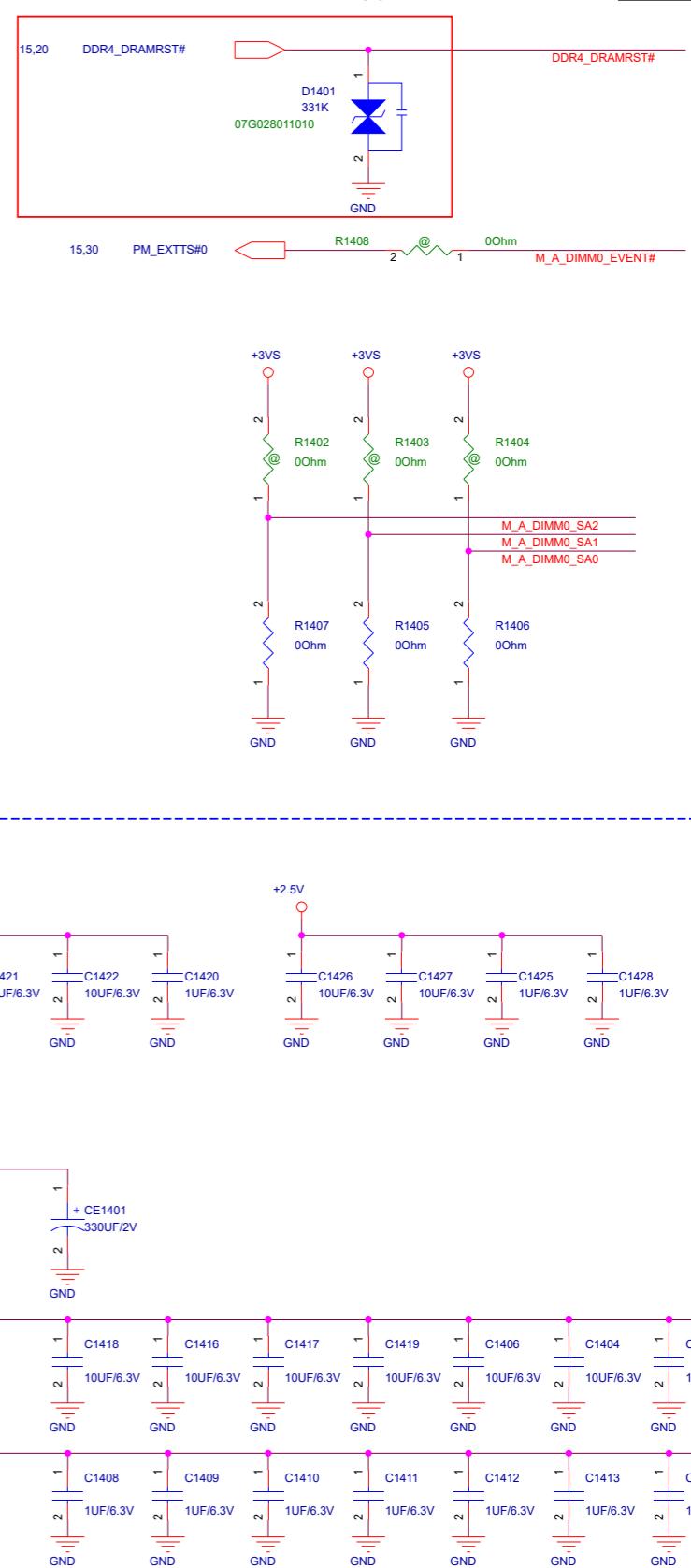
TOP H4.0mm REV (J1401)

12002-00080600
DDR4 DIMM 260P 4H REV



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

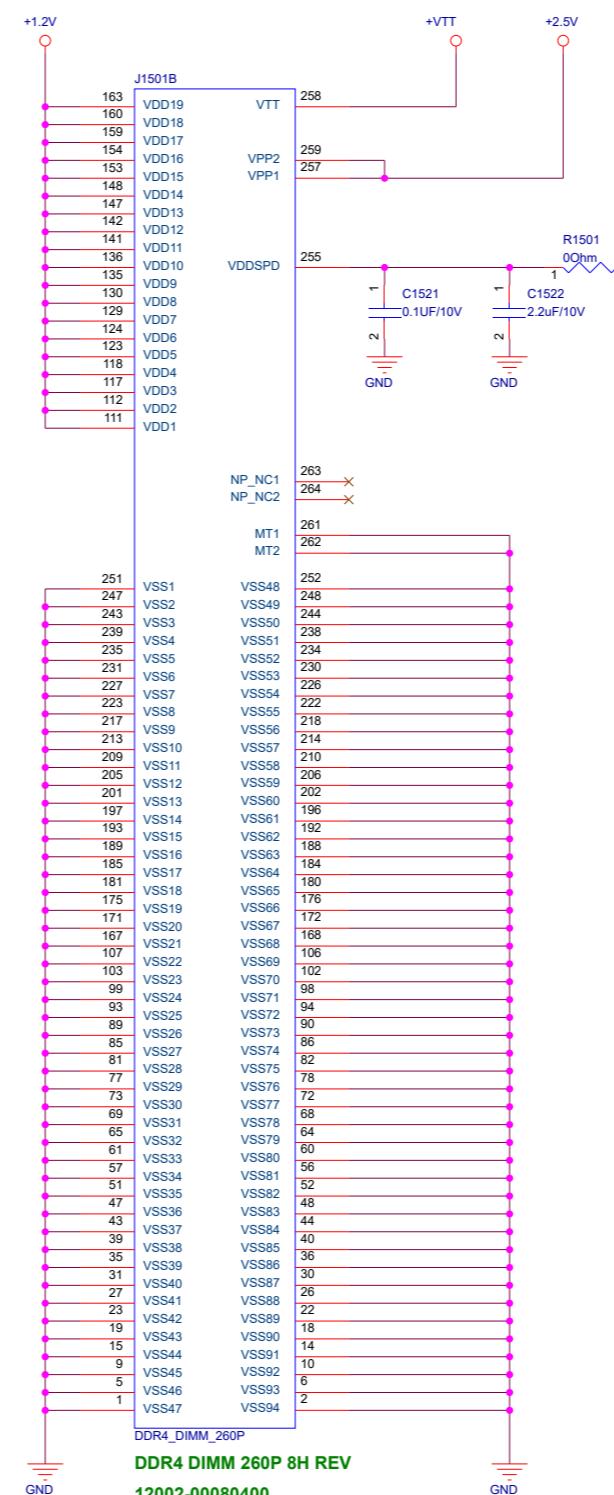
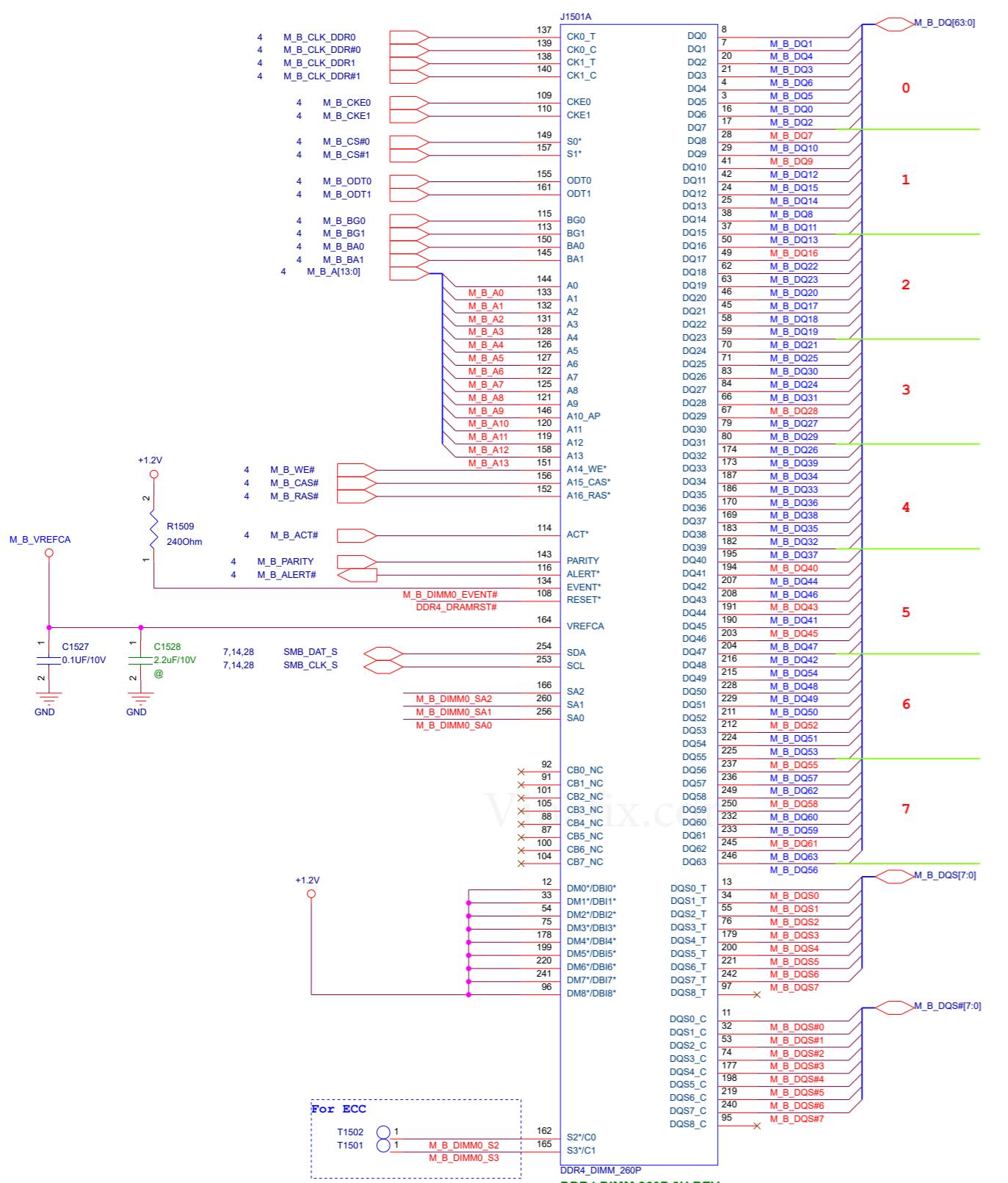
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



SODIMM CHB-DIMM0

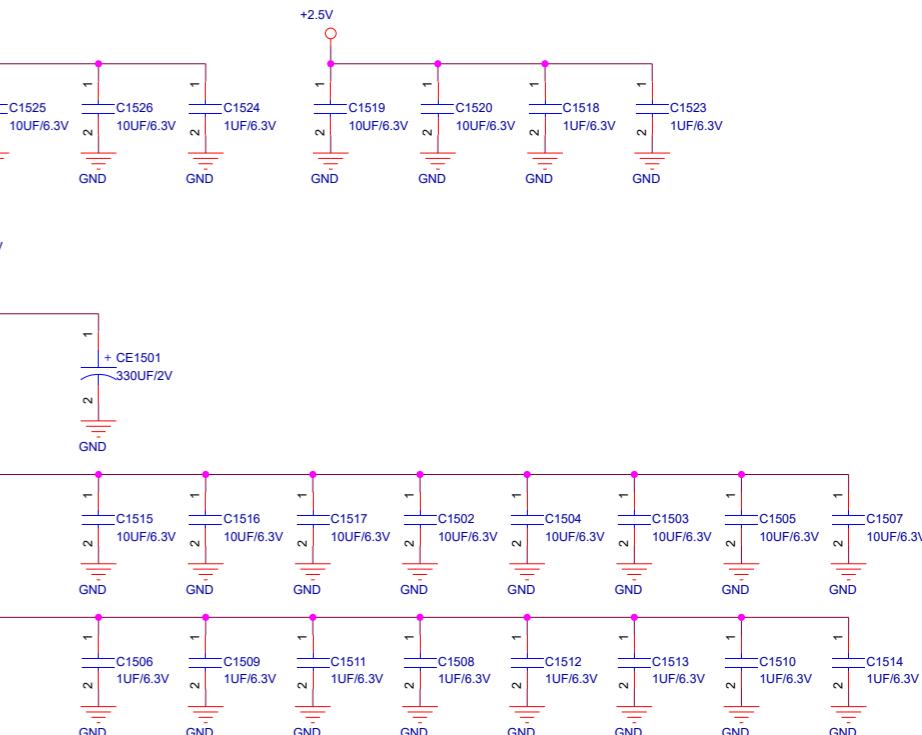
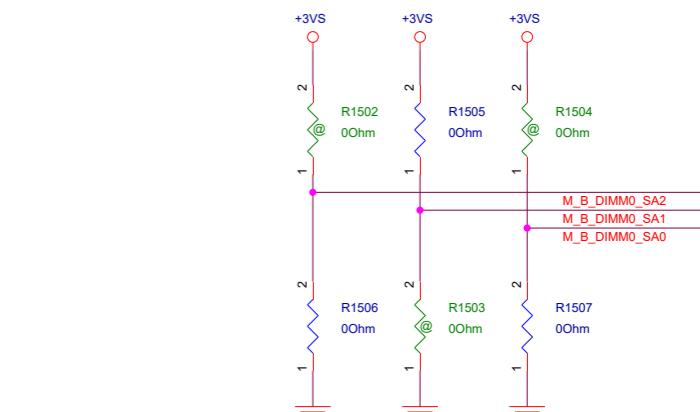
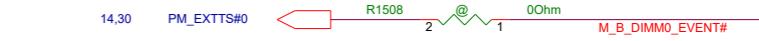
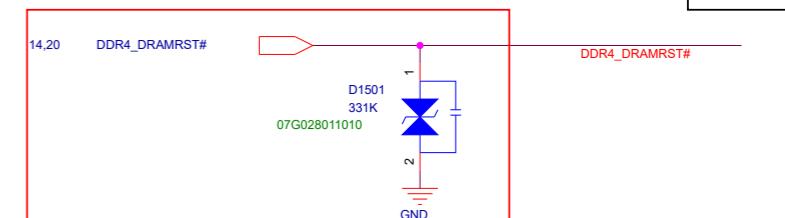
TOP H8.0mm REV (J1501)

12002-00080400
DDR4 DIMM 260P 8H REV

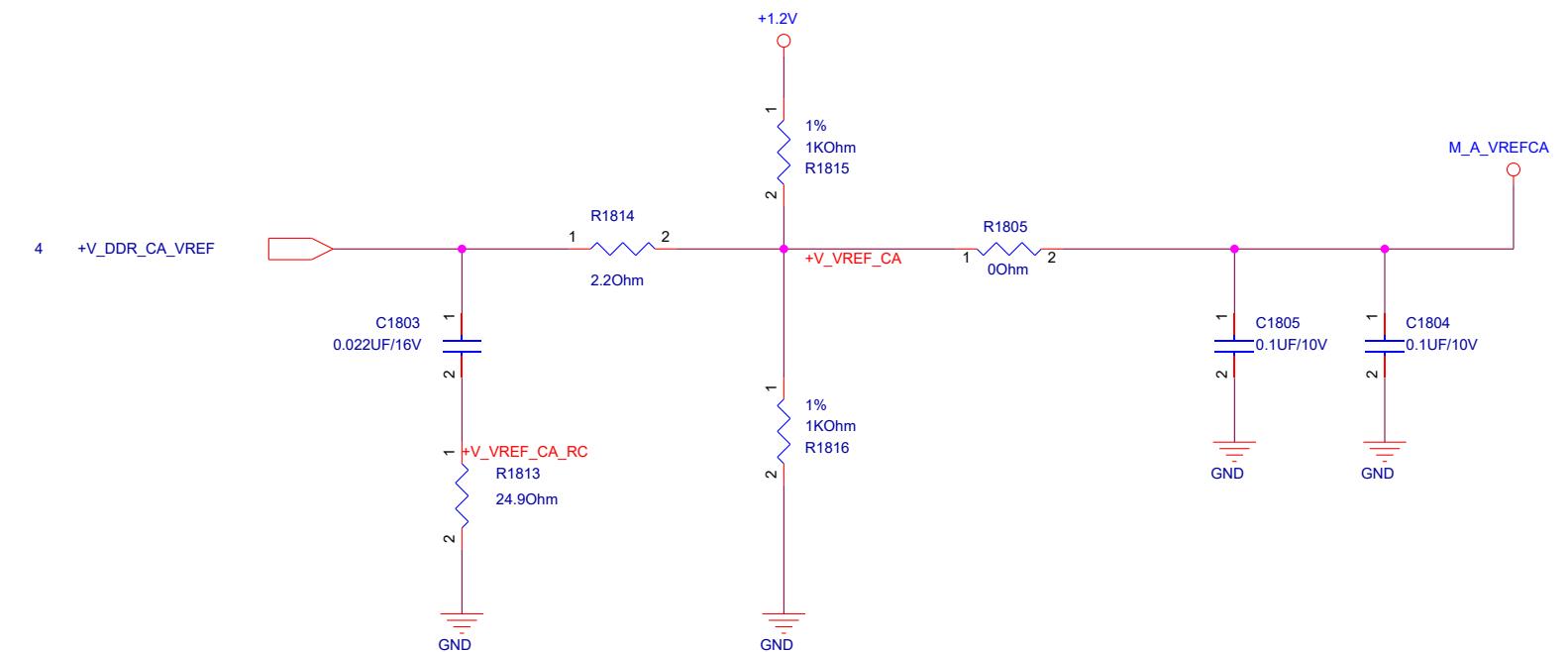


SO-DIMMs that do not support ECC (x64 only)
will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a
combined SPD/Thermal Sensor with EVENT#
wired.

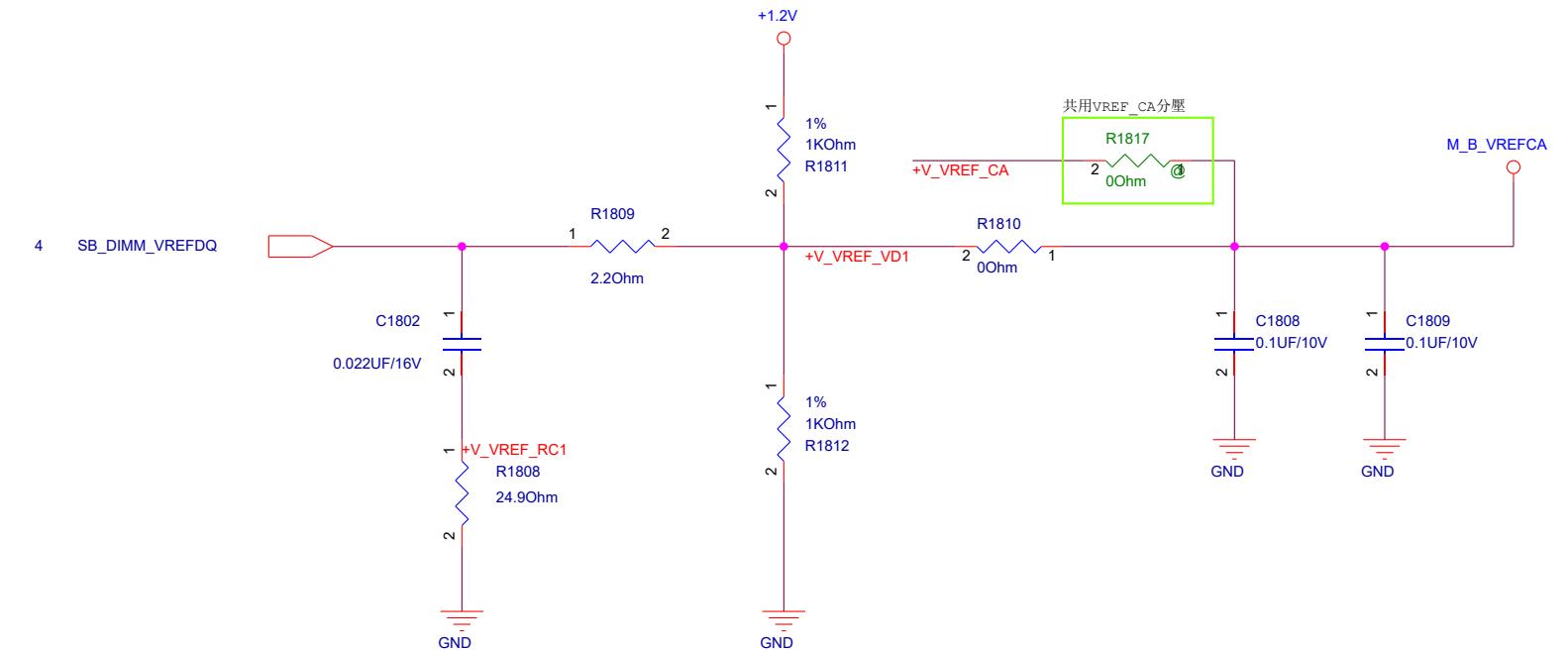
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



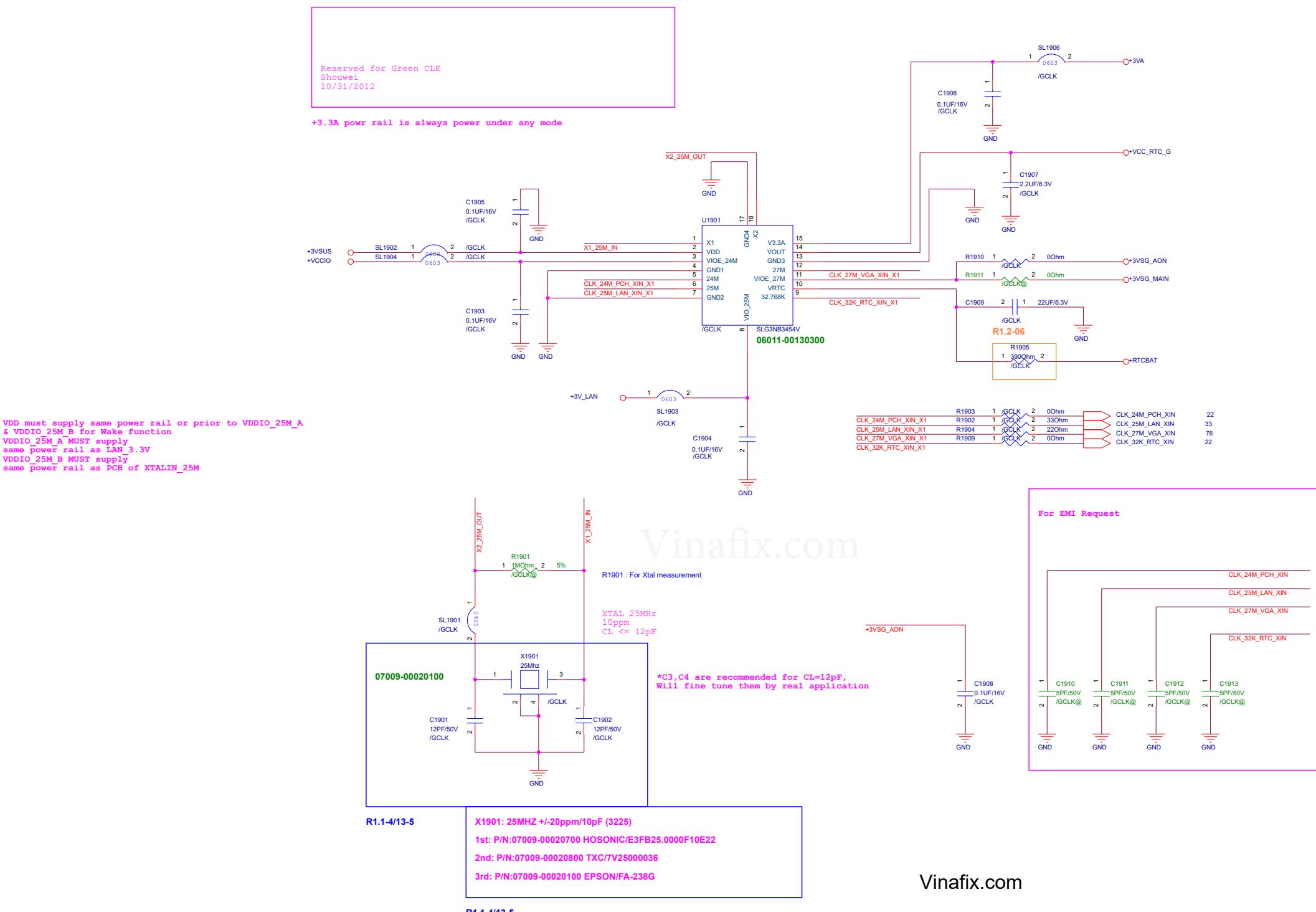
SO-DIMM0 Vref



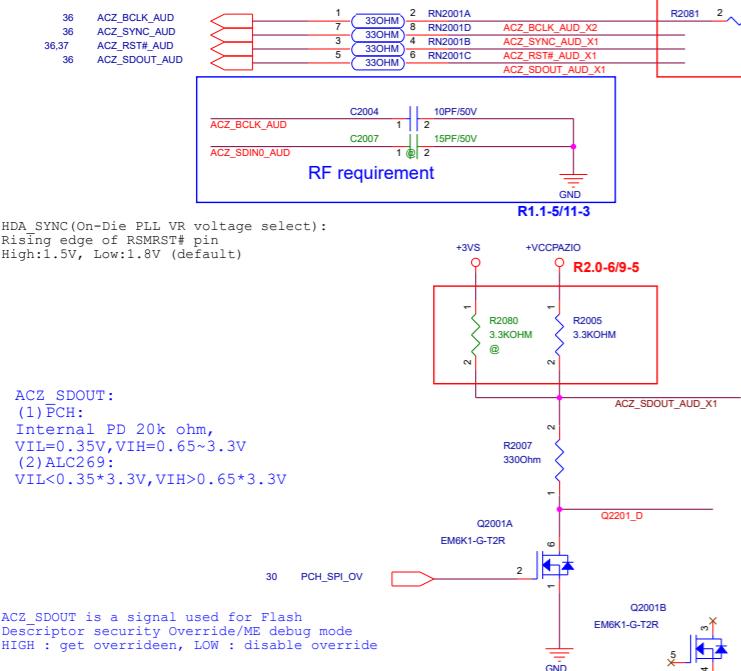
SO-DIMM1 Vref



Silego Green CLK



HD Audio



R2.0-6/23-2

R2.081

1

0Ohm

ACZ_BCLK_AUD_X1

R2081A

2

330ohm

RN2001A

1

ACZ_BCLK_AUD_X2

RN2001D

2

ACZ_SYNC_AUD_X1

RN2001B

3

ACZ_RST#_AUD_X1

RN2001C

4

ACZ_SDOUT_AUD_X1

RN2001

5

ACZ_SDOUT_AUD_X1

RN2001

6

ACZ_SDOUT_AUD_X1

RN2001

7

330ohm

ACZ_BCLK_AUD

C2004

1

10PF/50V

ACZ_SDIN0_AUD

C2007

1

15PF/50V

GND

RF requirement

R1.1-5/11-3

R2.0-6/9-5

R2080

3.3KOHM

@

R2005

3.3KOHM

ACZ_SDIN0_AUD

R2007

330ohm

ACZ_SDOUT_AUD_X1

Q2001A

1

EM6K1-G-T2R

Q2001_D

2

EM6K1-G-T2R

Q2001B

1

EM6K1-G-T2R

Q2001

30

PCH_SPI_OV

1

GND

X

X

X

X

X

X

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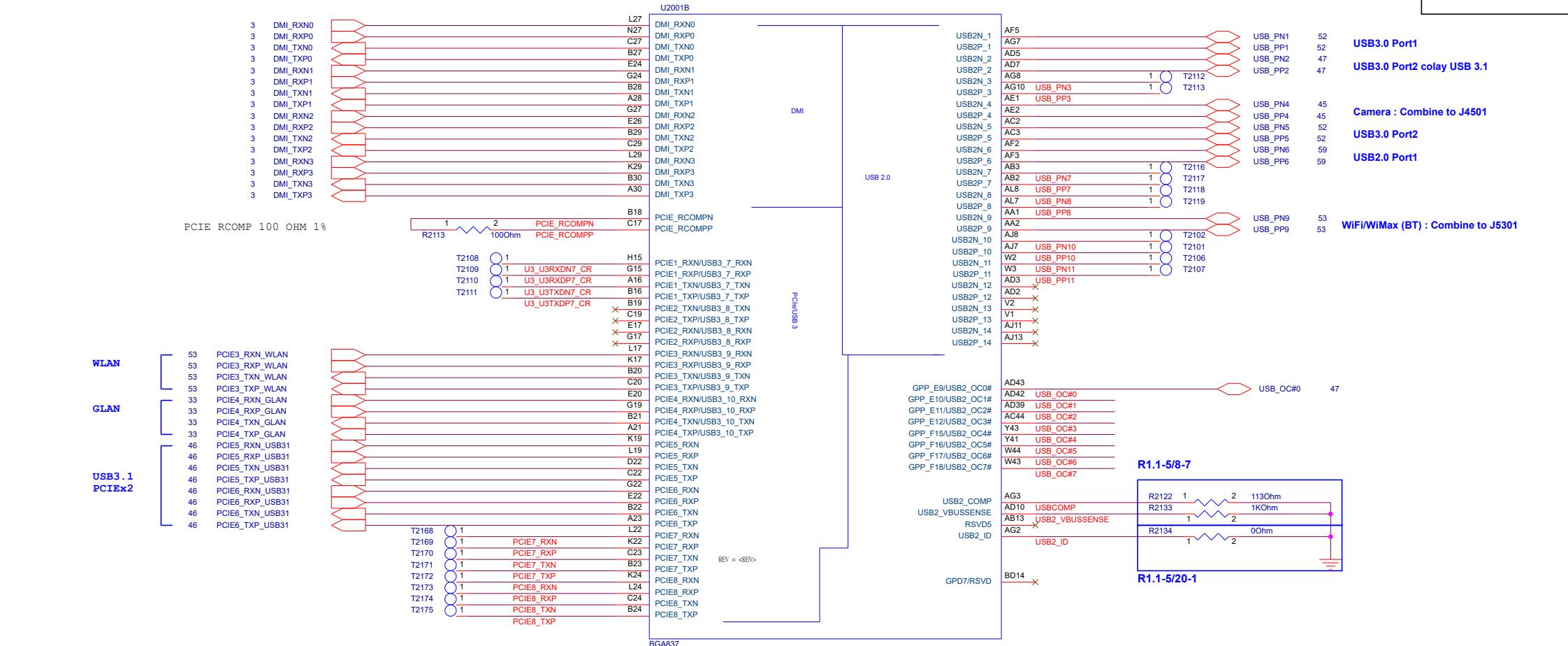
X

X

PCIE Setting

GL552VW PCIE Function define
Skylake HM170

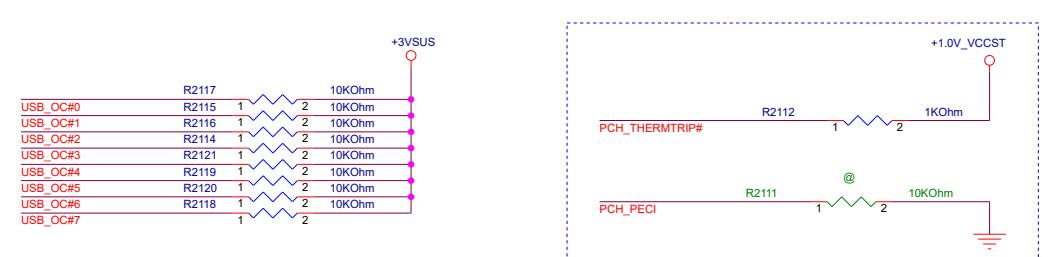
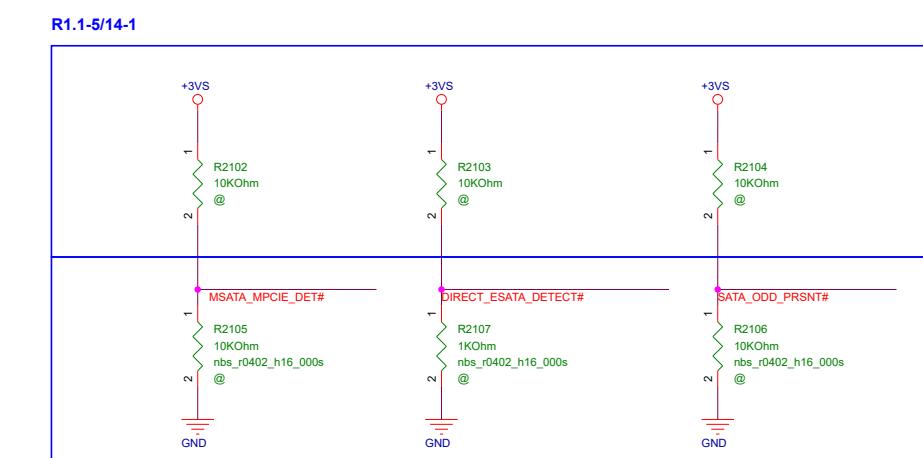
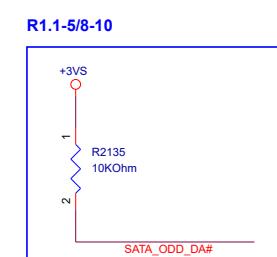
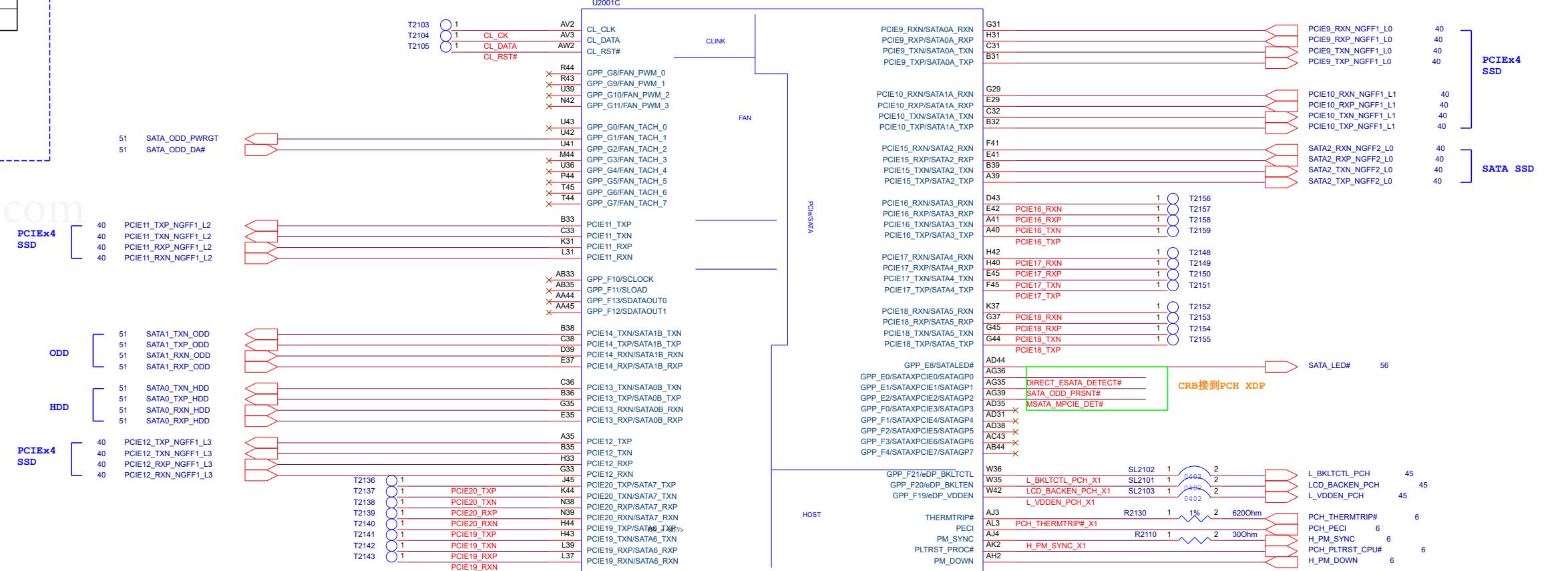
HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01	USB3.0 IO colay USB3.1	
03	USB3#03 / SSIC#02	USB3.0 IO colay USB3.1	
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06		
07	USB3#07 / PCIE#01		
08	USB3#08 / PCIE#02		
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN & CardReader	SRC4
11	PCIE#05 / GBE		SRC5
12	PCIE#06	USB 3.1	
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE		
16	PCIE#10 / SATA#1		
17	PCIE#11	PCIE*4 SSD	SRC6
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE	1st HDD	
20	PCIE#14 / SATA#1	ODD	
21	PCIE#15 / SATA#2	SATA SSD	
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

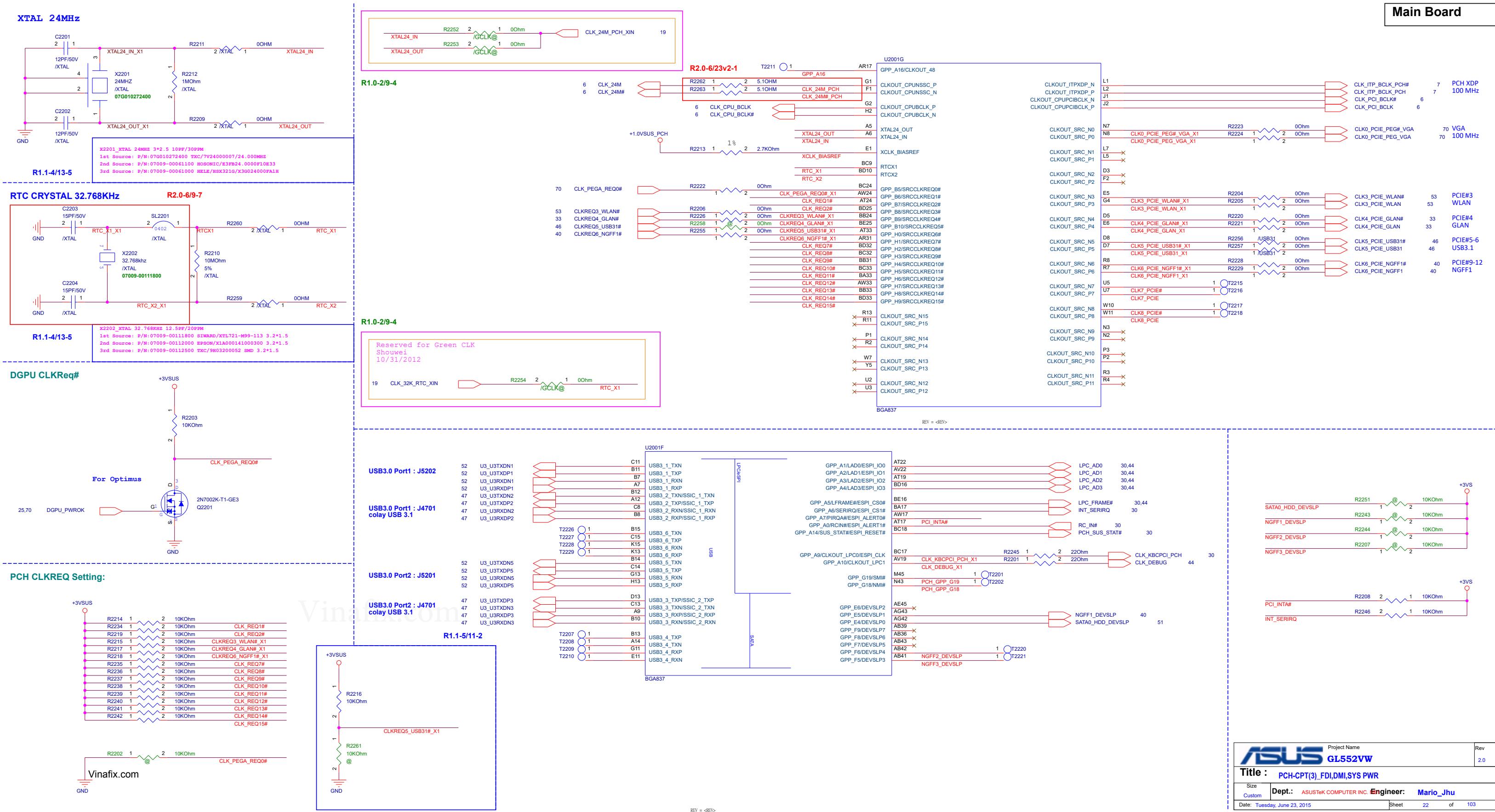


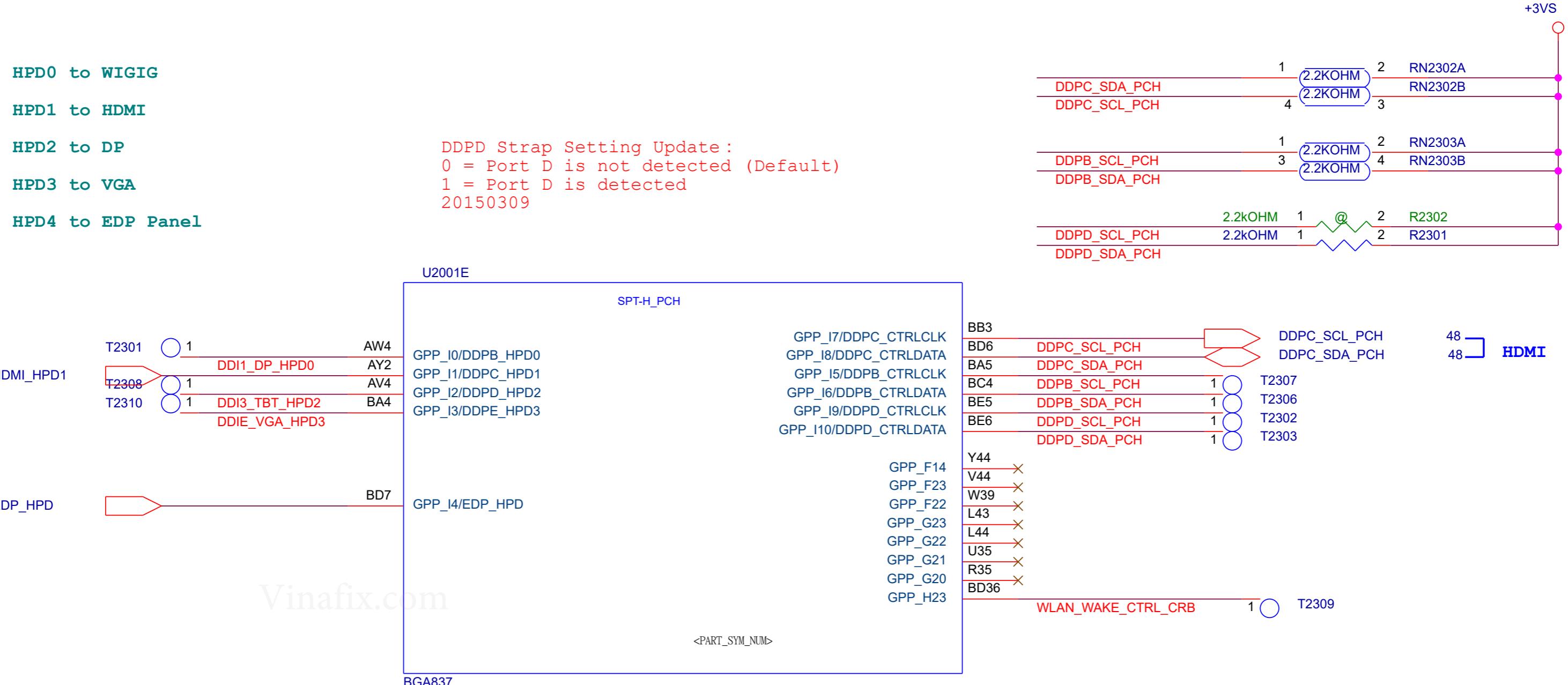
USB Setting

GL552VW USB Function define
Skylake HM170

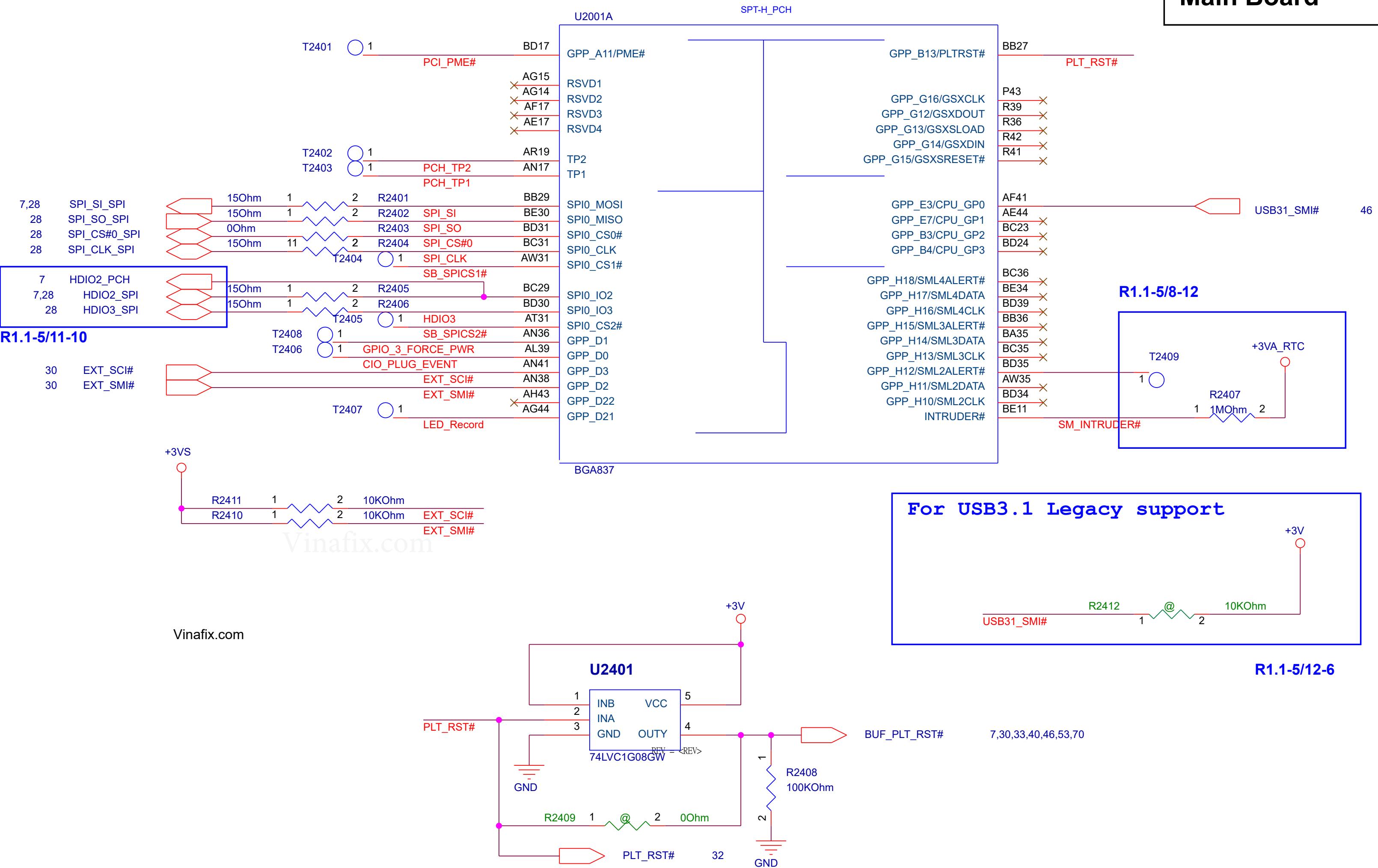
USB 2.0	Function	USB 3.0	Function
USB2_01	USB3.0 IO	USB3_01	USB3.0 IO
USB2_02	USB3.0 IO colay USB3.1	USB3_02	USB3.0 IO colay USB3.1
USB2_03		USB3_03	USB3.0 IO colay USB3.1
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 IO	USB3_05	USB3.0 IO
USB2_06	USB2.0 IO	USB3_06	
USB2_07		USB3_07	
USB2_08		USB3_08	
USB2_09	BT/WLAN		
USB2_10			
USB2_11			
USB2_12			







Main Board

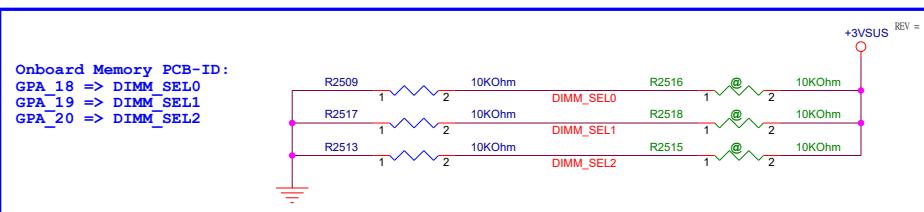
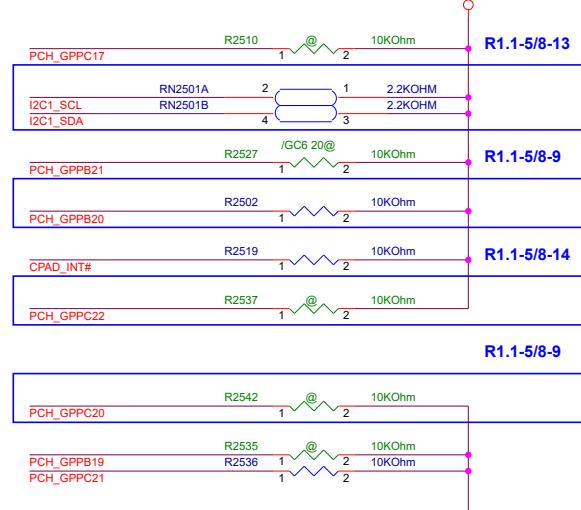
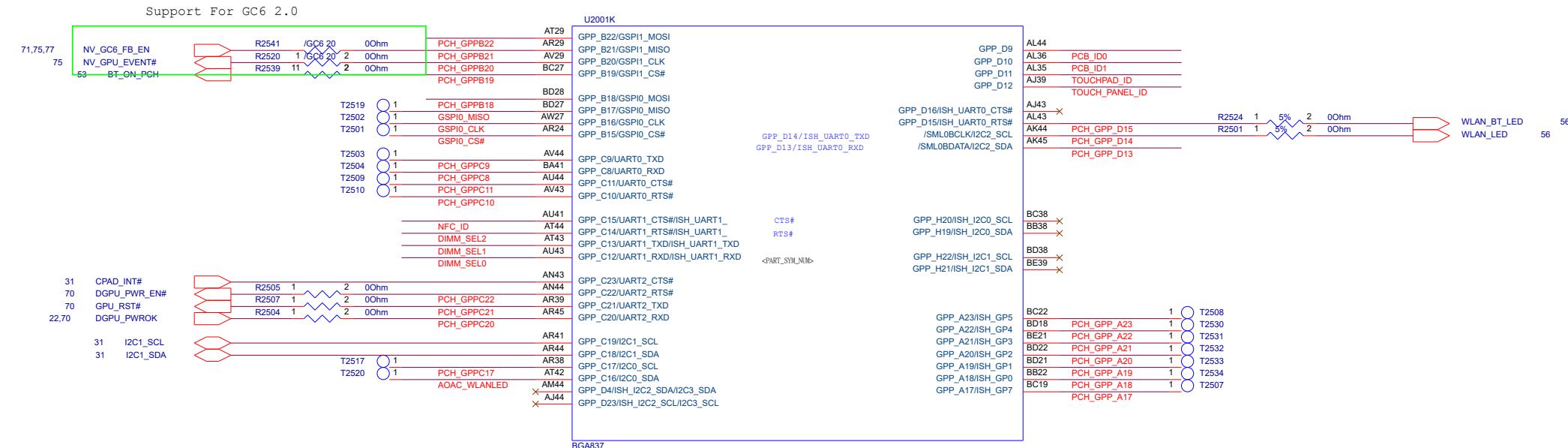


For USB3.1 Legacy support



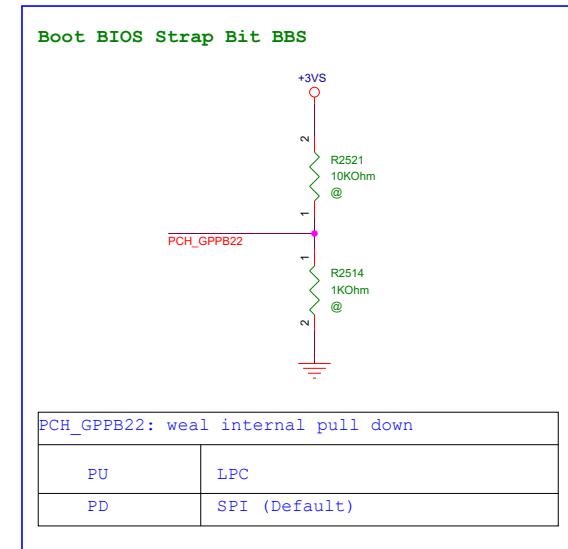
R1.1-5/12-6

ASUS	Project Name GL552VW	Rev 2.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size A	Dept.: ASUSTeK COMPUTER INC. ME	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet	24 of 103



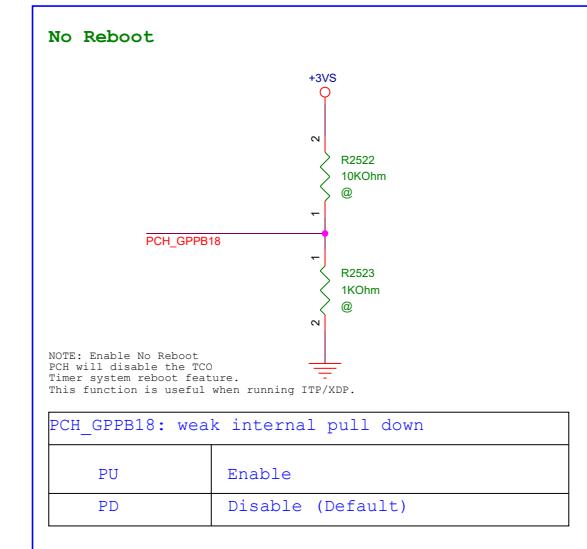
	Hynix(2Gb)	XXX (2Gb)	Micron(2Gb)	
DIMM_SEL0				
DIMM_SEL1				
DIMM_SEL2				

	HYNIX (4Gb) 03006-00011600 DDR3L_1600_512M*8 1.35V HYNIX/HSTC4683APR-PBA	ELPIDA (4Gb) 03006-00011400 DDR3L_1600_512M*8 1.35V MICRON/MT41K512M8RH-125	Micron(4Gb) 03006-00011400 DDR3L_1600_512M*8 1.35V MICRON/MT41K512M8RH-125	
DIMM_SEL0	L		L	
DIMM_SEL1	L		L	
DIMM_SEL2	H		L	



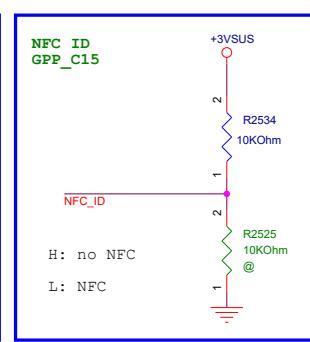
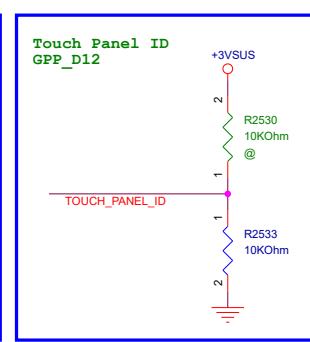
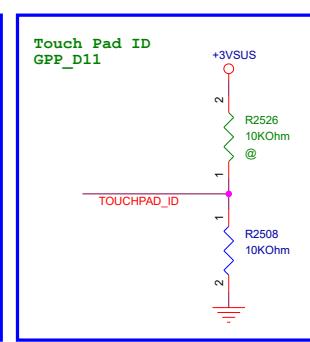
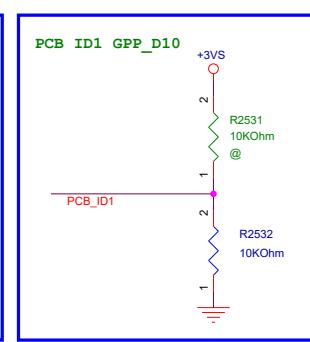
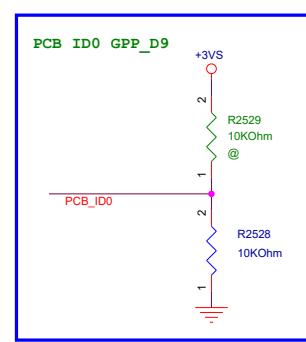
PCH_GPPB22: weak internal pull down

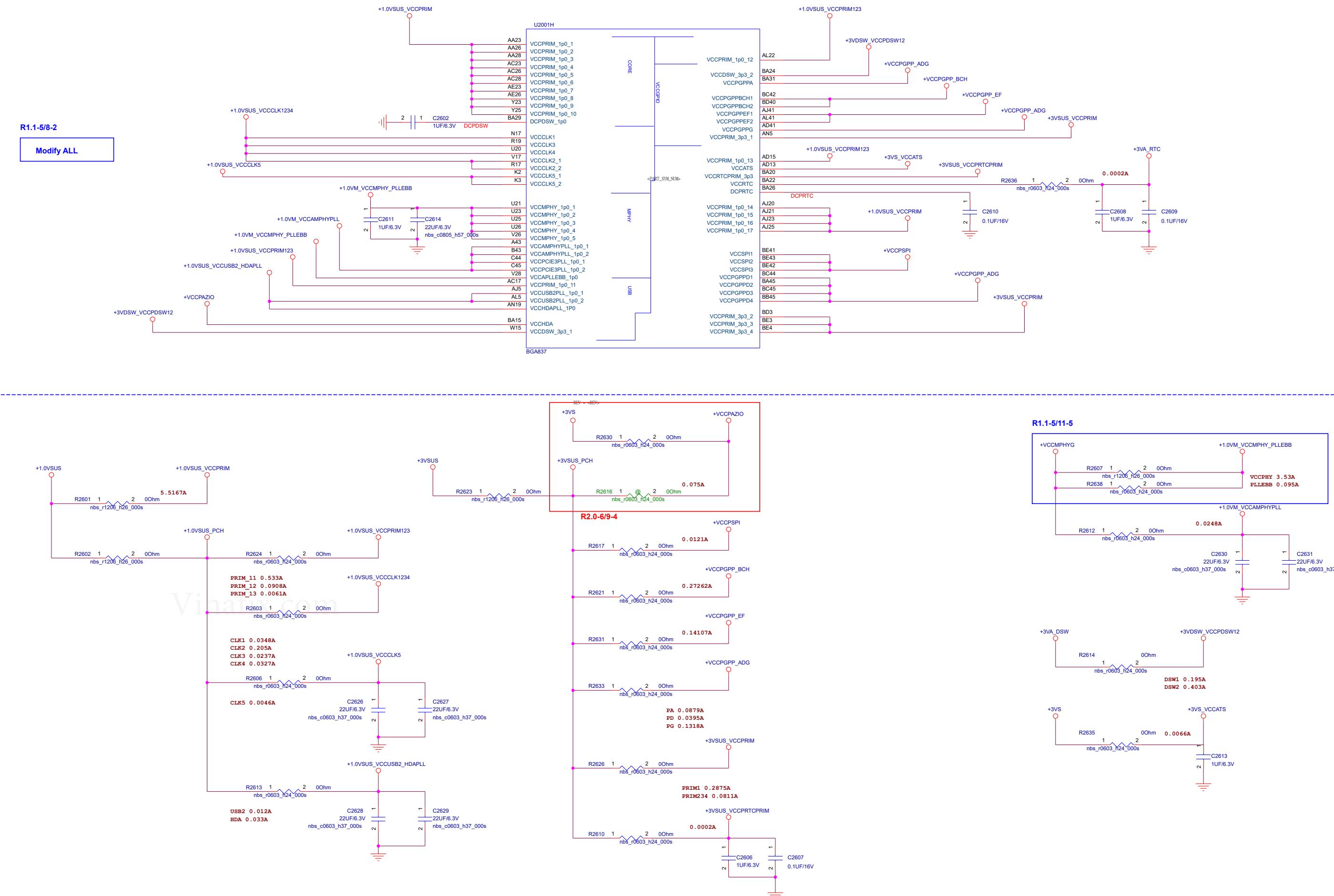
PU	LPC
PD	SPI (Default)

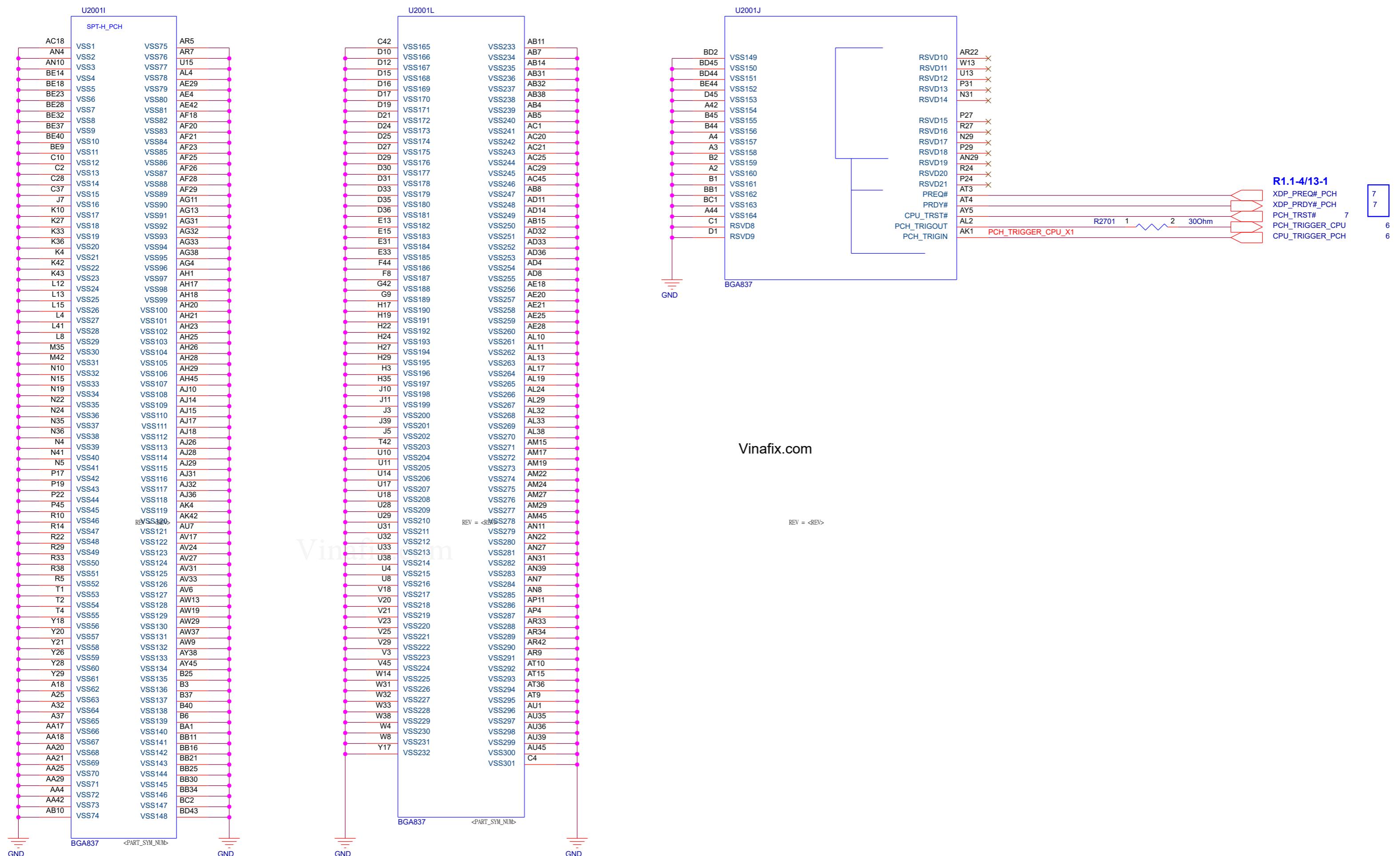


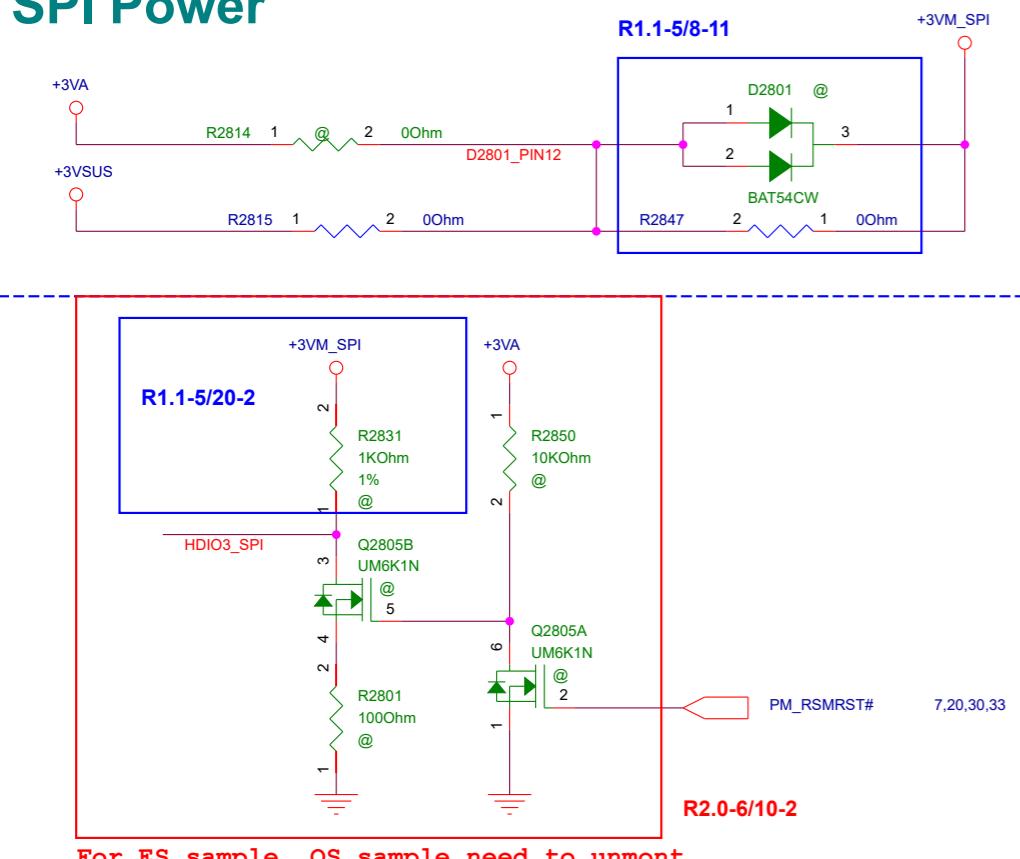
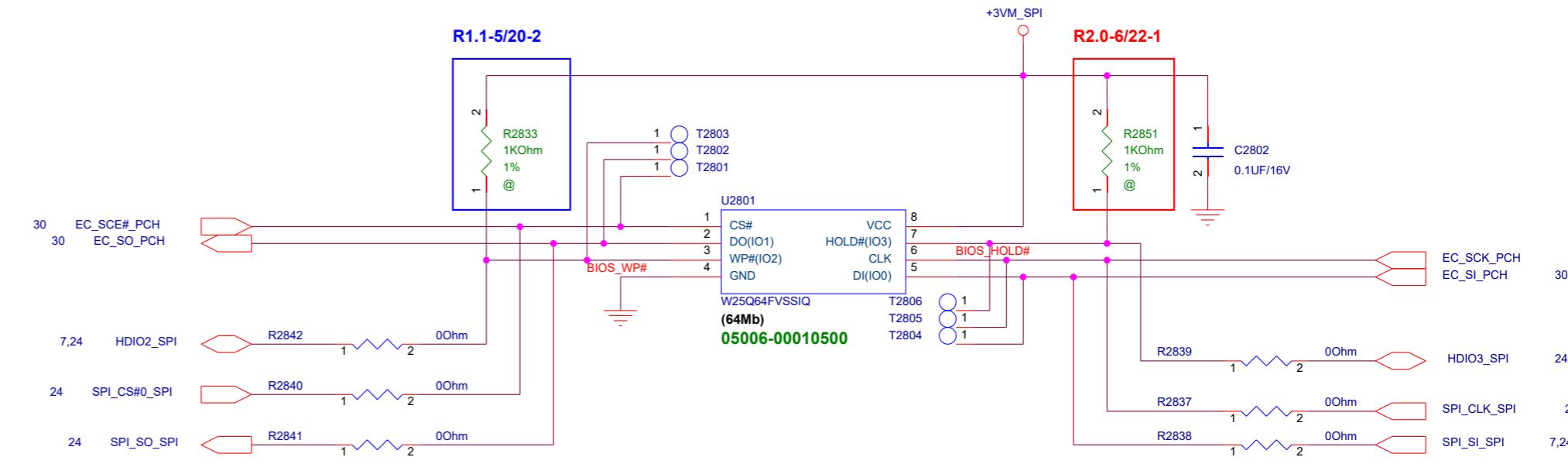
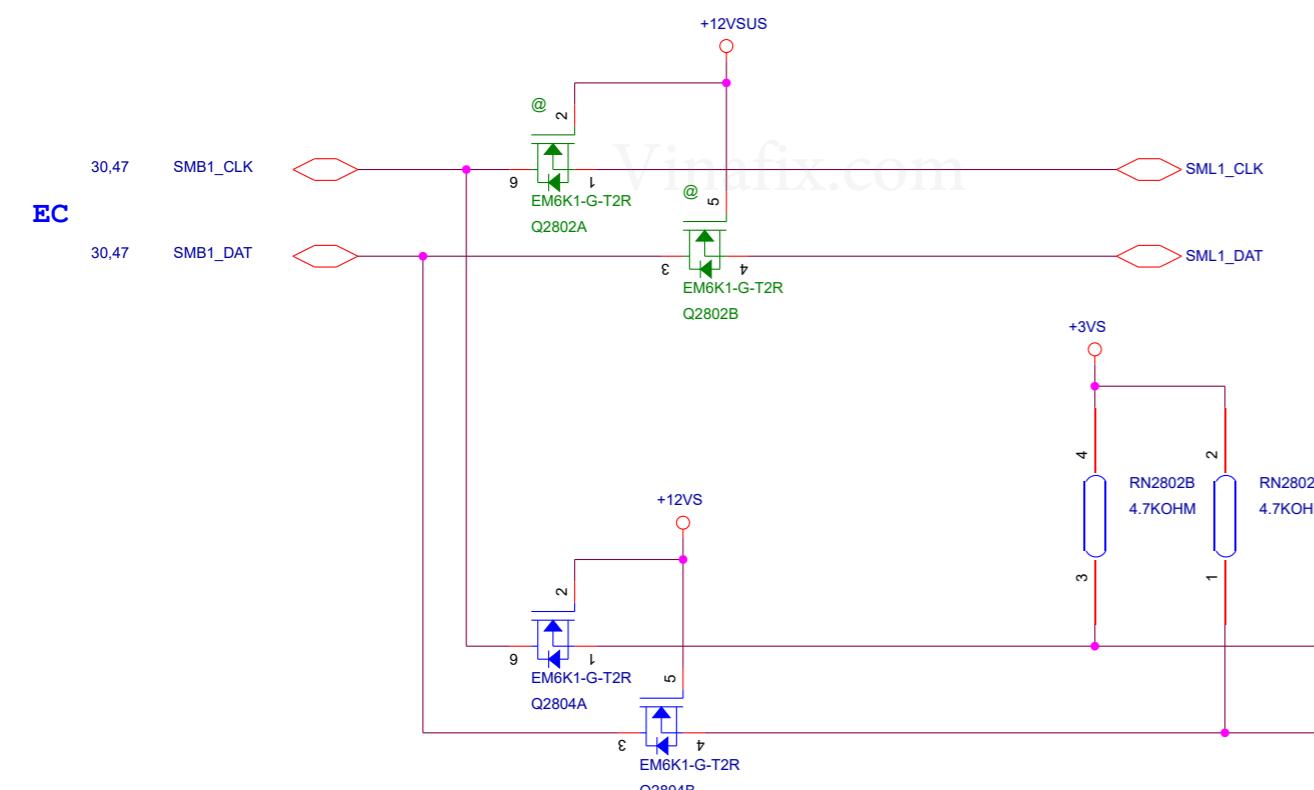
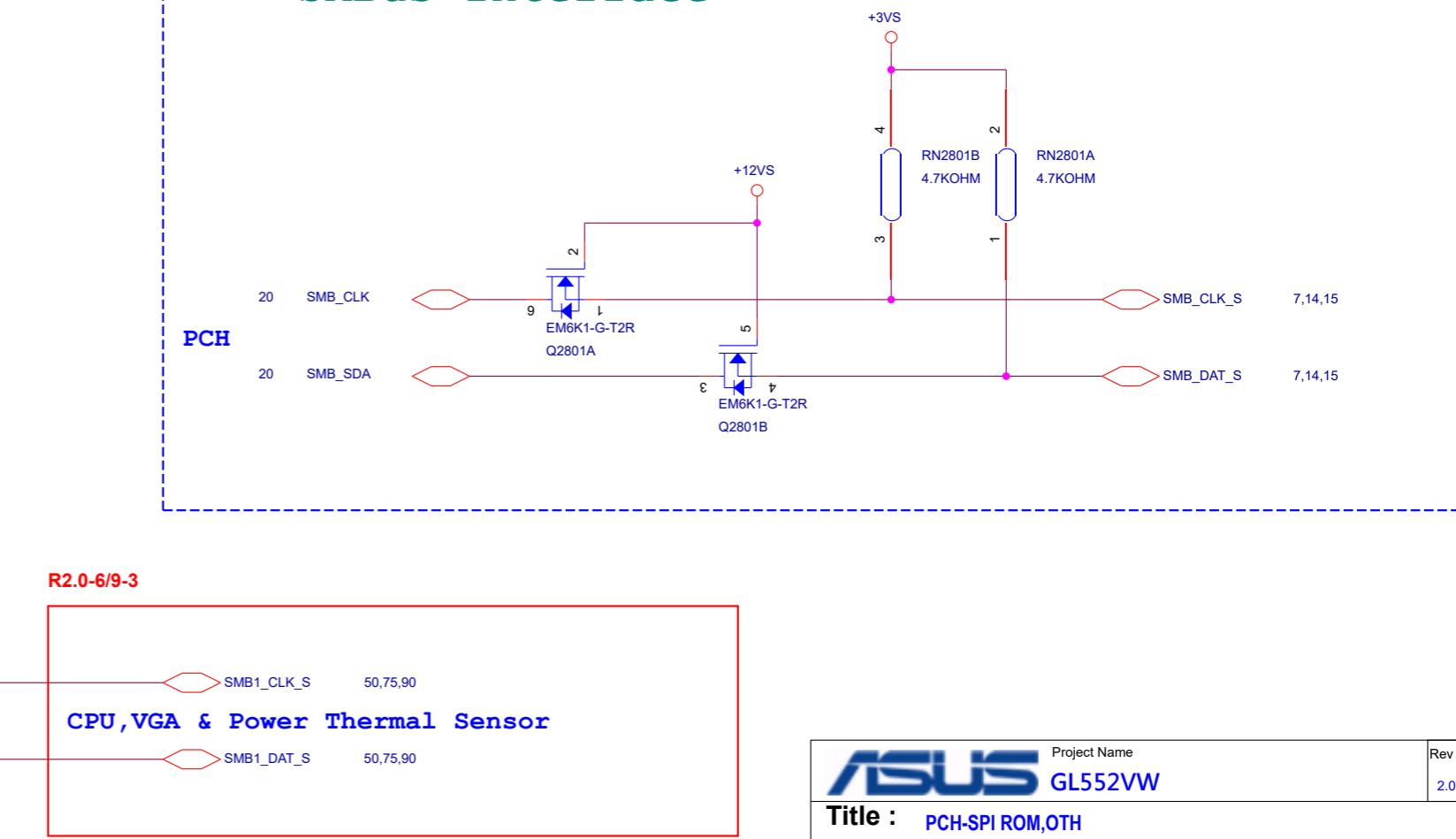
PCH_GPPB18: weak internal pull down

PU	Enable
PD	Disable (Default)







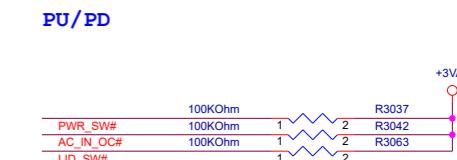
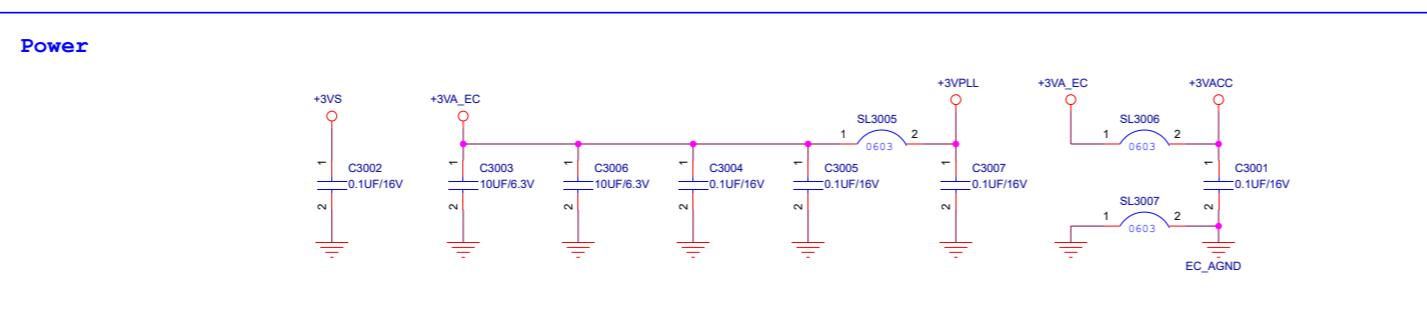
SPI Power**1st SPI ROM****System Management Interface****SMBus Interface**

Only 3V Torlence

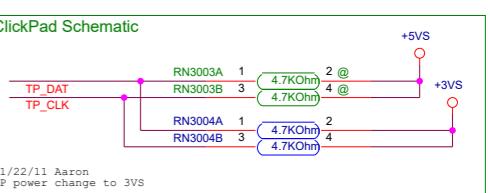
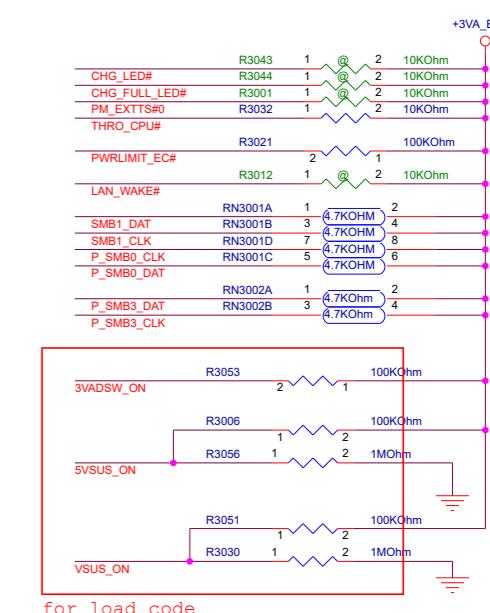
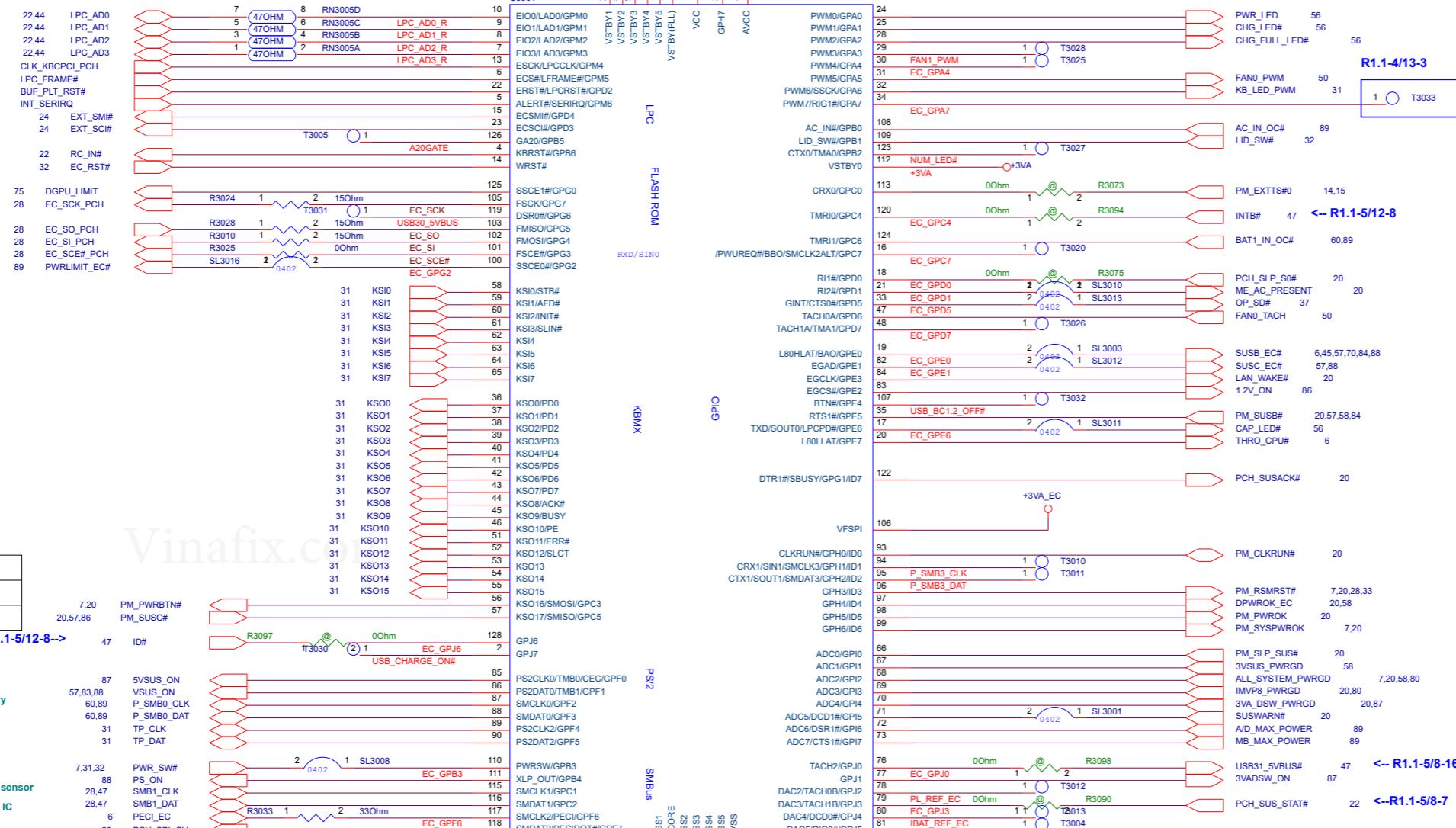
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GFI [0 : 7]
GJJ[0:7]

Can be adjusted to
Open-Drain for port:

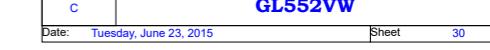
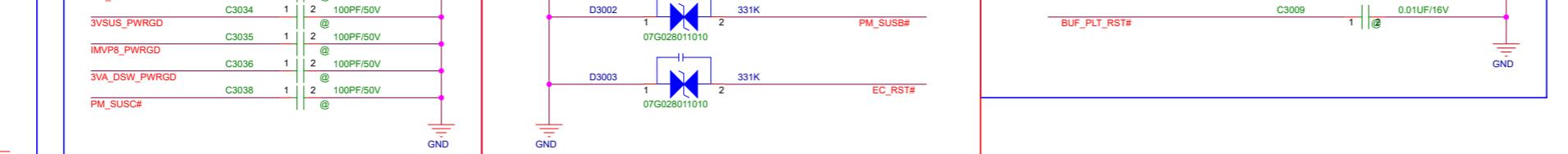
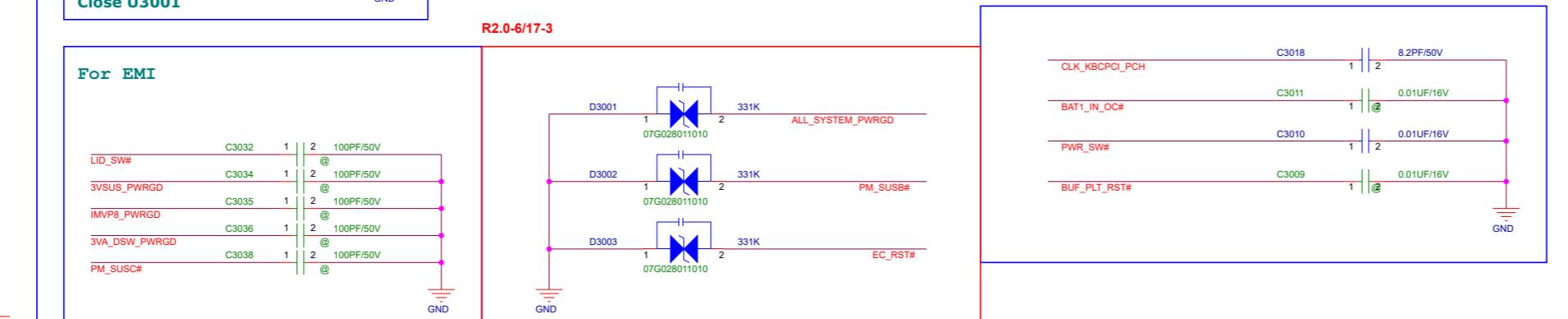
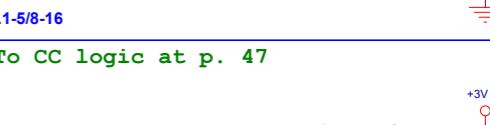
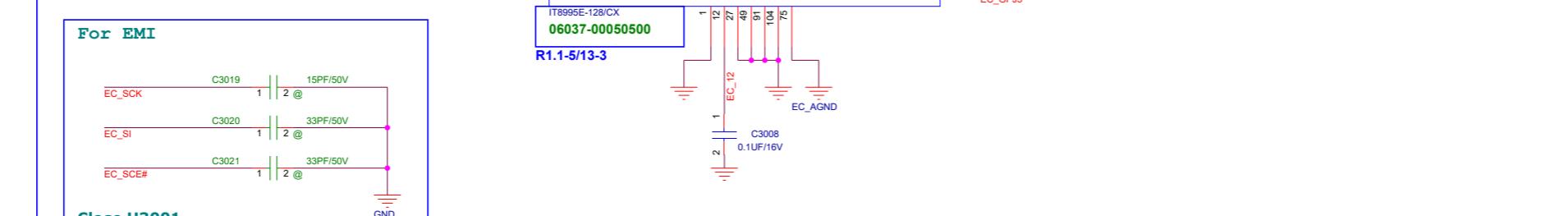
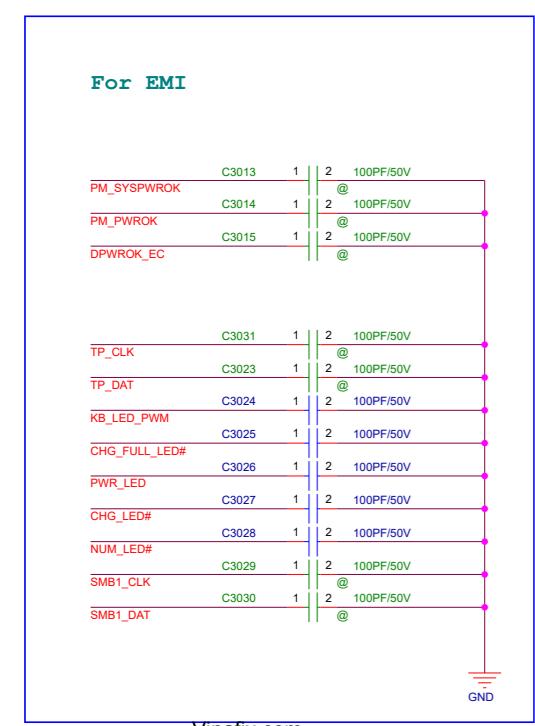
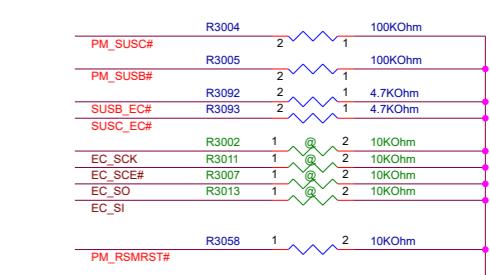
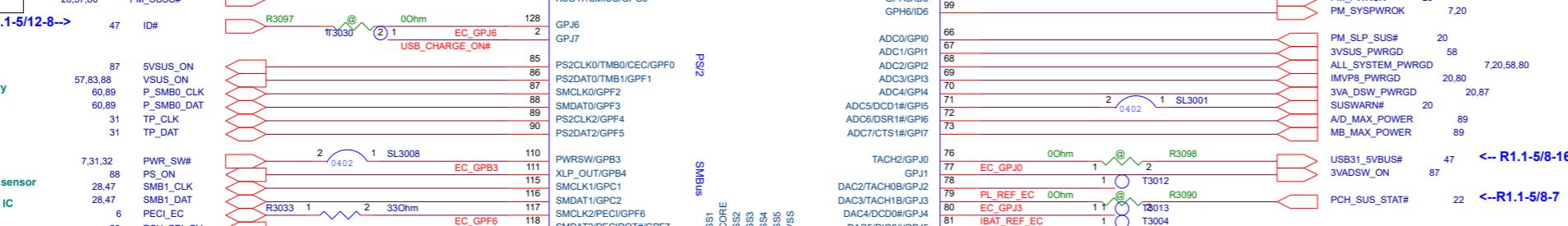
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5



EC Require

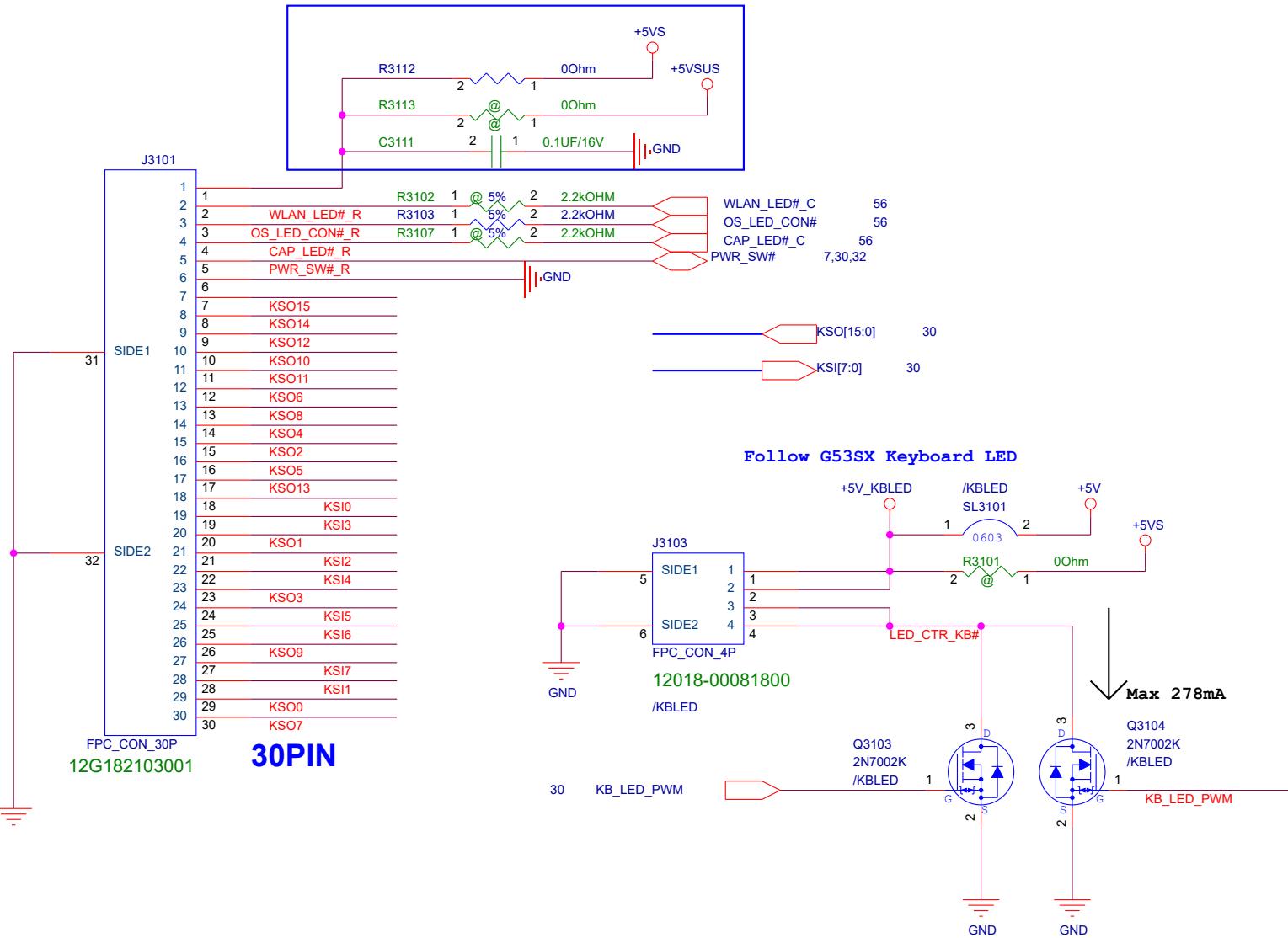


ITE Version	ASUS P/N
IT8995E-128/CX	06037-00050500

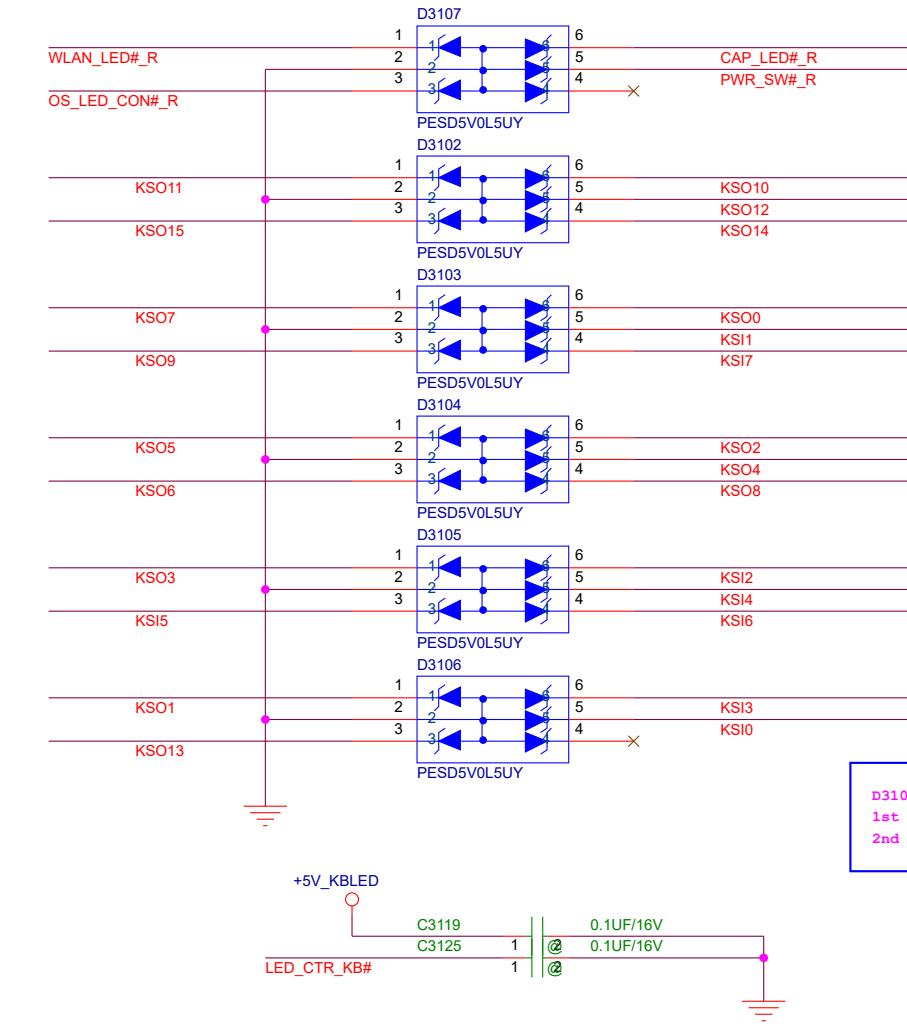


Keyboard Connector

R1.1-5/8-8

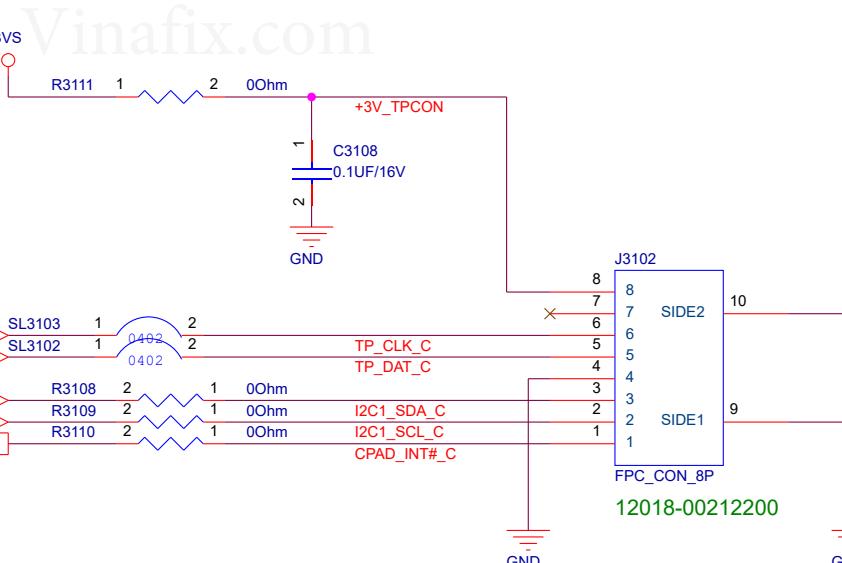


For EMI

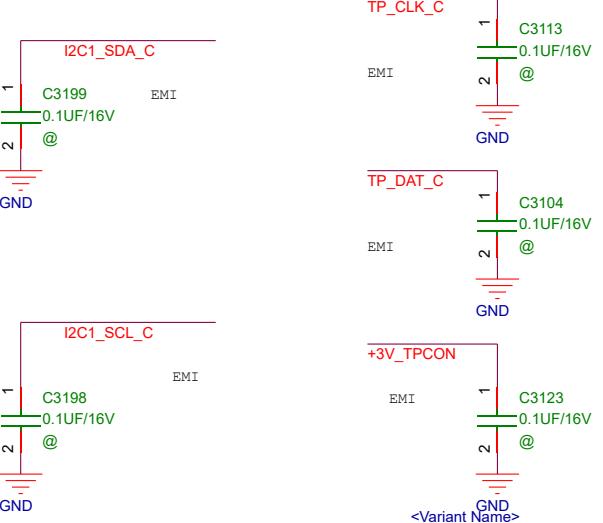


R1.1-4/13-5

Click touch Pad Connector

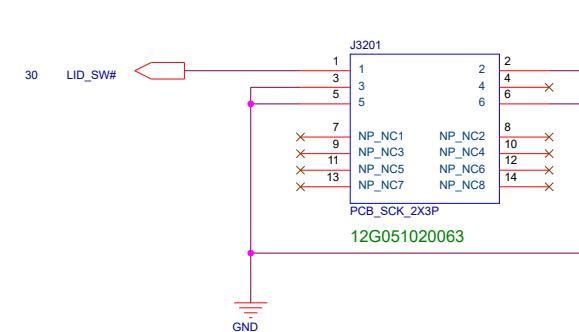
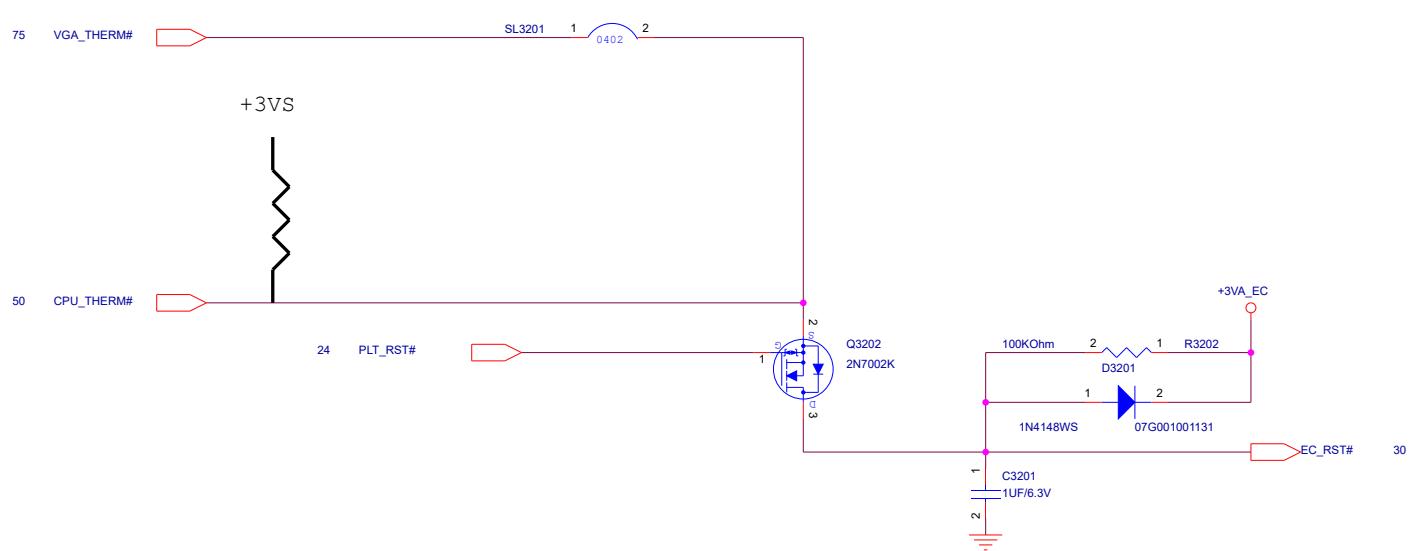


Reserved for EMI

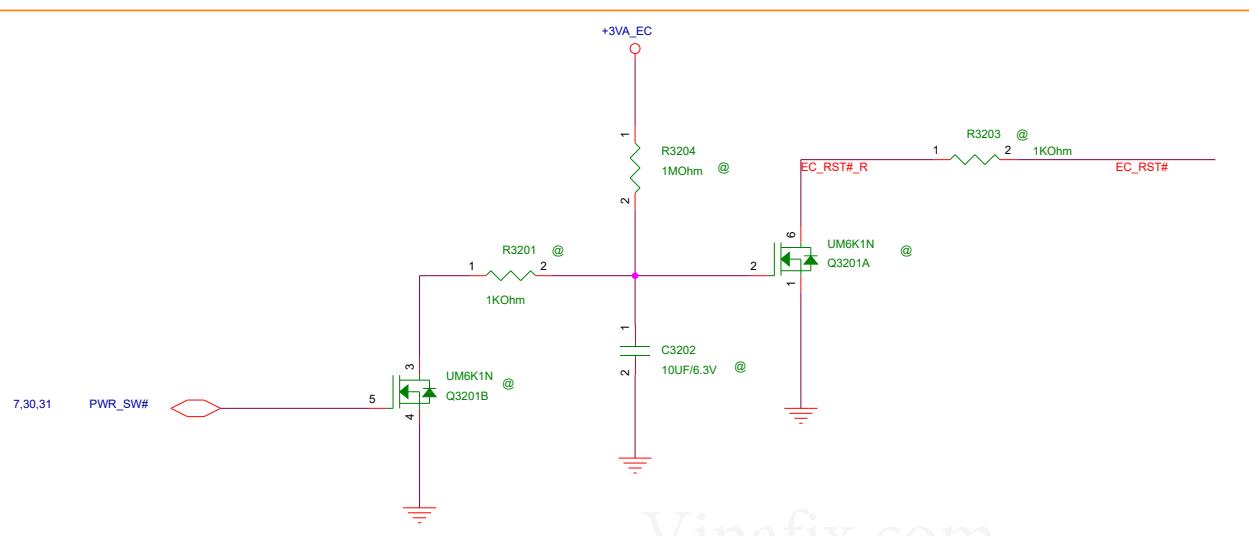


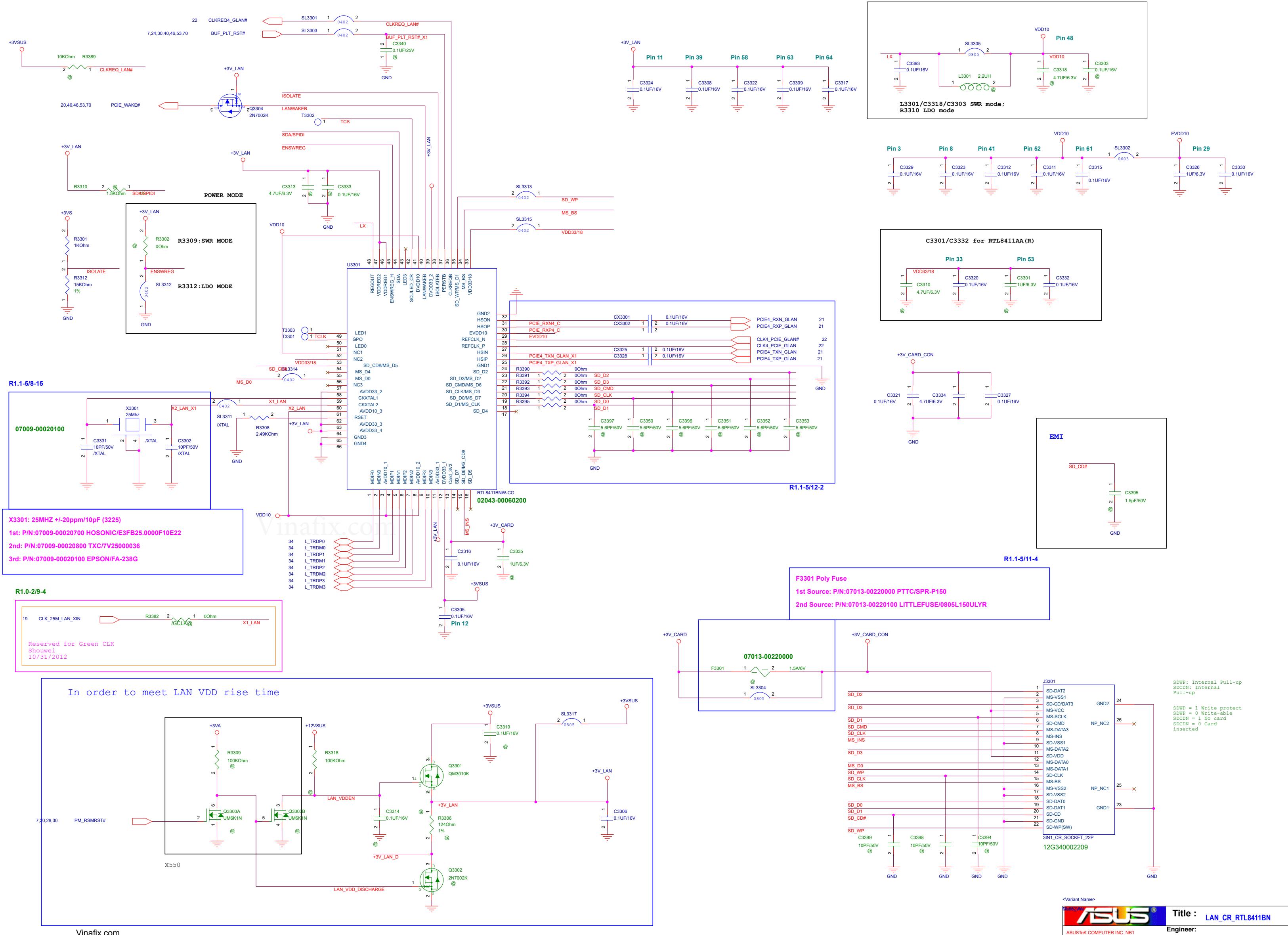
Reset Circuit

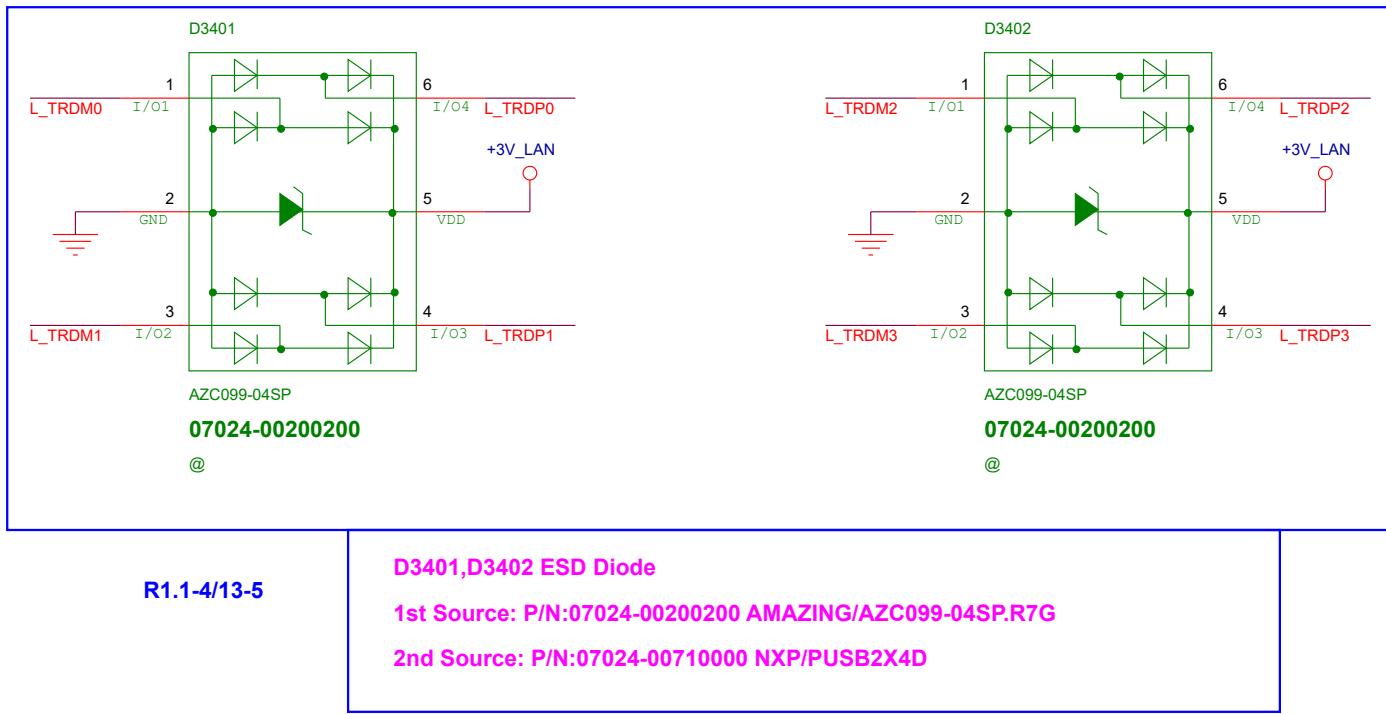
Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in paralle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



For battery embedded case (press pwr_sw 10sec, then reset ec) (need to modify)



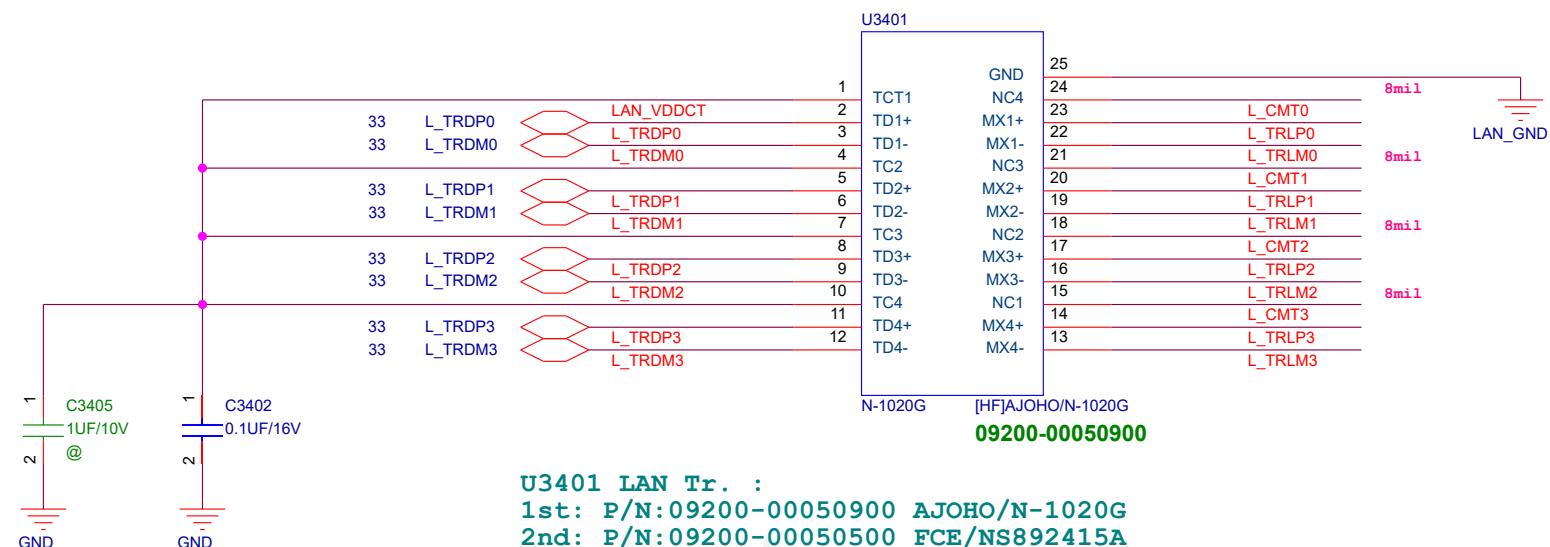




R1.1-4/13-5

D3401,D3402 ESD Diode

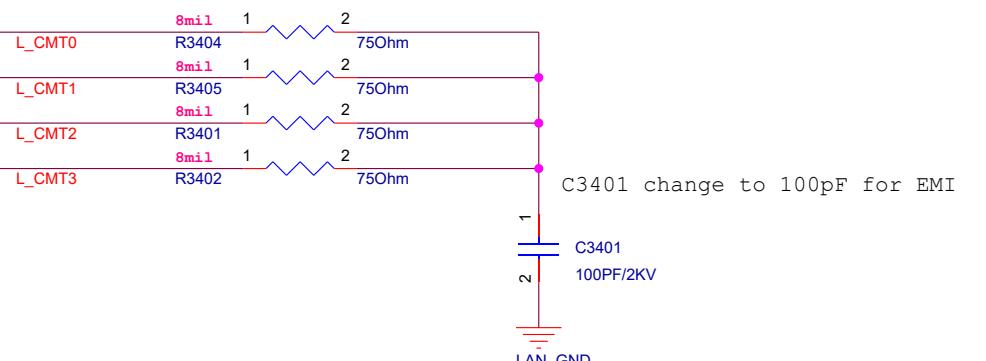
2nd Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G



U3401 LAN Tr. :
1st: P/N:09200-00050900 AJOHO/N-1020G
2nd: P/N:09200-00050500 FCE/NS892415A
3rd: P/N:09G051059A20 BOTHHAND/GST5009BML

Test Point LAN Tr.

拿掉ATE測點，改由layout主動加



The diagram illustrates three parallel ground connection paths originating from a common central node. Each path consists of a capacitor in series with a resistor, followed by a direct ground connection. The first path, at the top, connects to GND through a 0.1UF/25V capacitor and a 1Ω resistor. The second path, in the middle, connects to LAN_GND through a 0.1UF/25V capacitor and a 1Ω resistor. The third path, at the bottom, connects to LAN_GND through a 0.1UF/25V capacitor and a 2Ω resistor. All connections are labeled with component values and types in green text.

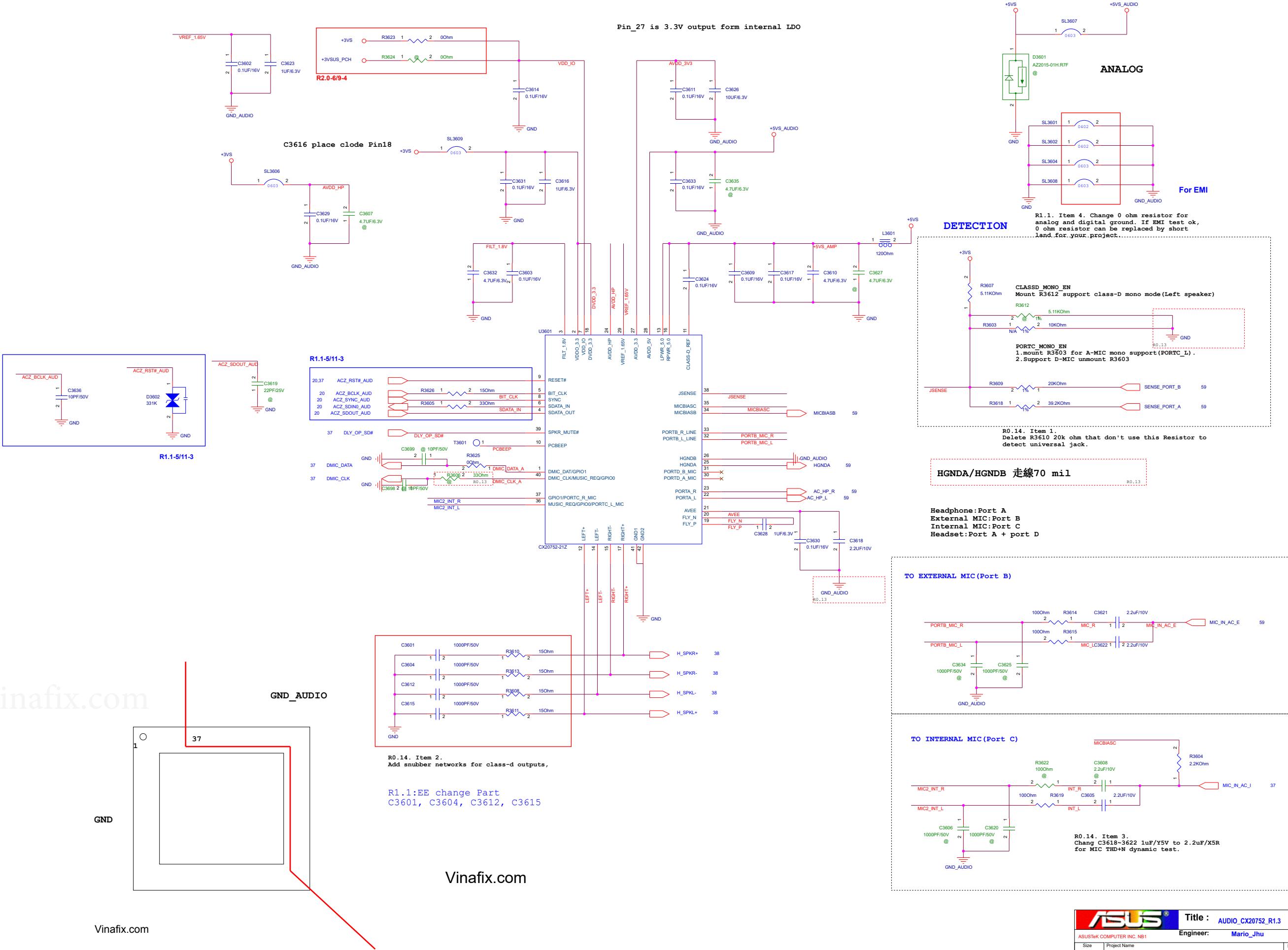
<Variant Name>



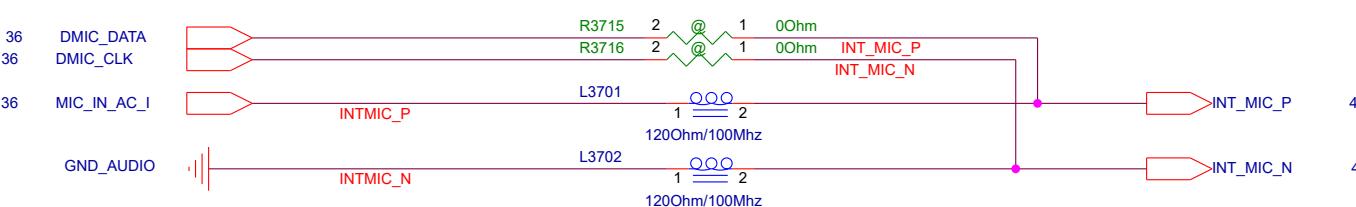
Title : LAND USE

Engineer: Mario Ibu

ASUSTEK COMPUTER INC. NB1		Engineer.:	Mario_01u		
Size B	Project Name GL552VW			Rev 2.0	
Date: Tuesday, June 23, 2015	Sheet		34	of	103

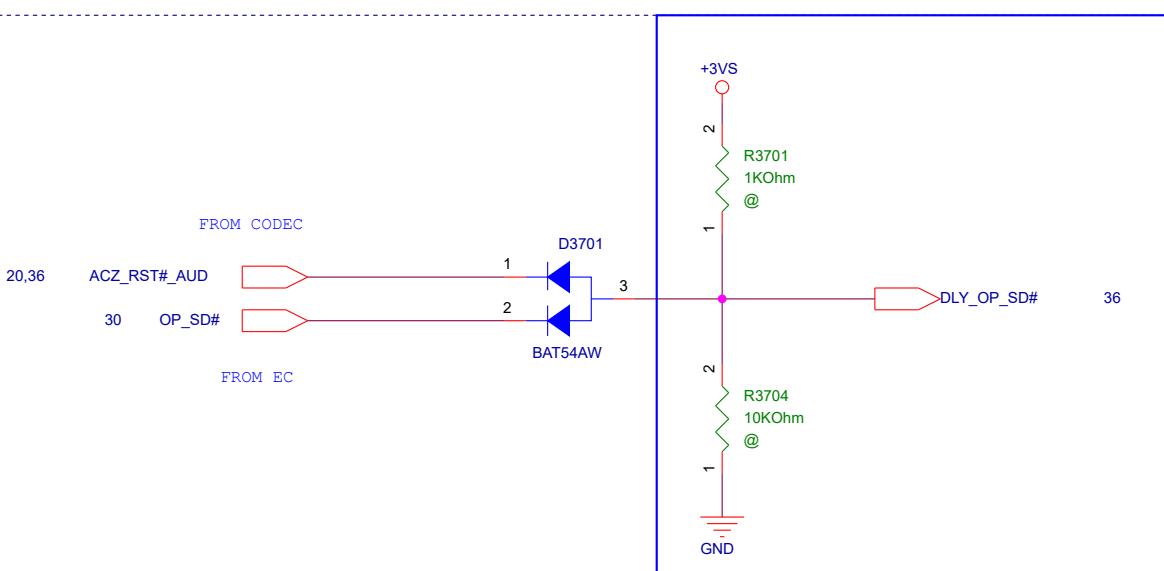


INTERNAL MICROPHONE



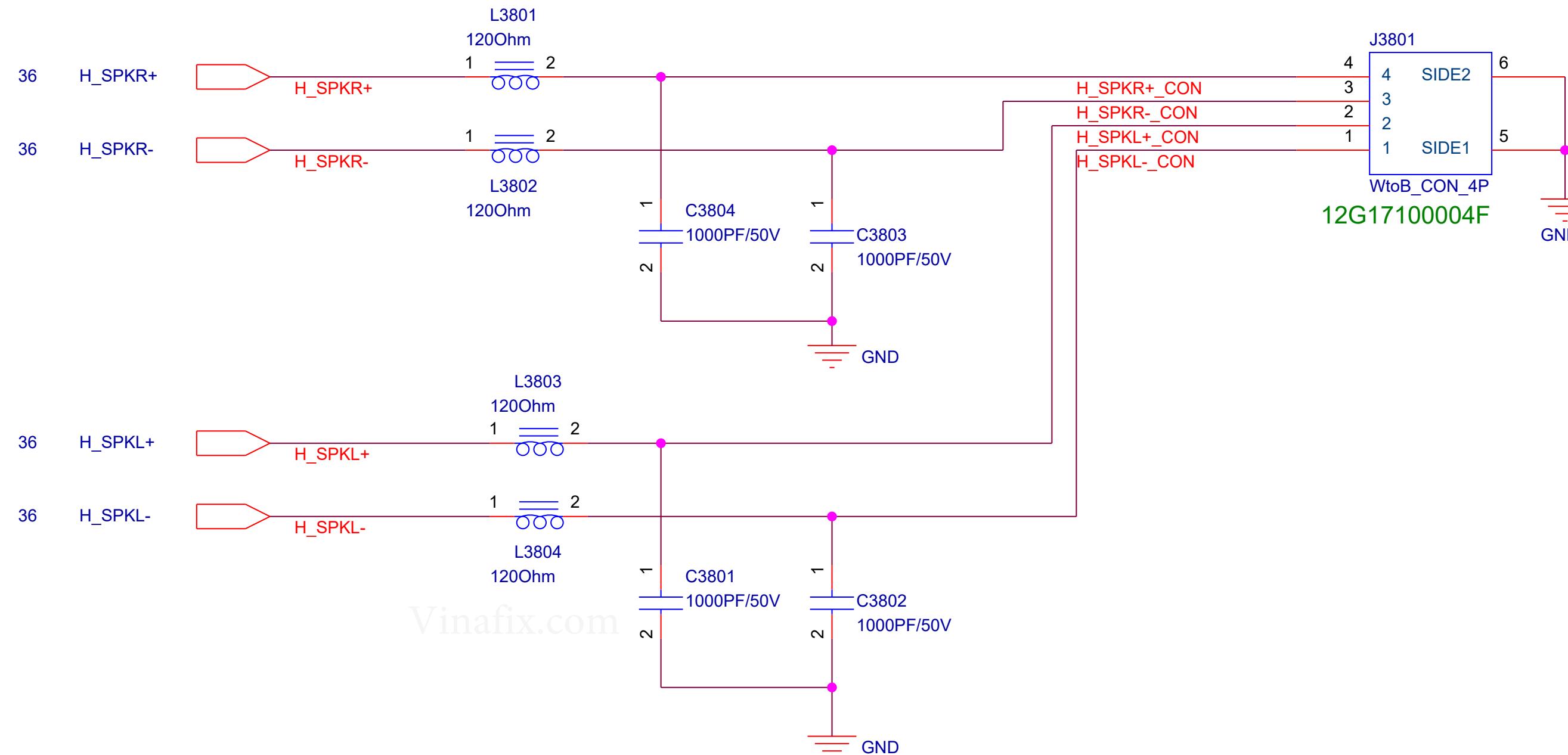
MUTE CONTROL

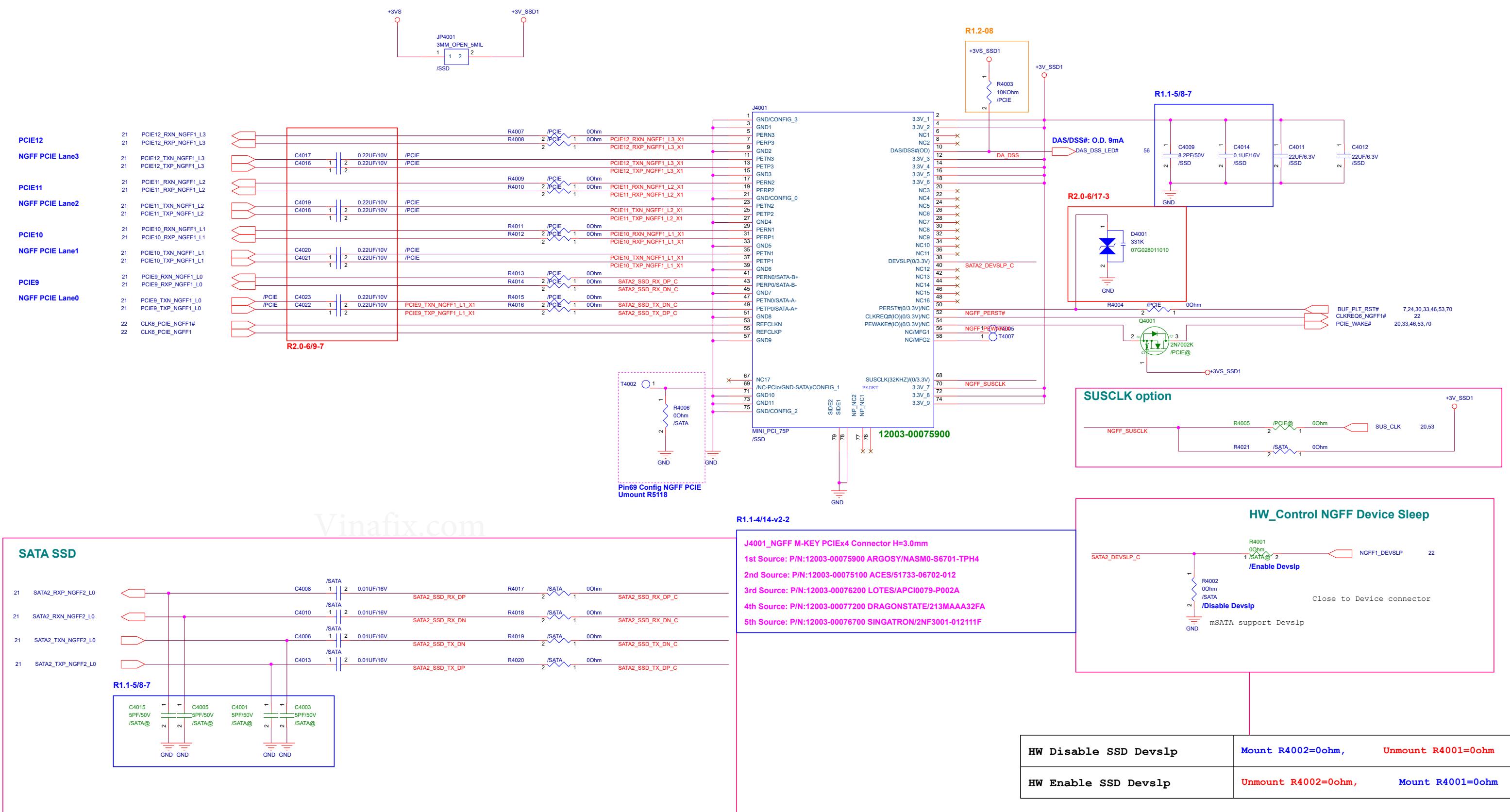
R1.1-5/12-9



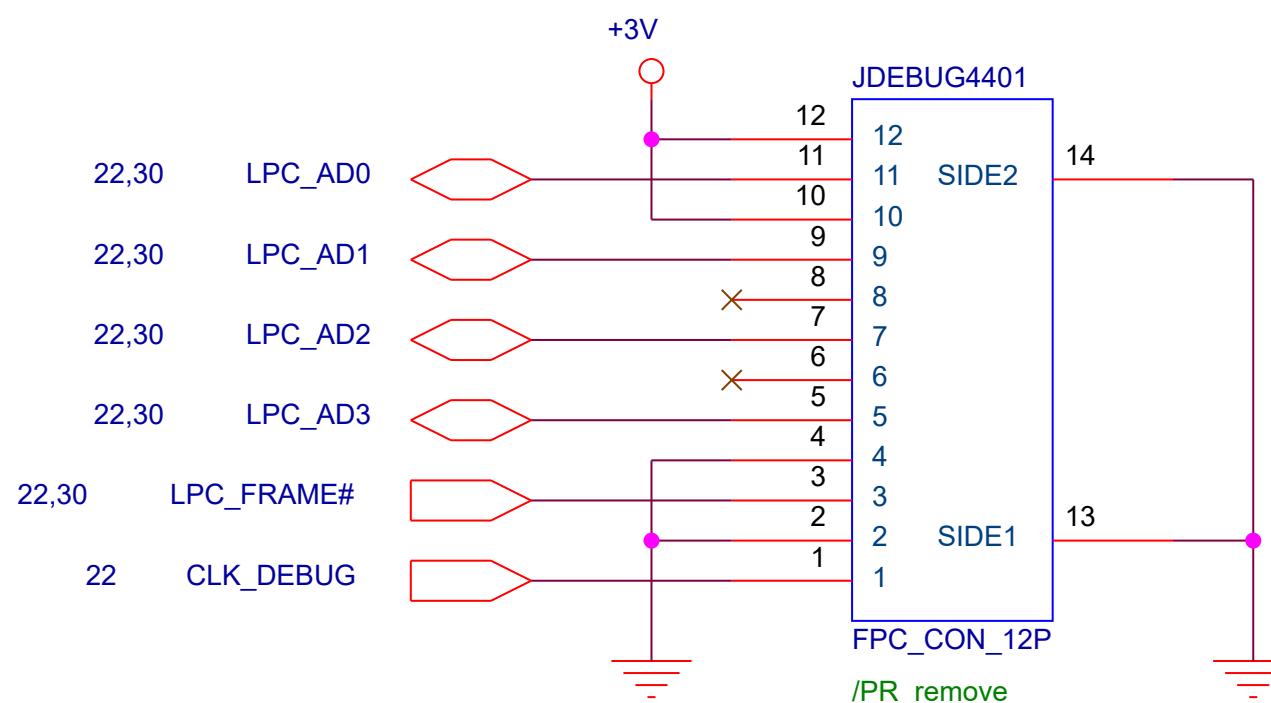
Vinafix.com

ASUS®		Title :	AUD-AMP
ASUSTek COMPUTER INC. NB1		Engineer:	Mario_Jhu
Size	Project Name		Rev
B			2.0
Date: Tuesday, June 23, 2015	Sheet	37	of 103





LPC Debug Port



R1.1-4/13-5

JDEBUG4401 Connector (MP USE)

1st Source: P/N:12018-00102400 P-TWO/196479-12041-3

2nd Source: P/N:12018-00102100 ENTRY/6705K-Y12N-00L

3rd Source: P/N:12018-00102300 ACES/51578-01201-001

12018-00102900

R1.1-4/13-5

JDEBUG4401 Connector (NPI USE)

1st Source: P/N:12018-00102900 ENTRY/6705K-Y12N-20L

2nd Source: P/N:12018-00103000 ACES/51578-01201-002

Vinifix.com

<Variant Name>



Title : DEBUG_LPC

ASUSTeK COMPUTER INC. NB1

Engineer: Mario_Jhu

Size
A

Project Name

GL552VW

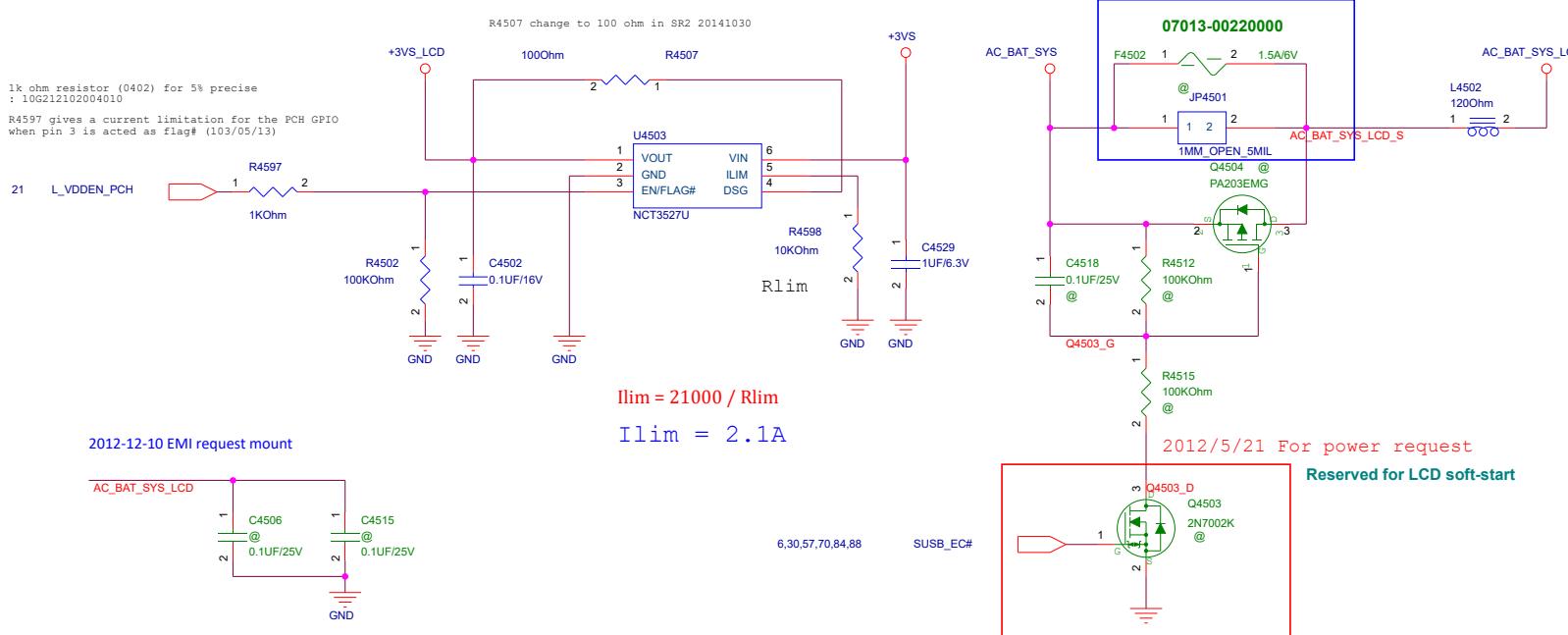
Rev

2.0

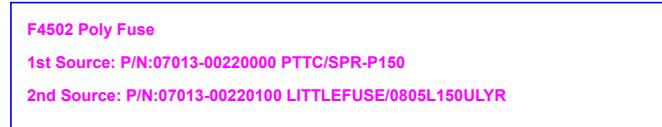
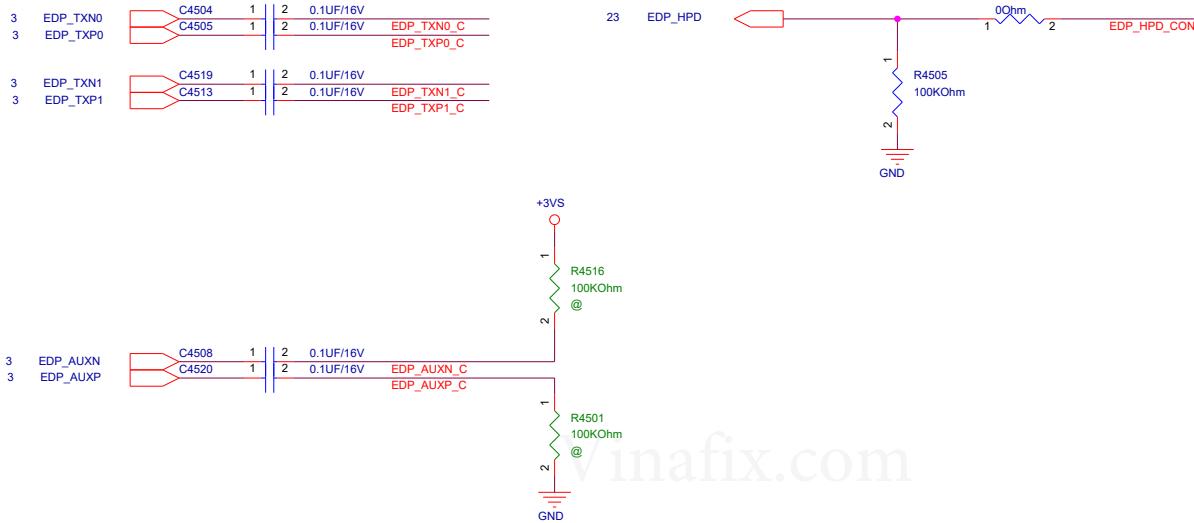
Date: Tuesday, June 23, 2015

Sheet 44 of 103

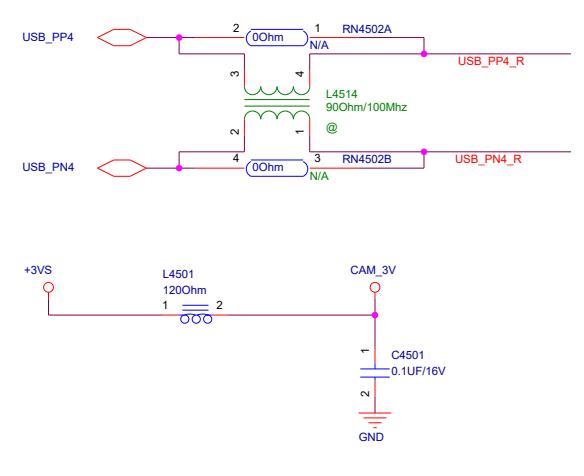
LCD Power switch



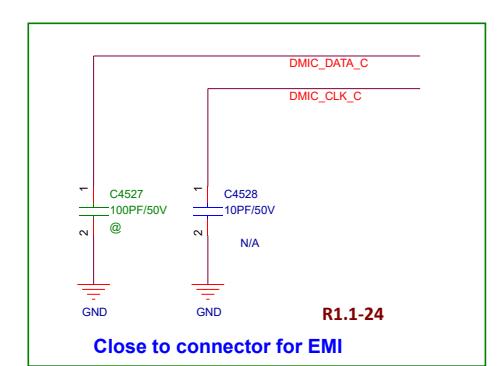
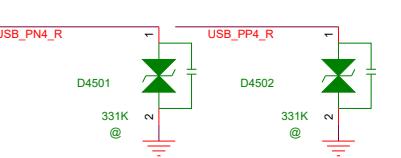
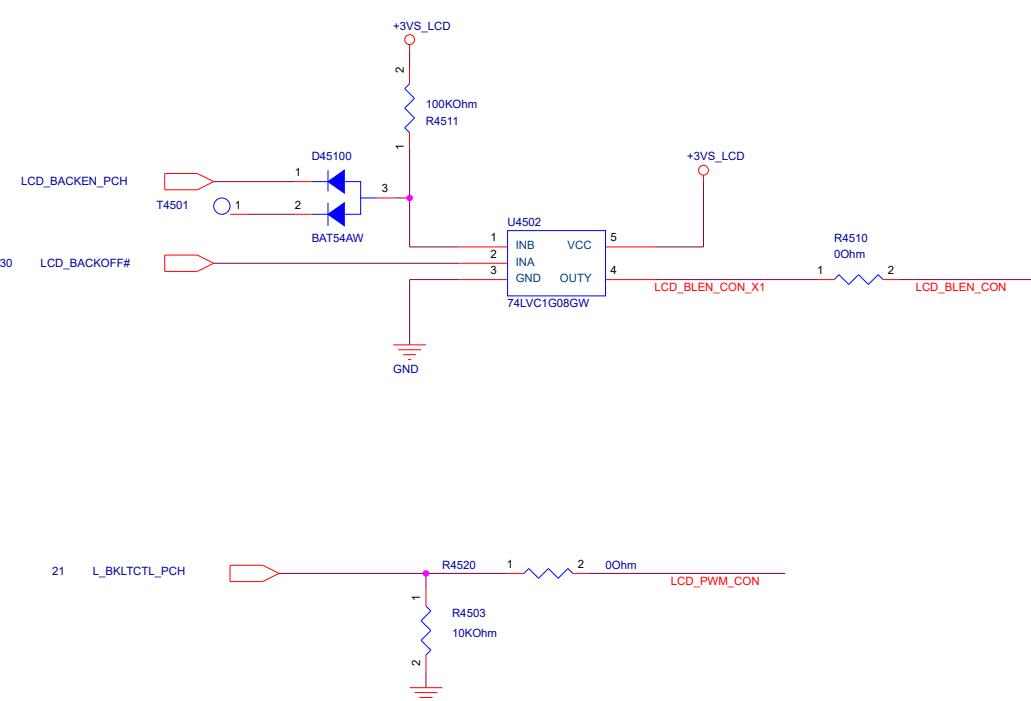
eDP from CPU



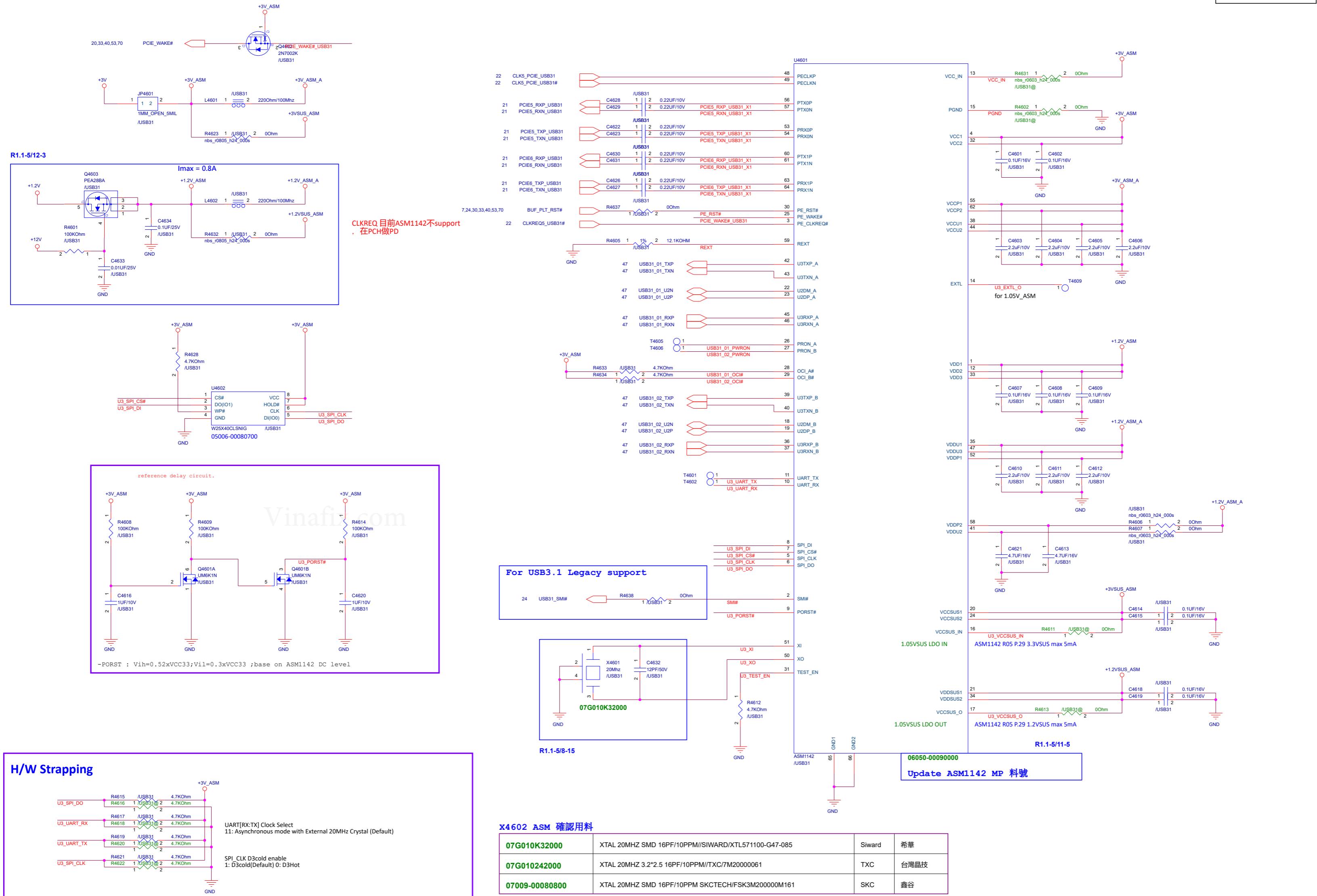
Camera module



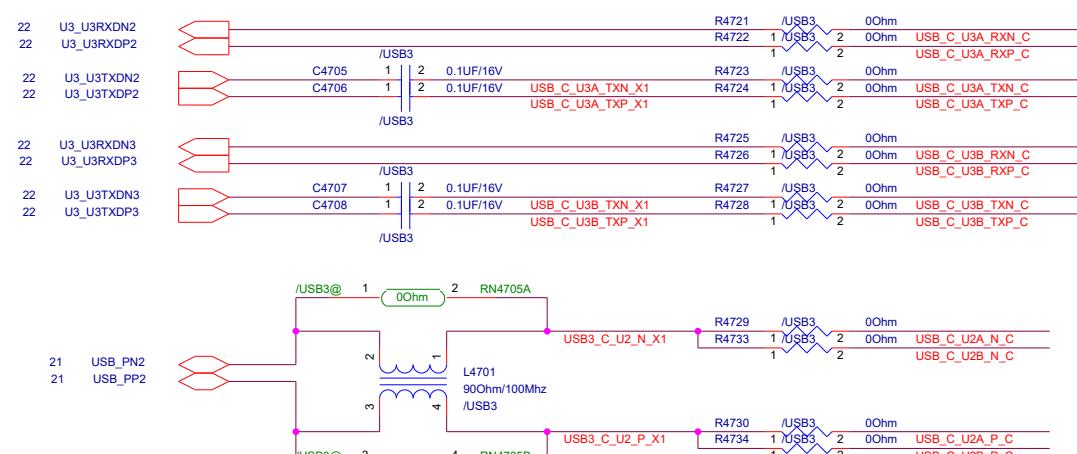
R1.1-5/11-4



Title : CRT_eDP	
ASUSTeK COMPUTER INC. NB1	Engineer: Mario_Jhu
Size C	Project Name GL552VW
Rev 2.0	Date: Tuesday, June 23, 2015

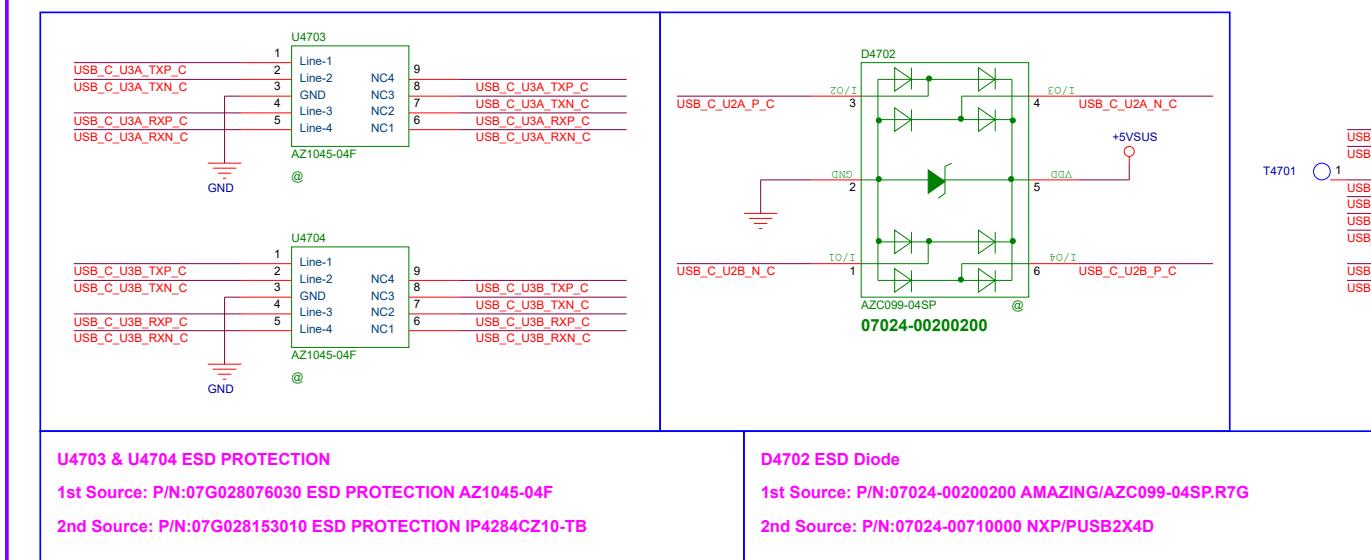


PCH USB3.0



Type C Con. & USB3.0 EMI protect

R1.1-5/12-4



U4703 & U4704 ESD PROTECTION

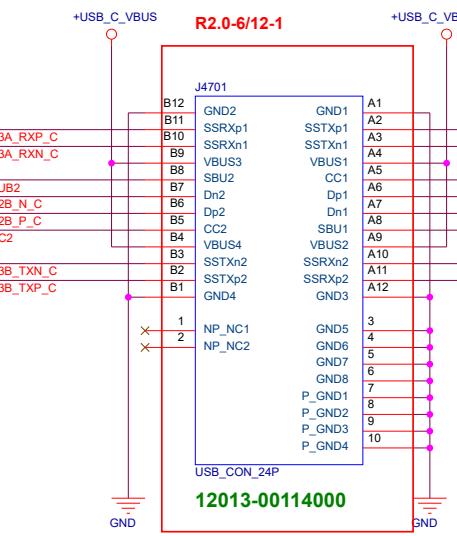
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

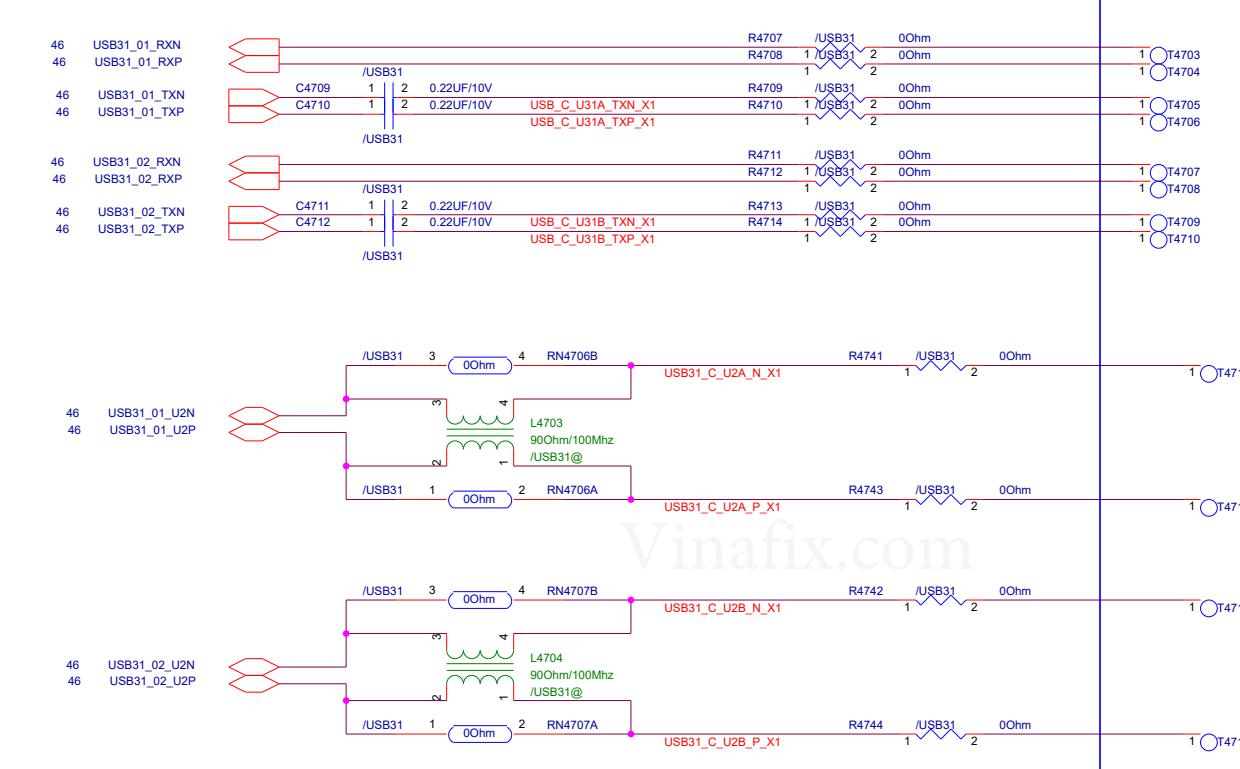
D4702 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

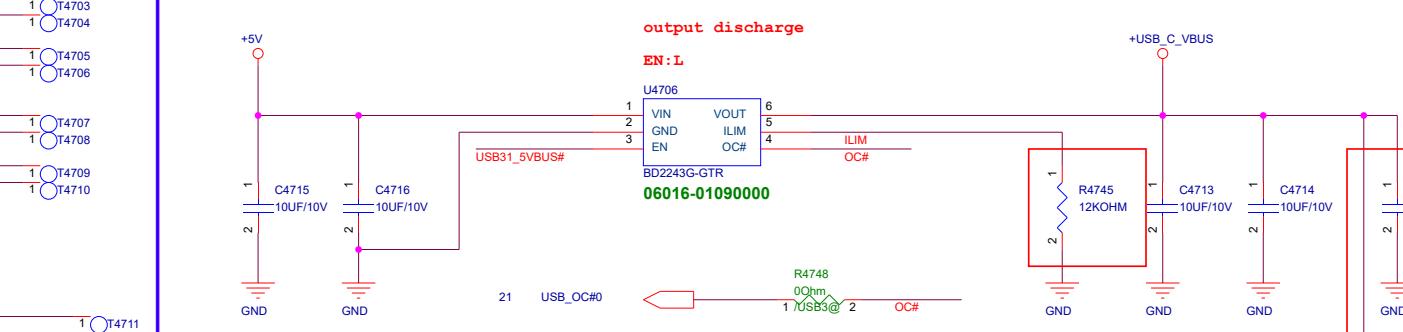
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



ASM1142 USB3.1



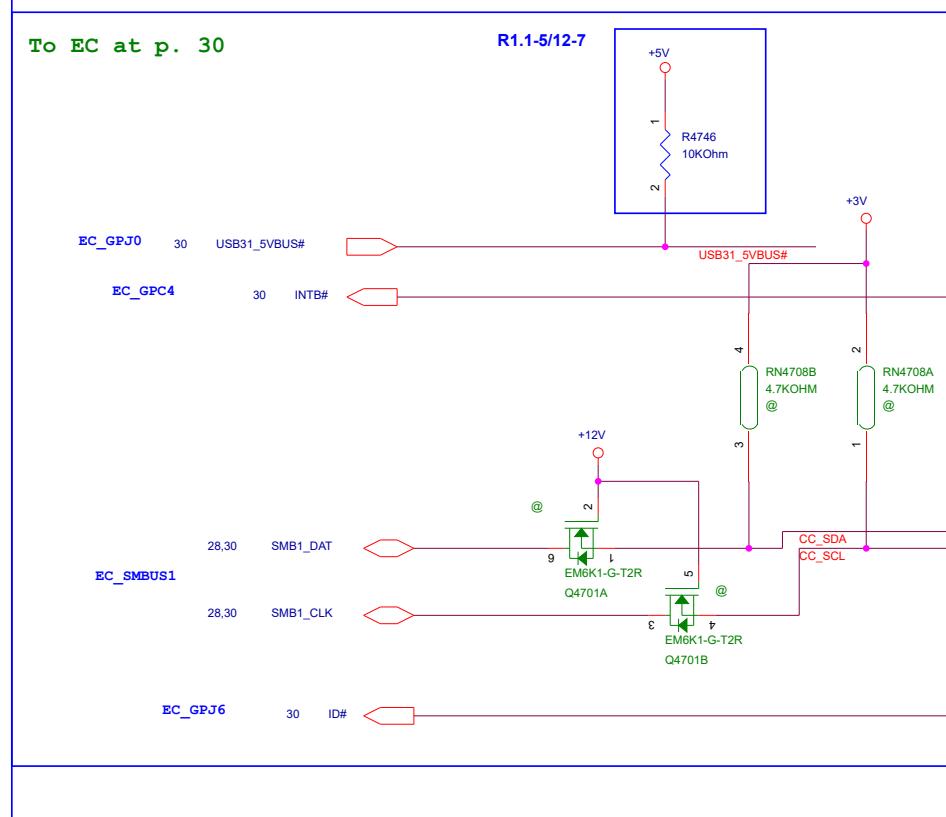
Type-C CC logic IC PI5USB30216 & VBUS POWER Switch



	Min	Typ	Max	R4745
112	212	313	100kohm	
911	1028	1145	20kohm	
1566	1696	1826	12kohm	

R2.0-6/9-7

R1.1-5/8-16



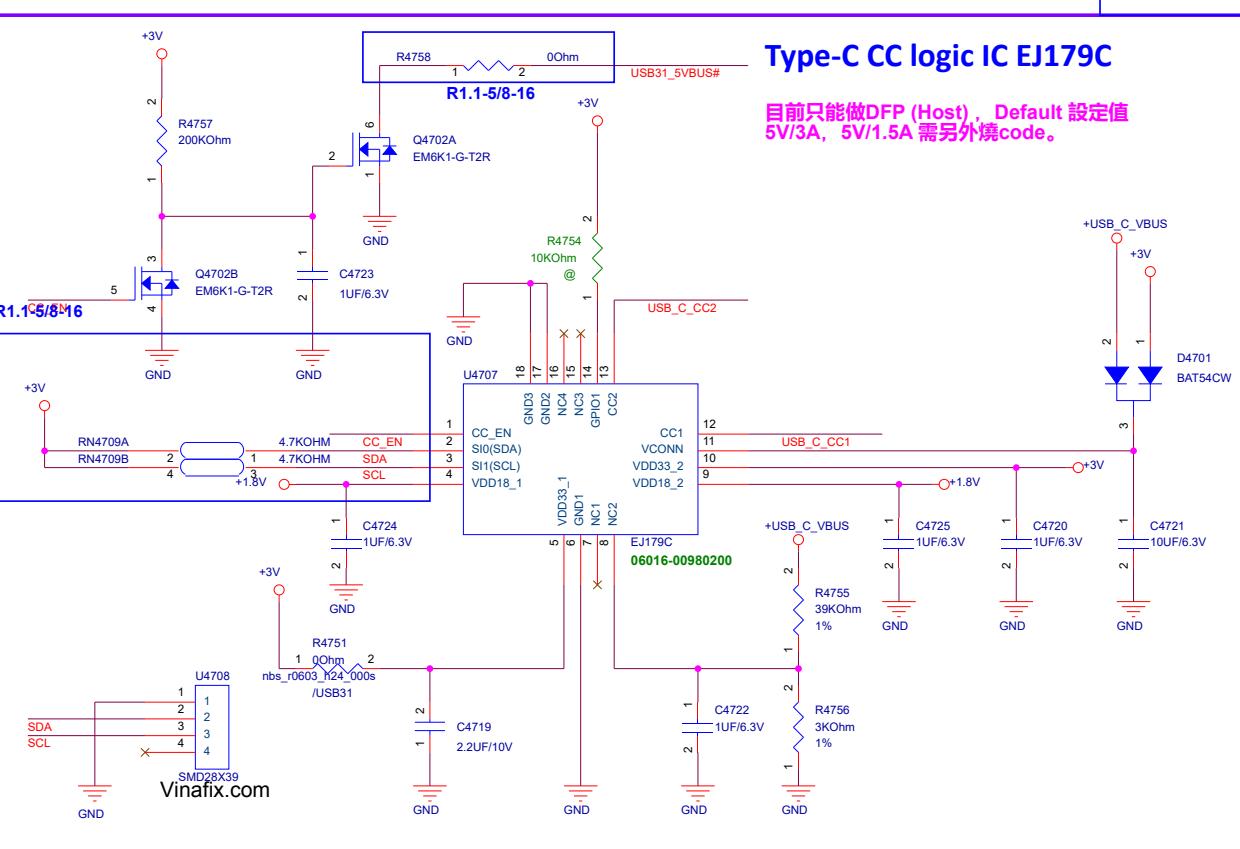
CC logic IC I2C address		
ADDR	High	0x7A
ADDR	Low	0x3A

R1.1-5/13-1

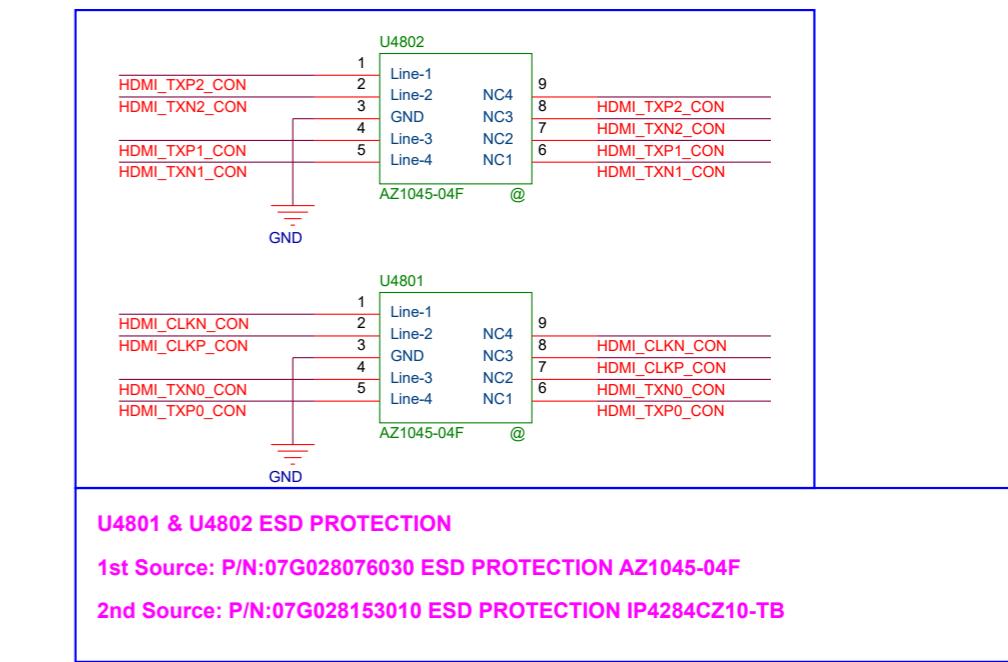
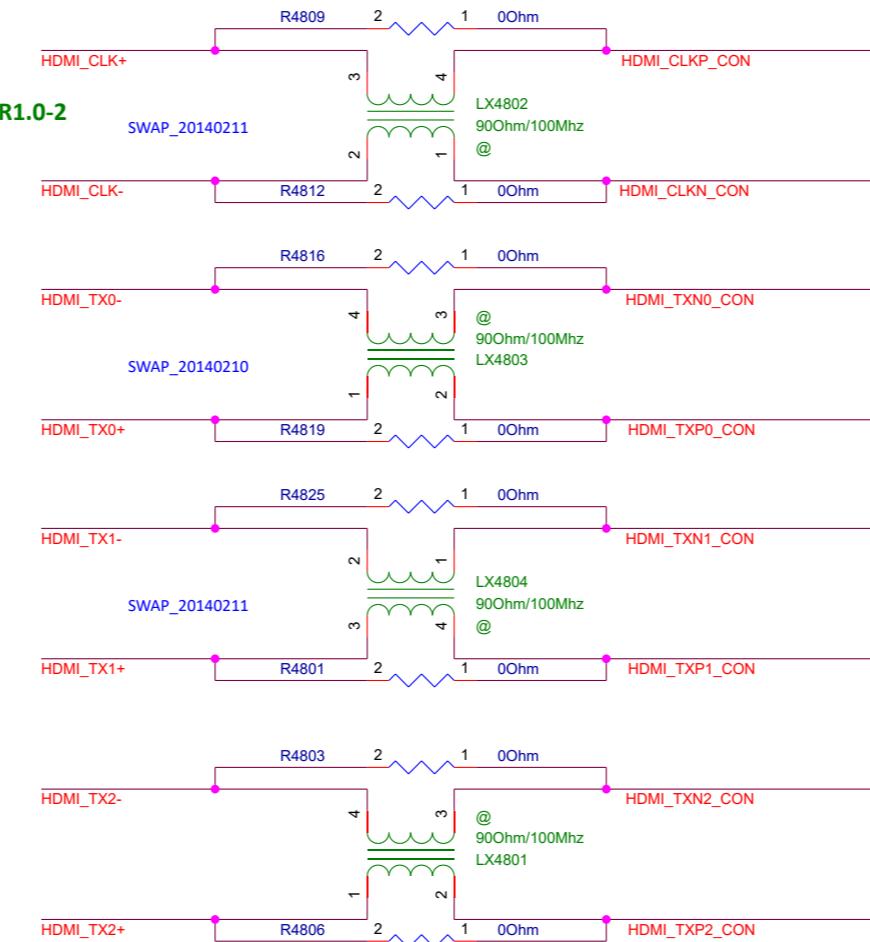
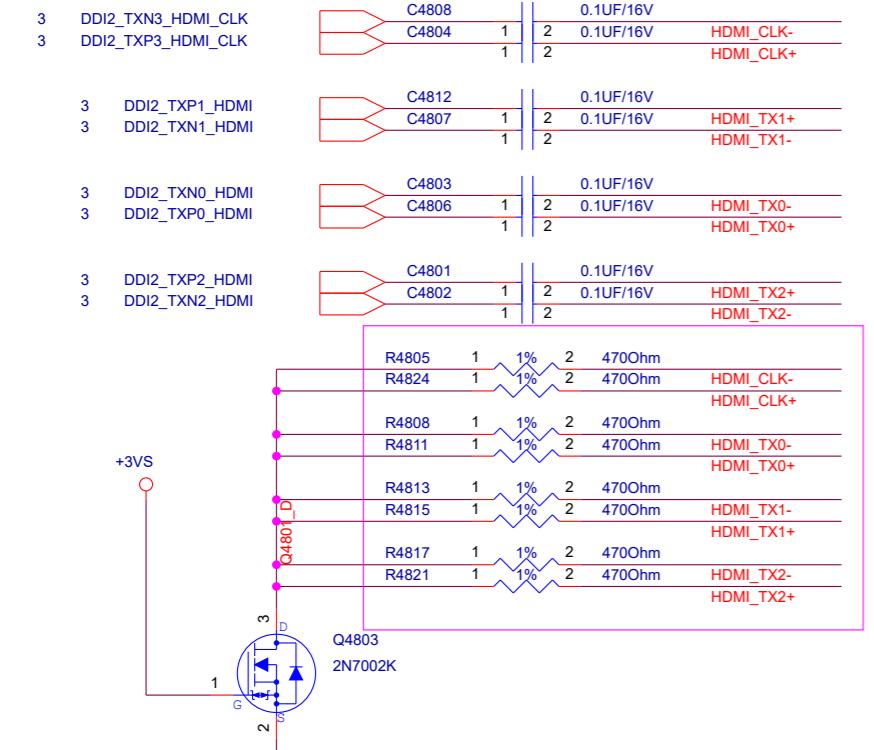
Port setting		
PORT	High	Host (DFP)
PORT	Low	Device (UFP)
NC	Dual role (DRP)	

Type-C CC logic IC EJ179C

目前只能做DFP (Host), Default 設定值
5V/3A, 5V/1.5A 需另外燒code。

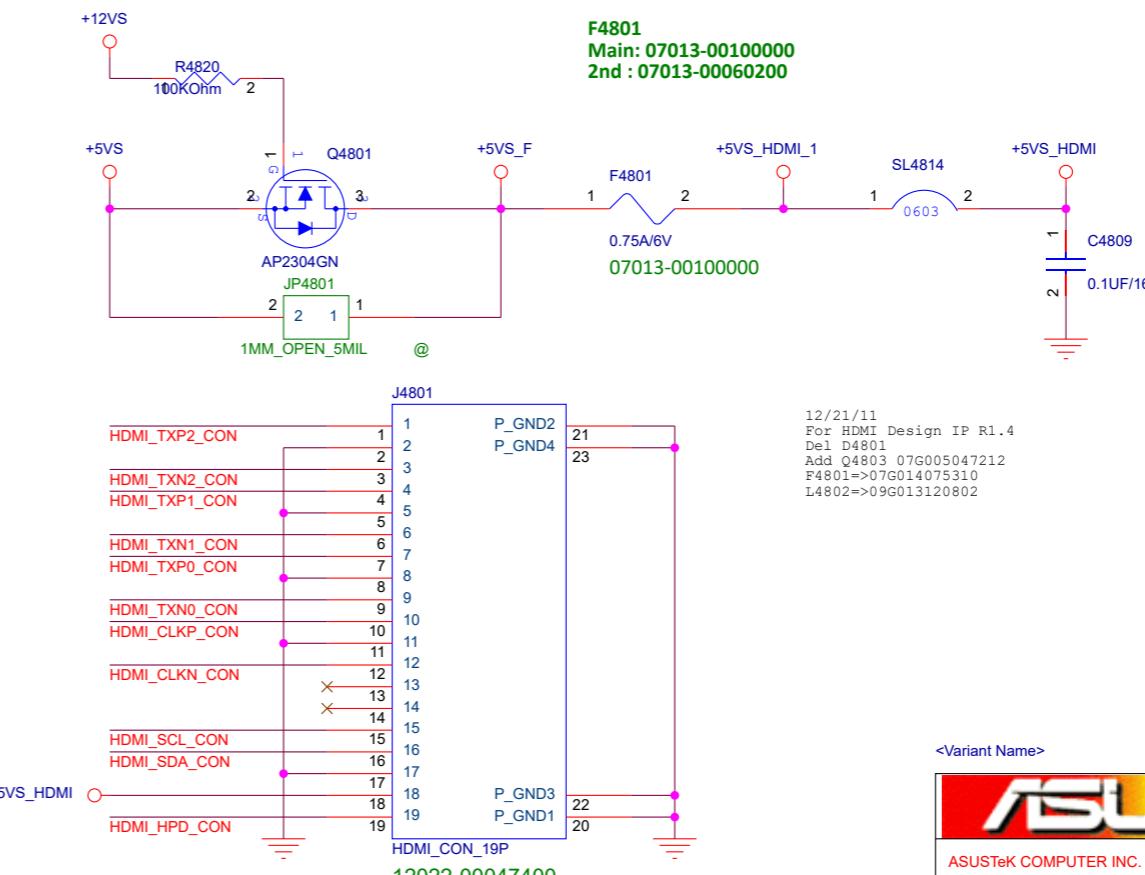
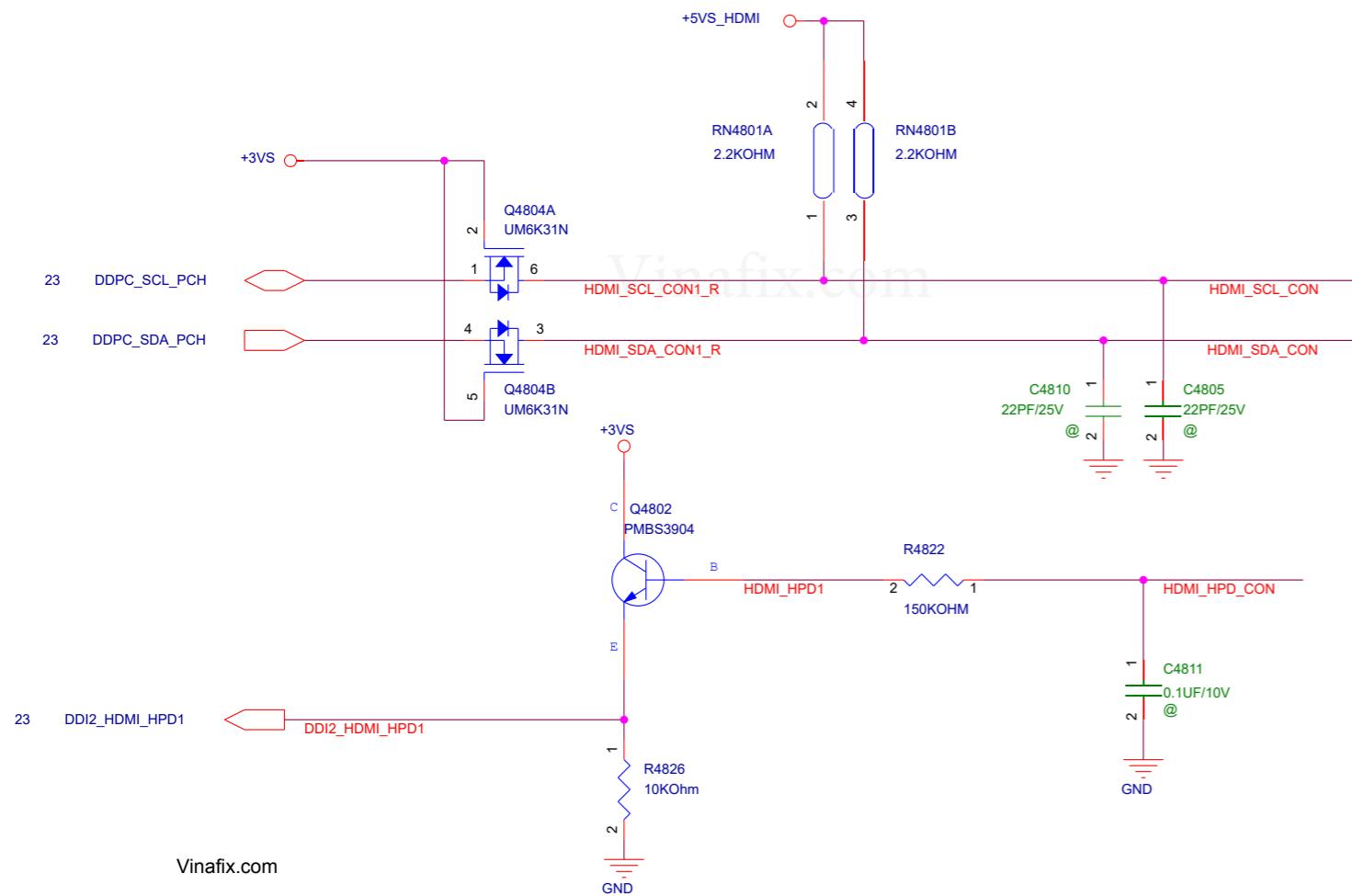


CPU DDIC

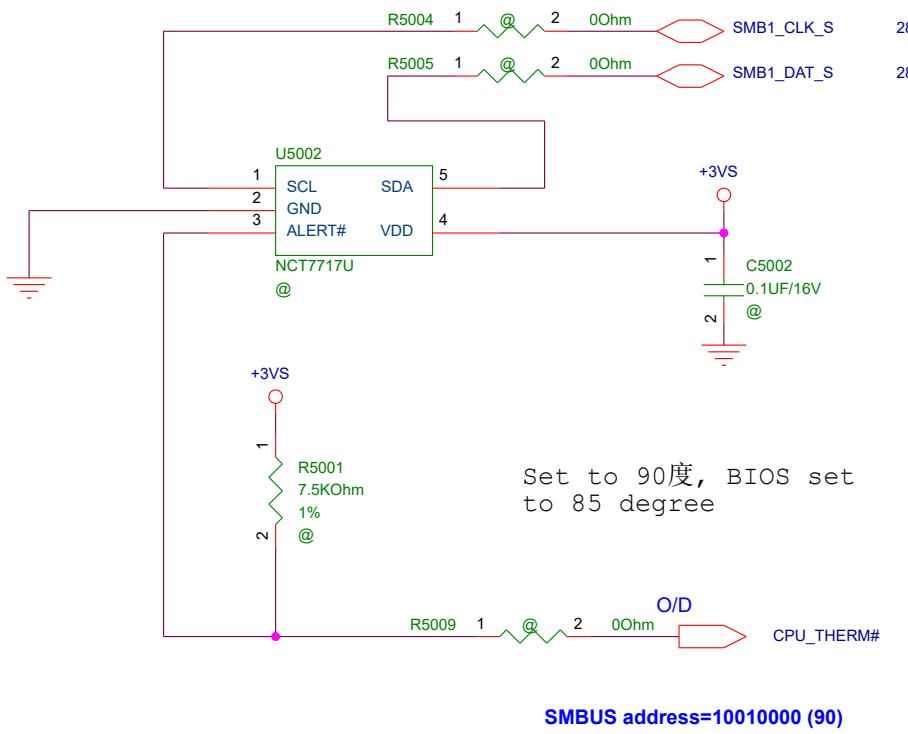


R1.1-4/13-5

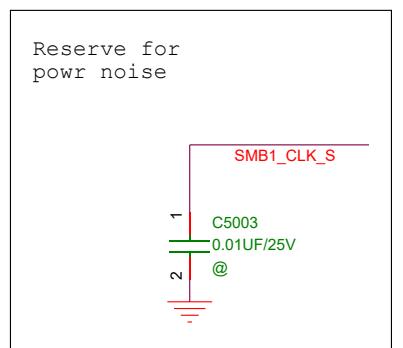
Vinifix.com



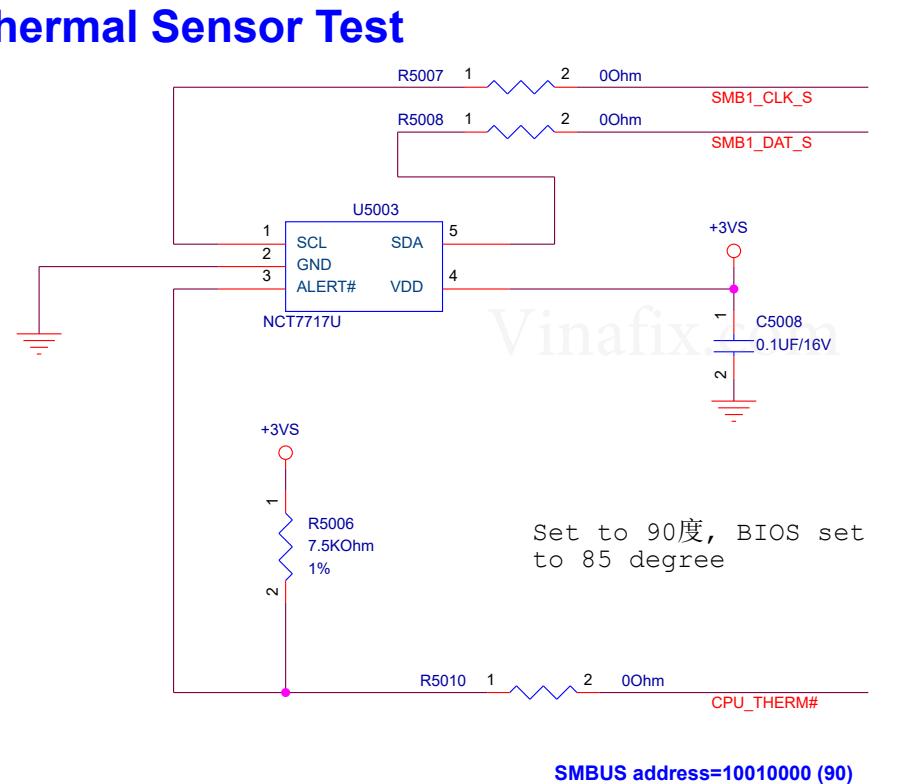
CPU Thermal Sensor



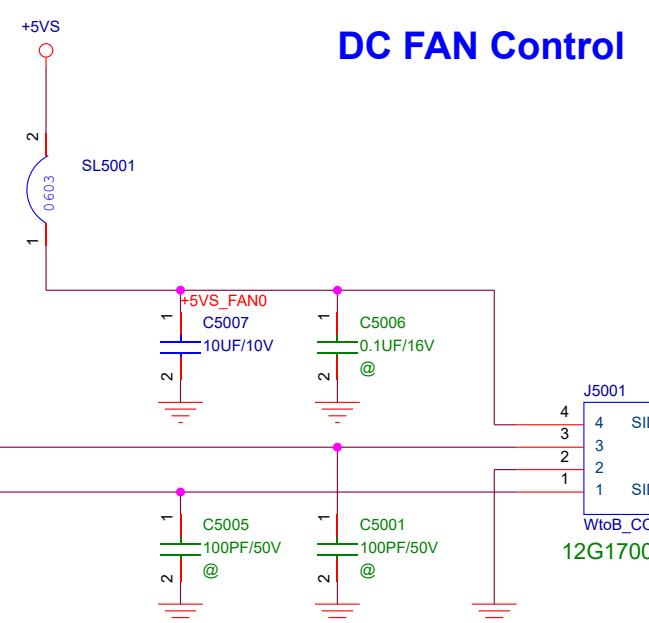
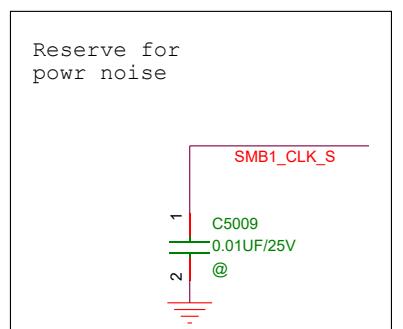
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm



R2.0-6/23-1

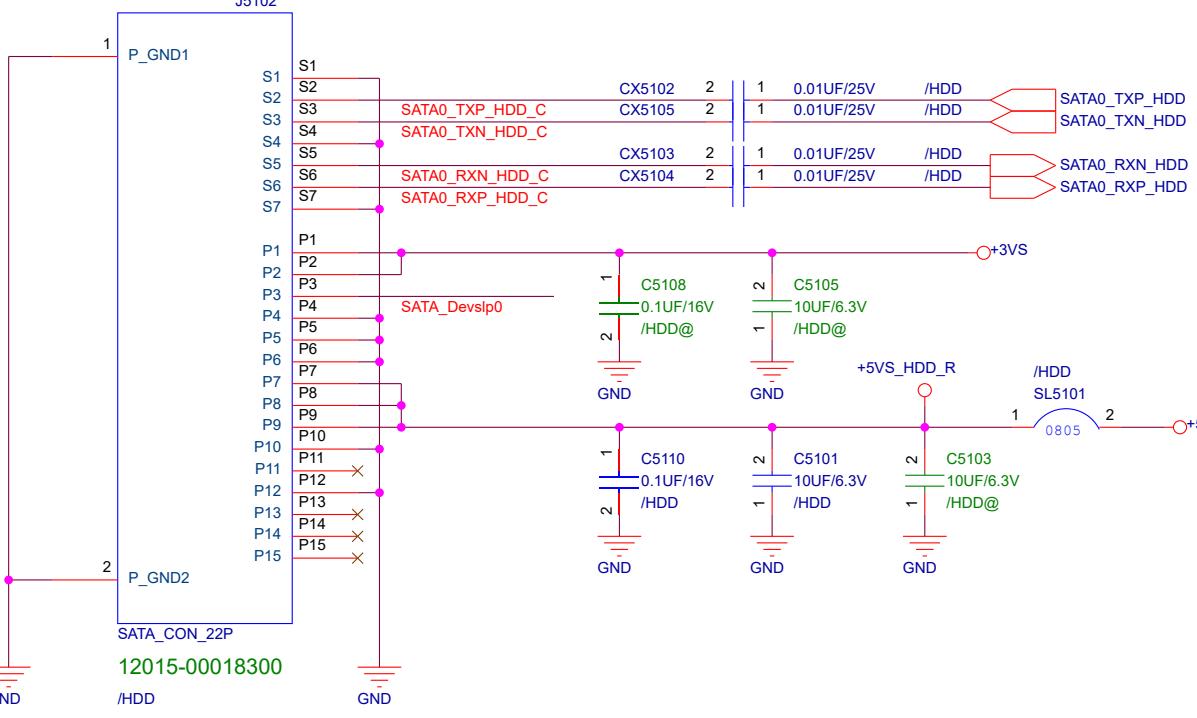


Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

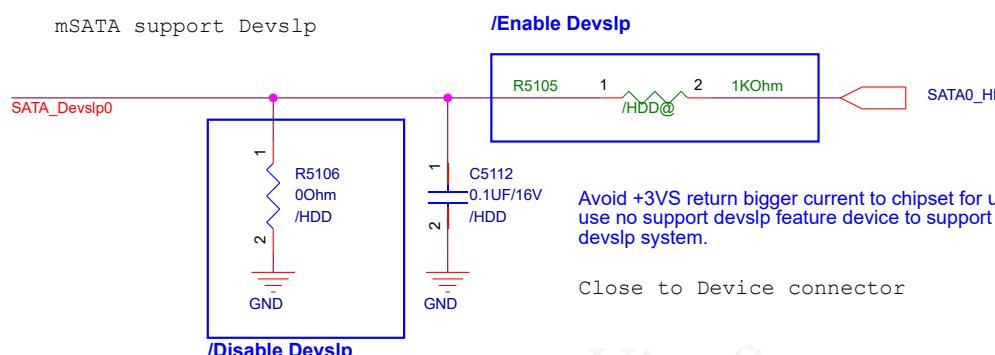


DC FAN Control

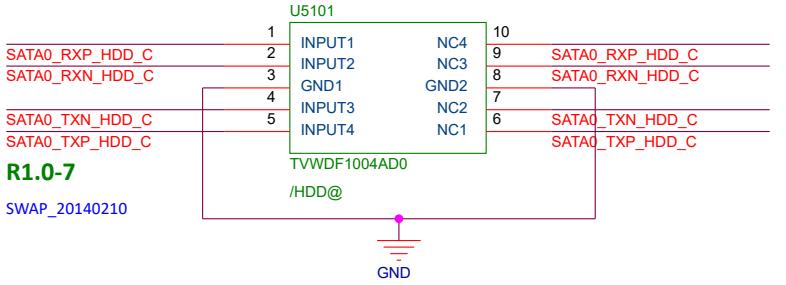
HDD



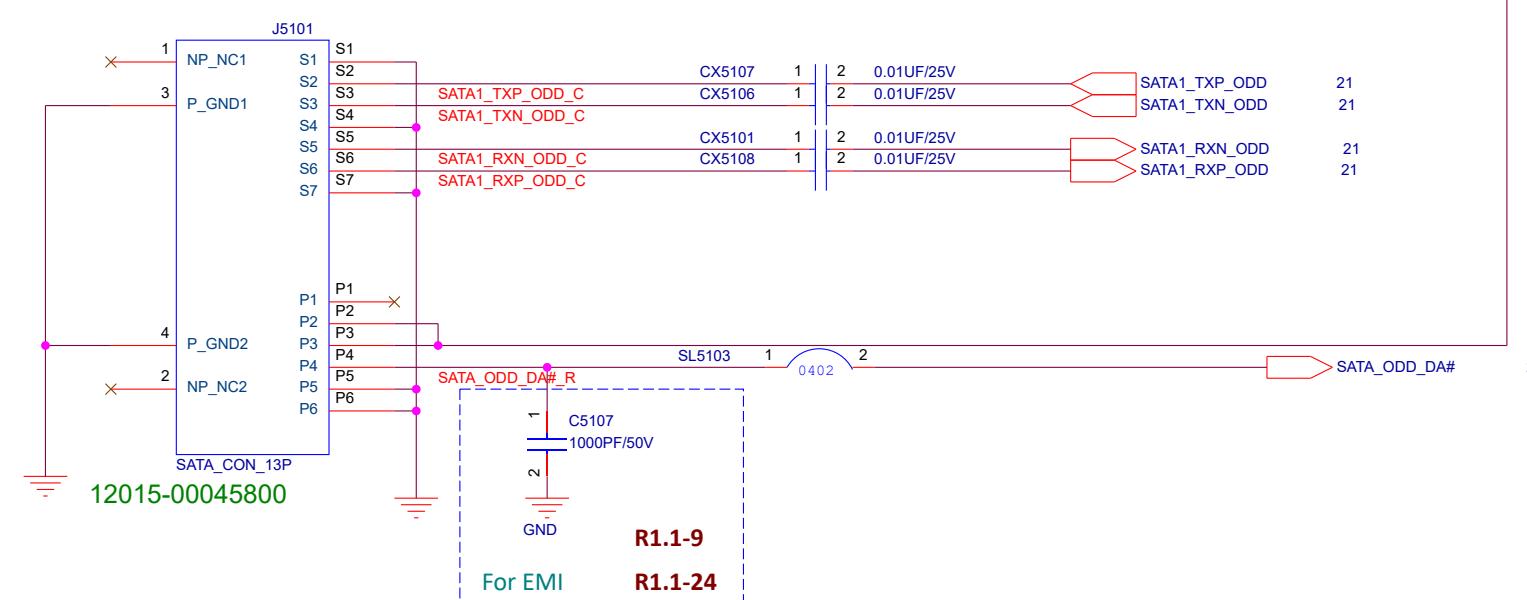
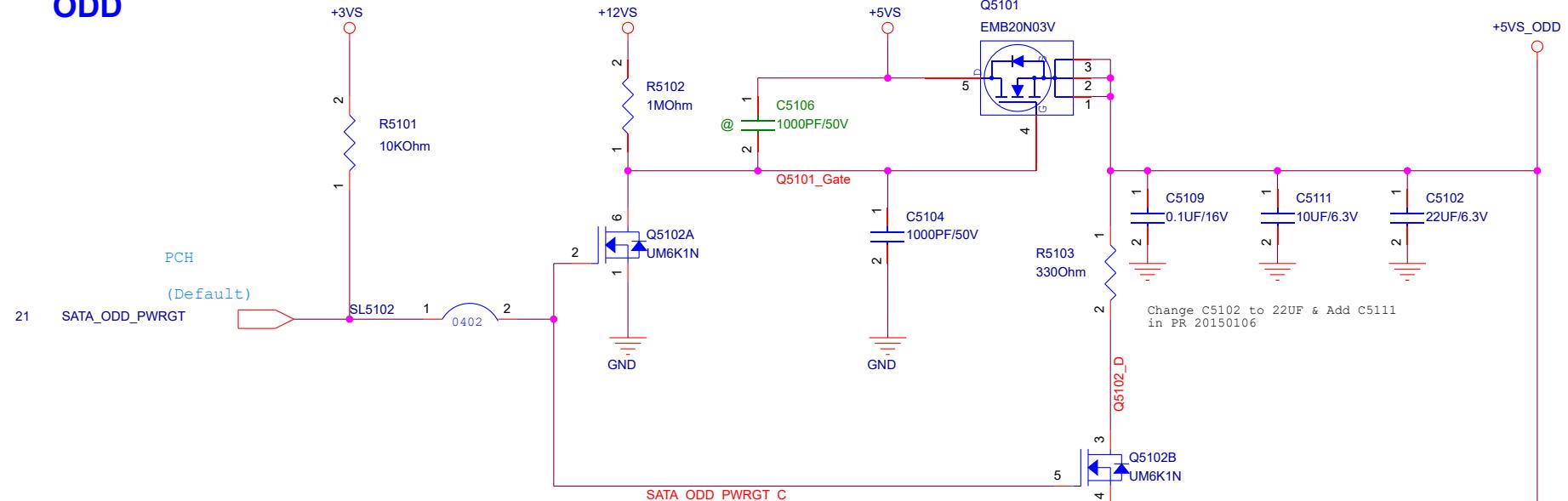
HW_Control SATA Device Sleep



For EMI



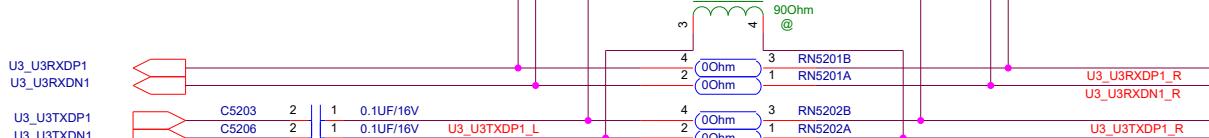
ODD



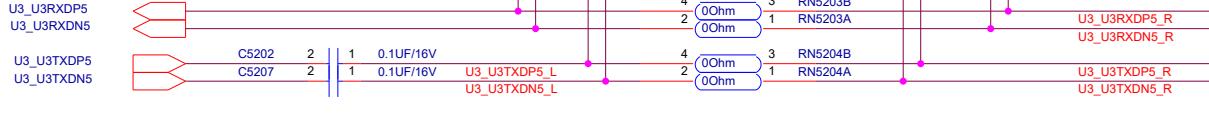
<Variant Name>

USB3.0 EMI-Protection

12/10/25
L5201, L5202, L5207, L5208
09G092090400

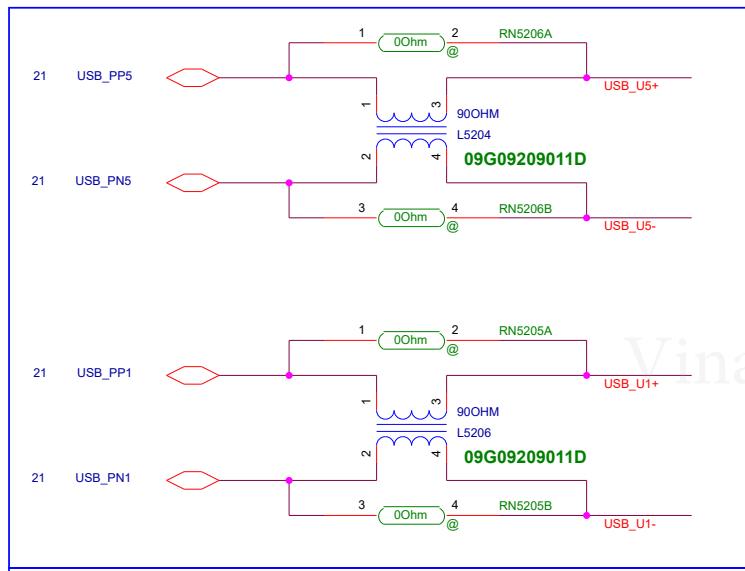


From PCH



USB2.0 EMI-Protection

R1.1-4/13-5



L5204 & L5206 C.M. CHOKE(0805)90 OHM/330mA

1st Source: P/N:09G09209011D INPAQ/MCM2012D900FBE

2nd Source: P/N:09G092090300 TAI-TECH/WCM2012F2SF-900T04

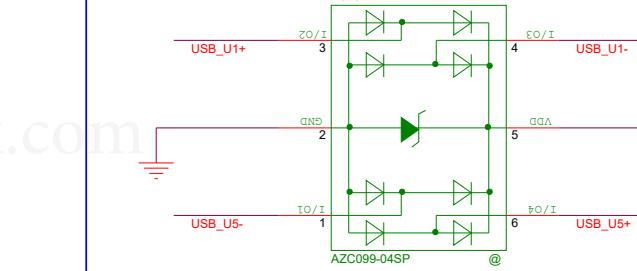
3rd Source: P/N:09G092090110 MURATA/DLW21SN900SQ2L

4th Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S

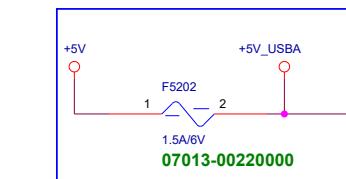
5th Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L

R1.1-4/13-5

D5201 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



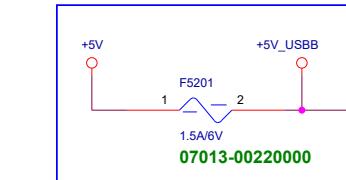
R1.1-5/11-4



R1.1-5/11-4

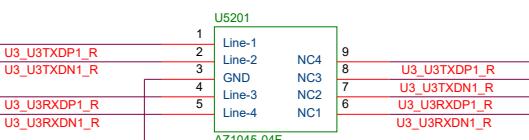
F5201, F5202 Poly Fuse
1st Source: P/N:07013-00220000 PTTC/SPR-P150
2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR

R1.1-5/11-4



USB3.0/USB 2.0 ESD-Protection

R1.1-4/13-5

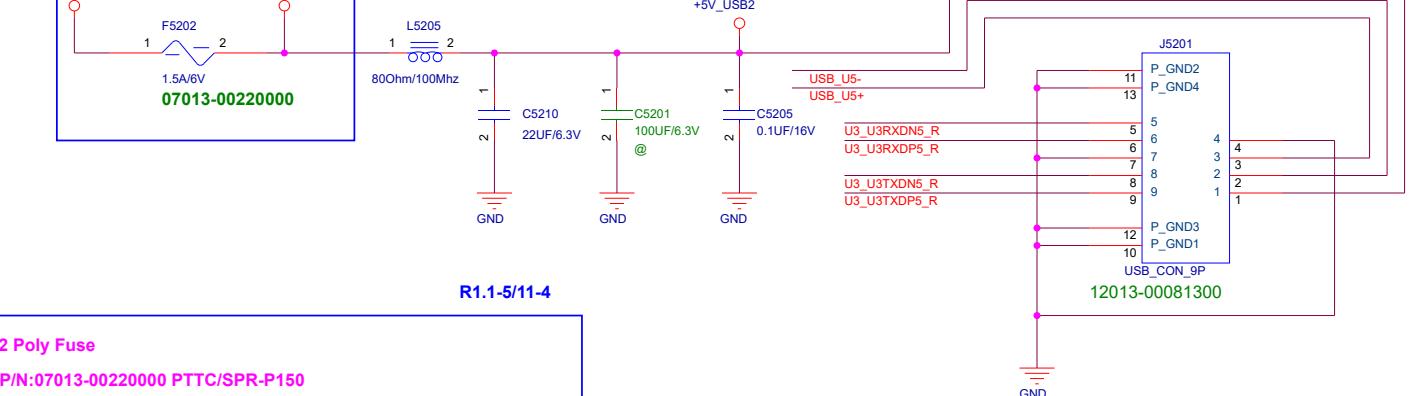


U5201 & U5203 ESD PROTECTION

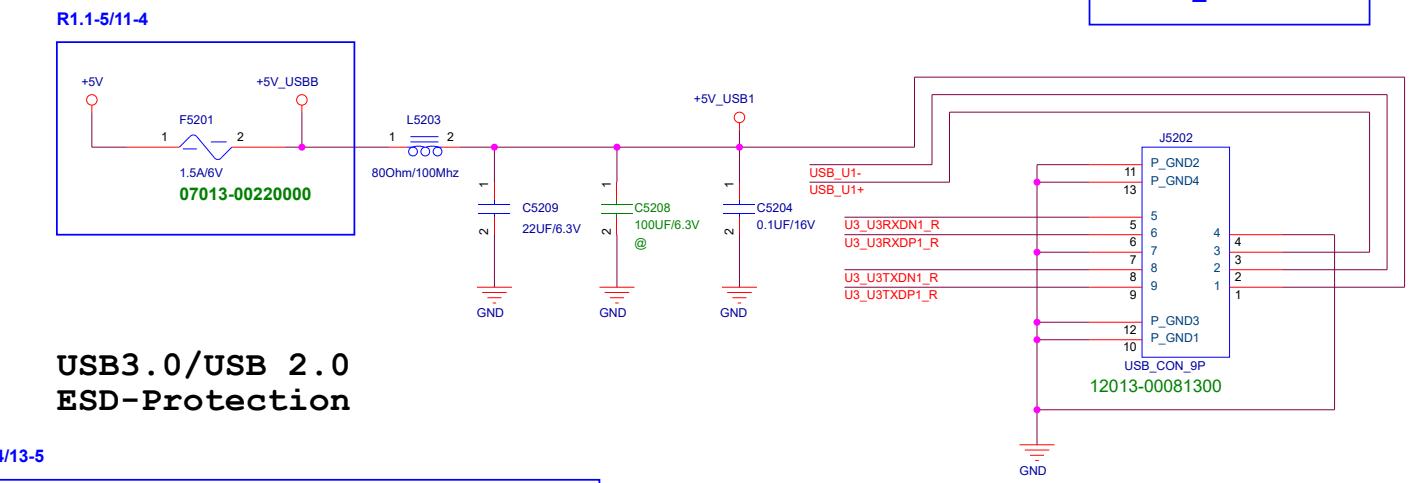
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

USB3.0_Port 2



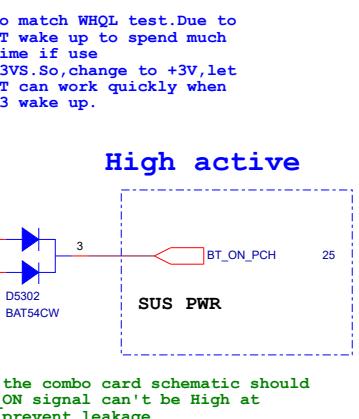
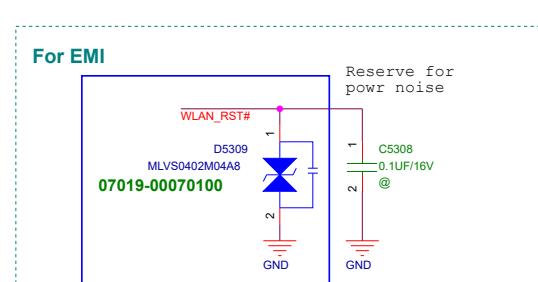
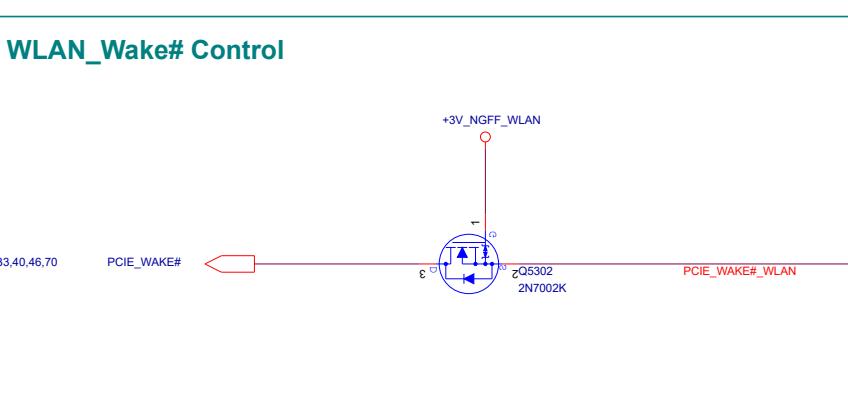
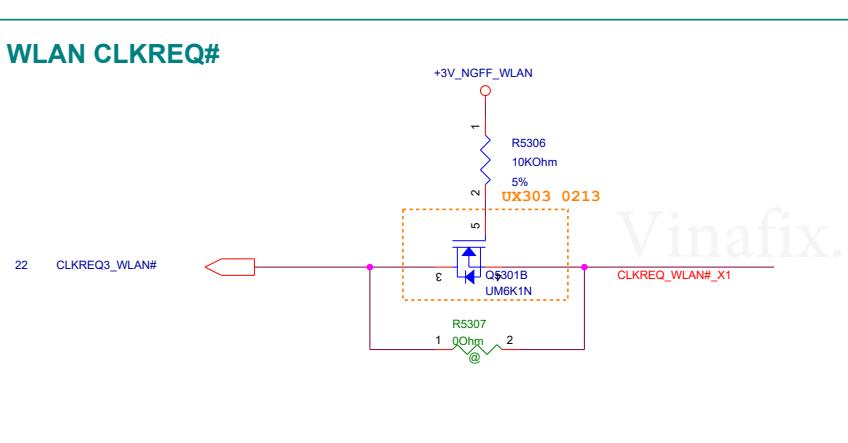
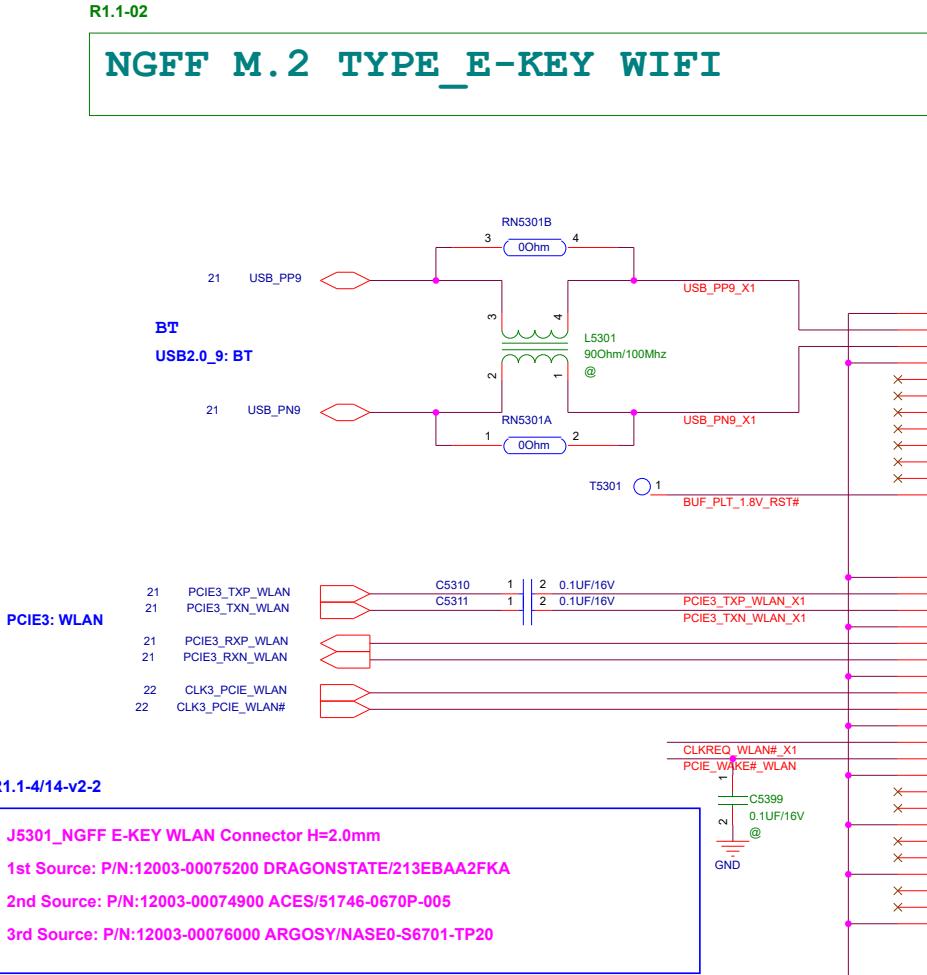
USB3.0_Port 1



<Variant Name>

ASUS®		Title : USB Port
ASUSTeK COMPUTER INC. NB1		Engineer: Mario_Jhu
Size	Project Name	
Custom	GL552VW	Rev 2.0
		Date: Tuesday, June 23, 2015
		Sheet 52 of 103

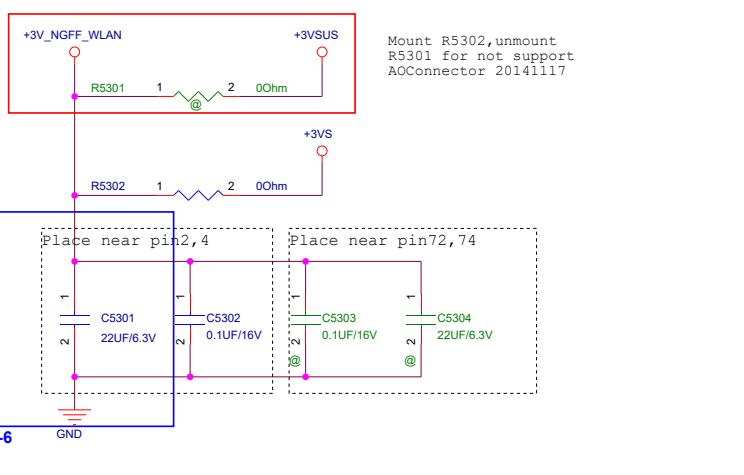
NGFF M.2 TYPE_E-KEY WIFI



WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

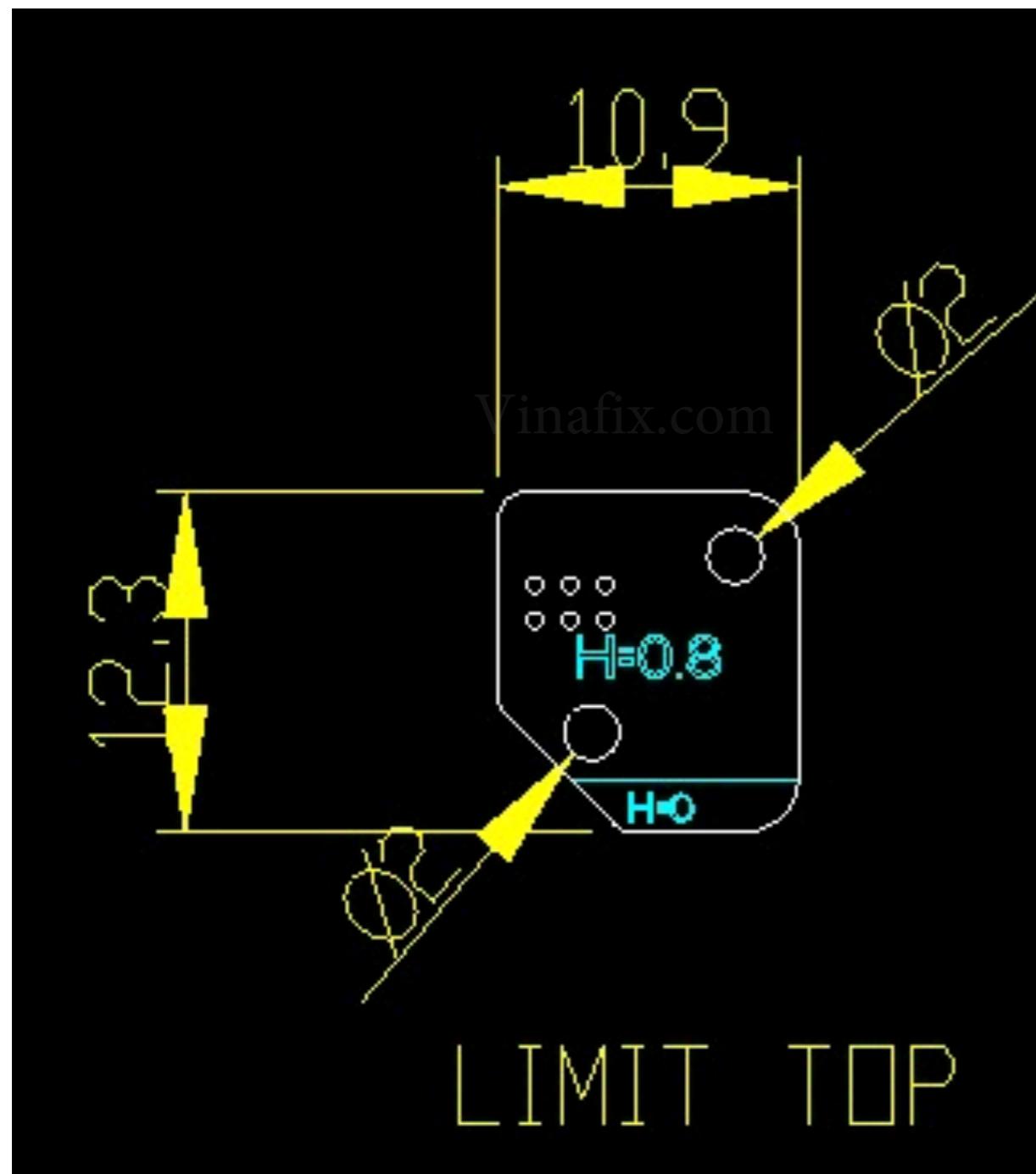
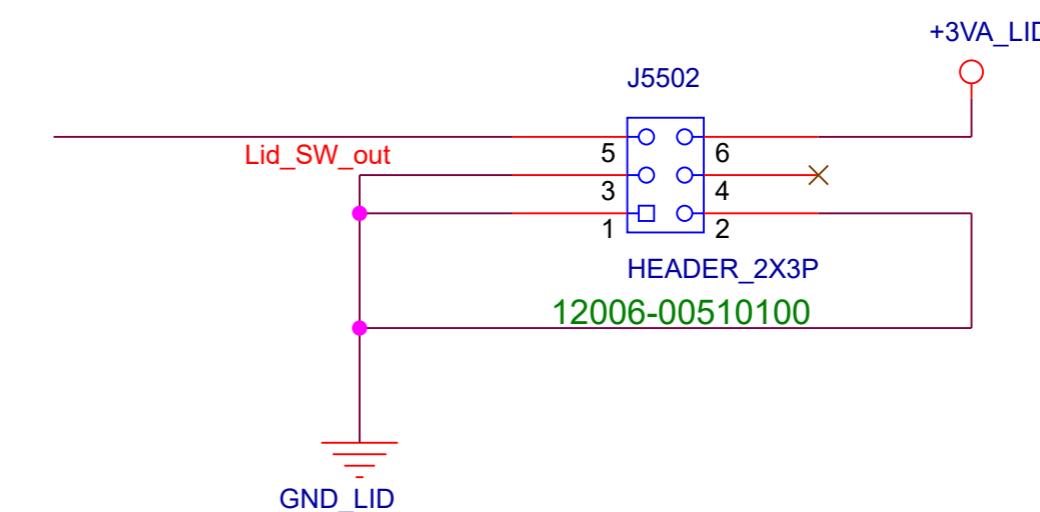
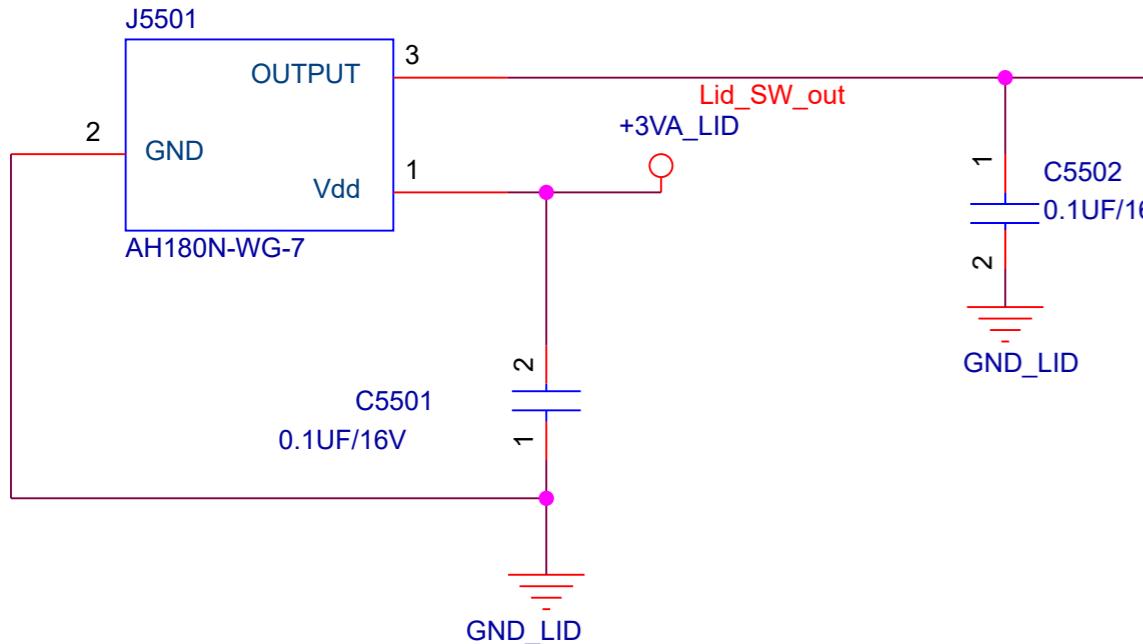
WLAN PWR to +3VSUS



74	3.3aux	GND	/5
72	3.3aux	RESERVED	71
70	RESERVED	RESERVED	69
68	RESERVED	GND	67
66	RESERVED	Reserved/2nd Lane PERn1	65
64	GPI00 NFC Reset# (MGPIO7)(O)(0/3.3V)	Reserved/2nd Lane PERp1	63
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	Reserved/2nd Lane PETn1	61
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETp1	59
58	NFC I2C SM DATA (IO)(0/3.3)	W_DISABLE#(O)(0/3.3V)	57
56	W_DISABLE#(O)(0/3.3V)	PEWake#(IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	CLKREQ#(IO)(0/3.3V)	53
52	PERST#(O)(0/3.3V)	PERST#(O)(0/3.3V)	51
50	SUSCLK(32kHz)(O)(0/3.3V)	SUSCLK(32kHz)(O)(0/3.3V)	49
48	COEX1(?)@1.8V	REFCLK0	47
46	COEX2(?)@1.8V	PERn0	45
44	COEX3(?)@1.8V	PERp0	43
42	CLink CLK	GND	41
40	CLink DATA	PERn0	39
38	CLink RESET (O)(0/3.3V)	PERp0	37
36	UART CTS (O)(0/1.8V)	PETn0	35
34	UART RTS (I)(0/1.8V)	PETp0	33
32	UART Tx (O)(0/1.8V)	GND	Key
	Key	Key	Key
	Key	Key	Key
22	UART Rx (I)(0/1.8V)	SDIO Rx(O)(0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake (I)(0/1.8V)	21
18	GND	SDIO DA2(I)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DA2T(I)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(I)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DATA(I)(0/1.8V)	13
10	PCM_SYNC (O)(0/1.8V)	SDIO CMD(I)(0/1.8V)	11
8	PCM_CLK (O)(0/1.8V)	SDIO CLK(I)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3aux	USB_D-	5
2	3.3aux	USB_D+	3
		GND	1

LID Switch

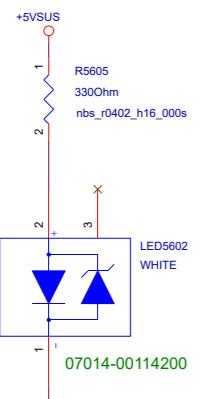
Vinifix.com



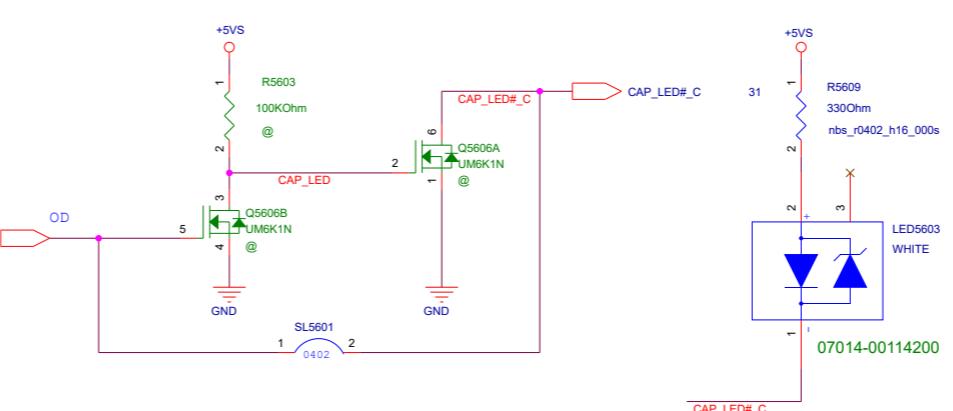
<Variant Name>

	Title : Lid_SW_BD
ASUSTeK COMPUTER INC. NB1	Engineer: Mario_Jhu
Size A	Project Name GL552VW
Rev 2.0	
Date: Tuesday, June 23, 2015	Sheet 55 of 103

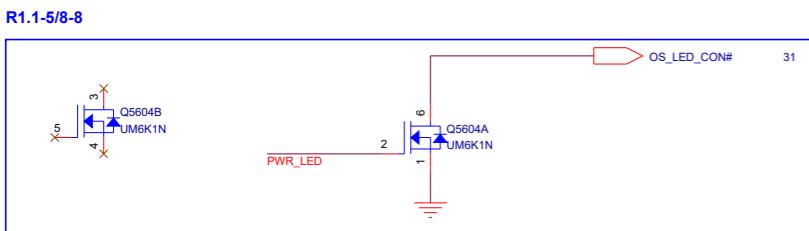
POWER LED



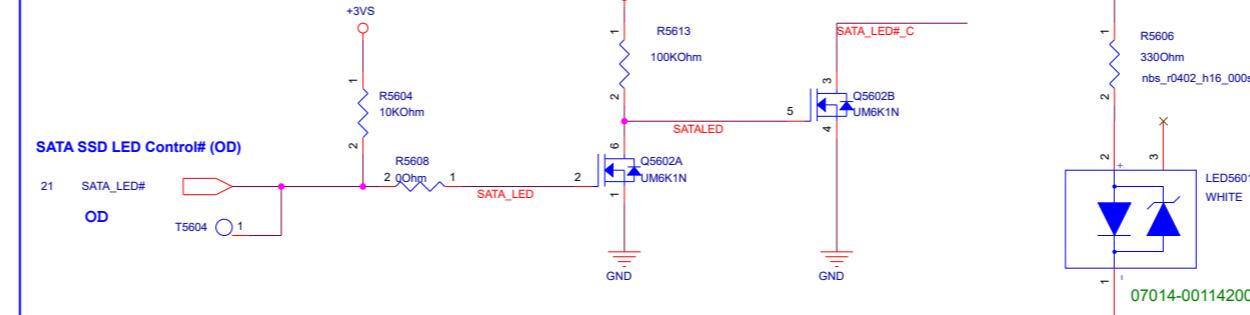
CAP LED



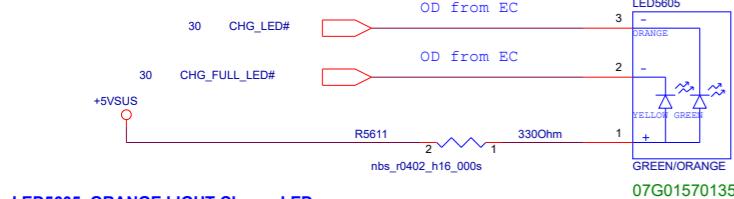
OS_LED#



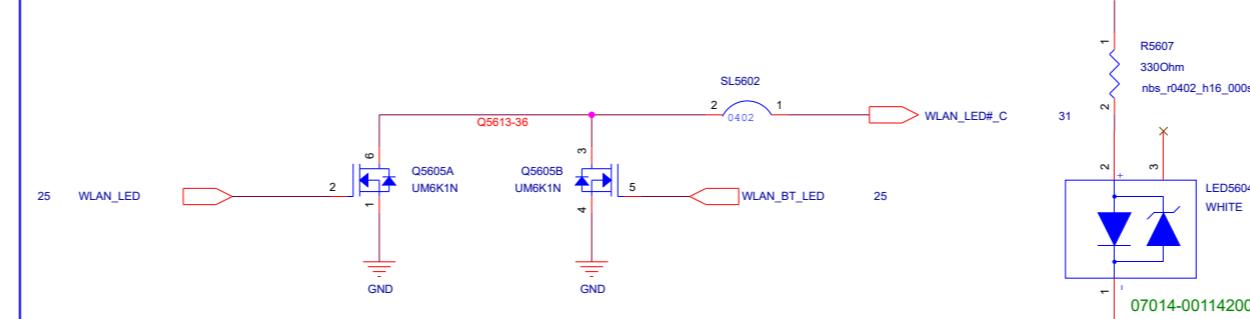
HDD LED



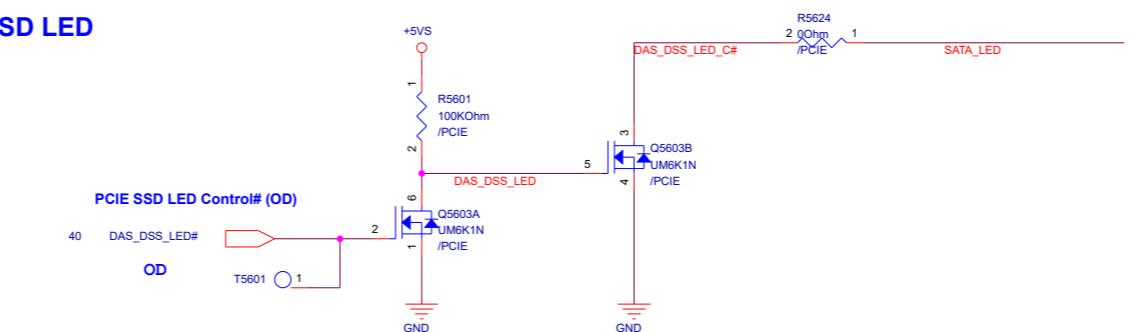
Charger LED



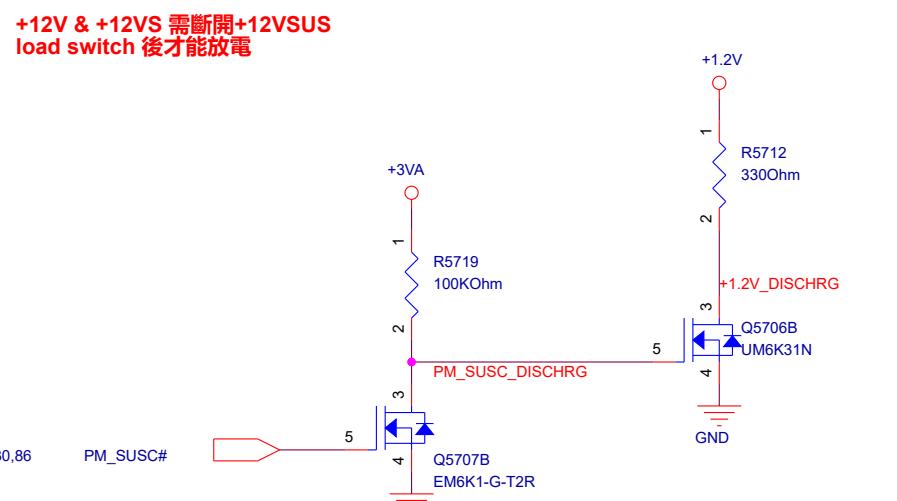
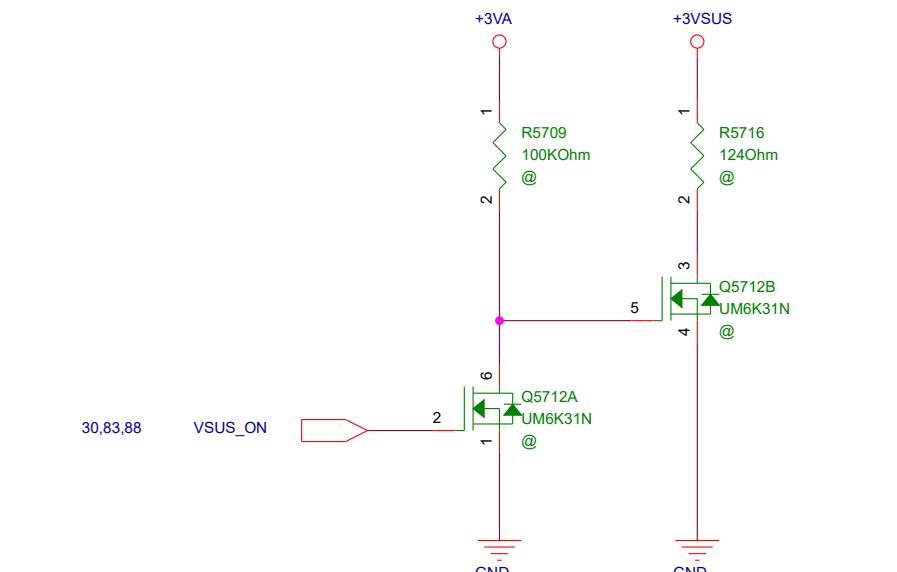
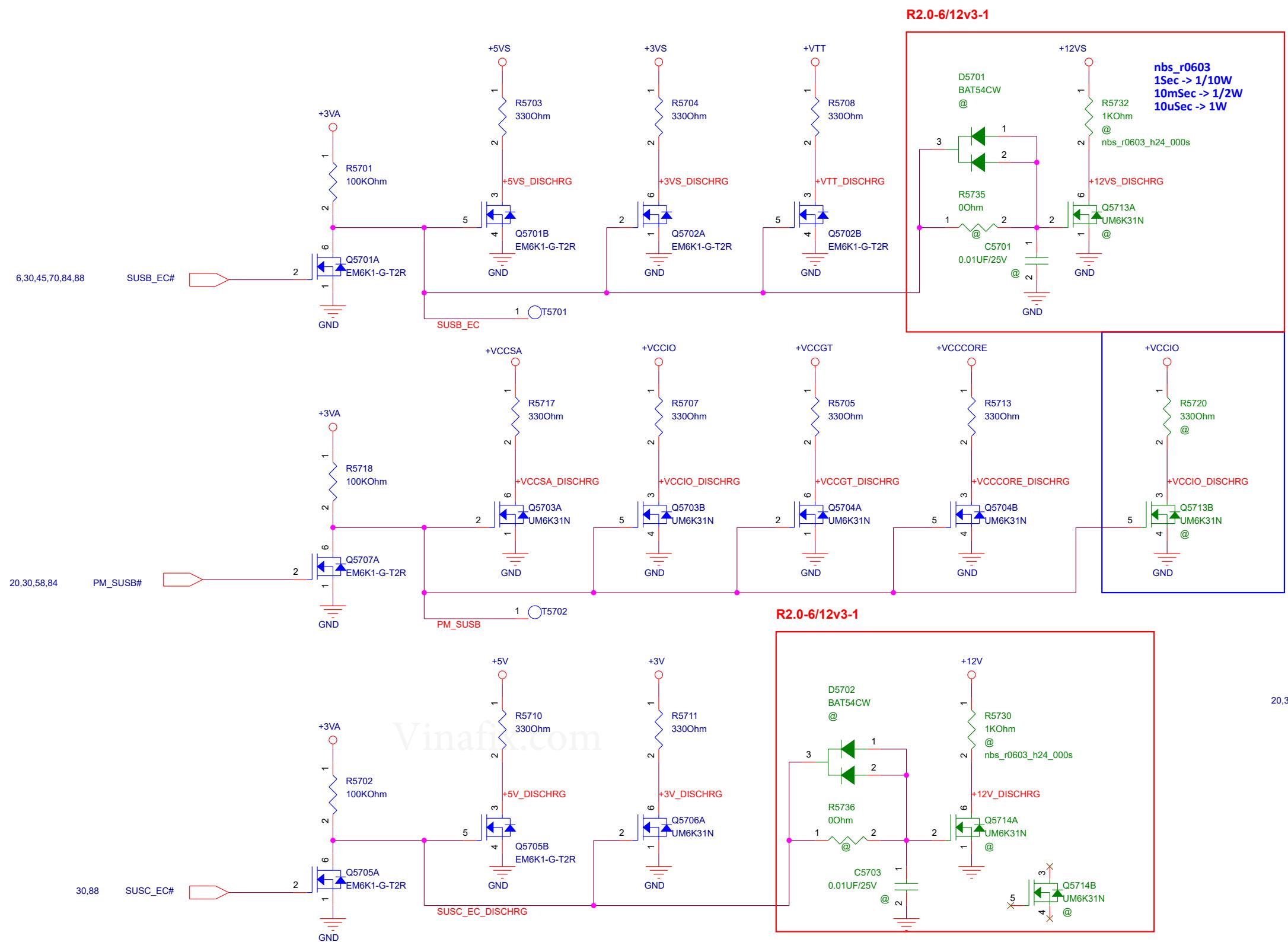
WireLess/BT LED

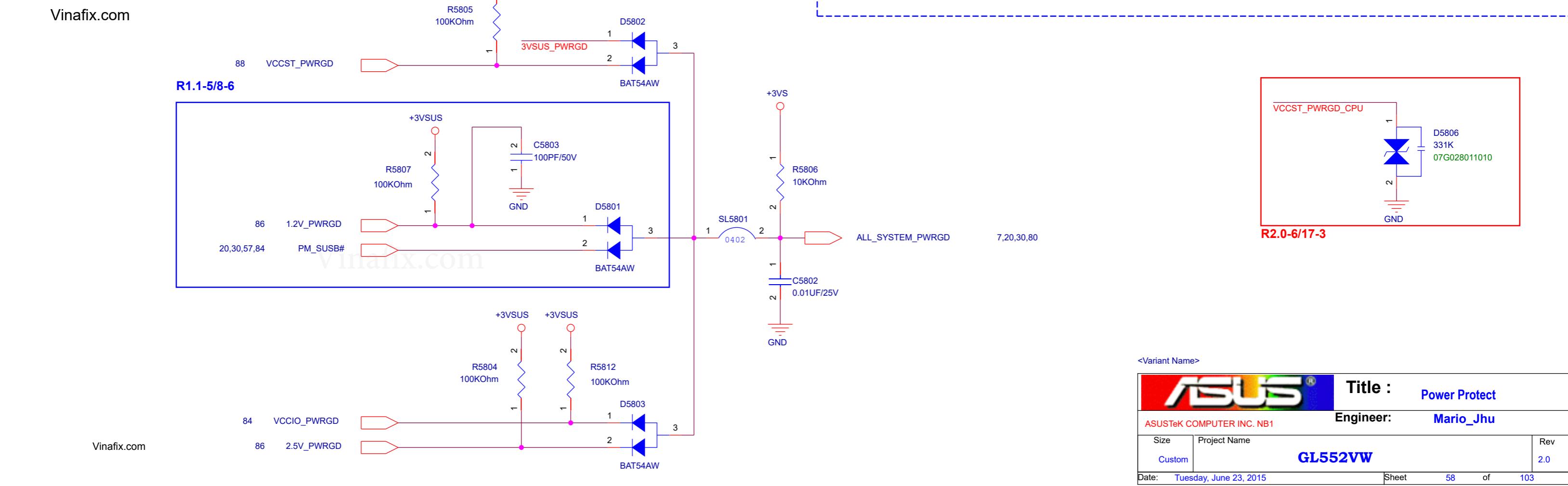
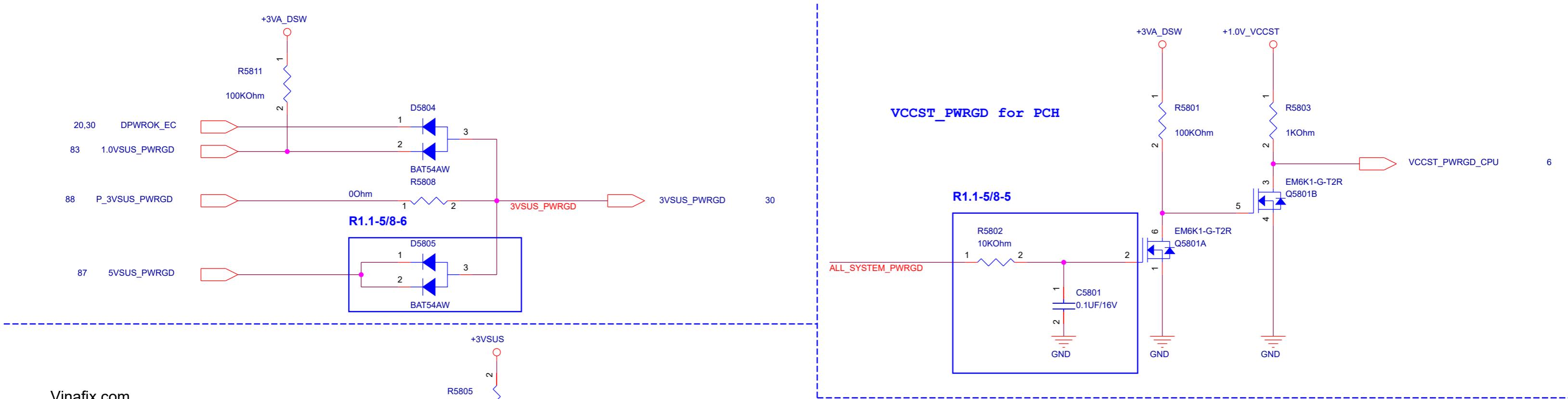


SSD LED



<Variant Name>





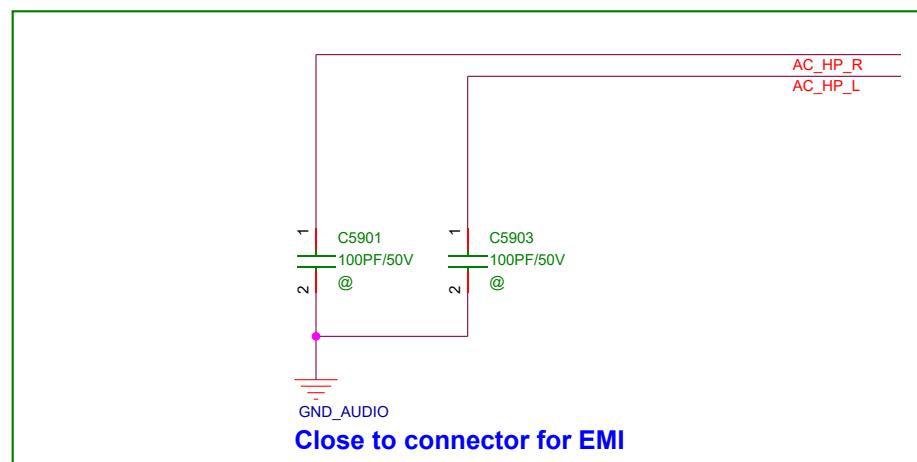
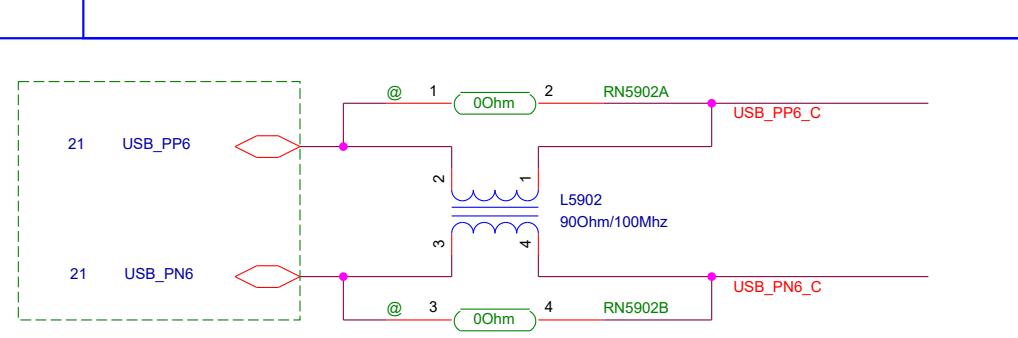
To I/O Board

R1.1-5/11-3

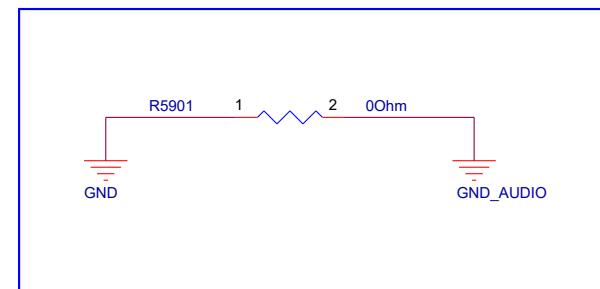
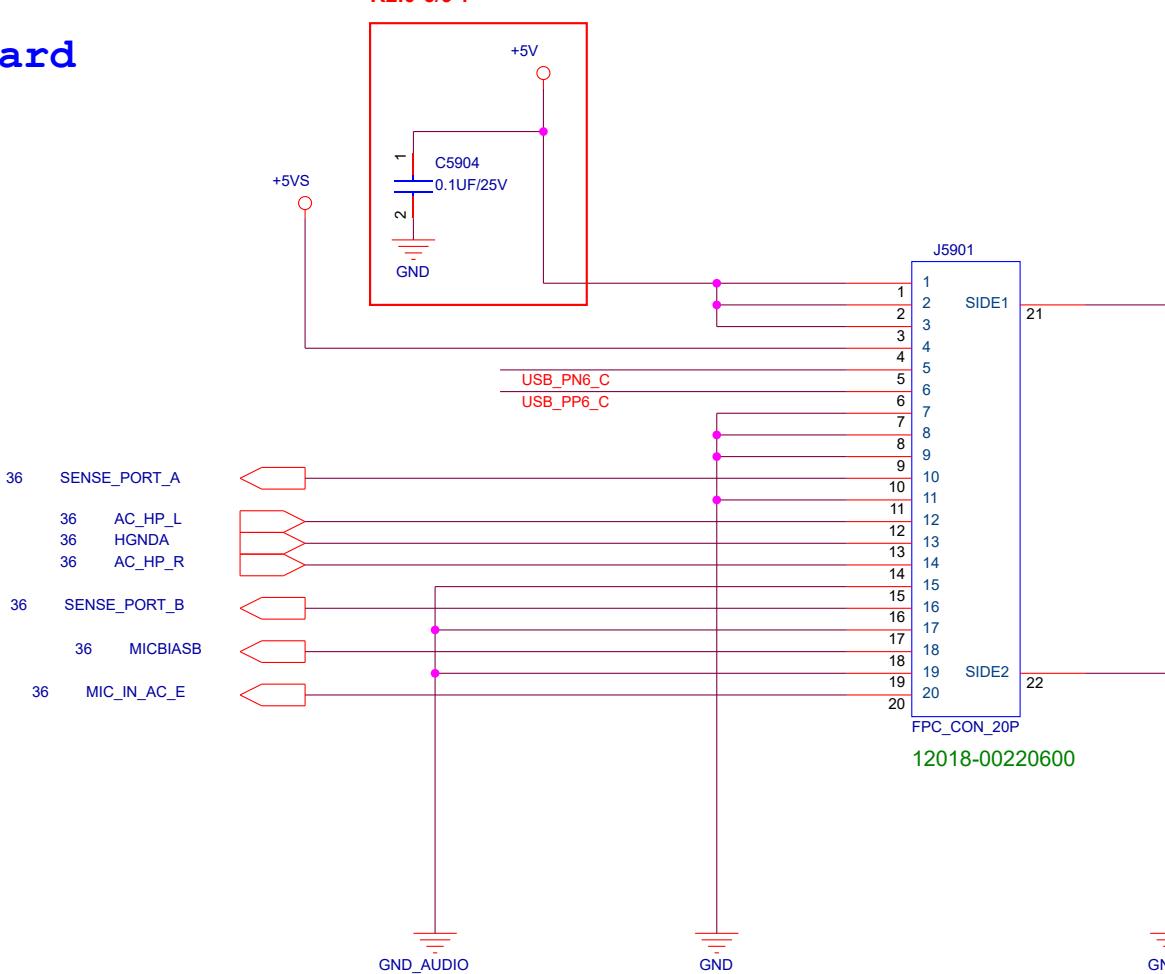
L5902 Choke

1st Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L <G>

2nd Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S <G>



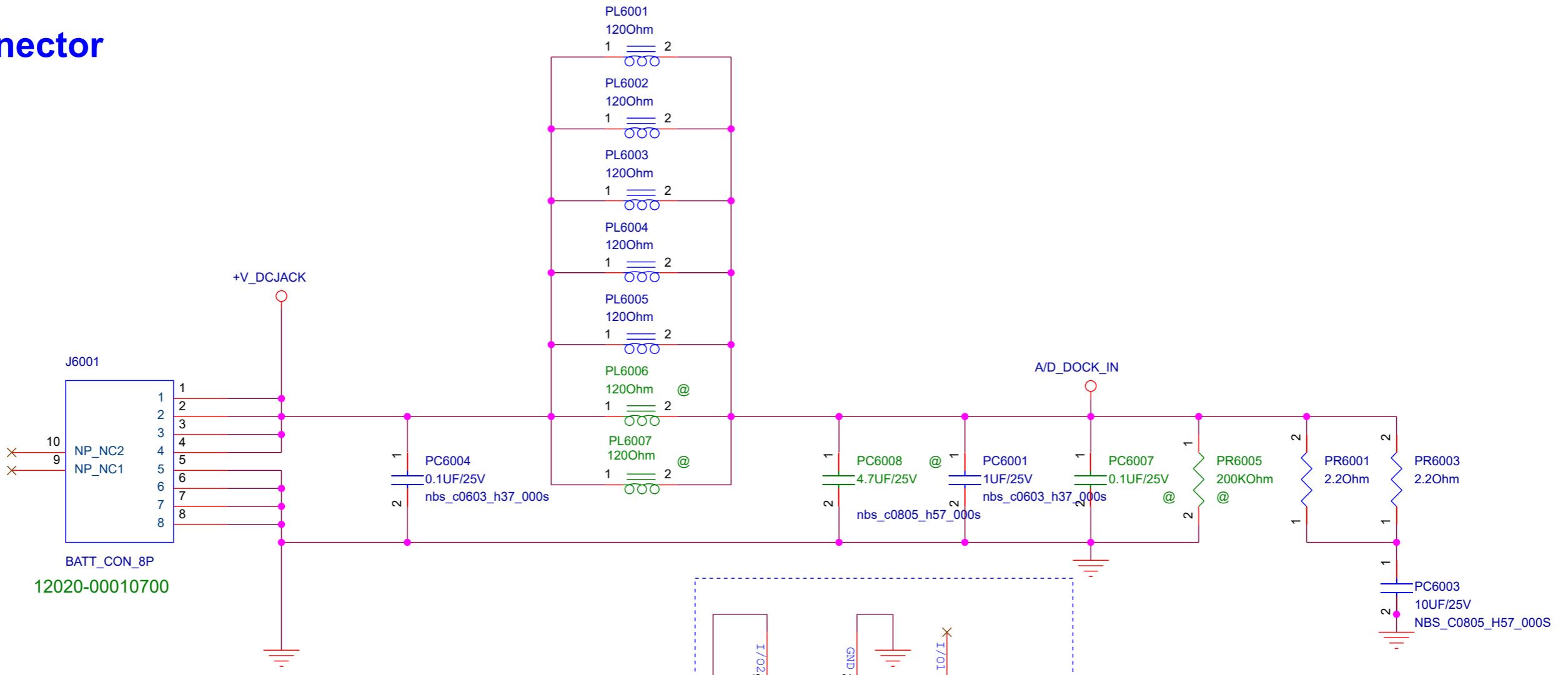
R2.0-6/9-7



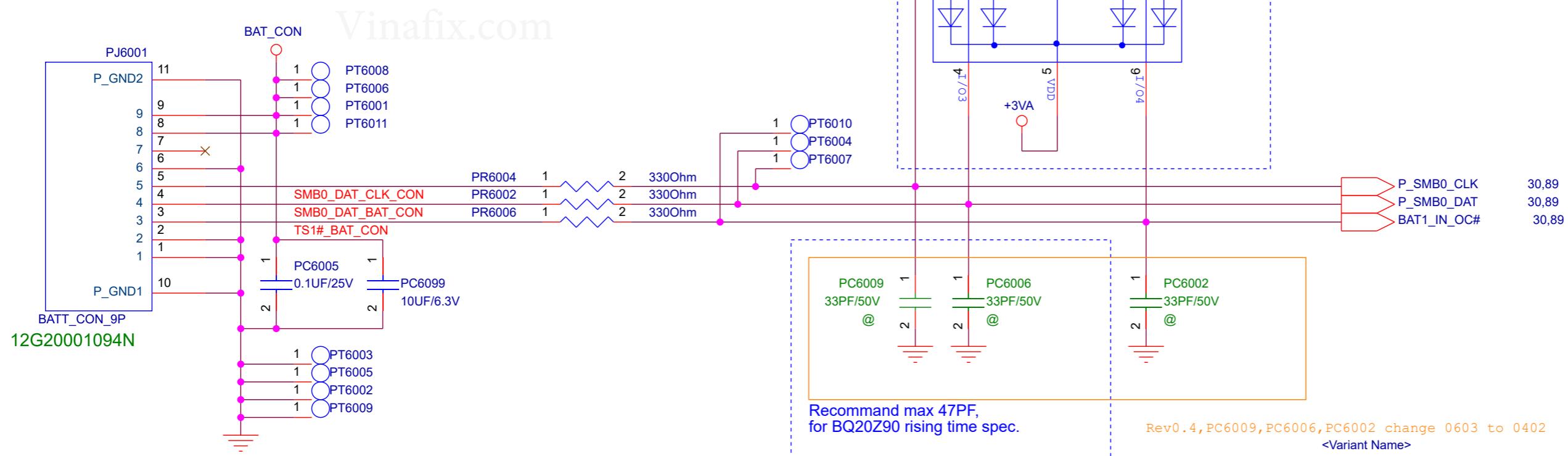
R1.1-5/11-3

Vinafix.com

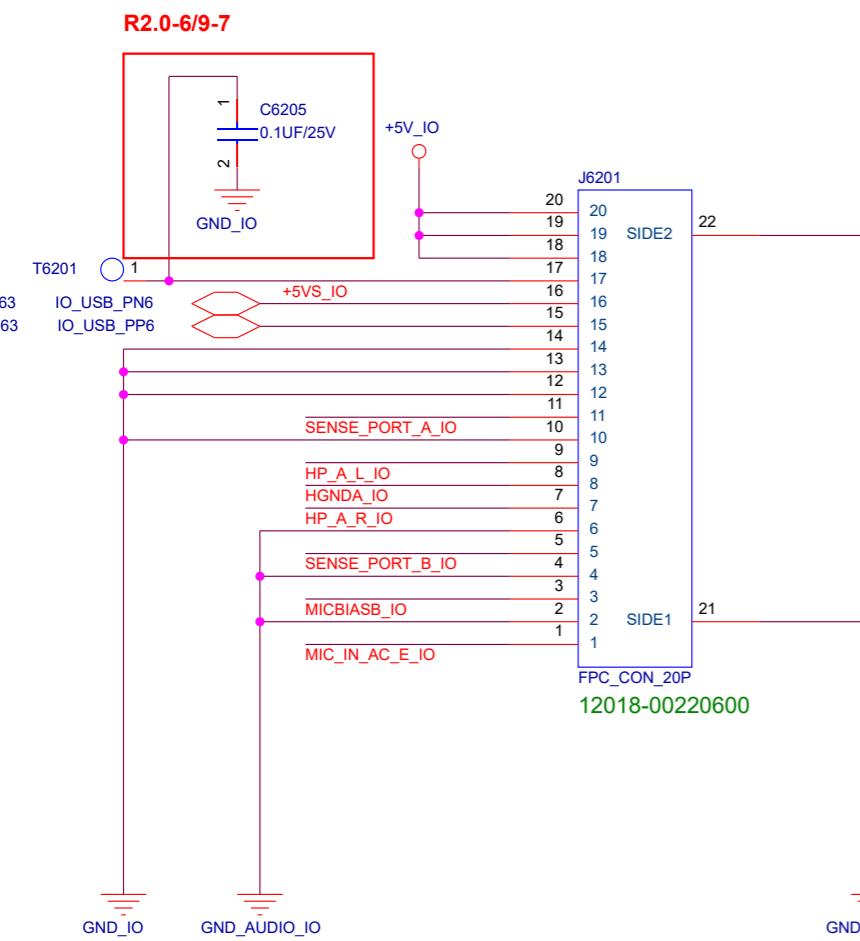
DC-IN Connector



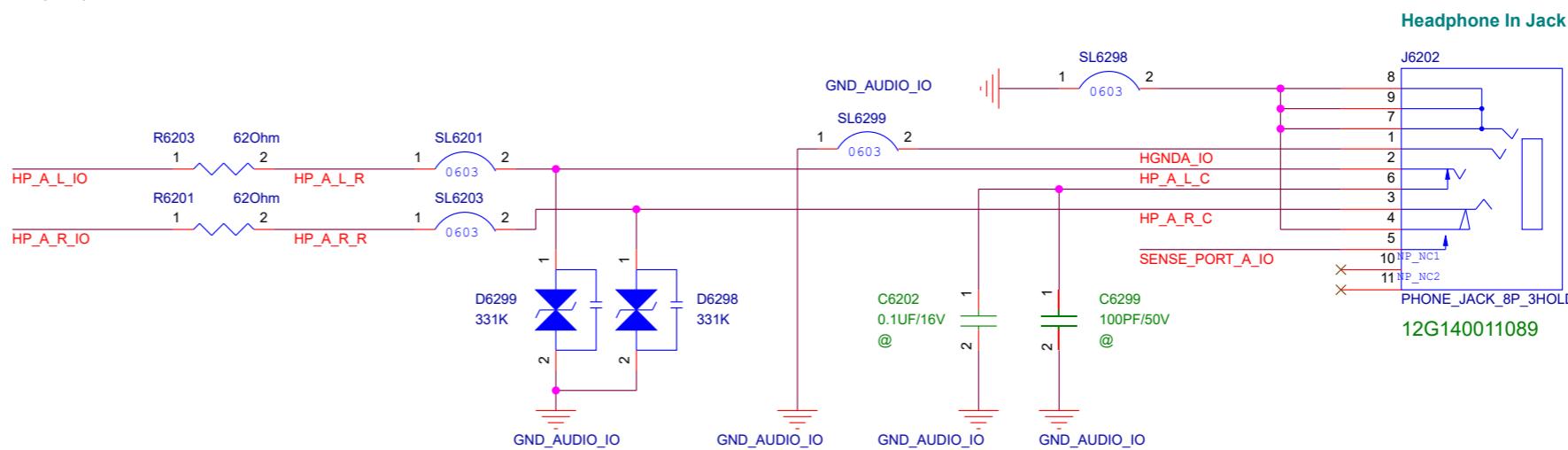
Battery Connector



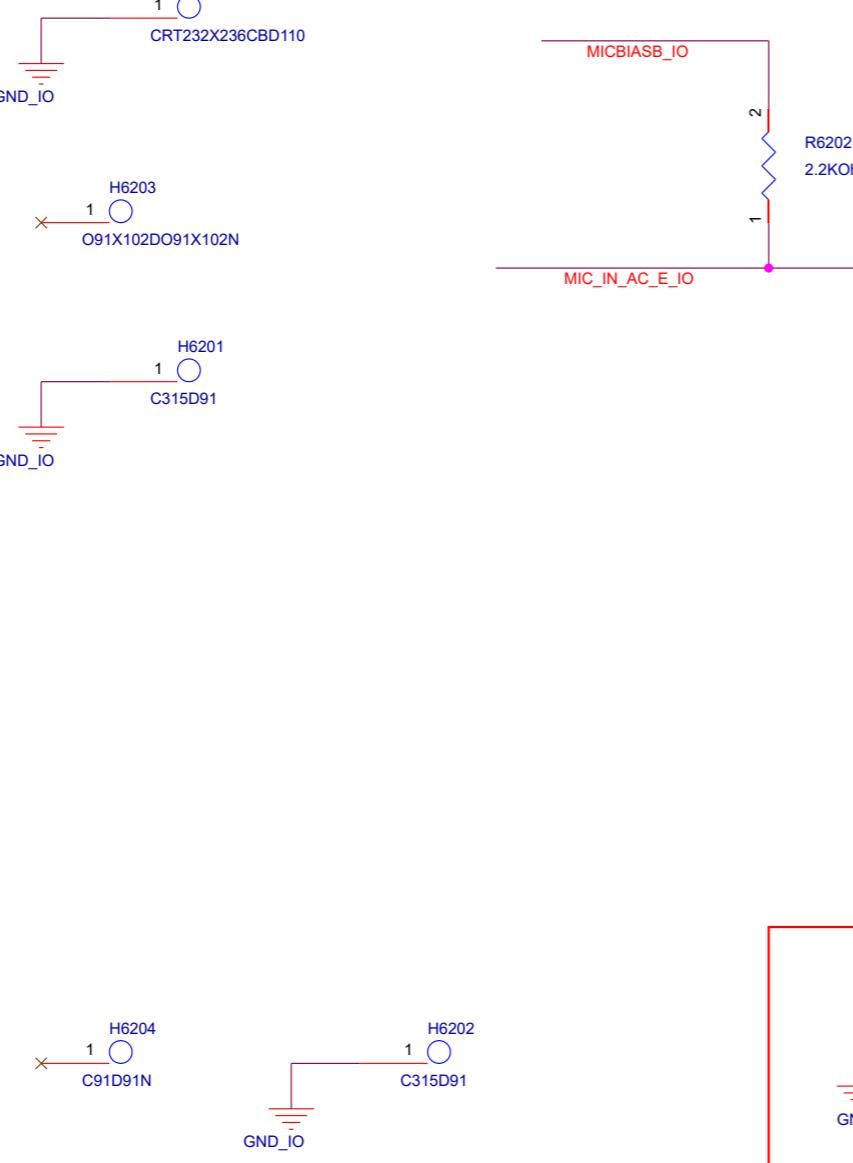
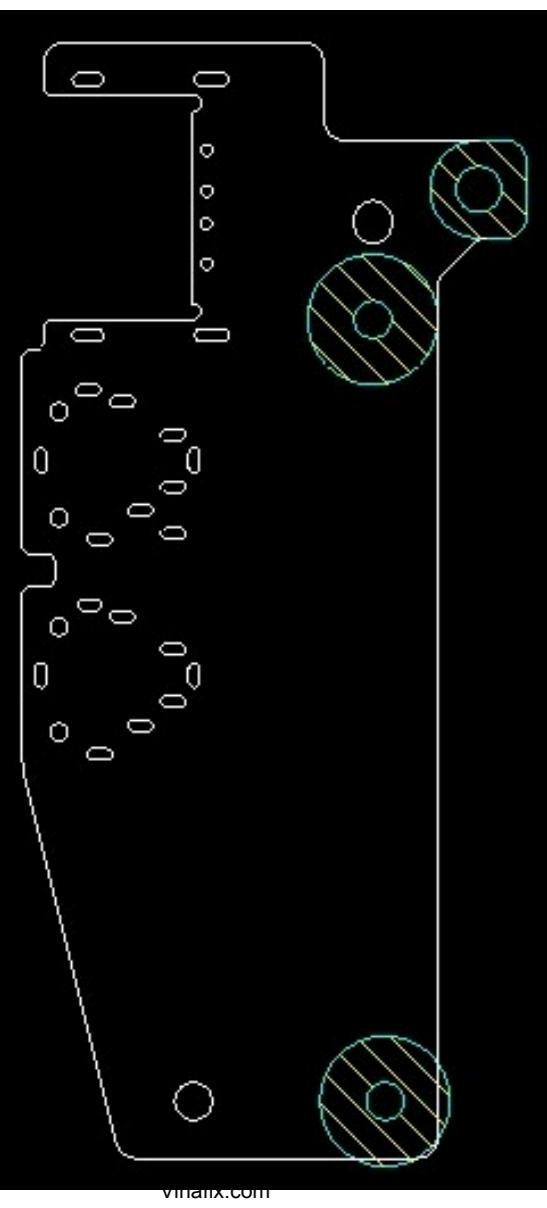
081111 -> 090604:
1. Change PD6001 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.
Vinafix.com



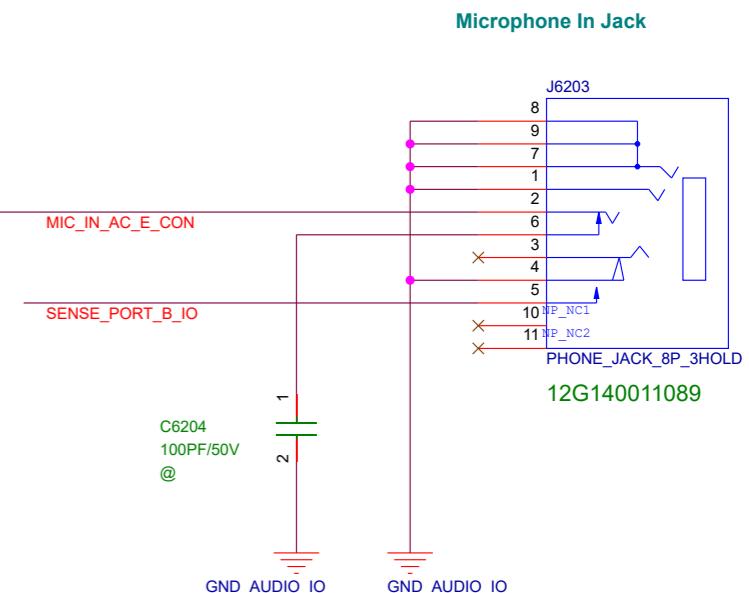
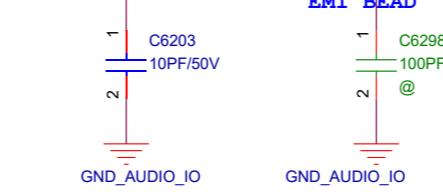
Change to 07g005000313
SR2 20141027



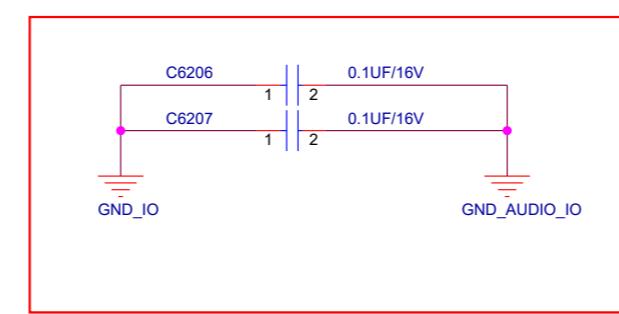
EXTERNAL MICROPHONE



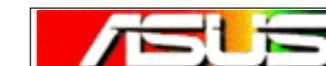
E



R2.0-6/22-3



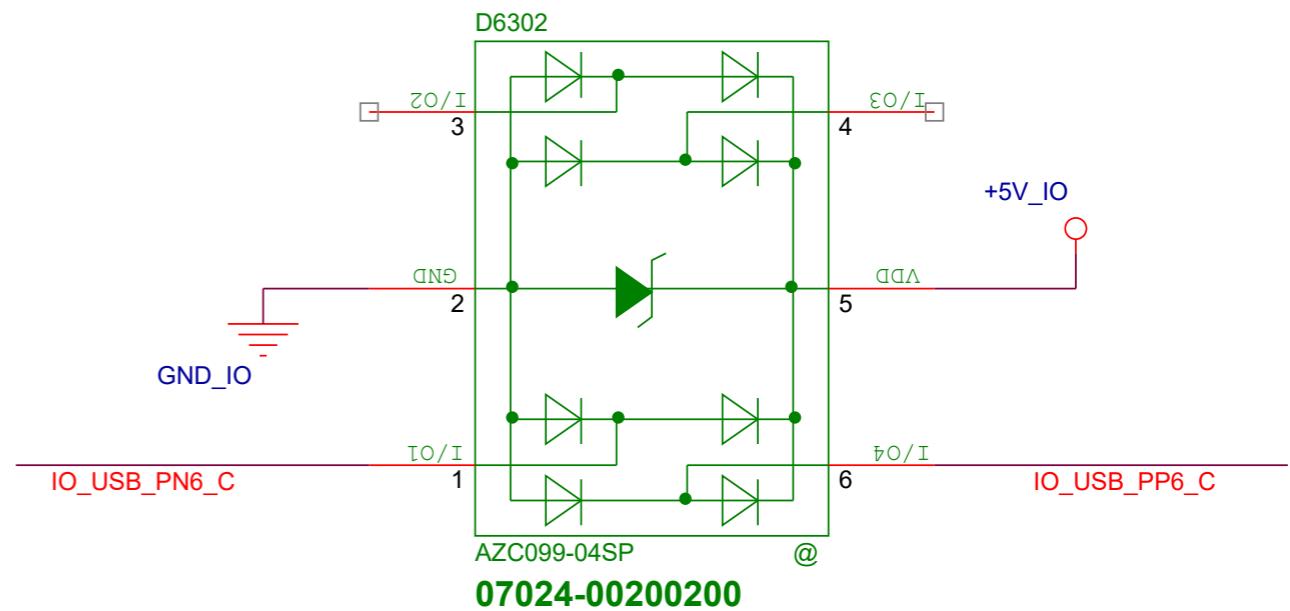
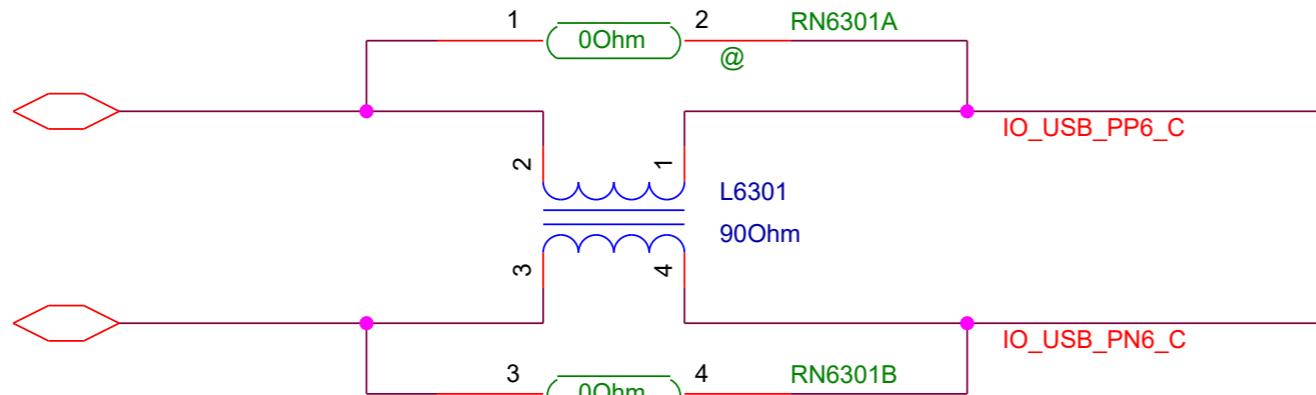
<Variant Name>



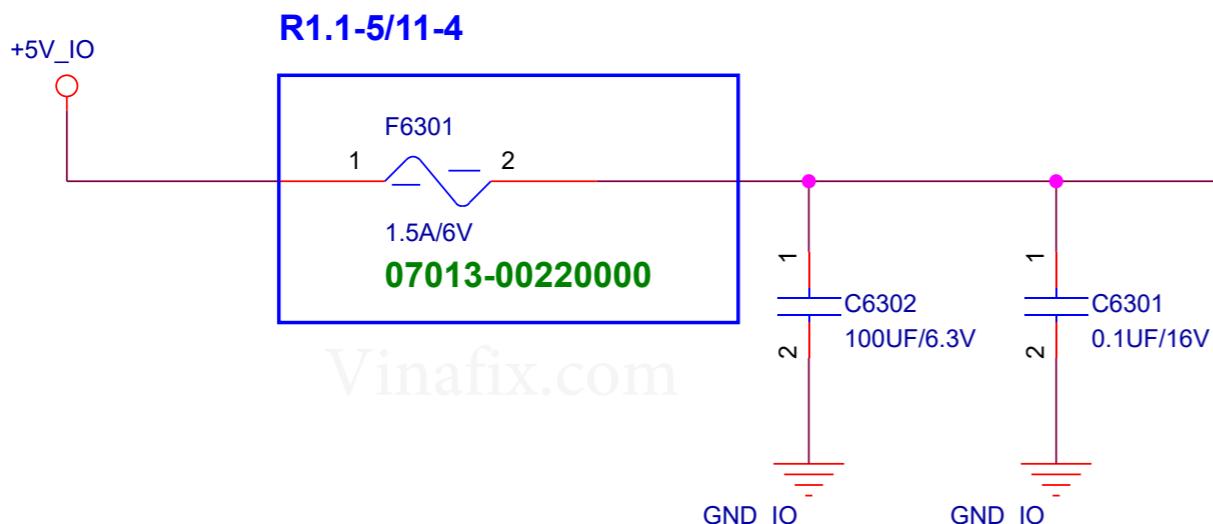
Title : I/O board(1) MIC/HP

Engineer: Mario Jhu

ASUSTEK COMPUTER INC. NDT			
Size Custom	Project Name GL552VW		Rev 2.0
Date: Tuesday, June 23, 2015	Sheet	62	of 103



USB2.0_Port 3



R1.1-5/11-4

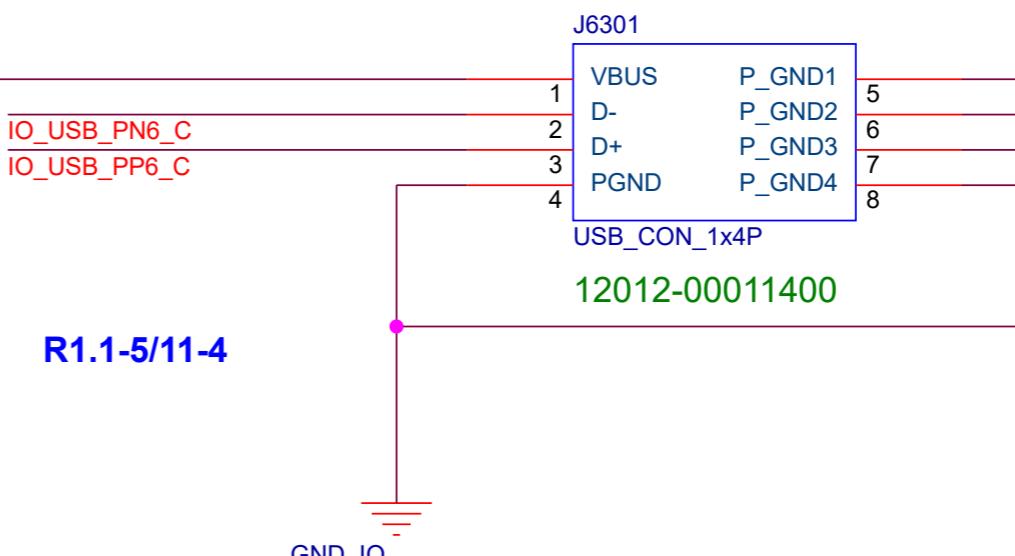
F6301 Poly Fuse
1st Source: P/N:07013-00220000 PTTC/SPR-P150
2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR

R1.1-4/13-5

D6302 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



R1.1-5/11-4

<Variant Name>

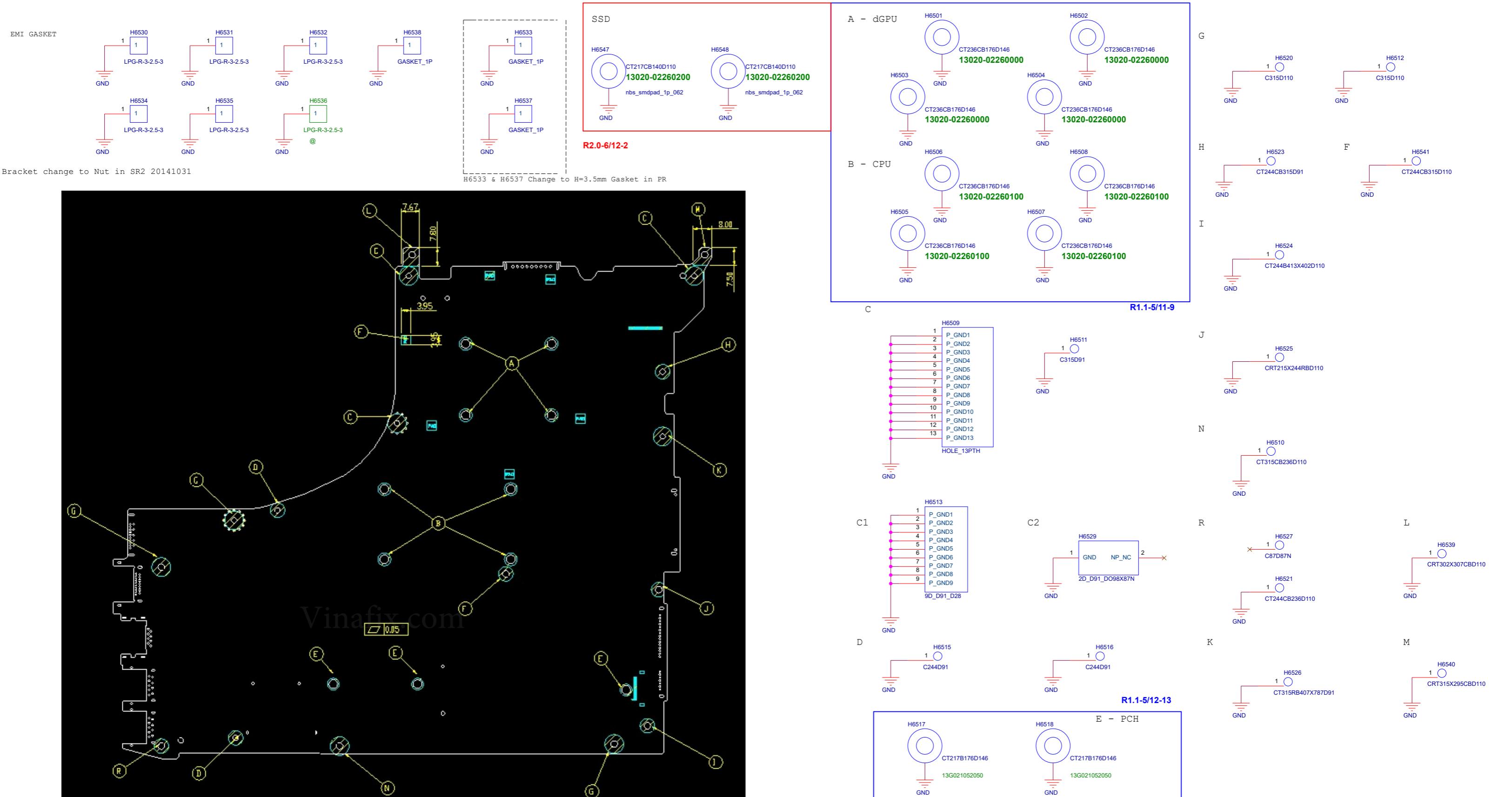


ASUSTeK COMPUTER INC. NB1

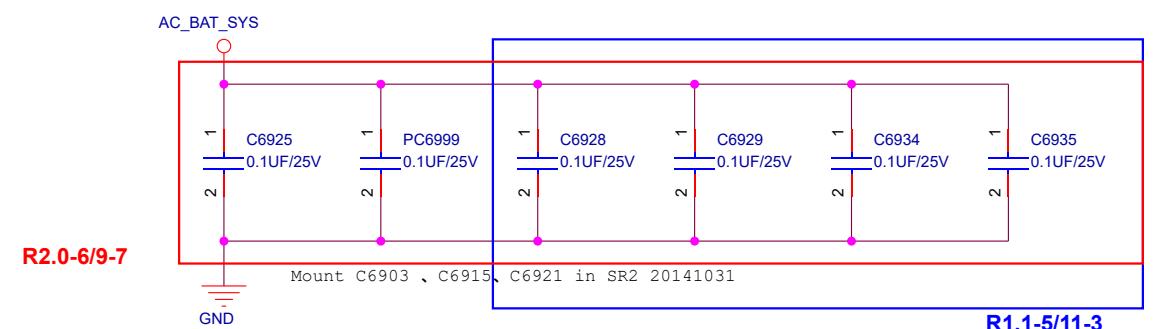
Title : I/O board(2)_USB

Engineer: Mario_Jhu

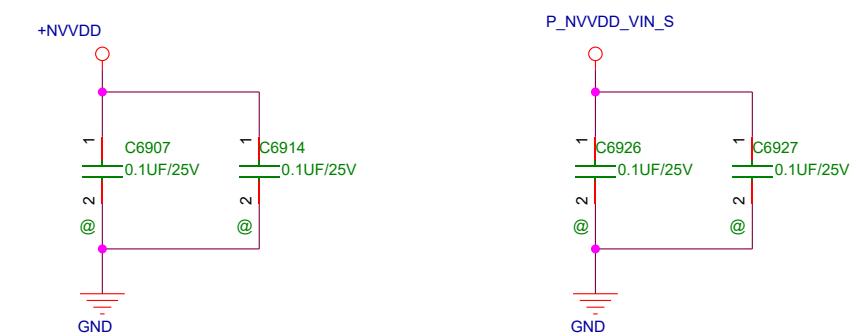
Size	Project Name	Rev
A	GL552VW	2.0
Date: Tuesday, June 23, 2015	Sheet	63 of 103



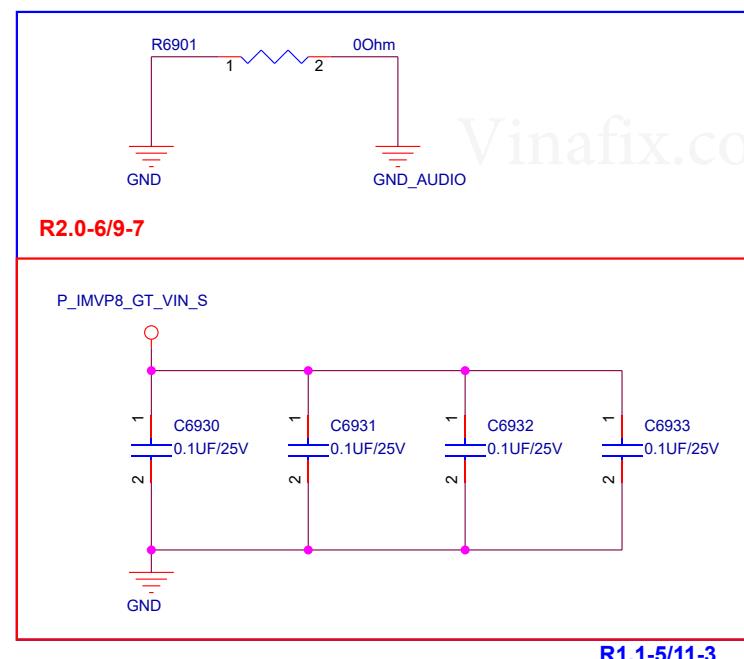
2014-02-12 Add EMI solution
 (6042.00 6728.00)、(1947.00 3850.00)、
 (1757.00 1852.00)、(6369.00 -299.00)



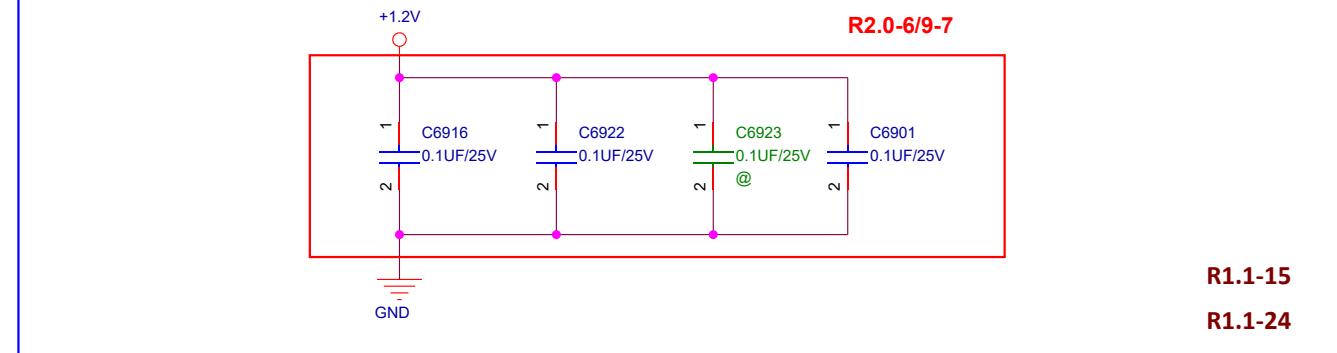
(6490.00 4706.00)、(7437.00 3852.00)



(8004.00 585.00)

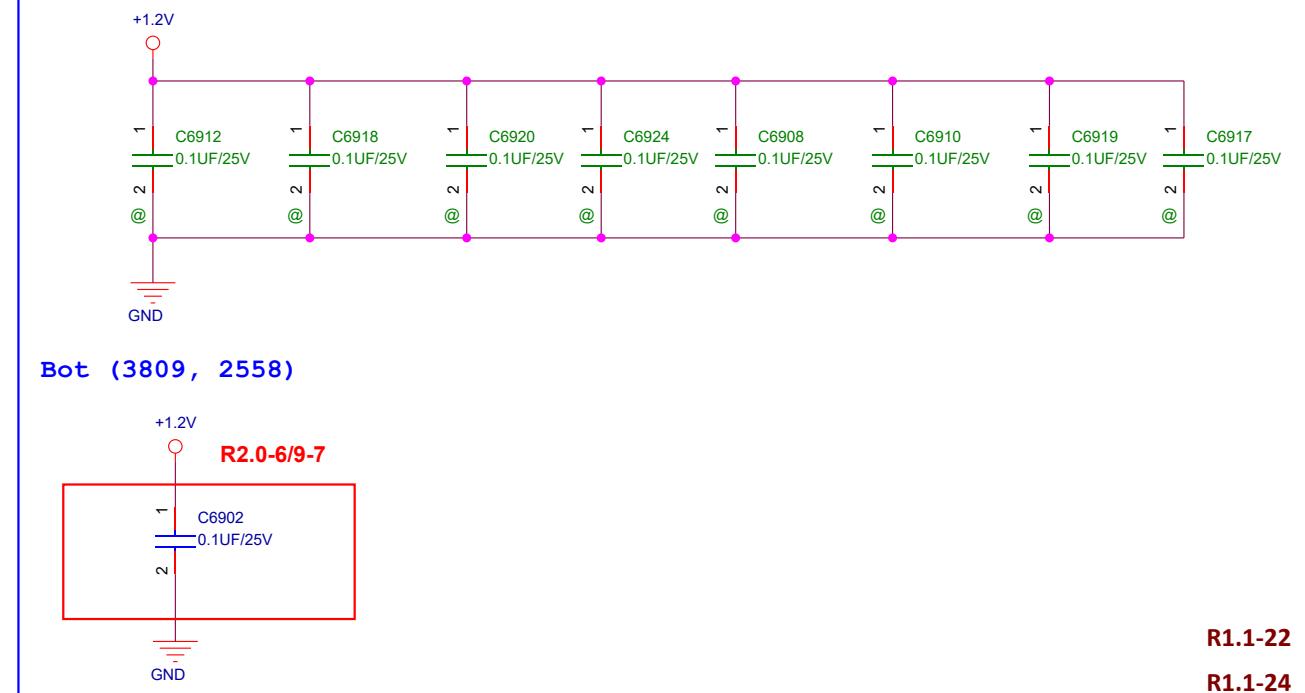


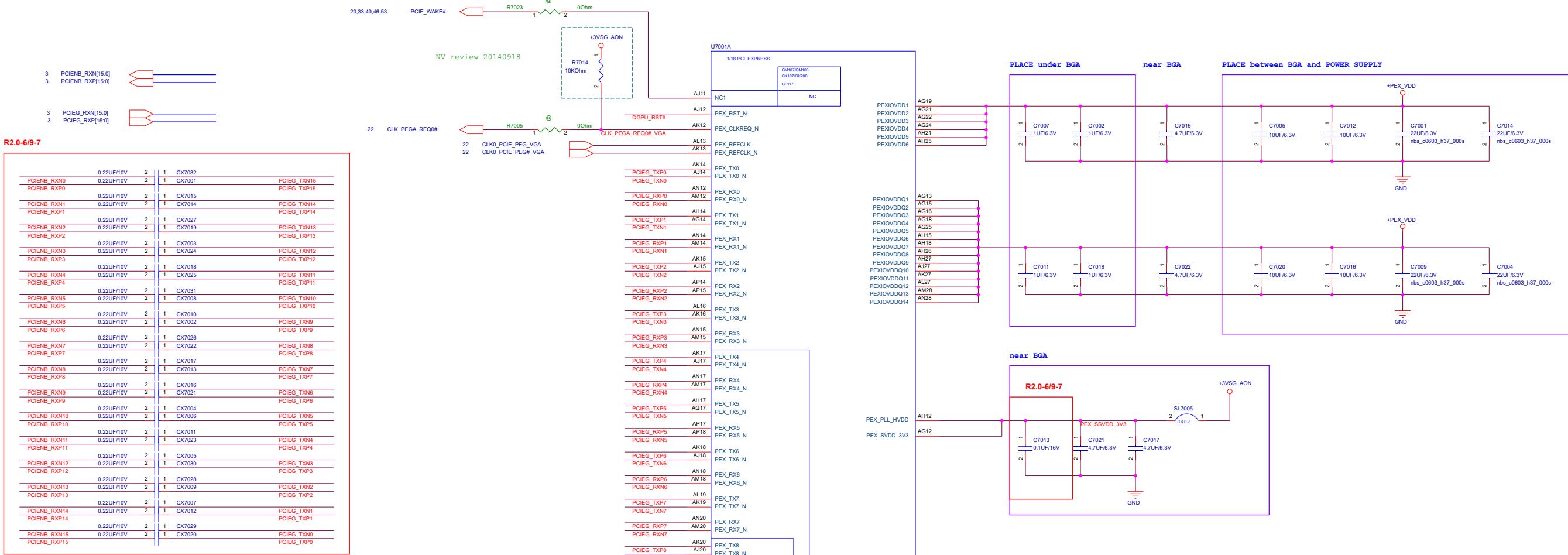
2014-04-03 Add EMI solution
 (3678, 2622)、(4011, 2594)、(4975, 2580)、(5169, 2585)



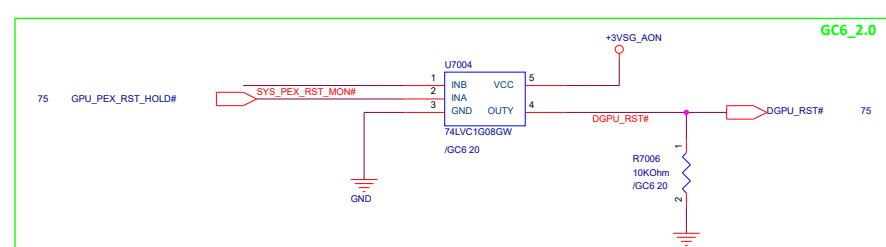
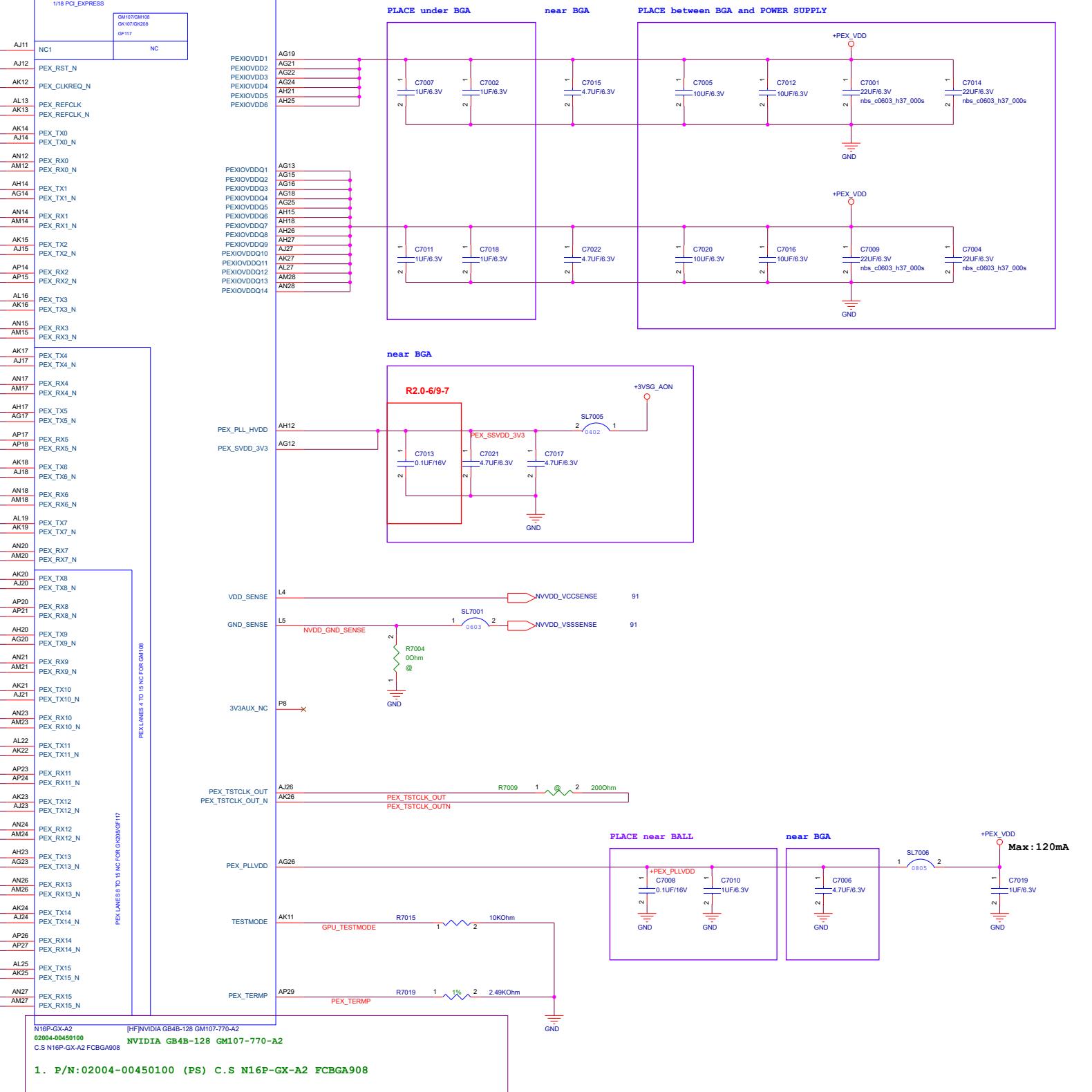
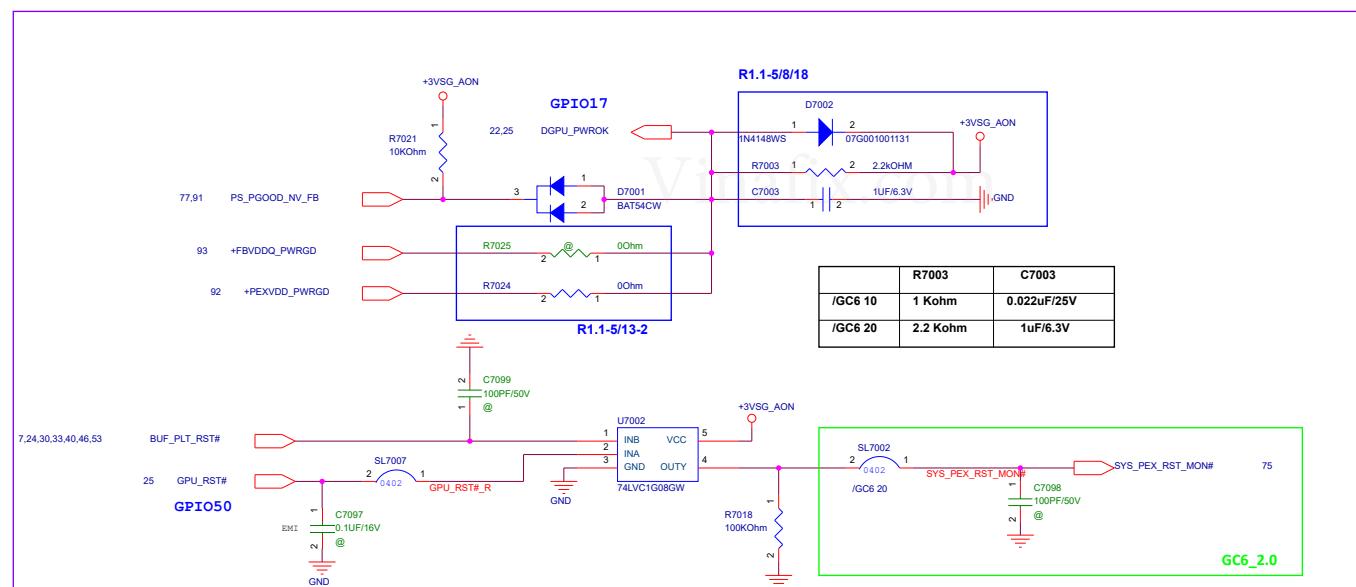
2014-04-03 Add EMI solution

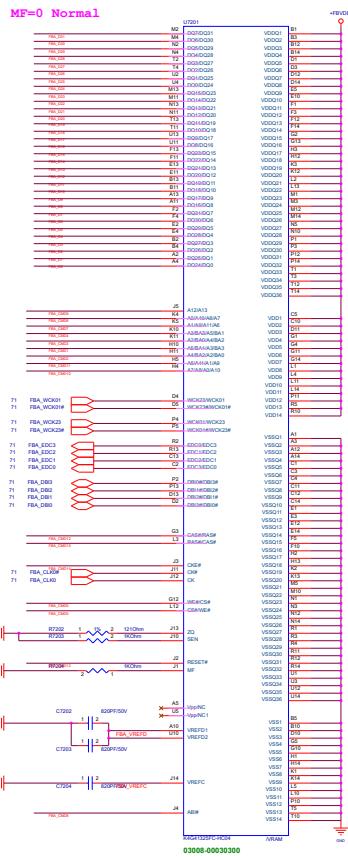
Top
 (3541, 2591)、(3339, 2115)、(3807, 2452)、(4030, 2118)、
 (3367, 1670)、(3583, 1965)、(3819, 1953)、(4013, 1650)





Control Signal from PCH





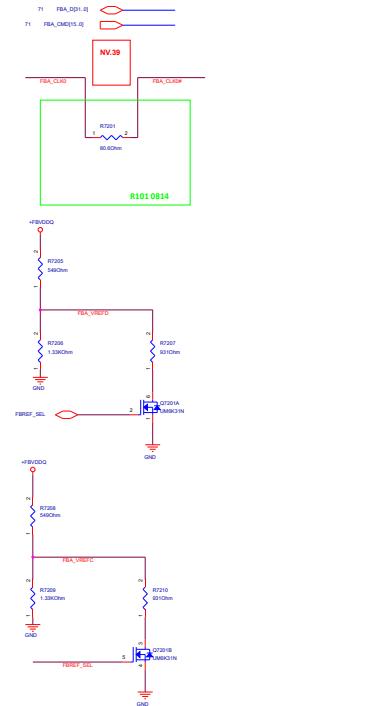
FBA Partition Memory (1 of 2)

GDD5 MODE SELECTION

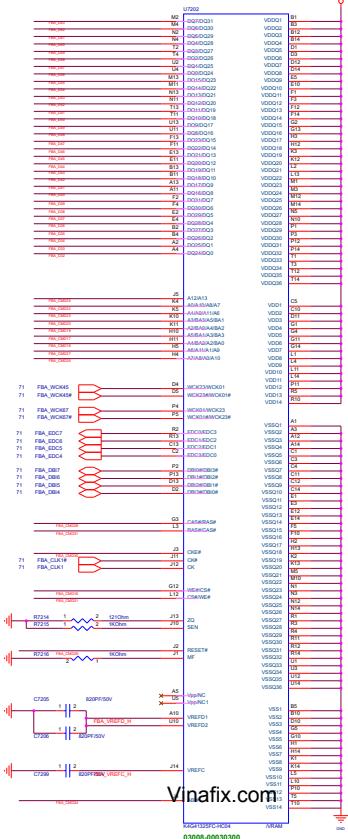
MODE	MIF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

USE GDDR5 VRAM 128Mb x 32 (512MB)
1st: P/N: 03008-00030900 HYNIX/H5GCG24A4JR-T2C(A-die),Strap: 0x6 (+1.35V)
2nd: P/N: 03008-00030400 Micron/EDW4032BAGB-60-F (A-die),Strap: 0x4 (+1.35V)
3rd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, nor)

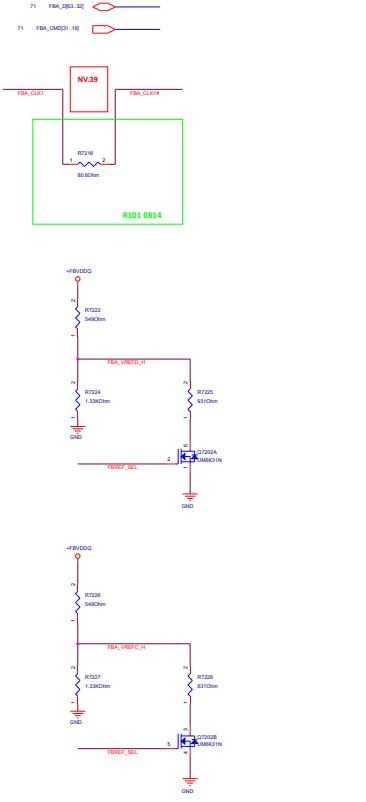
	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm



MF=0 Normal

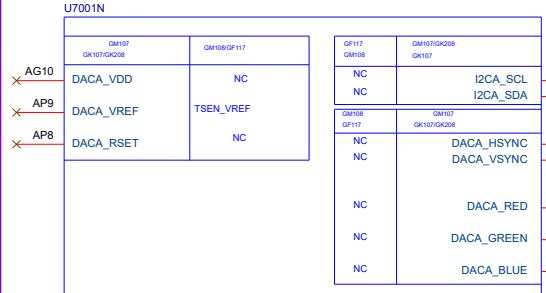


FBA Partition Memory (2 of 2)



CRT DAC_A

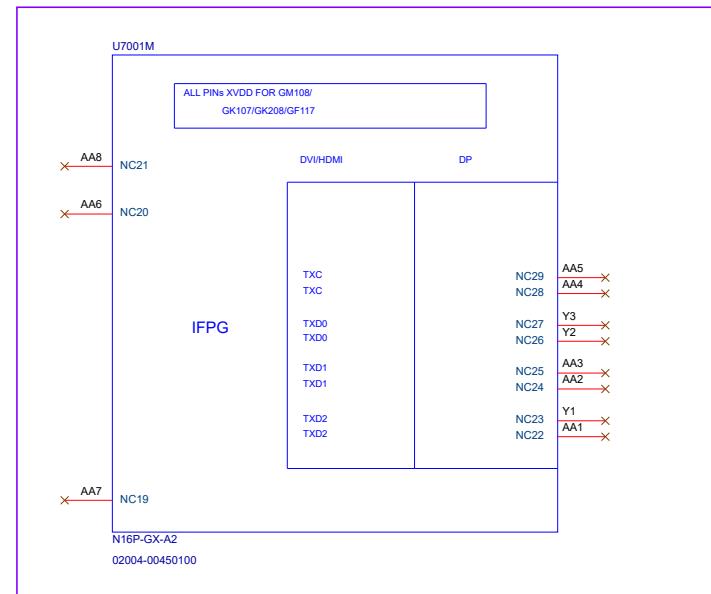
DG-06246-001_v04 DG9.6 p170
DAC interface not used
Leave DACA_VDD floating
All Other pin (DACA_VREF,DACA_RSET) NC



N16P-GX-A2
02004-00450100



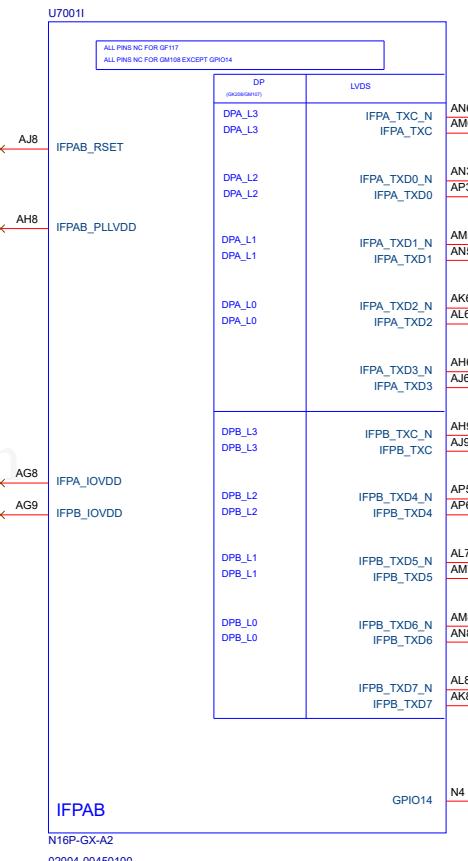
LVDS IFPG



N16P-GX-A2
02004-00450100

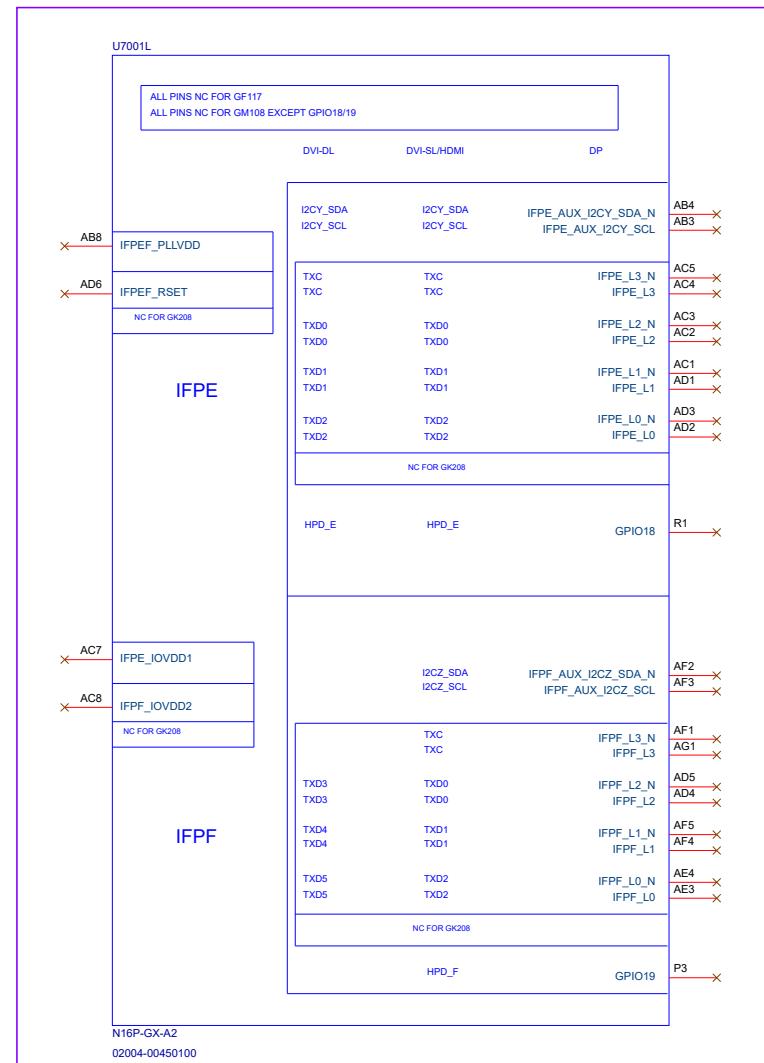
LVDS IFPA/B

DG-06246-001_v04 DG8.6 p162
Float IFPx_IOCDD/IFPx_PLLVDD
Other pin NC



N16P-GX-A2
02004-00450100

LVDS IFPE/F



N16P-GX-A2
02004-00450100

<Variant Name>

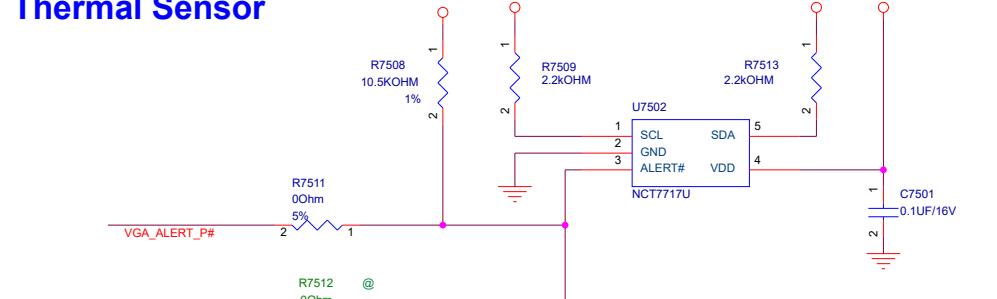
	Title : VGA_CRT/LVDS(5)
ASUSTek COMPUTER INC. NB1	Engineer: Mario_Jhu
Size C	Project Name GL552VW
Rev 2.0	Date: Tuesday, June 23, 2015

GPIO ASSIGNMENTS

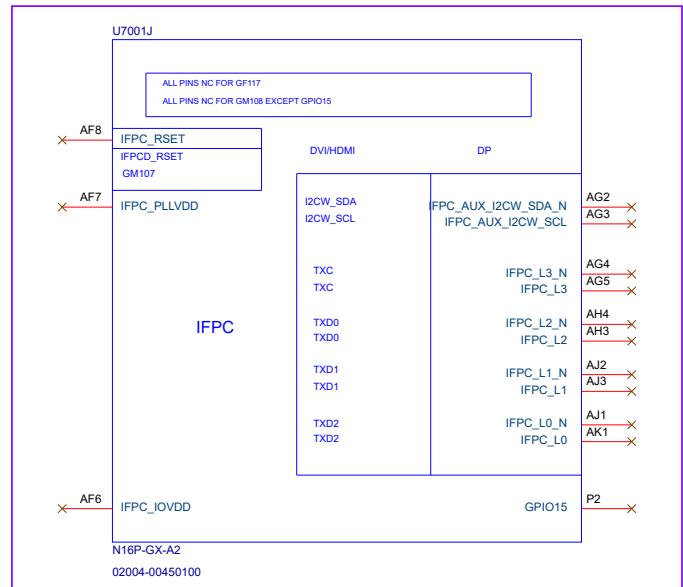
GPIO	I/O	ACTIVE	USAGE
0	OUT	Low	GC6_FBN
1	OUT	High/Low	MEM_VDD_CTL
2	OUT	Low	LCD_BL_PWM
3	OUT	Low	LCD_VCC
4	OUT	Low	LCD_BLEN
5	OUT	High	3V3_MAIN_EN
6	IN	High	GPU_EVENT#
7	OUT	Low	3DVision
8	IN	High	SYS_PEX_RST_MON#
9	I/O	High	THERM_ALERT
10	OUT	Low	MEM_VREF_CTL
11	OUT	Low	PWM_VID
12	IN	High	PWR_LEVEL
13	OUT	High	PSI
14	IN	Fig. 12-1	HPD_IFPAB
15	IN	Fig. 12-1	HPD_IFPC
16	IN	High	FRAME_LOCK#
17	IN	Fig. 12-1	HPF_IFPD
18	IN	Fig. 12-1	HPD_IFPE
19	IN	Fig. 12-1	HPD_IFPPB
20	OUT	High	Reserved
21	OUT	High	GPU_PEX_RST_HOLD#
OVERT	I/O	High	OVERT

Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

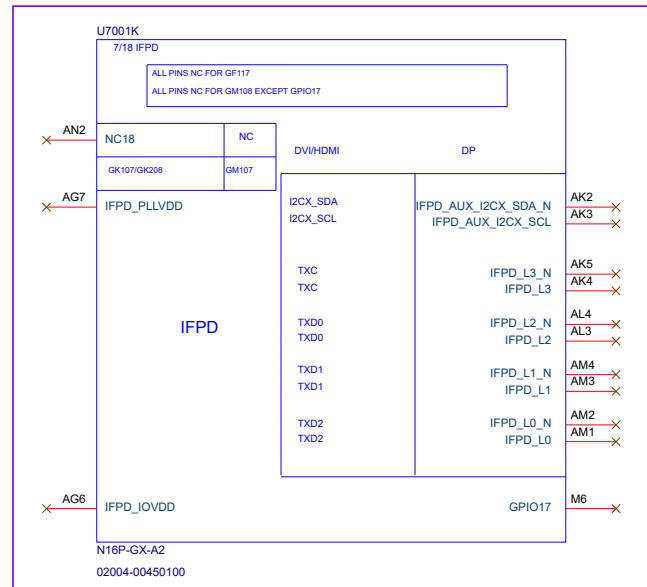
Thermal Sensor



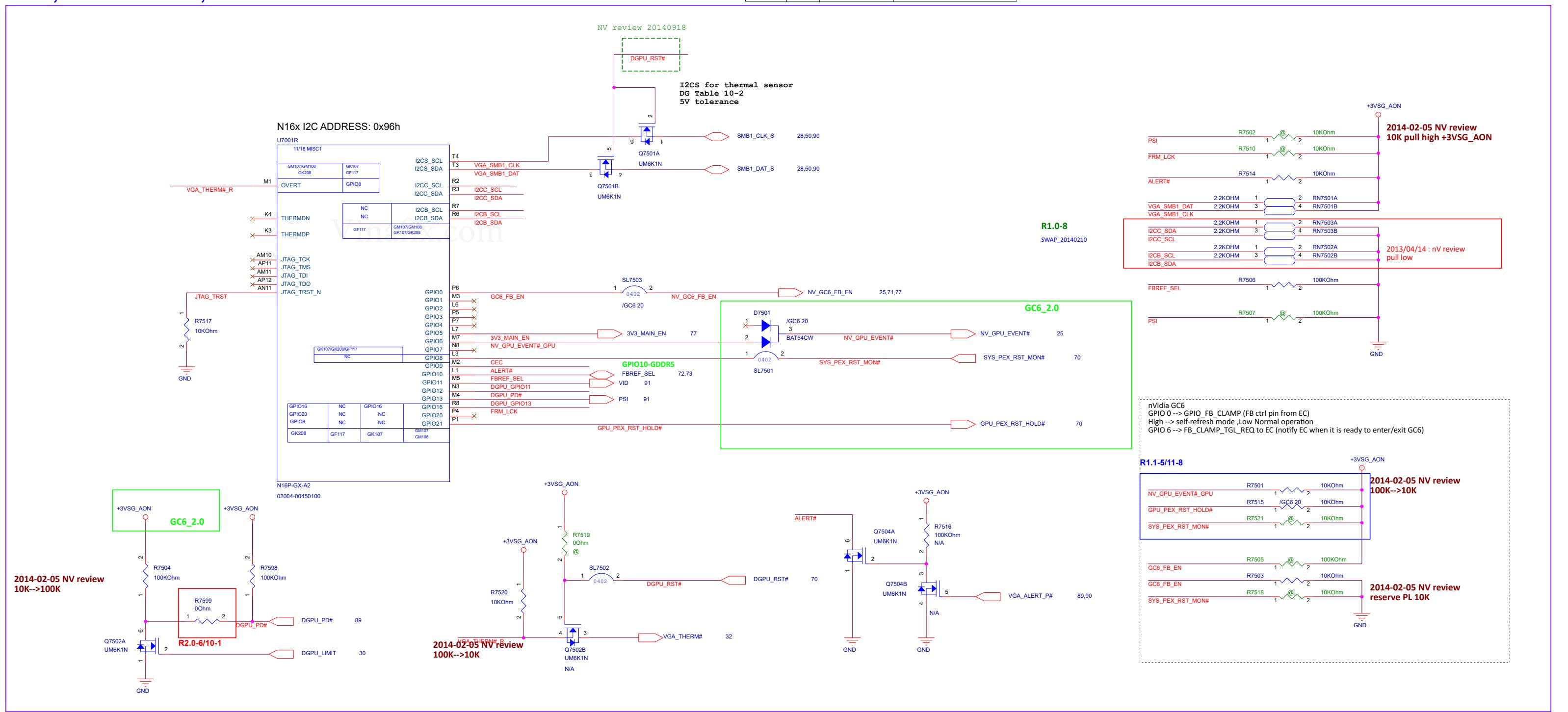
DP(link C)

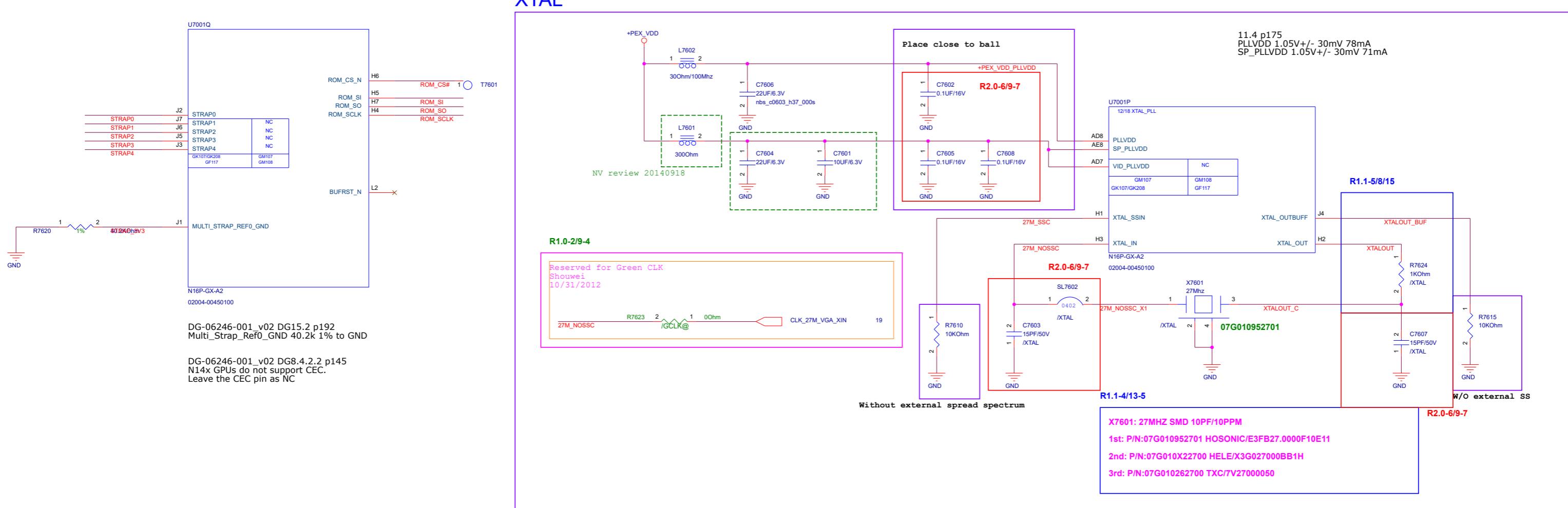


DVI(link D)

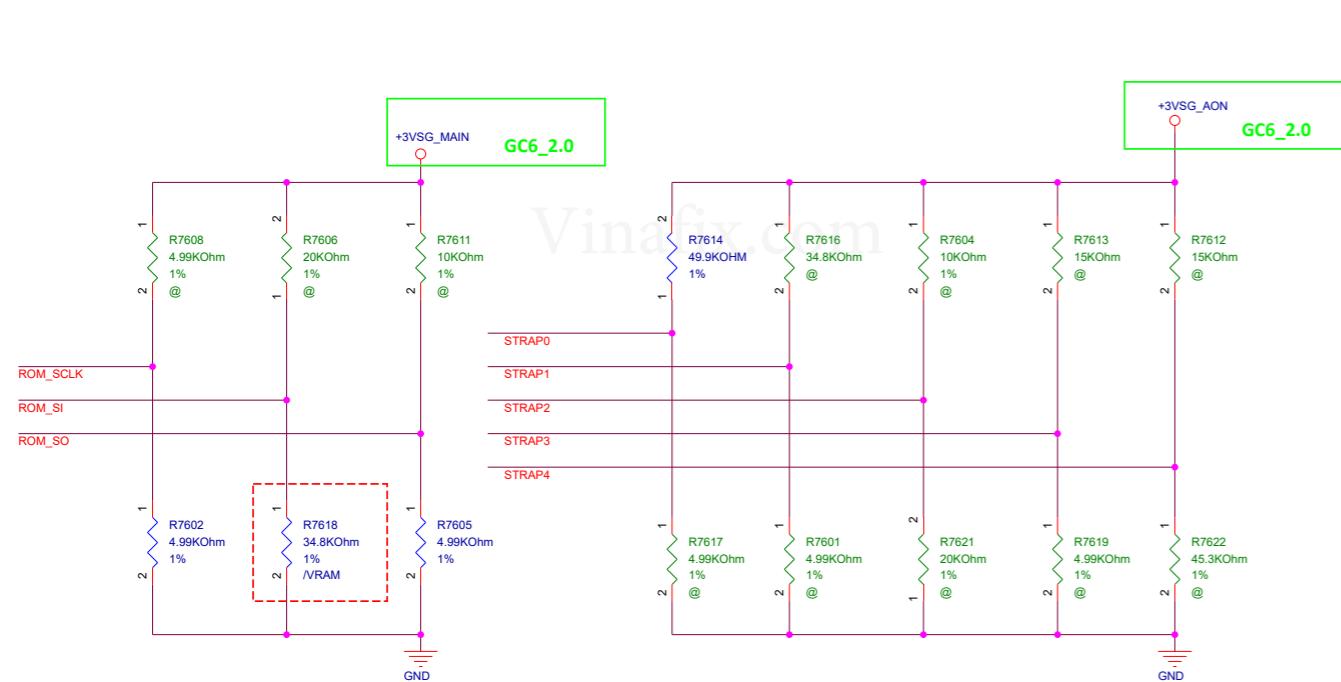


GPIO, TEMP SENSOR, JTAG





STRAPPING OPTIONS for N16P



Change R7618 VRAM Vendor

USE GDDR5 VRAM 128Mb x 32 (512MB)

Hynix strap 0x6 HYNIX/H5GC4H24AJR-T2C - 34.8Kohm +1.35V

[View Details](#) | [Edit](#) | [Delete](#)

Micron strap 0x4 Micron/EDW4032BABG-60-F - 24.9Kohm +1.35V

Samsung strap 0x3 Samsung/K4G41325FC-HC04 - 20Kohm +1.5V non-RV

DG-07158-001_v05_secured p.197
Table 15-3. GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kohm pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not Stuff.			

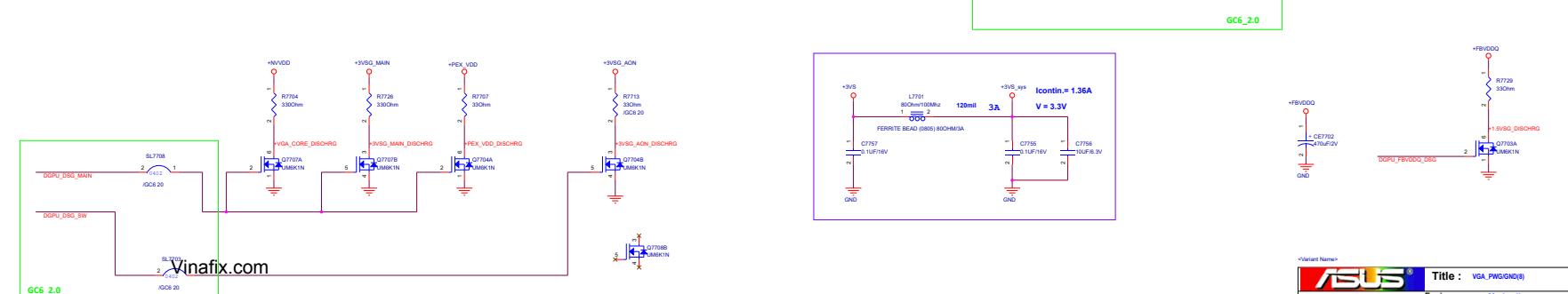
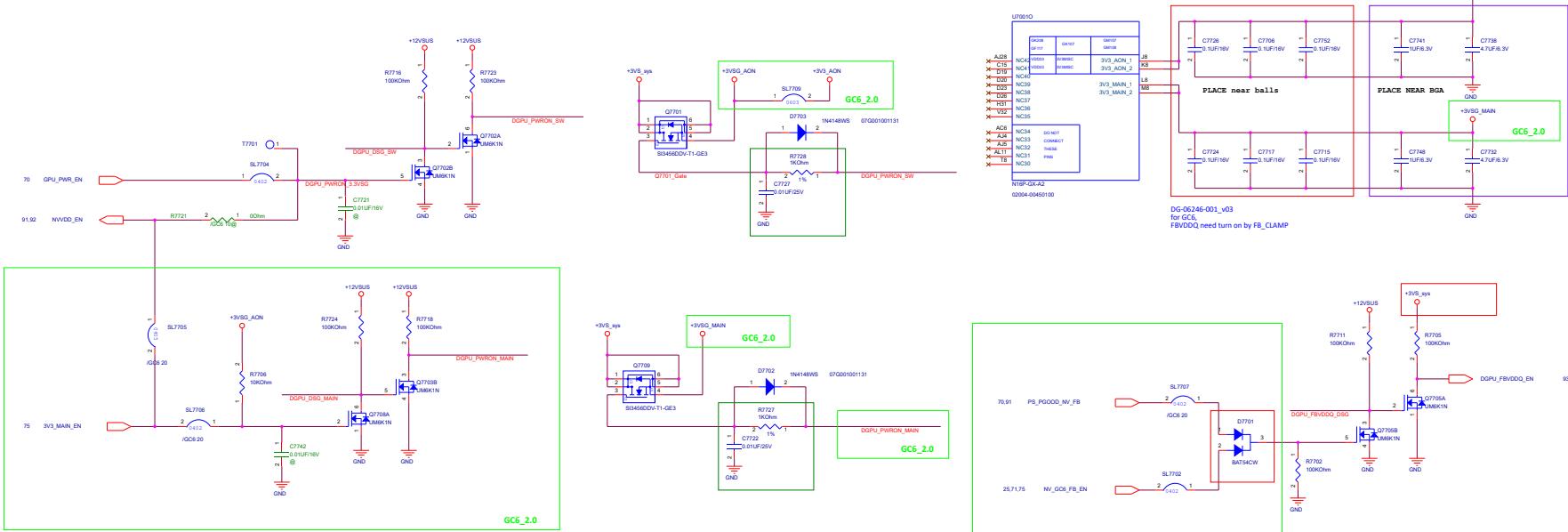
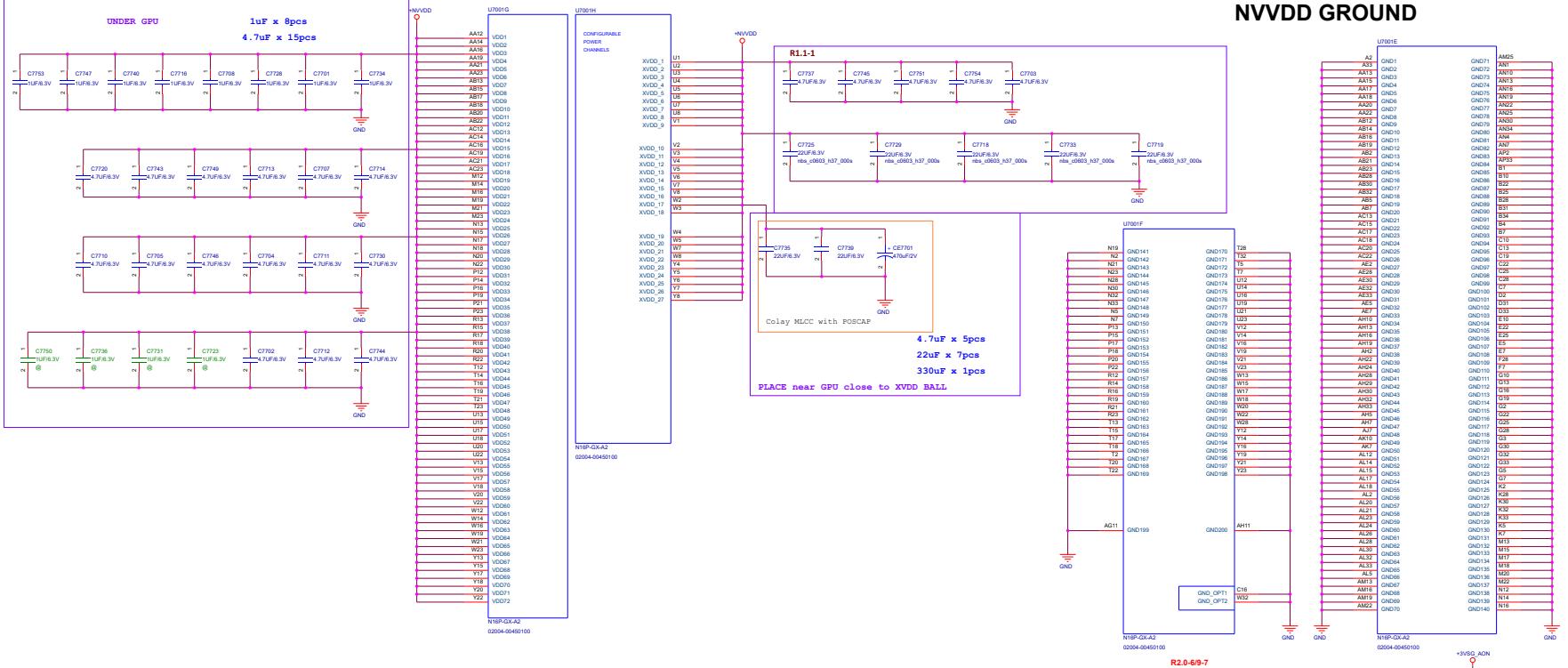
Table 15-2.

	PU	PD
4.99Kohm	1000	0000
10.0Kohm	1001	0001
15.0Kohm	1010	0010
20.0Kohm	1011	0011
24.9Kohm	1100	0100
30.1Kohm	1101	0101
34.8Kohm	1110	0110
45.3Kohm	1111	0111

	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

NVVDD POWER AND DECOUPLING

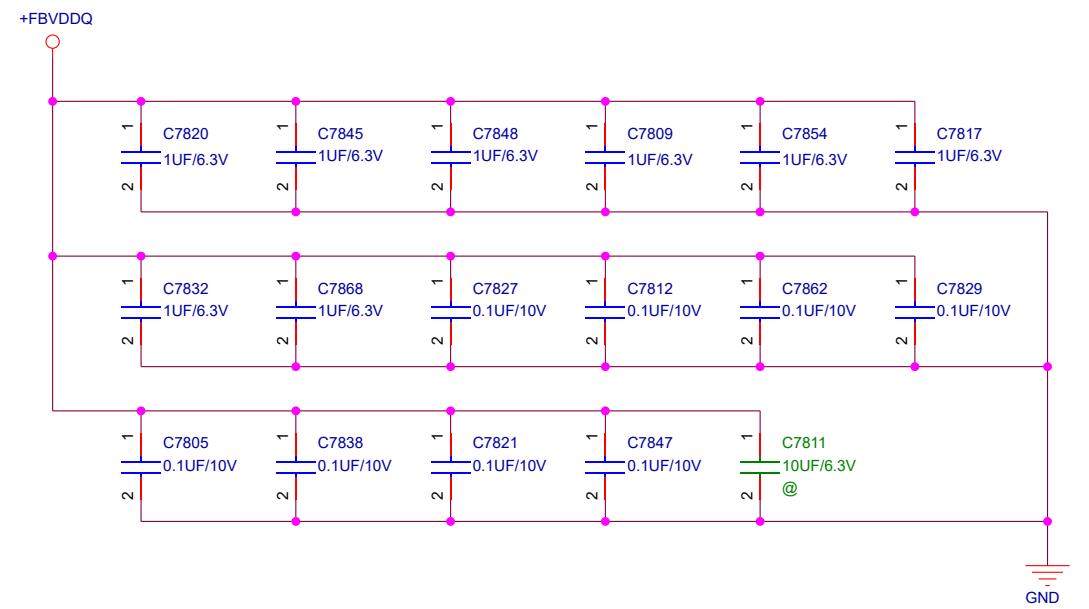
NVVDD GROUND



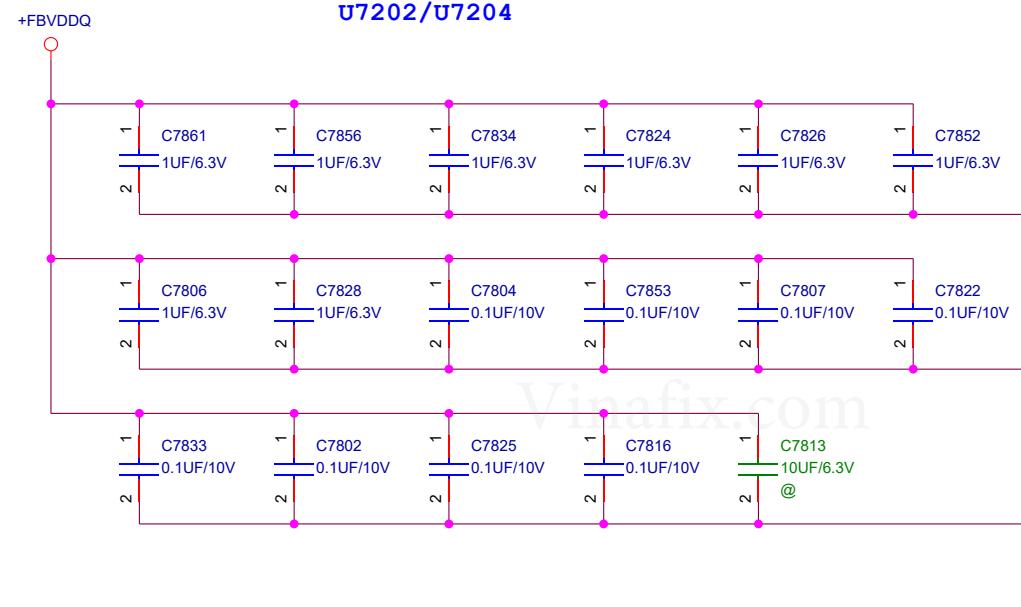
Location is close to DRAM for clamshell mode

0.1uF X8
1uF X 8

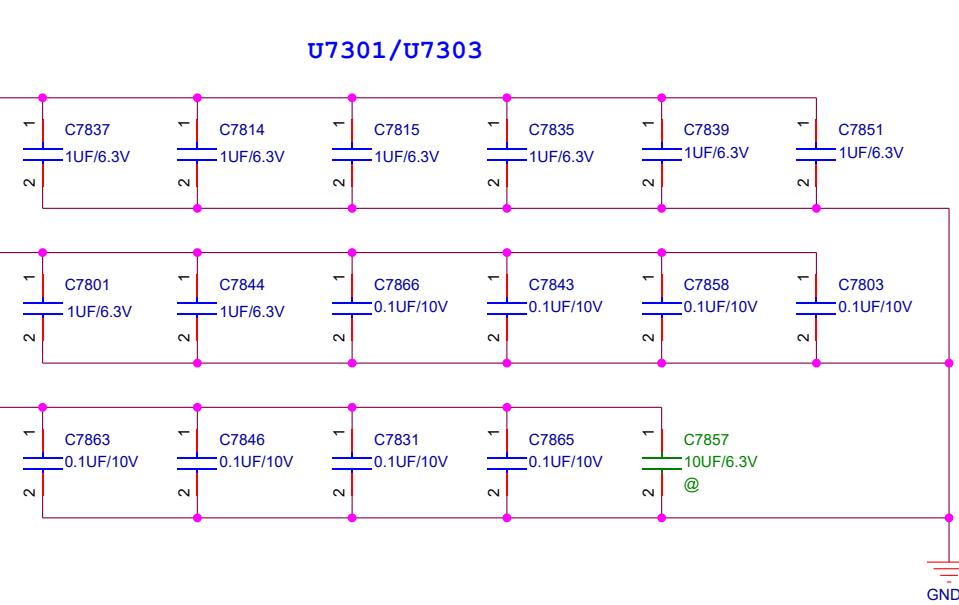
U7201/U7203



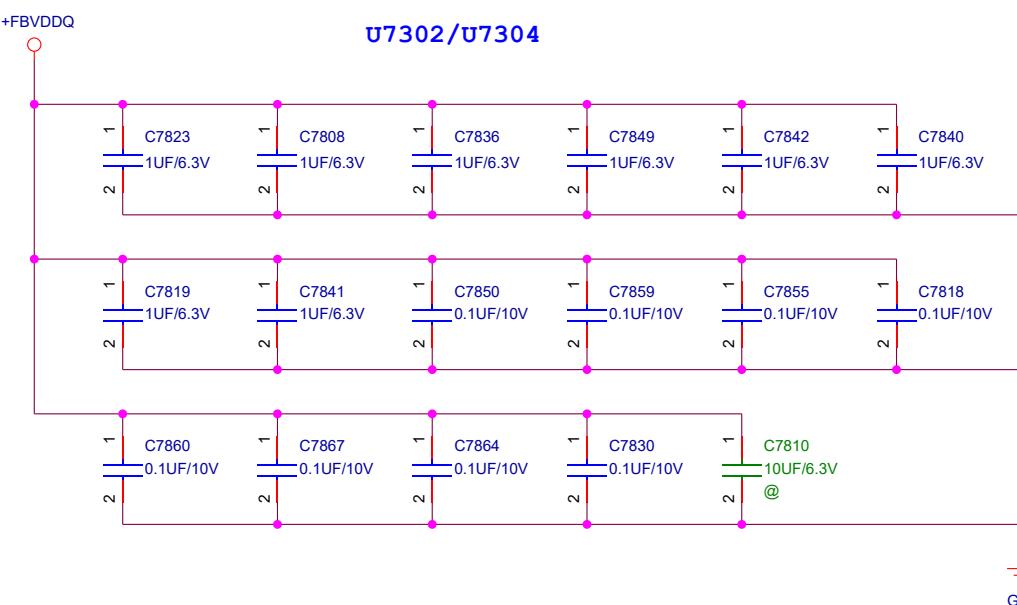
U7202/U7204



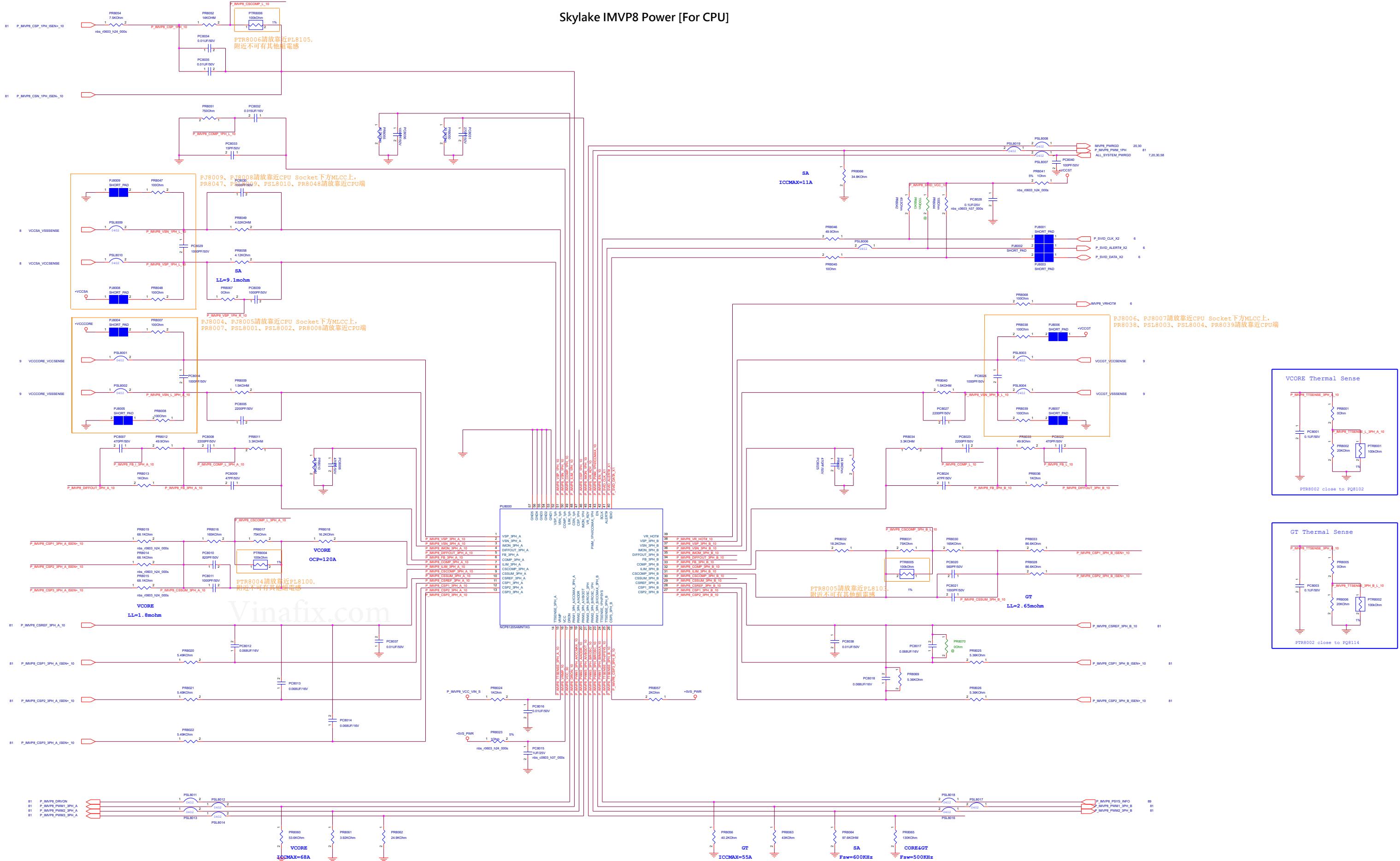
U7301/U7303



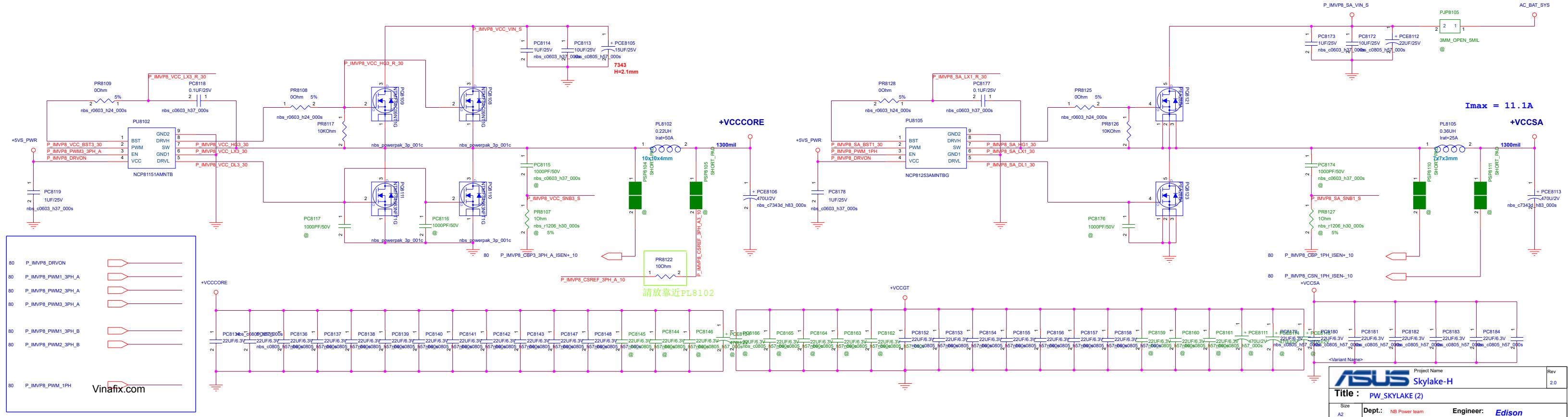
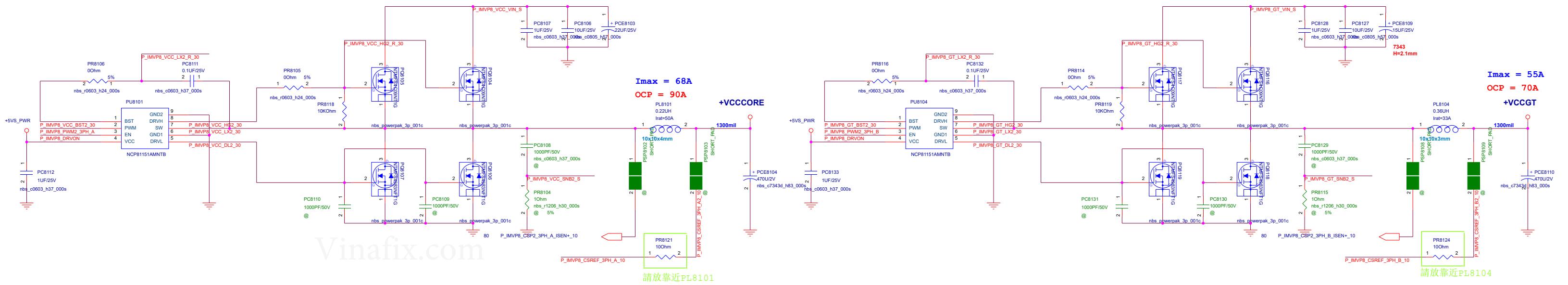
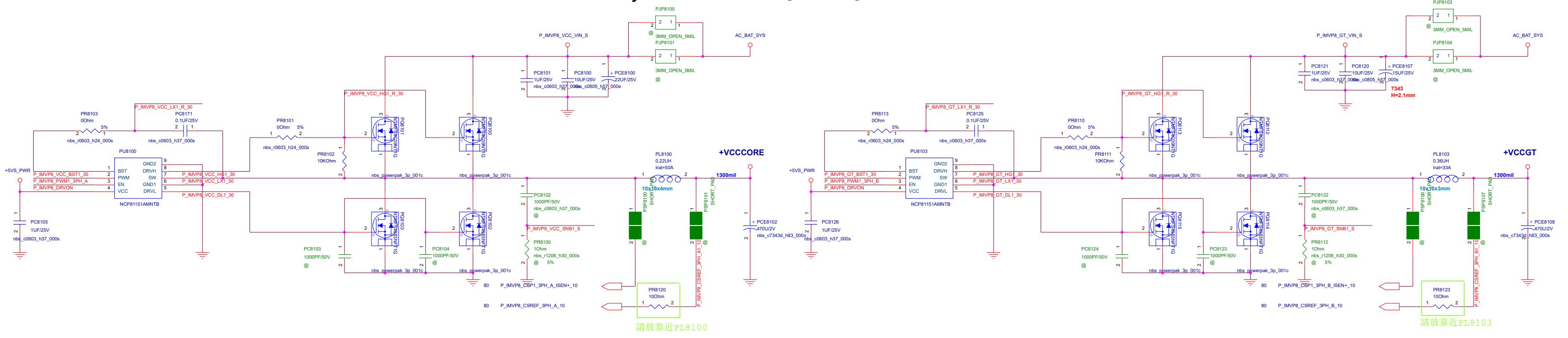
U7302/U7304



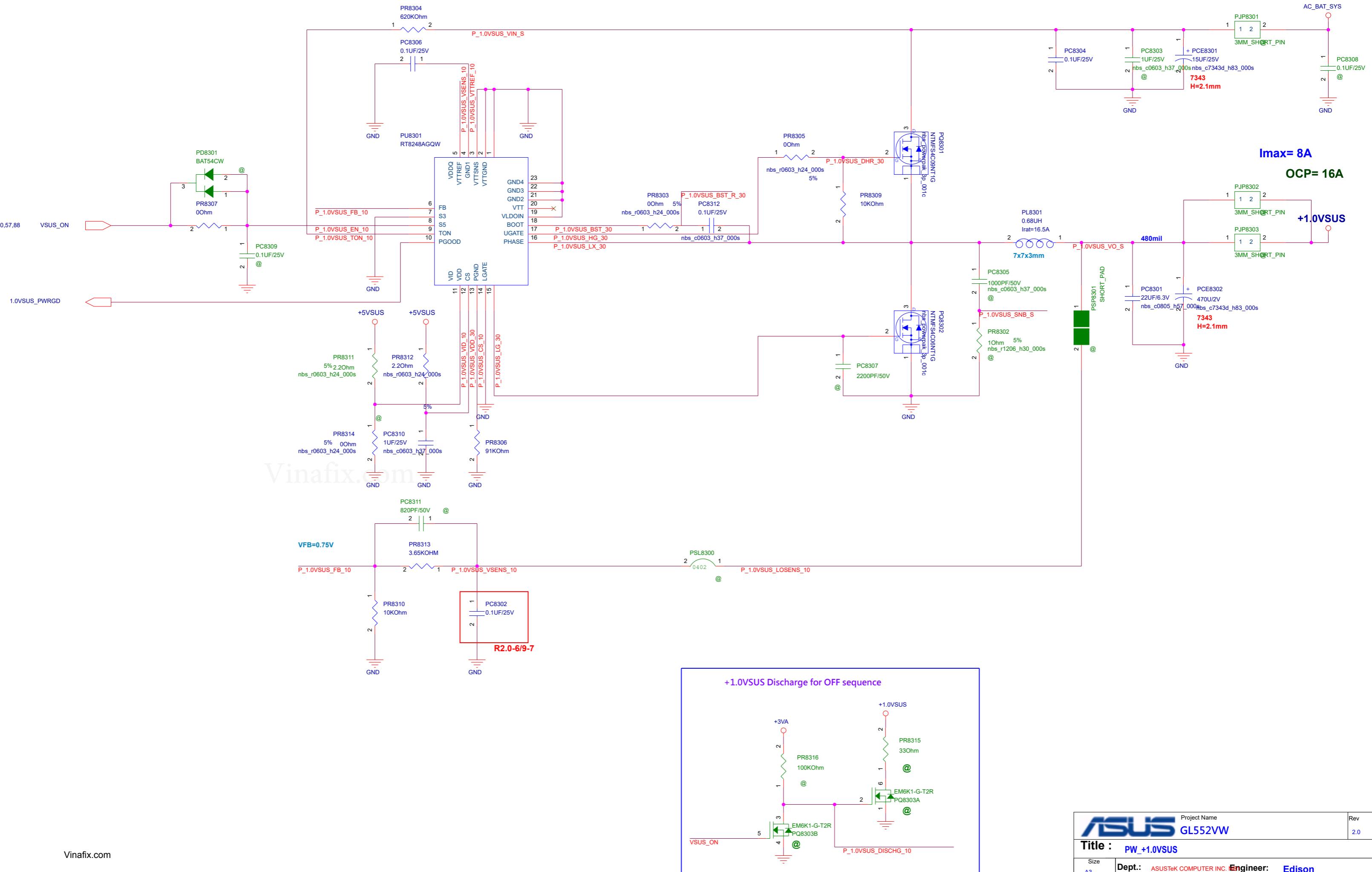
Skylake IMVP8 Power



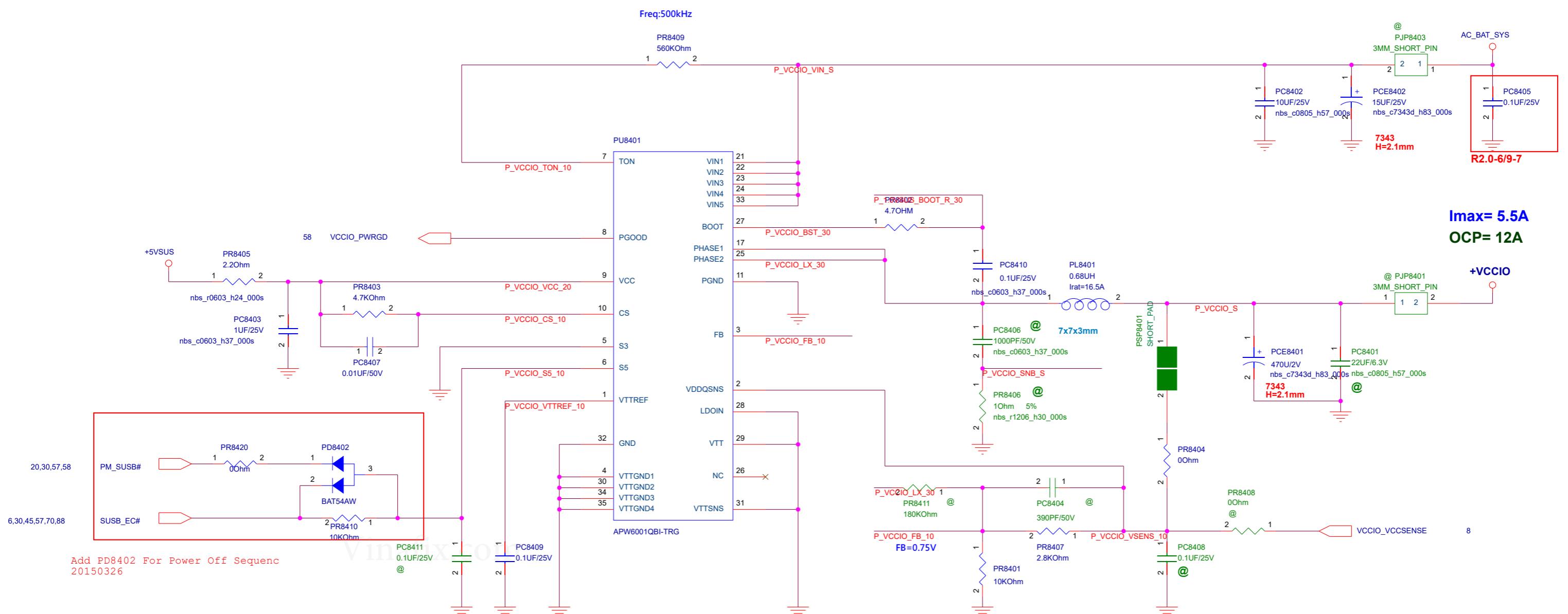
Skylake IMVP8 Power [For CPU]



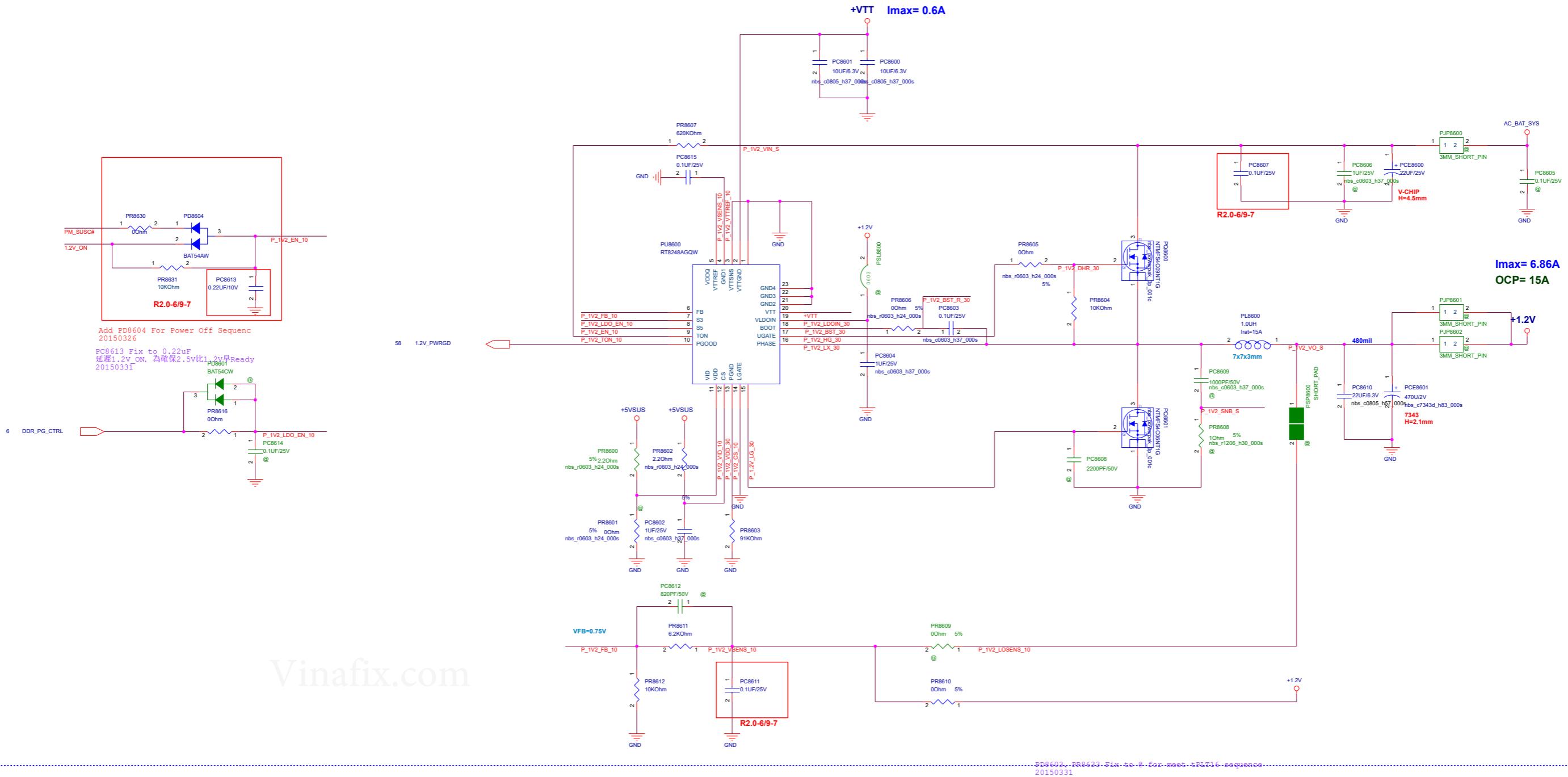
+1.0VSUS [For PCH]



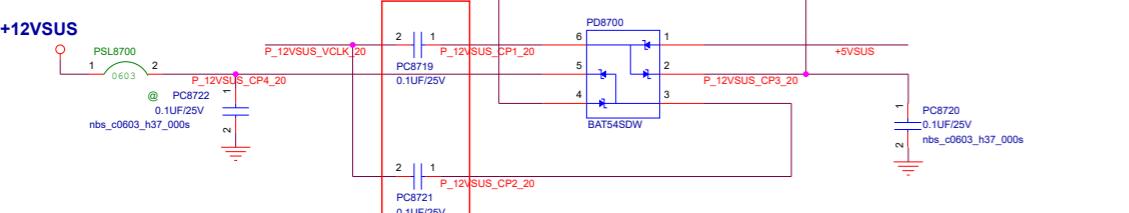
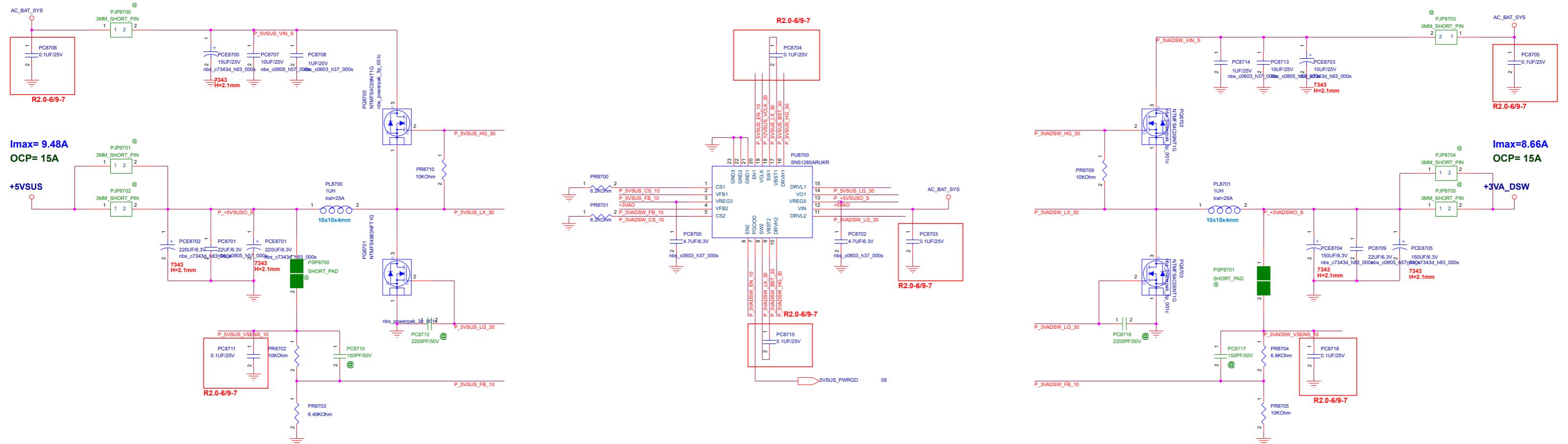
+VCCIO [For CPU]



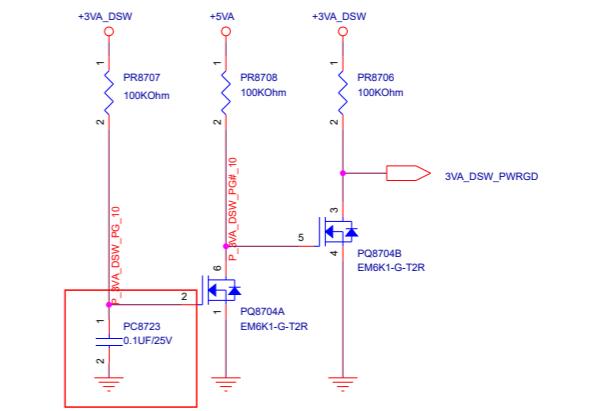
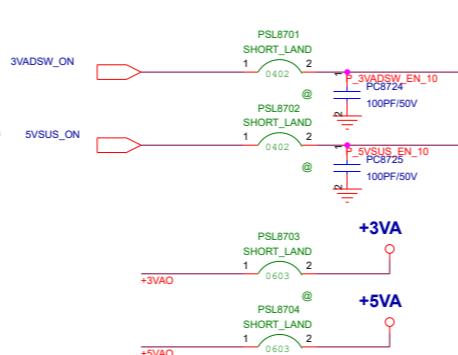
+1.2V / VTT / 2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]



請 check 整份線路 +12V/SUS total 並聯對地電阻不得小於10kOhm

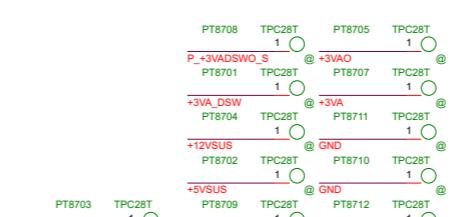


Adaptor Mode (IMVP8)

Adaptor Mode (mV/s)							
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

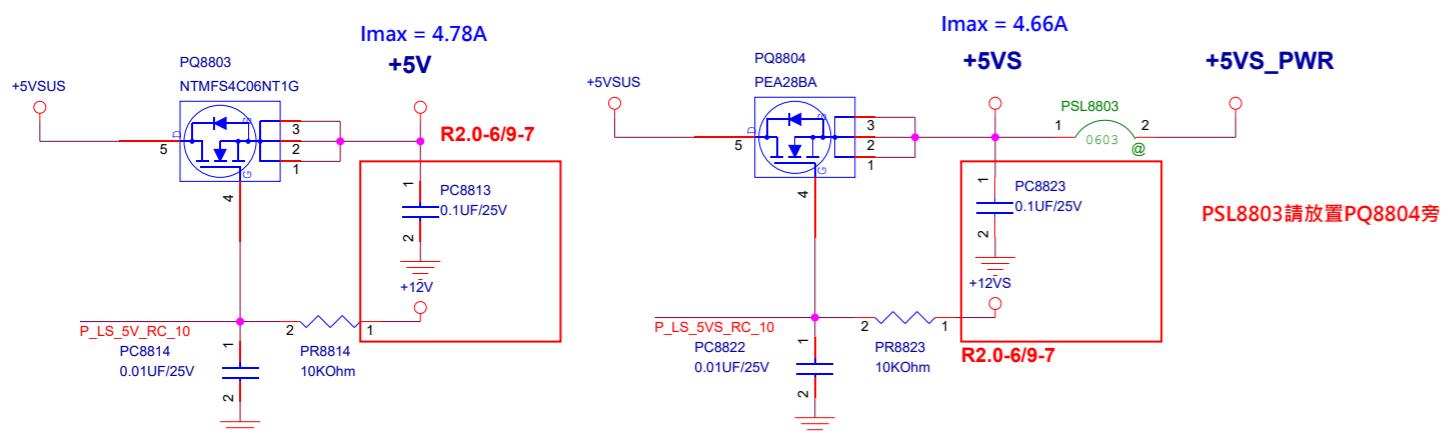
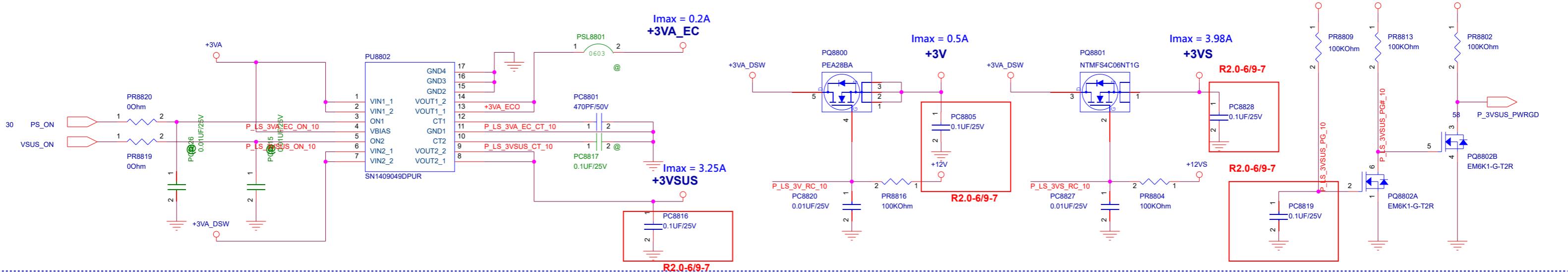
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



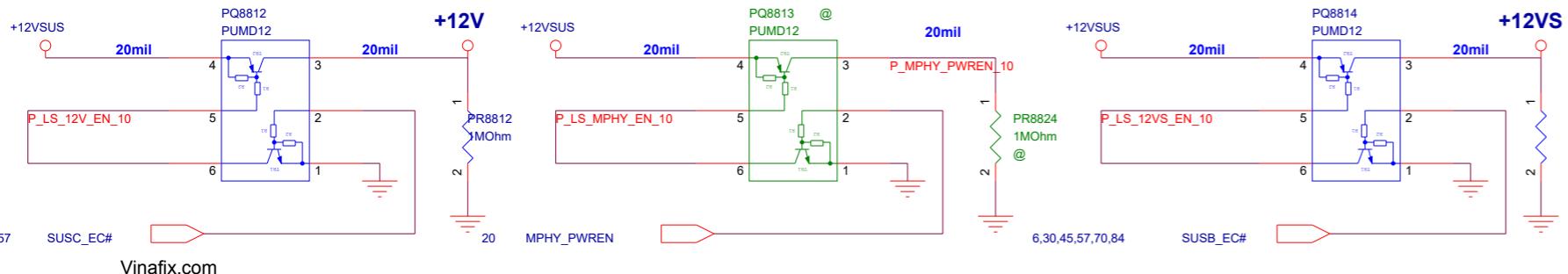
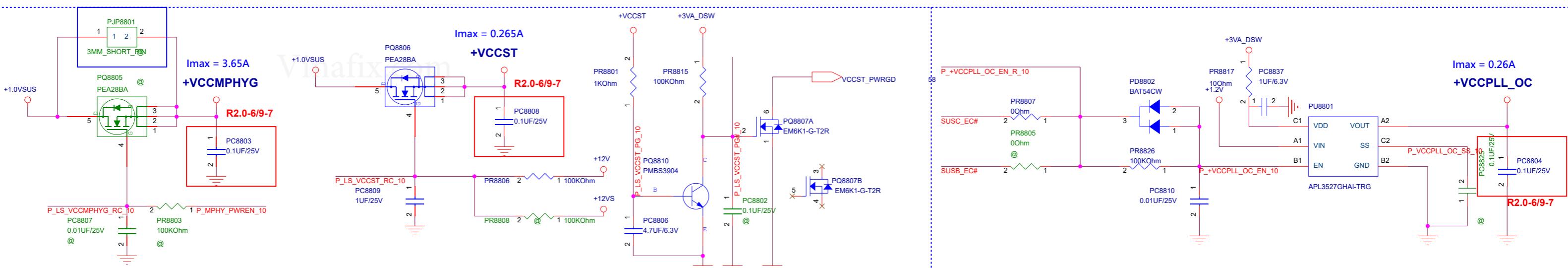
Project Name		Rev
Skylake-H		2.0
Title :	PW_+3VA_DSW/+5VSUS	
Size	Dept.:	Engineer:
2	NB Power team	Edison
e: Tuesday, June 23, 2015	Sheet	87 of 103

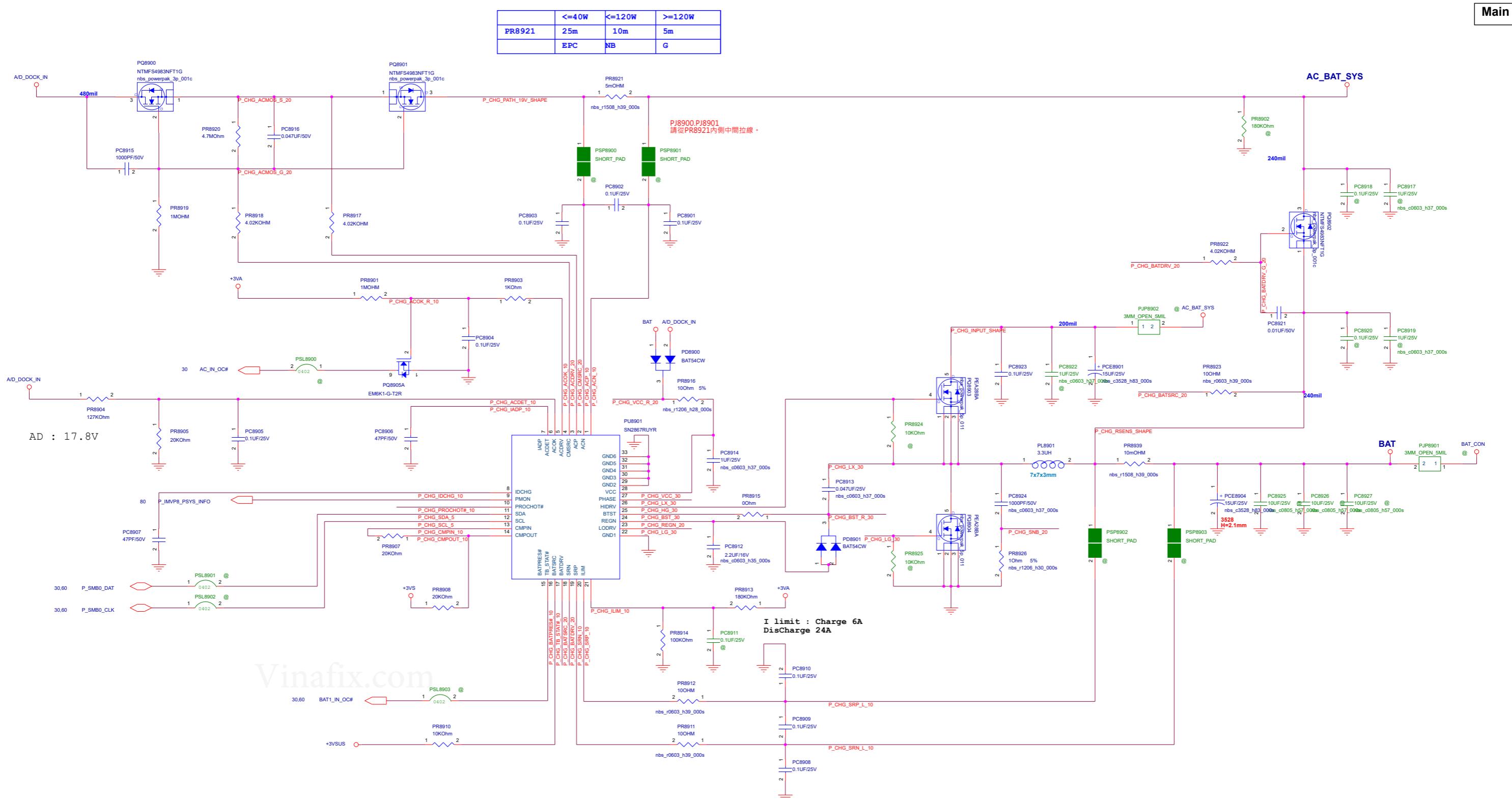
Load Switch

Main Board

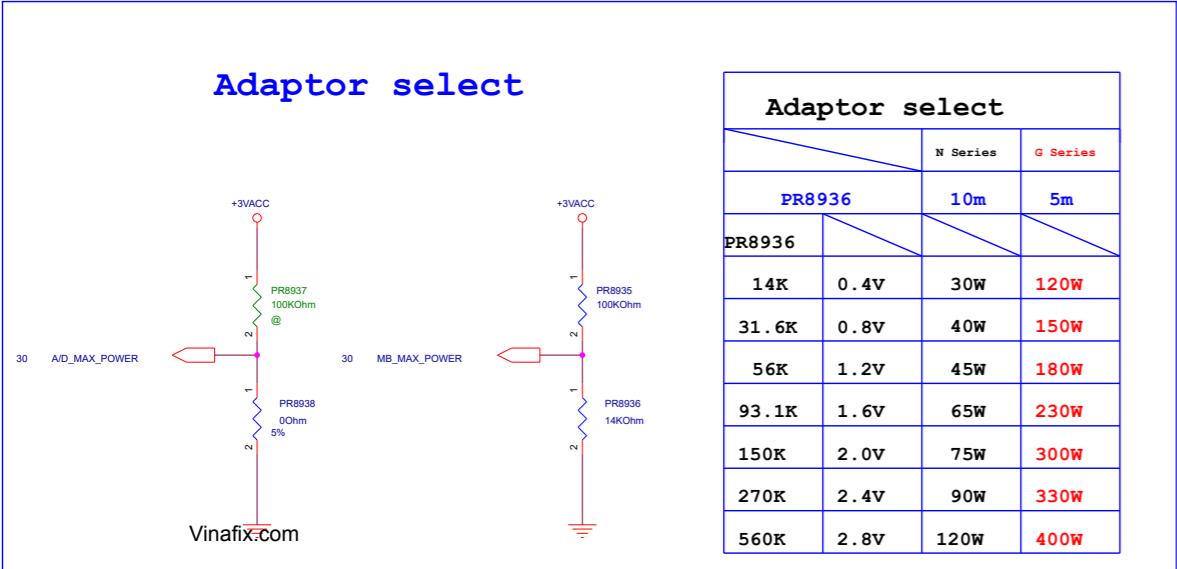


R1.1-4/13-5 必上件

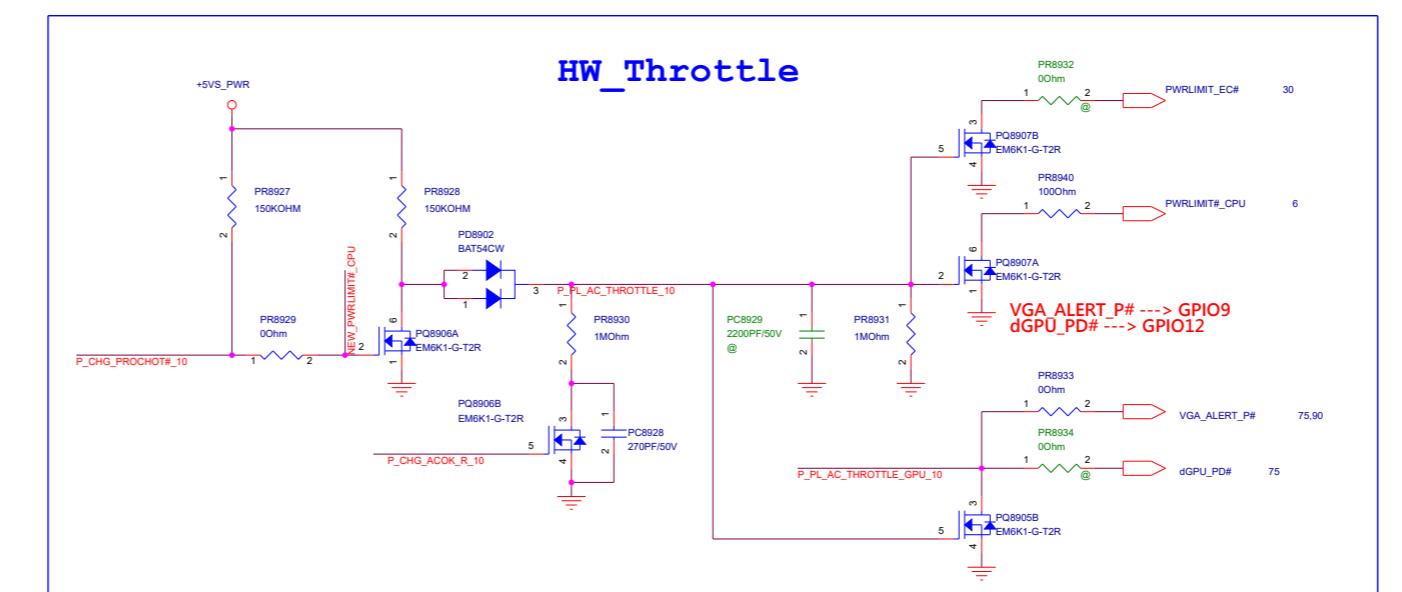




Adaptor select



HW_Throttle

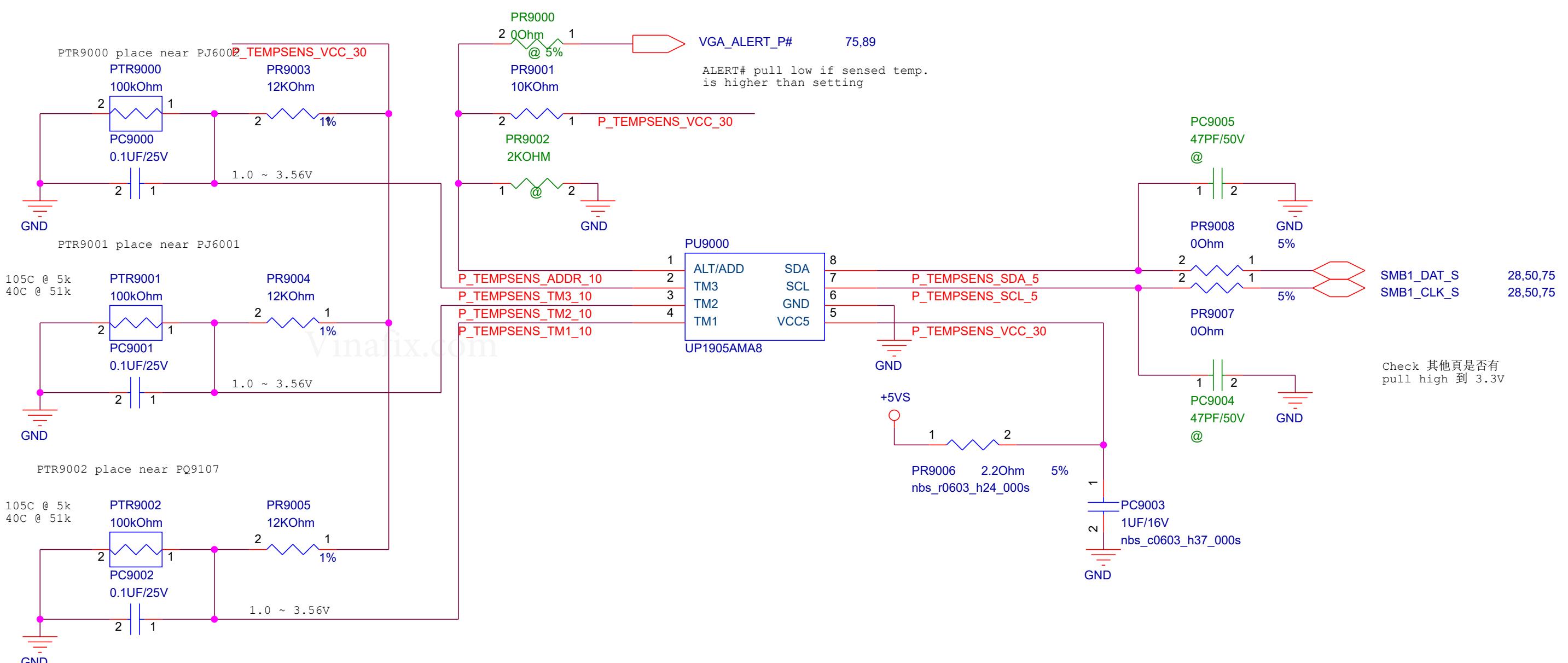


Address Selection Table

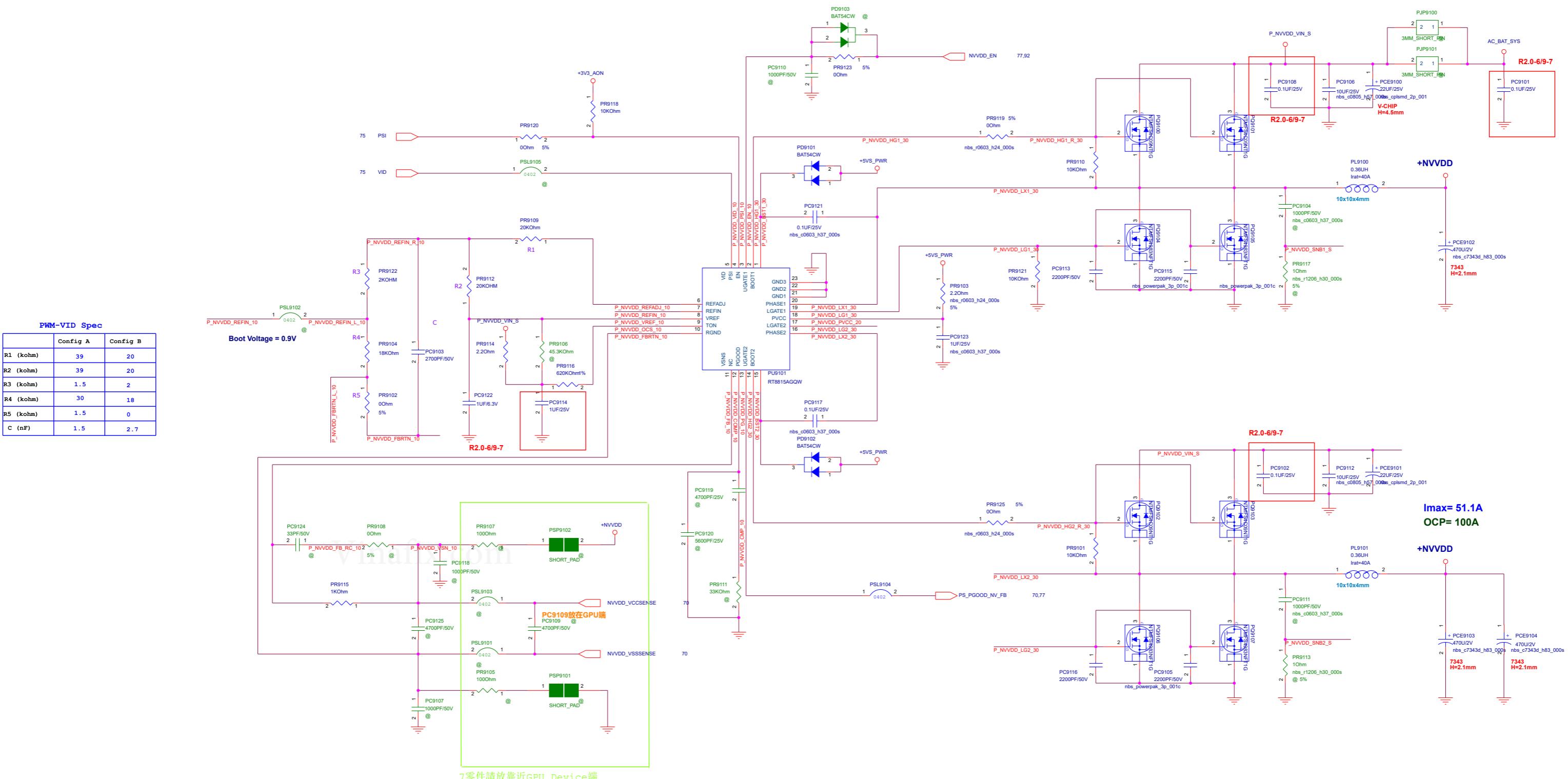
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9404	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9405	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

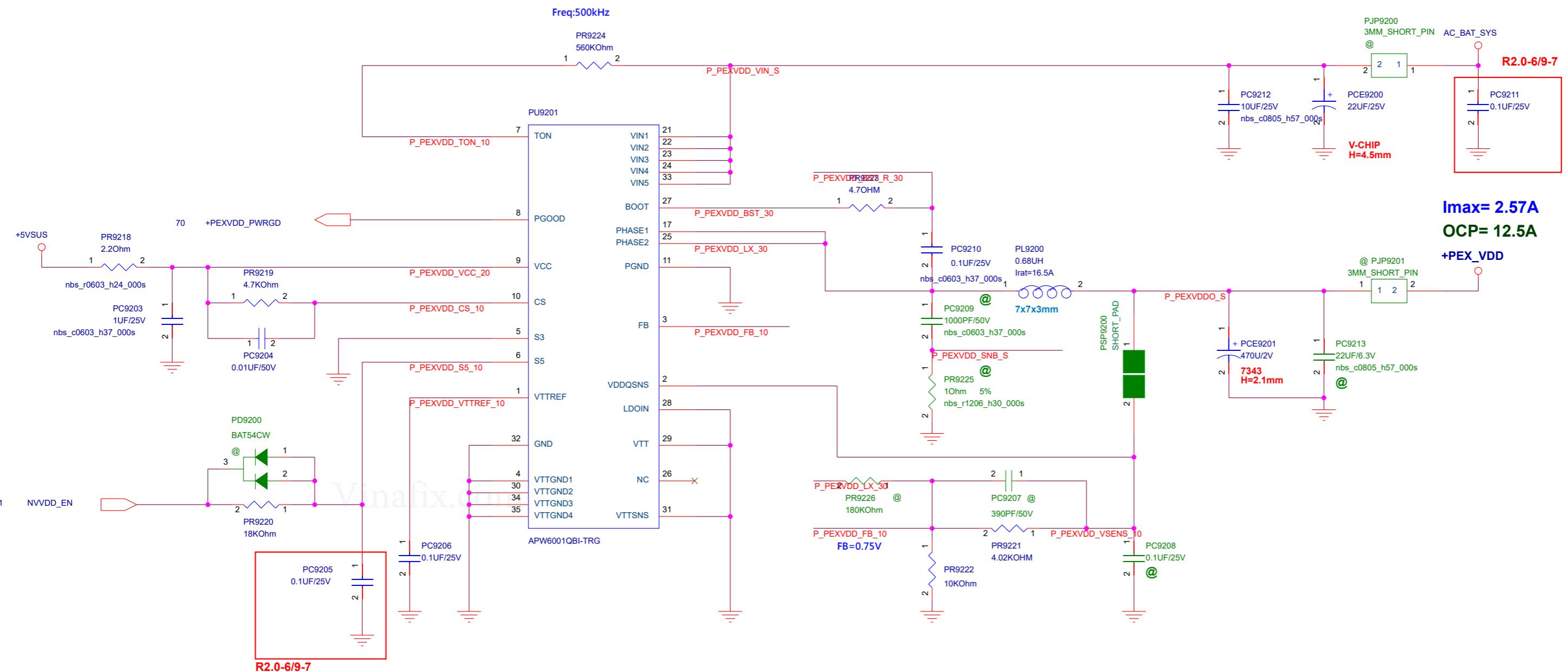


+NVVDD [For DGPU]



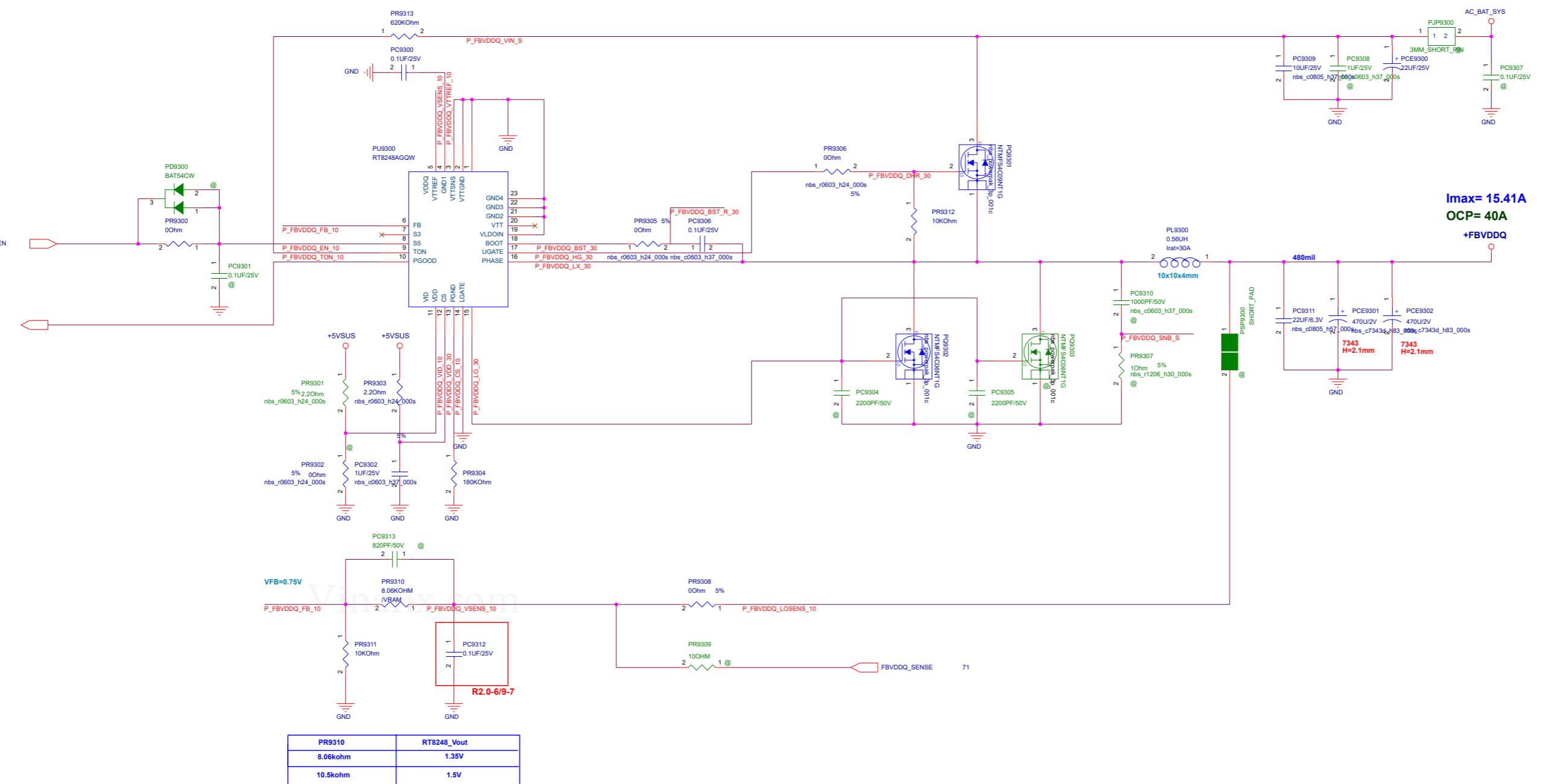
Vinafix.com

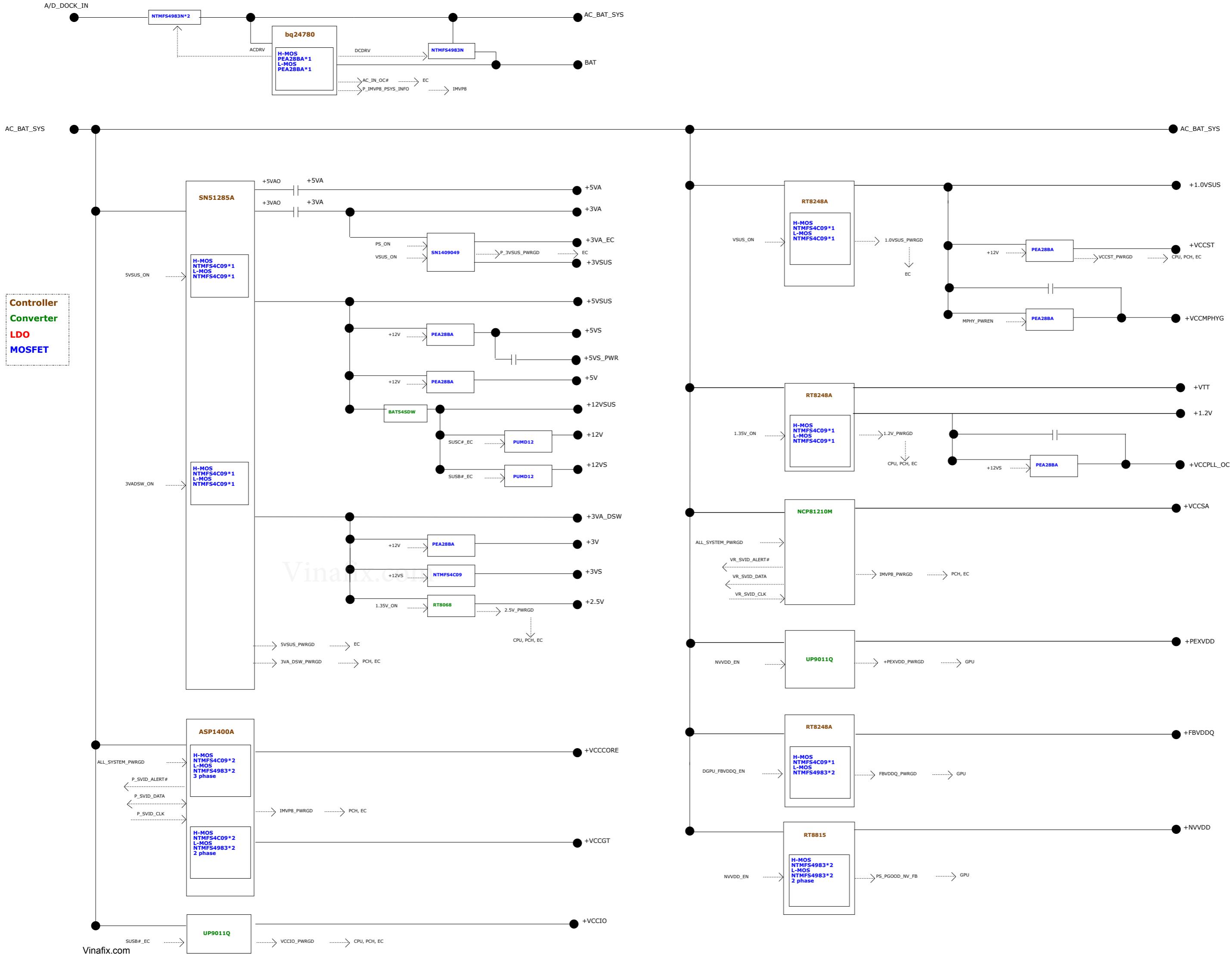
+PEX_VDD [For DGPU]



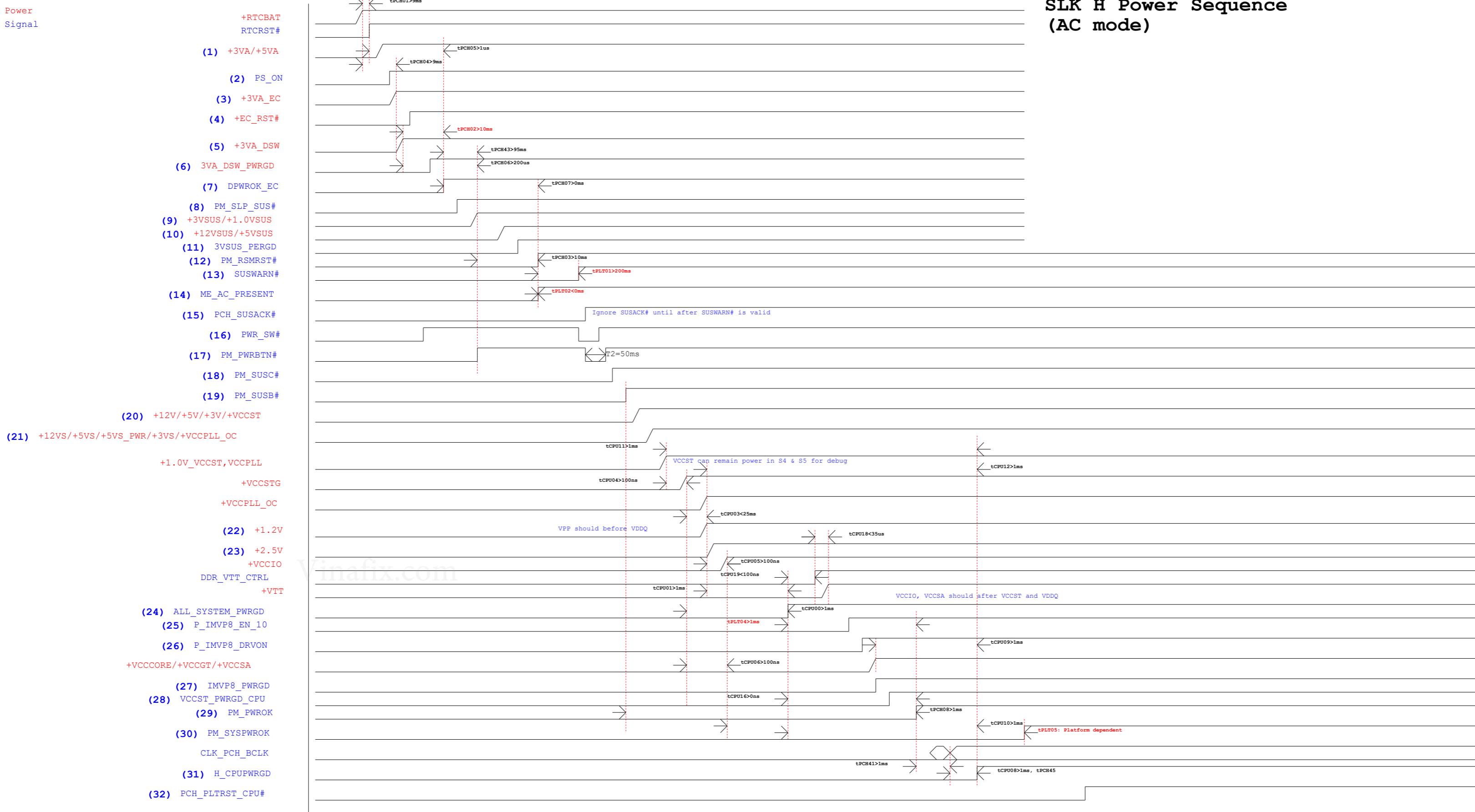
PR9221	UP1740Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

+FBVDDQ [For VRAM]

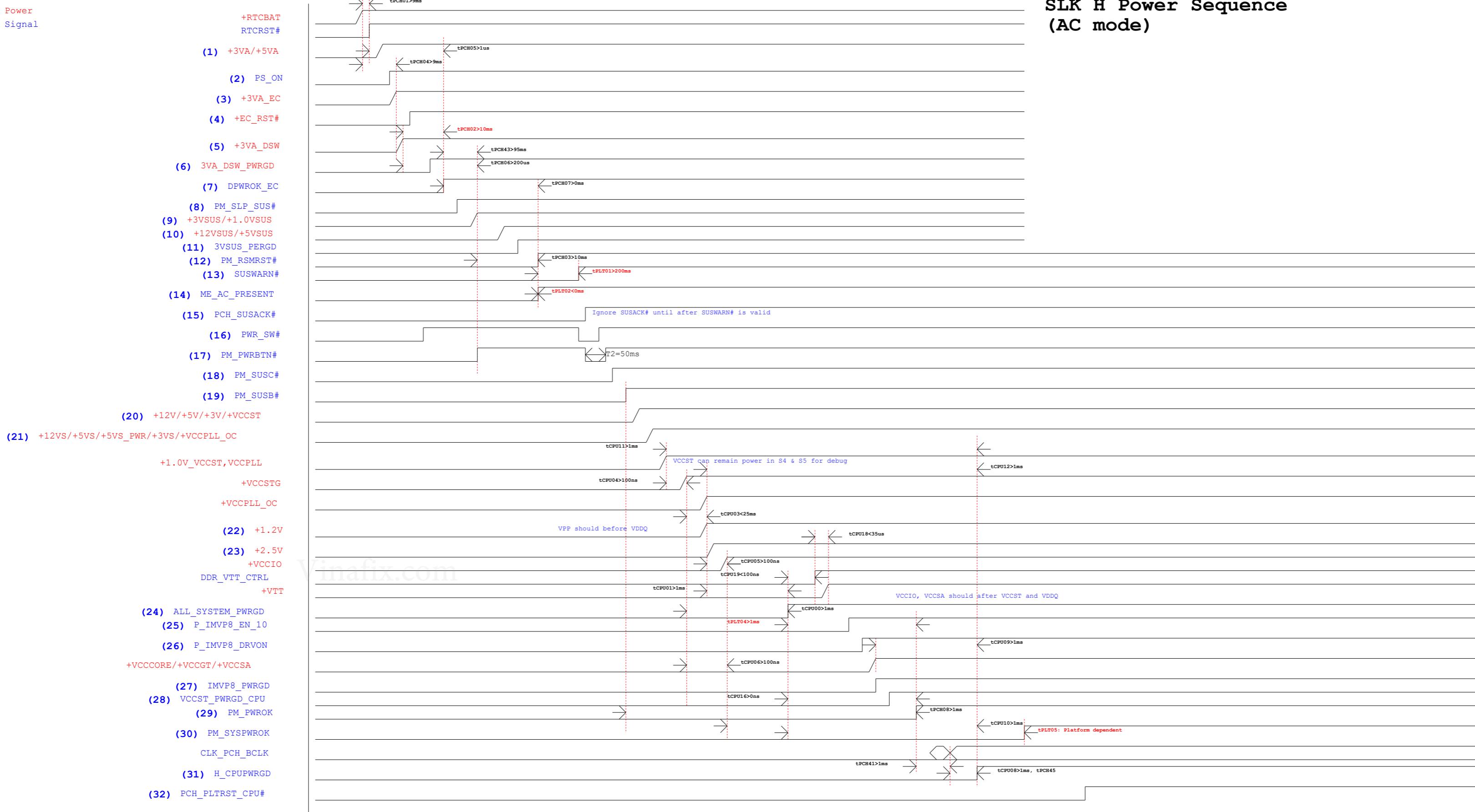




AC-IN Mode



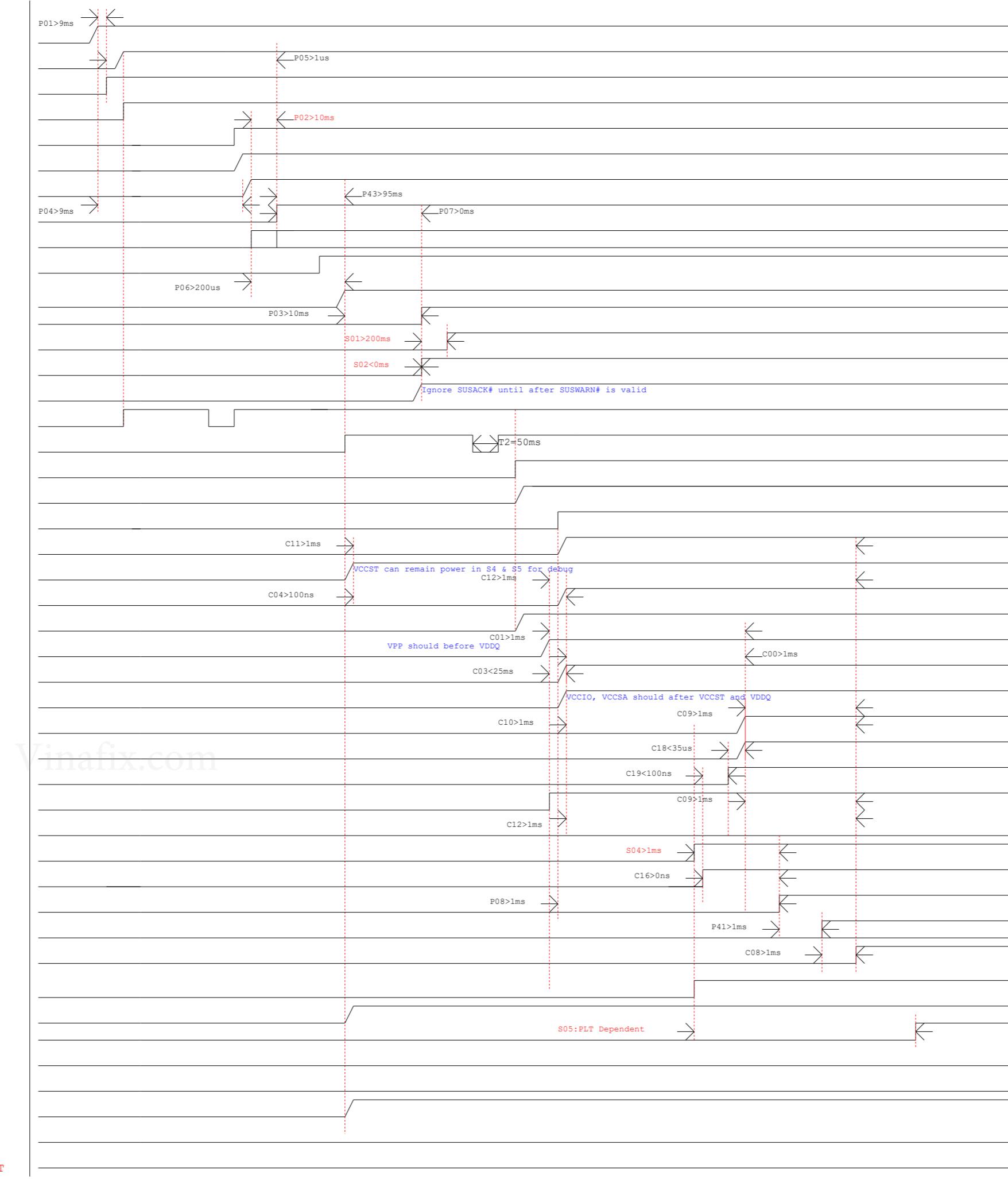
AC-IN Mode



SLK H Power Sequence (AC mode)

DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
 P:PCH (AC_BAT_SYS)+3VA/+5VA
 S:PLT (+3VA_RTC) RTCRST# (PCH)
 Power Signal (Power) AC_IN_OC# (EC)
 (EC) PS_ON (+3VA_EC)
 (PS_ON)+3VA_EC (EC)
 (3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
 (EC) DPWROK_EC (PCH)
 (+3VA_DSW) PM_BATLOW# (PCH)
 (PCH) PM_SLP_SUS# (EC)
 (VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
 (EC) PM_RSMRST#_PCH (PCH)
 (PCH) SUSWARN# (EC)
 (EC) ME_AC_PRESENT_PCH (PCH)
 (EC) PCH_SUSACK# (PCH)
 (PWR_Switch) PWR_SW# (EC)
 (EC) PM_PWRBTN# (PCH)
 (EC) SUSC_EC# (Power)
 (SUSC_EC#)+12V/+5V/+3V
 (EC) SUSB_EC# (Power)
 (SUSB_EC#)+12VS/+5VS/+3VS
 (VSUS_ON)+1.0V_VCCST, VCCPLL(VCCST_PWRGD)
 (+VCCIO)+VCCSTG
 (1.2V_ON)+2.5V(2.5V_PWRGD)
 (1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
 (+12VS)+VCCPLL_OC
 (SUSB_EC#)+VCCIO(VCCIO_PWRGD)
 (ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
 (DDR_VTT_CTRL)+0.6V
 (CPU) DDR_VTT_CTRL(Power)
 (Power) 1.2V_PWRGD(AND)
 (Power) IMVP8_PWRGD
 (AND) ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
 (ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
 (EC) PM_PWROK_PCH (PCH)
 (PCH) CLK_PCH_BCLK (CPU)
 (PCH) H_CPUPWRGD (CPU)
 (ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
 (CPU) P_SVID_DATA_X2 (Power)
 (EC) PM_SYSPWROK_PCH (PCH)
 (PCH) PLT_RST# (CPU/EC/Device)
 (P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
 (CPU) H_THERMTRIP# (PCH)
 (PCH) DDR4_DRAMRST# (Memory)
 +VCCGT



SLK H Power Sequence (DC mode)

Rev	Date	Description	Rev	Date	Description	Rev	Date	Description	Rev	Date	Description
2.0 Red	06/09/2015 First Release	1. Update Power schematic, 詳見GL552VW_PSR_DSN檔修改事項 20150609 2. 修改DDR_VTT_CTRL power plane to +3VS for 薦電Issue at p. 6 3. 修改Power Thermal sensor power protection at p. 28 4. change HDA power plane to +3VS power with Intel confirm at p. 26 5. change R208 & R2005 to 3.3KOHM pull-high follow VC at p. 20 6. Change net name SUS_CLK# to SUS_CLK_X1 at p. 20 7. fix Samsung 禁用料 at p. 3, 6, 22, 40, 47, 59, 62, 69, 70, 71, 76, 77, 83, 84, 86, 87, 88, 91, 92, 93 8. add Intel QS sample ASUS PIN at p. 3 & 20									
06/10/2015		1. mont R7599 for Power request at p. 75 2. unmont SPI IO3 circuit for Intel QS Sample at p. 28 3. Update Power schematic, 詳見GL552VW_PSR_DSN檔修改事項 20150610									
06/12/2015		1. change [ARGOSY] Type-C Connector to Pin 長 1.1mm at p.47 2. change SSD NUT at p. 65									
06/12/2015 v2		1. PU801由POWER SW_UP9020BF86_00/06016-01110000上件 改為POWER SW_APL3527GHAI-TRQ(06016-00160300)上件 2. PC8837由MLCC 1UF/16V(0603)XTR 10%/(11G233110511030)上件 改為MLCC 4.7UF/16V (0603) XSR 10%/(11204-0003F000)上件									
06/12/2015 v3		1. add DSG circuit for +12V & +12VS follow VC at p. 57									
06/17/2015		1. DRAMRST# issue, change C2008, C1402 & C1501 for EMI & VC at p. 14, 15 & 20. 2. 預留 CLK_24M 0 ohm EMI at p. 22 3. Add Varister for EMI request at p. 6, 20, 30, 40, 58									
06/18/2015		1. PR8056由RES 20K OHM 1/16W (0402) 1%/(10G21220214030)上件改為 RES 40.2K OHM 1/16W (0402) 1%/(10G212402214010)上件 2. Update GPIO Table at p. 2									
06/22/2015		1. 預留SPI_IO3 PU電阻 R2851 for Intel at p. 28 2. change RTC small at p. 20 3. change 0 Ohm to 0.1uF for EA Audio test at p. 6 4. PR8117由RES 2.2 OHM 1/10W(0603)5%/(10G2132R2003010)上件改為 RES 10 OHM 1/16W (0402) 1%/(10G2127R014030)上件 5. PC8837由MLCC 4.7UF/16V (0603) XSR 10%/(11204-0003F000)上件 改為MLCC 1UF/6.3V (0402) XSR 10%/(11G232210515070)上件									
06/23/2015		1. SSD Thermal Sensor 上件, CPU Thermal Sensor 不上件 at p. 50 2. 預留0 Ohm for EMI BCLK at p. 20 3. change 0 Ohm to 5.1 Ohm for EMI request at p. 6									
06/23/2015 v2		1. change 5.1 Ohm to PCH for EMI request at p. 6 & 22 2. PCE8402 CAP PL 15UF/25V 7343 SMD(11020-00275100)由不上件改上件 3. PCE9200 CAP PL 22UF/25V 4.6*6.3 20%/(11032-0006F000)由不上件改上件									

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+RTCBAT->3.3V
RTCCLK->on
RTC_RST->High

AC-IN Mo

AC TN OC->T

