FURKAN ERCAN

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EDUCATION

McGill University *October 2020*
Ph.D., Electrical & Computer Engineering
Research: Advanced Polar Code Decoder Algorithms & Implementations for the 5G New Radio

Middle East Technical University *June 2015*
M.Sc., Sustainable Environment & Energy Systems
Research: Energy-Efficient Multiplier VLSI Architectures & Design

Middle East Technical University *June 2011*
B.Sc., Electrical & Electronics Engineering (1^{st} Rank in Department)

WORK EXPERIENCE

Intel Corporation Dec 2022 - Present
Staff Research Scientist/Engineer *Hudson, MA, USA*

- Spearheading algorithm development and hardware implementations for cutting-edge reconfigurable systems tailored to next-generation space-based communications.
- Orchestrating the design and optimization of multiple error-correcting code architectures within a singular communication node, aimed at bolstering and future-proofing prevalent communication standards.
- RTL design utilizing SystemVerilog, in tandem with golden reference modeling, MATLAB Coder for stimulus generation, and Simulink HDL Coder for the creation of system-level RTL models.
- Conducting comprehensive validation and lint checks and fostering cross-validation collaboration with fellow project teams to ensure a holistic approach to development.
- In preparation of patents in advanced wireless and optical wireless communication techniques, centering on state-of-the-art error correction codes, spanning both algorithm and implementation levels.

Boston University Nov 2021 - Dec 2022
Postdoctoral Associate *Boston, MA, USA*

- Spearheaded the development of cutting-edge algorithms, software, and hardware implementations for the next generation of universal decoding techniques.
- Engineered a dynamic software framework for the GRAND algorithm family in C++, offering configurable options for error correction codes, channel characteristics, modulation schemes, and decoder settings. This versatile framework served as the backbone for algorithm design, statistical analysis, profiling, hardware testing, metadata generation in precise bit-exact forms, and optimization of memory/runtime utilization.
- Pioneered the creation of novel software-based physical layer security algorithms to counteract intricate channel conditions like jamming and interference. Employed innovative in-decoder detection and estimation methods grounded in random processes.
- Provided guidance and management in the development of microchips for the forthcoming ultra low-energy universal decoder. Contributed expertise in optimizing hardware resources, conducting pre-silicon validation, and executing critical feature testing.

Octasic Inc. Jun 2020 - Aug 2021
5G PHY Algorithm Developer *Montréal, QC, Canada*

- Drove the design and optimization of cutting-edge 5G PHY Wireless Protocol Systems. This encompassed the complete lifecycle, from developing MATLAB reference models to fine-tuning embedded C/ASM DSP implementations. Proficiently conducted memory and runtime profiling to ensure optimal performance.

- Executed MATLAB/C co-development through MEX subroutines, facilitating seamless development and comprehensive testbenching of proprietary wireless chips.
- Orchestrated the entire 5G polar encoder and decoder chain for both downlink and uplink channels, contributing to the advancement of essential components of 5G communication systems.
- Spearheaded the optimization of the 5G polar decoder across various tiers, spanning algorithmic enhancements to SIMD-level optimizations. This transformation rendered it not only highly flexible but also exponentially faster than existing in-house solutions.
- Profoundly engaged with critical components of the 5G PHY, encompassing PDCCH, PBCH, PUCCH channels, as well as expertise in LDPC codes.
- Demonstrated a personal track record of rapid learning, proactive initiative-taking, adeptness in adapting to new challenges, and the ability to execute efficient debugging.

McGill University Sep 2015 - Oct 2020
Teaching & Research Assistant *Montréal, QC, Canada*

- Pioneered the development of a comprehensive C++ framework encompassing a wide array of polar code decoder algorithms. This framework included meticulously designed bit-exact versions with quantization for streamlined hardware development, debugging, and rigorous testing.
- Masterminded the creation of multiple advanced post-synthesis polar decoder architectures in hardware. These architectures consistently showcased remarkable performance metrics, excelling in throughput, latency, area/energy efficiency, and unparalleled error correction capabilities.
- Played an instrumental role in shaping and delivering coursework, notably contributing to subjects like Computer Organization, Digital System Design, and Digital Logic. Efforts in designing and conducting these courses enriched the educational experience for students.

Middle East Technical University Sep 2012 - Jun 2015
Teaching & Research Assistant *Ankara, Turkey*

- Spearheaded the design and execution of coursework spanning Digital Logic, Electronics, Computer Architecture, and VLSI Design. Ensured engaging and comprehensive learning experiences for students across diverse subjects.

Intel Corporation Jul 2011 - Jul 2012
Graduate Intern (Full-Time) *Hillsboro, OR, USA*

- Took a pivotal role in the development, implementation, and validation of system-level energy-aware power management policies on the Nehalem architecture. This included targeted optimization for CPUs and RAMs.
- Garnered hands-on familiarity with Intel's cutting-edge server and PC architecture platforms, and conducted analyses utilizing the SPEC CPU benchmark.

ASELSAN Summer 2010
Summer Intern (Full-Time) *Ankara, Turkey*

- Drove the optimization of wireless signal processing software on software-defined radio products, contributing to enhanced performance and efficiency.

TECHNICAL STRENGTHS

Strengths	RTL Development & Validation, Reference Modeling, Algorithm Development
Languages	System Verilog, C/C++, MATLAB, Simulink, VHDL, LaTeX, ASM
Tools & Platforms	ASIC, FPGA, Quartus, Xilinx, Visual Studio, ModelSim, Questa, Cadence, Git, SVN

BOOK CHAPTERS

1. S. M. Abbas, M. Jalaleddine, **F. Ercan**, T. Tonnellier, W. J. Gross, "Hardware Architecture for GRAND with ABandonment (GRANDAB)", in *Guessing Random Additive Noise Decoding*, pp. 21-38, Springer, 2023.

2. S. M. Abbas, M. Jalaleddine, **F. Ercan**, T. Tonnellier, W. J. Gross, "Hardware Architecture for Ordered Reliability Bits GRAND (ORBGRAND)", in *Guessing Random Additive Noise Decoding*, pp. 39-71, Springer, 2023.

JOURNAL PUBLICATIONS

1. S. M. Abbas, T. Tonnellier, **F. Ercan**, M. Jalaleddine, W. J. Gross, "High-Throughput and Energy-Efficient VLSI Architecture for Ordered Reliability Bits GRAND", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 6, pp. 681-693, 2022.
2. **F. Ercan**, T. Tonnellier, N. Doan, W. J. Gross, "Practical Dynamic SC-Flip Decoders: Algorithm and Implementation", *IEEE Transactions on Signal Processing*, vol. 68, pp. 5441-5456, 2020.
3. N. Doan, S. A. Hashemi, **F. Ercan**, T. Tonnellier, W. J. Gross, "Neural Successive Cancellation Flip Decoding of Polar Codes", *Journal of Signal Processing Systems*, vol. 93, pp. 631–642, 2021.
4. **F. Ercan**, T. Tonnellier, W. J. Gross, "Energy-Efficient Hardware Architectures for Fast Polar Decoders", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 1, pp. 322-335, 2020.
5. **F. Ercan**, T. Tonnellier, C. Condo, W. J. Gross, "Operation Merging for Hardware Implementations of Fast Polar Decoders", *Journal of Signal Processing Systems*, vol. 91, no. 9, pp. 995-1007, 2019.
6. C. Condo, S. A. Hashemi, A. Ardakani, **F. Ercan**, W. J. Gross, "Design and Implementation of a Polar Codes Blind Detection Scheme", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 943-947, 2019.
7. **F. Ercan**, C. Condo, W. J. Gross, "Improved Bit-Flipping Algorithm for Successive Cancellation Decoding of Polar Codes", *IEEE Transactions on Communications*, vol. 67, no. 1, pp. 61-72, 2019.
8. S. A. Hashemi, C. Condo, **F. Ercan**, W. J. Gross, "Memory-Efficient Polar Decoders", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 7, no. 4, pp. 604-615, 2017.

CONFERENCE PUBLICATIONS

1. A. Riaz, Z. E. Kizilates, A. Yasar, **F. Ercan**, W. An, K. Galligan, M. Medard, K. R. Duffy, R. T. Yazicigil, "Universal Soft-Detection Decoder with Ultra-Low Energy Consumption using ORBGRAND", in *IEEE 24th International Symposium on a World of Wireless, Mobile and Multimedia Networks (WoWMoM)*, 2023.
2. **F. Ercan**, K. Galligan, D. Starobinski, M. Medard, K. R. Duffy, and R. T. Yazicigil, "GRAND-EDGE: A Universal, Jamming-resilient Algorithm with Error-and-Erasure Decoding", in *IEEE International Conference on Communications* **(ICC)**, 2023.
3. A. Riaz, A. Solomon, **F. Ercan**, M. Medard, R. T. Yazicigil, K. R. Duffy, "Noise Recycling using GRAND for Improving the Decoding Performance", in *15th International Conference on Communication Systems & Networks*, 2023.
4. **F. Ercan**, K. Galligan, K. R. Duffy, M. Medard, D. Starobinski, R. T. Yazicigil, "A General Security Approach for Soft-information Decoding against Smart Bursty Jammers", in *IEEE GLOBECOM Workshops*, 2022.
5. A. Riaz, A. Solomon, **F. Ercan**, M. Medard, K. R. Duffy, R. T. Yazicigil, "Interleaved Noise Recycling using GRAND", in *IEEE International Conference on Communications* **(ICC)**, 2022.
6. N. Doan, S. A. Hashemi, **F. Ercan**, W. J. Gross, "Fast SC-Flip Decoding of Polar Codes with Reinforcement Learning", in *IEEE International Conference on Communications* **(ICC)**, 2021.
7. S. M. Abbas, T. Tonnellier, **F. Ercan**, M. Jalaleddine, W. J. Gross, "High-Throughput VLSI Architecture for Soft-Decision Decoding with ORBGRAND", in *IEEE International Conference on Acoustics, Speech, and Signal Processing* **(ICASSP)**, 2021.
8. S. M. Abbas, T. Tonnellier, **F. Ercan**, W. J. Gross,
"High-Throughput VLSI Architecture for GRAND",
in *IEEE International Workshop on Signal Processing Systems* **(SiPS)**, 2020.
9. **F. Ercan**, W. J. Gross, "Fast Thresholded SC-Flip Decoding of Polar Codes", in *IEEE International Conference on Communications* **(ICC)**, 2020.
10. **F. Ercan**, T. Tonnellier, N. Doan, W. J. Gross, "Simplified Dynamic SC-Flip Polar Decoding", in *IEEE International Conference on Acoustics, Speech, and Signal Processing* **(ICASSP)**, 2020.
11. N. Doan, S. A. Hashemi, **F. Ercan**, T. Tonnellier, W. J. Gross, "Neural Dynamic Successive Cancellation Flip Decoding of Polar Codes", in *IEEE International Workshop on Signal Processing Systems* **(SiPS)**, 2019.

12. **F. Ercan**, C. Condo, S. A. Hashemi, W. J. Gross, "Partitioned Successive-Cancellation Flip Decoding of Polar Codes", in *IEEE International Conference on Communications* **(ICC)**, 2018.
13. C. Condo, **F. Ercan**, W. J. Gross, "Improved successive cancellation flip decoding of polar codes based on error distribution", in *IEEE Wireless Communications and Networking Conference Workshops* **(WCNCW)**, 2018.
14. S. A. Hashemi, C. Condo, **F. Ercan**, W. J. Gross, "On the Performance of Polar Codes for 5G eMBB Control Channel", in *Asilomar Conference on Signals, Systems, and Computers* **(ACSSC)**, 2017.
15. **F. Ercan**, C. Condo, W. J. Gross, "On Error-Correction Performance and Implementation of Polar Code List Decoders for 5G", in *Annual Allerton Conference on Communication, Control, and Computing* **(Allerton)**, 2017.
16. **F. Ercan**, C. Condo, W. J. Gross, "Reduced-memory high-throughput fast-SSC polar code decoder architecture", in *IEEE International Workshop on Signal Processing Systems* **(SiPS)**, 2017.
17. **F. Ercan**, A. Muhtaroglu, "Power-delay analysis of an ABACUS parallel integer multiplier VLSI implementation", in *IEEE International Conference on Energy Aware Computing Systems & Applications* **(ICEAC)**, 2015.
18. **F. Ercan**, A. Muhtaroglu, "Comparative power-delay performance analysis of threshold logic technologies", in *IEEE International Conference on Energy Aware Computing Systems & Applications* **(ICEAC)**, 2015.
19. **F. Ercan**, A. Muhtaroglu, "Energy-delay performance of capacitive threshold logic (CTL) circuits for threshold detection", in *IEEE International Conference on Energy Aware Computing Systems and Applications* **(ICEAC)**, 2014.
20. **F. Ercan**, M. Yenen, M. Fahrioglu, "Method and Case Study for Wind Power Assessment in Cyprus", in *Renewable Energy Sources Symposium*, 2013.
21. M. Yenen, **F. Ercan**, M. Fahrioglu, "Solar Thermal System Analysis of Northern Cyprus", in *Renewable Energy Sources Symposium*, 2012.
22. **F. Ercan**, N. A. Gazala, H. David, "An integrated approach to system-level CPU and memory energy efficiency on computing systems", in *IEEE International Conference on Energy Aware Computing* **(ICEAC)**, 2012.

LEADERSHIP & PROFESSIONAL ACTIVITIES

Ongoing Associate Editor in IEEE Communications Letters.
Ongoing Lead Guest Editor in MDPI Special Issue VLSI Architectures for Wireless Communications and Digital Signal Processing.
Ongoing Active member of IEEE Wireless Communications Technical Committee.
Ongoing Reviewer for numerous top-tier international conferences and journalsin multiple fields such as Wireless Communications, Circuits & Systems, Digital Signal Processing.
2022 Technical Committee Co-Chair of IEEE Future Networks World Forum 2022.
2022 Technical Program Chair of IEEE Vehicular Technology Conference - 2022 Spring & 2022 Fall.
2021 Vice-Chair of IEEE Montreal Section.
2021 Demos & Exhibits Co-Chair of IEEE 5G World Forum 2021.
2021 Lead organizer and panelist of IEEE Montreal Section Keynote Event 2021.
2021 Technical Organization Committee at IEEE ICC 2021 Women in Engineering Panel.
2018 Volunteer instructor at Montréal Turkish Community Center for pre-college education.
2017 Volunteer coordinator in 5^{th} IEEE Global Conference on Signal and Information Processing Conference.
2016 Chair of McGill IEEE Student Branch.
2013 Graduate Program Student Representative at Middle East Technical University NCC.
2012 Technical organization of 3^{th} IEEE International Conference on Energy Aware Computing Systems.
2011 Founder and chair of IEEE METU NCC Student Branch.
2010 Technical organization of Mediterranean Microwave Symposium (MMS).

AWARDS

2024 Intel Patent Award.
2023 Intel IDP Divisional Recognition Award.
2023 Best Demo Award at IEEE COMSNETS Conference.
2021 Exemplary Keynote Organization Award by the IEEE Montreal Section.

2020 IEEE Communications Society Student Grant Award for ICC 2020.
2020 Third place in the province at Quebec Engineering Competition Graduate Research Track.
2019 First place award at McGill Engineering Competition Graduate Research Track for the oral presentation featuring "Energy-efficient hardware architectures for fast polar decoders".
2019 Second place award at the 6th IEEE Montreal Research Boost for the poster presentation titled "Energy-efficient polar decoders for 5G and beyond".
2018 Outstanding Teaching Assistant Award from the Faculty of Engineering, McGill University for tutoring Digital System Design course.
2018 Graduate Research Enhancement and Travel (GREAT) award for conference paper at IEEE Wireless Communications and Networking Conference (WCNC), Barcelona, Spain.
2017 Exemplary Student Branch Award for chairing McGill IEEE Student Branch.
2015 McGill Engineering Doctoral Award (Roger Boudreault Doctoral Fellowship).
2015 Best Paper Award at the 5th International Conference on Energy Aware Computing Systems & Applications (ICEAC) 2015, Cairo, Egypt.
2007-2011 Dean's List throughout the B.Sc. degree.

RESOURCES

Personal Webpage / **LinkedIn** / **Google Scholar** / **GitHub** /

ResearchGate / **Web of Science**