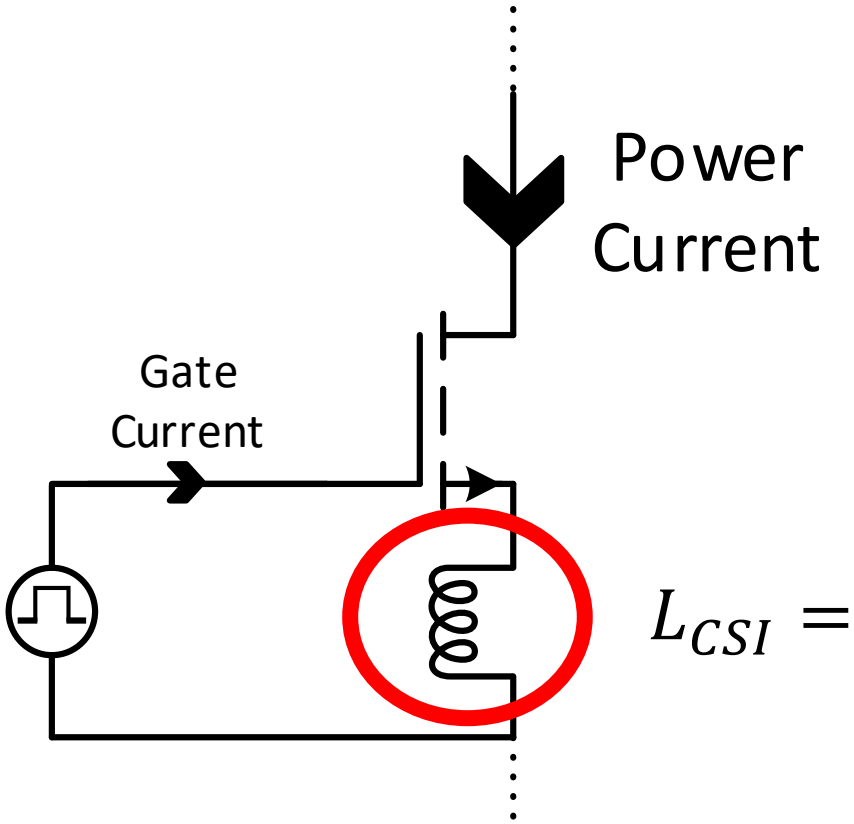
Common Source Inductance (CSI)



$$L_{CSI} = L_s + M_{pg}$$

Common Source Inductance is caused by

- Common path for power loop and gate loop currents

and/or

- Mutual coupling from power loop to gate loop

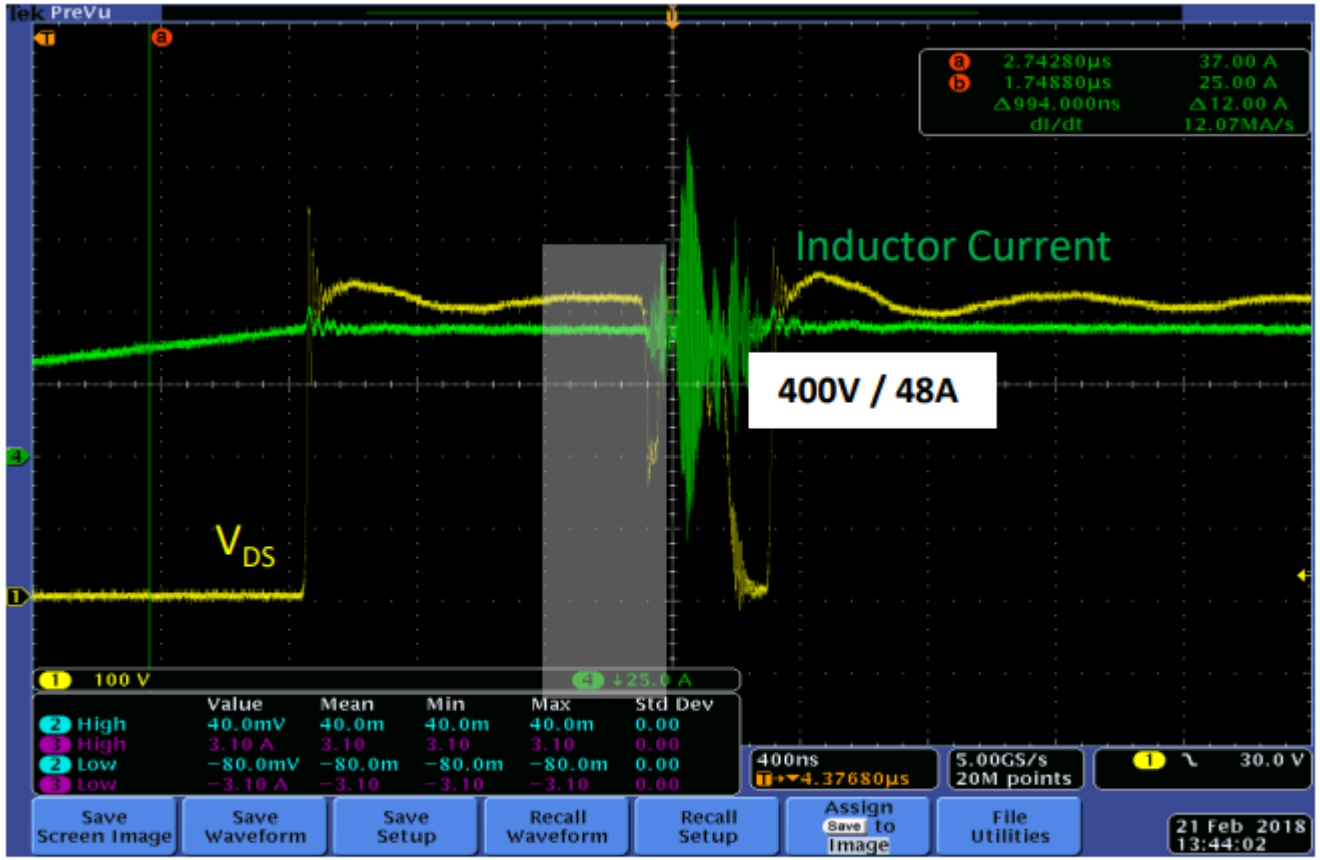
Common Source Inductance (CSI)

Effects of Parasitics

Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} L_{D1-4}	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{S1}-L_{S4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	Smaller the better, as equal as possible for paralleled devices
L_{QS1-6}	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	

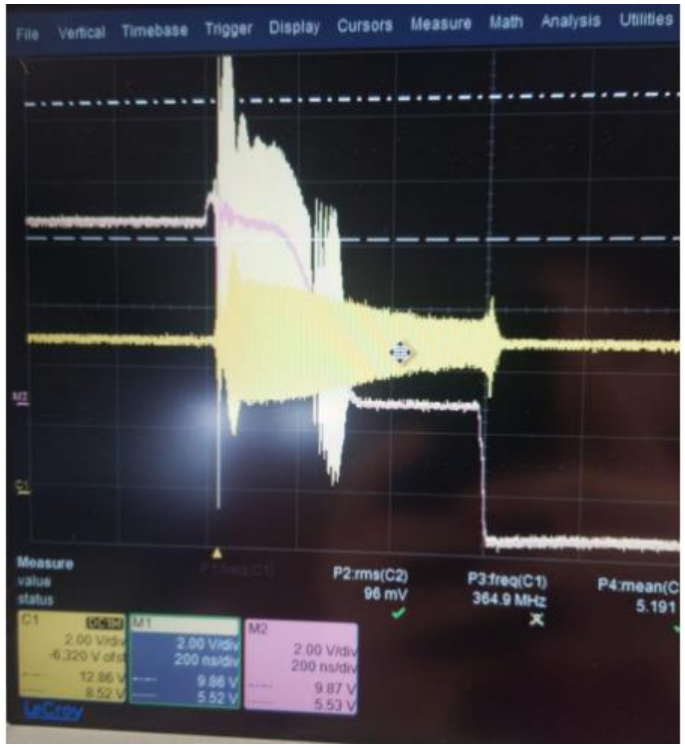
It is very important to keep this inductance as minimum as possible.

Common Source Inductance (CSI)



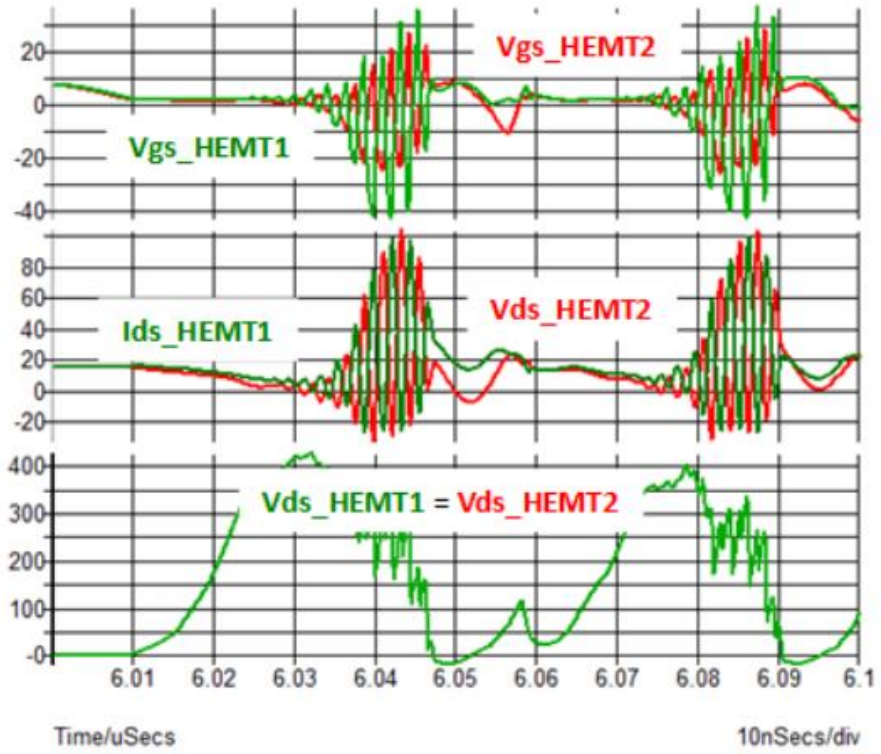
Example of an unsuccessful design caused by unbalanced quasi-common source inductance

This oscilloscope view is from GaNSystem's App. Note
and
This is very similar what we see on oscilloscope



Common Source Inductance (CSI)

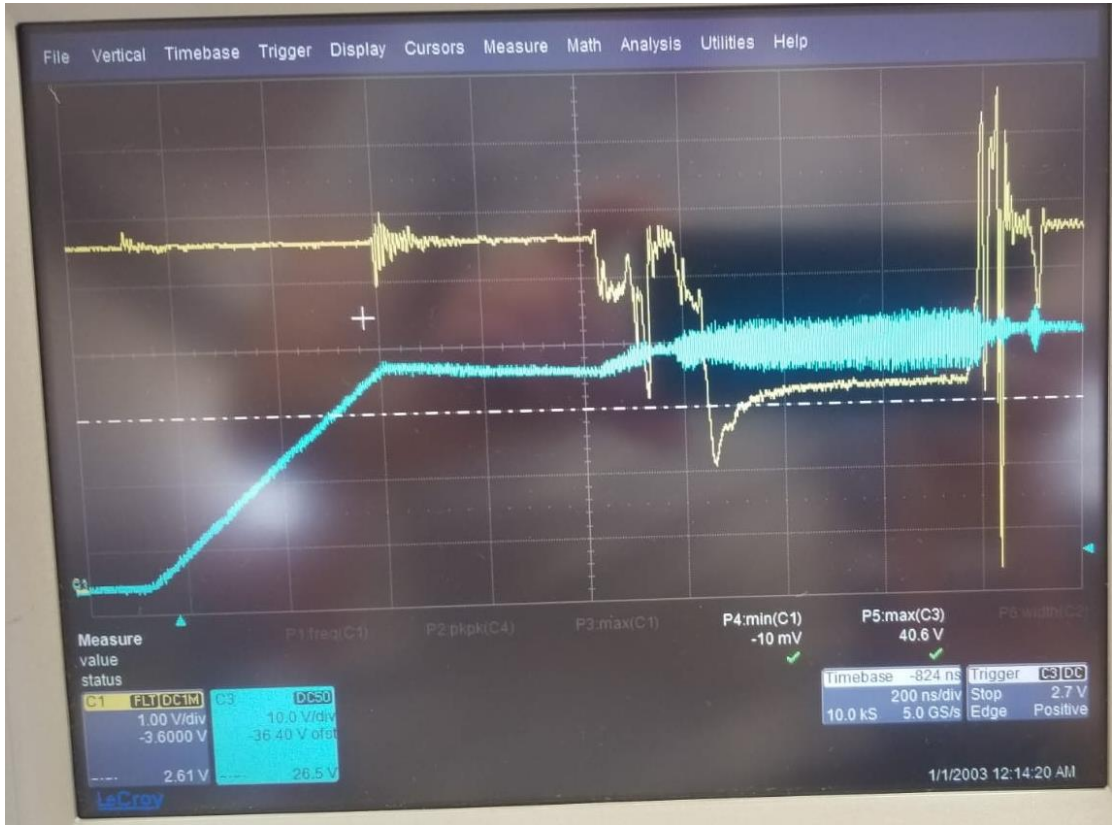
«1nH difference between the common-source inductance (Ls1 and Ls2) of two paralleled GaN HEMTs will result in the huge ringing on the gate, which will mis-trigger switches or damage the gate.»



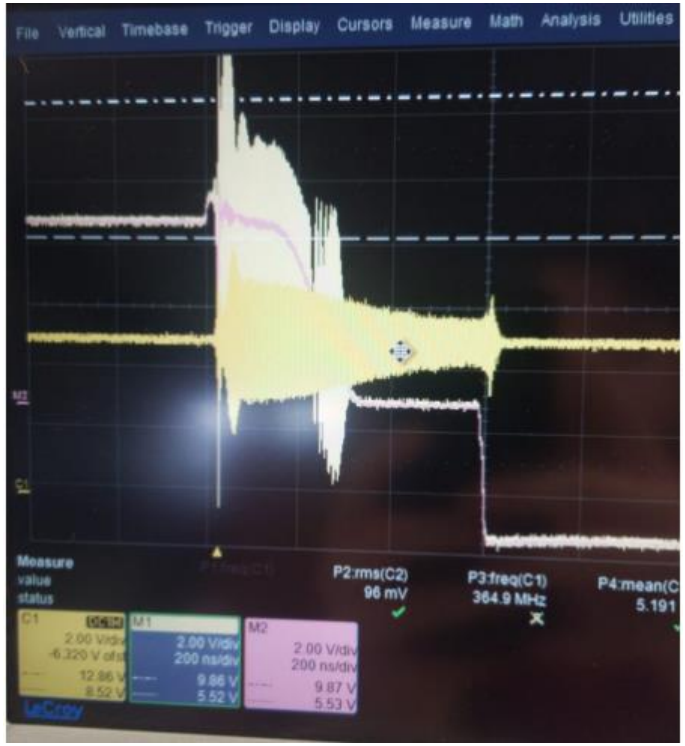
J. Lu, H. Bai, A. Brown, M. McAmmond, D. Chen, and J. Styles, "Design consideration of gate driver circuits and PCB parasitic parameters of paralleled E-mode GaN HEMTs in zero-voltage-switching applications," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, vol. 2016-May, pp. 529–535.

Common Source Inductance (CSI)

Interestingly, we experience the oscillation only when high side transistor is being turned-on and the current is at higher levels (high dI/dt)



DPT Waveform



SC Test Waveform

Interestingly, we experience the oscillation only when high side transistor is being turned-on and the current is at higher levels (high dI/dt) but nothing happens for the low side.

Low Side Transistors	Left Transistor	Right Transistor
Negative Gate Loop	1.8 nH	2.03 nH
Positive Gate Loop	1.93 nH	1.65 nH
Mutual to NGL	46 pH	20 pH
Mutual to PGL	33 pH	11 pH

Mutual coupling between power loop and gate loops are very low for Low Side transistors

What about the high side transistors?

Common Source Inductance (CSI)

High Side Transistors	Left Transistor	Right Transistor
Negative Gate Loop	3.88 nH	4.04 nH
Positive Gate Loop	4.14 nH	4.23 nH
Mutual to NGL	114 pH	117 pH
Mutual to PGL	545 pH	554 pH

We have the greatest CSI for high side turn-on gate loop and we are experiencing oscillations only for those transitions

→ Okay, but is 0.5 nH that big?

↓ We saw that SC current increases with 6.7 A/ns speed.

↓ $$V_{CSI} = M_{PG} * \frac{dI}{dt} = 0.5 * 6.7 = 3.35\ V$$

← 3.35V is a lot to be on the gate loop considering the threshold level of transistor (1.7V)

Common Source Inductance (CSI)

What can we do to solve this problem?

New design with a proper gate loop on high side

Increase the turn-on resistance for high-side

Considering soft switching nature of our topology, we can continoue with this option for now.