

Dear Prof. Joseph Olorunfemi Ojo,

Tennessee Tech University, USA

Editor-in-Chief,

IEEE Journal of Emerging and Selected Topics in Power Electronics

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We would like to submit the enclosed manuscript entitled “*Layout Based Ultra-Fast Short-Circuit Protection Technique for Parallel Connected GaN HEMTs*,” which we wish to be considered for publication in IEEE Journal of Emerging and Selected Topics in Power Electronics. The novelty of the paper is sensing the induced voltage on the layout for detection of short-circuit fault on a parallel GaN HEMTs configuration. The implementation of short-circuit protection techniques on parallel configuration is not studied for GaN HEMTs in the literature. It is experimentally shown that the proposed method is able to detect short-circuit fault within 40 ns and it does not harm the normal switching operation.

The paper is composed according to IEEE Journal of Emerging and Selected Topics in Power Electronics journal submission format. No conflict of interest exists in the submission of this manuscript, and manuscript is approved by all authors for publication. The paper is an original piece and not under consideration for publication elsewhere.

I appreciate your consideration of our manuscript, and I look forward to receiving comments from the reviewers.

Kind regards,

Dr. Ozan Keysan