Layout Based Ultra-Fast Short-Circuit Protection Technique for Parallel Connected GaN HEMTs

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***Abstract*—Gallium Nitride Enhancement-Mode High Electron Mobility Transistors (GaN HEMTs) are subject to high power density converter circuits thanks to their superior efficiency, higher switching speed and small package size. However, increased switching speed results in a dramatic increase in short circuit (SC) current under a shoot-through fault. GaN HEMTs can withstand the SC current only for several hundred nanoseconds. Therefore, proactive SC protection solutions are critical for protecting power circuits. In this paper, an ultra-fast short-circuit protection technique based on sensing the voltage created by high slew rate of SC current on parasitic inductance of printed circuit board (PCB) layout is proposed. In the proposed design, an industrial example for parallel connected GaN HEMTs in a half-bridge configuration is implemented. In order to inhibit any over-voltage breakdown risk, a soft turn-off mechanism is utilized upon SC detection which discharges gate-source voltage slowly instead of a fast turn off. Experimental results show that the proposed protection technique is able to detect SC fault within 45 ns and fault is completely cleared in 550 ns. As a result of optimized layout design, voltage overshoot is X V under 300V / 30A switching condition. In addition, performance results of normal switching operation are provided to show the proposed technique does not affect the natural switching performance of GaN HEMTs.**

***Index Terms*—Circuit faults, Gallium Nitride, GaN HEMTs, Transistor paralleling, Layout design, Short circuit protection**

I. Introduction

CURRENT trend in power electronics is to increase efficiency, reduce volume without sacrificing the reliability. Gallium-Nitride (GaN) High Electron Mobility Transistors (HEMTs) are perfectly suitable for this thanks to their superior switching performance, low conduction losses and small packages [1]. However, reliability of GaN HEMTs are weak in comparison to other transistors in terms of their short-circuit (SC) ruggedness. The critical SC energy of p-GaN HEMTs are 2-3 times lower than cascade GaN transistors and 30 times lower than SiC MOSFETs [2], [3]. In addition, GaN HEMTs are extremely susceptible to circuit noise due to their low threshold levels [4]. This sensitivity requires a very careful layout design in order to eliminate the risk of false turn-on, [5], which can trigger a SC fault.

In order to maintain safe operation, a fast and reliable SC detection method is necessary. The protection technique should be capable of detecting fault and ceasing it in less than 500 ns if DC bus voltage is higher than 350V [6]. There are several methods reported in literature satisfying this requirements.

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The first basic method is adding a series resistor or a current sensor in series with GaN HEMTs to follow SC current [7]. A series resistor should be small enough to decrease power loss but in this case the sensed voltage gets lower and can be distorted easily [4]. The current sensors are not practical because they do not have enough current range or enough bandwidth for SC detection [8]. Also, adding a component in series increases the power loop inductance and reduces the switching performance [9].

Another method commonly referred is the desaturation technique which is basically used for sensing drain-source terminal voltage of GaN HEMTs. This technique suffers from its long settling time [7], [9]–[11]. Moreover, the diodes adds capacitive loading in parallel with the output capacitance of transistor and it increases the switching losses [10]. Lastly, due to high temperature dependence of conductivity [2], it is hard to set a reference level for desaturation technique [8].

More developed solutions are proposed in [6], [9], [10], [12]. The relation between gate current and drain current of GaN Gate Injected Transistors (GITs) is used for detecting SC fault in [10]. However, this is not applicable for GaN HEMTs because of their voltage driven gate structure. In [6], the sharp decrease on by-pass capacitors voltage is detected for identifying SC fault and desaturation technique is applied to verify it. However, this method is incapable of detecting SC for lower DC voltages and it includes the disadvantages of desaturation technique such as increased output capacitance. In both [6], [9], a soft turn-off (STO) mechanism is successfully adapted to prevent GaN HEMTs from over-voltage break down risk. In [9], the drain-source voltage is sensed like desaturation which has the similar weak characteristics: increased output capacitance and relatively hard identifiable threshold levels due to temperature dependency. In [12], a discrete protection circuit is proposed for parallel connected GaN HEMTs. However, this method is only applicable to specific devices which have packages with dual-gate pads.

Another technique is sensing the voltage on the printed circuit board (PCB) layout inductance induced by high dI/dt of SC current. It is capable of detecting SC fault faster than desaturation and as a result maximum fault current is reduced almost 20% [13]. This method is applied in [14] on a prototype and it is capable of detecting the fault in a couple of dozen of nanoseconds. However, sensing the voltage across an inductance is criticized for increasing the layout parasitics, [9], which results in higher switching losses.

In this paper, a similar method to [14], sensing the voltage across by layout inductance is applied on an industrial level

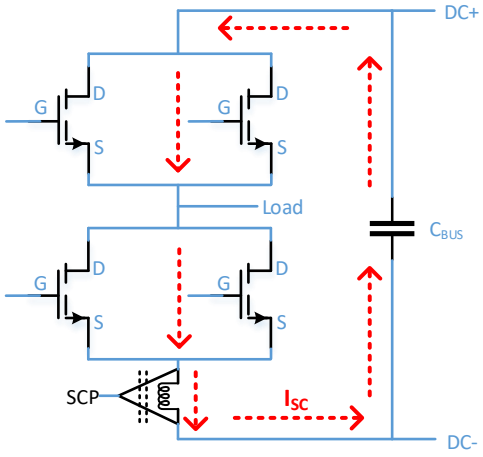

Fig. 1. Circuit schematic of half-bridge

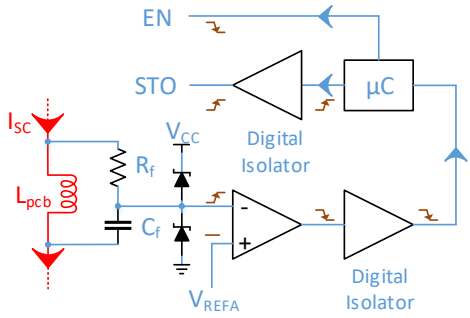

Fig. 2. Short circuit protection mechanism

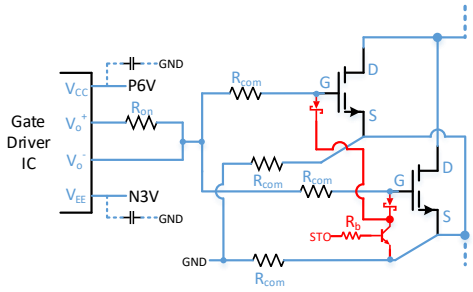

Fig. 3. Gate driver circuit schematic of parallel connected transistors (red components exist only for low side transistors for soft turn-off (STO))

half-bridge design where transistor paralleling is also applied for high-power applications. A SC fault can damage multiple number of GaN HEMTs for a parallel connected structure which increases the cost at least twice. In order to implement this SC protection, the power loop inductance and the coupling inductance for SC current sensing are characterized using a finite element analysis (FEA) tool. Also, a soft turn-off mechanism is employed to eliminate any risk of over-voltage breakdown when SC current is ceased. Experimental results show that this method does not deteriorate the layout inductance and it is capable of detecting SC fault in less than 50 ns. GaN HEMTs are completely turned off in less than 500 ns which ensures the safety of operation.

The rest of the paper is organized as follows. Section II describes the proposed protection technique and its operation. Section III presents the designed half-bridge employing parallel connected GaN HEMTs and application of the SC protection technique. In Section IV, experimental results are given to verify the proposed technique.

II. Theory of Operation

When a shoot-through type SC happens, the near bypass capacitors discharge through the transistors on the half-bridge. The stored energy on those capacitors leads SC current to reach harmful levels just in 100 ns to 200 ns. This energy transfer happens based on the components and circuit characteristics such as bus capacitance and inductance & resistance of the current path, i.e. PCB layout. The inductance of this path is called the power loop inductance. It is aimed to minimize the power loop inductance for normal switching operation. However, this minimized inductance leads SC current to increase rapidly which is a clear threat for GaN HEMTs.

As shown in Fig. 1, power loop is a closed current path which can be considered as tip to tip connected small layout portions. Note that, whenever a SC happens, all current flows through those portions as well. Since the change in current induces voltage on an inductance, a portion of the power loop can be used as a trigger for short-circuit protection (SCP) mechanism as illustrated in Fig. 2 without increasing the power loop inductance.

The induced voltage on the PCB trace due to SC current can be processed to detect SC faults. For this purpose, firstly, the sensed voltage, V_{SENSE} is filtered through a low-pass filter and it is compared with a reference level, V_{REF} to detect SC fault as given in Fig. 2. Whenever a SC fault is detected, a high frequency micro-controller (μC) is triggered to protect the circuit. The μC activates soft turn-off mechanism (STO) in order to diminish gate-source voltages of transistors. STO signal is applied to the base of a BJT which is connected between gate and source terminals of parallel connected transistors as shown in Fig. 3. Base resistor, R_b allows to control discharge time of stored gate charge. Therefore, turn-off speed of GaN HEMTs can be controlled. After soft turn-off process is completed, gate driver integrated circuit (IC) is disabled which results in complete turn-off.

A direct hard turn-off of transistors include a great risk of over-voltage breakdown. Although hard turn-off stops SC current immediately, it causes a voltage induction on power loop inductance as happened in regular switching operation. Since the SC current reaches extremely high levels, applying HTO causes high voltage induction which can go beyond the voltage rating of transistor easily. Therefore, a soft turn-off mechanism is a must and a Bipolar Junction Transistor (BJT) is used for this purpose in this design. As given in Fig. 3, a schottky diode is connected in series with BJT because a negative drive level of gate-source terminals could bias the NPN type BJT in reverse direction.

For the paralleled GaN HEMTs, a single BJT is used to ensure that parallel connected transistors turn-off simultane-

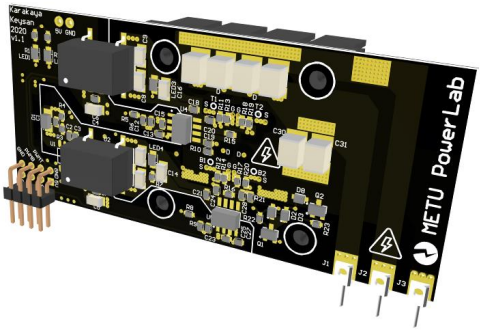

Fig. 4. Parallel switch half-bridge board with short circuit protection (90 mm (L), 40 mm (H), 30 mm (W))

ously. Otherwise, SC current might have to be carried by only one of them. Note that, SCP mechanism components and soft turn-off BJT are placed on low side of half-bridge because switching node has a varying voltage level. The rapid voltage transitions on the switching node could risk the common mode transition immunity (CMTI) ratings of isolated components and therefore, the digital signals might change state unpredictably.

III. Half-Bridge and SC Protection Design

The prototype parallel switch half-bridge board with short circuit protection is given in Fig. 4. In this design, GS66508T GaN HEMTs (650 V, 30 A) are used as device under test (DUT). The PCB is designed in a similar manner to manufacturer's evaluation board [15]. Even though this half-bridge is designed for a 4 kW bidirectional DC/DC converter operation, it can be used for different purposes. Multiple number of this half-bridge can be used to have different types of DC/DC converter or an inverter. The dimensions of the half-bridge board is 90 mm (L), 40 mm (H) and 30 mm (W).

A. Layout Design

A proper power loop layout design is critical for safe operation, especially for GaN HEMTs considering their rapid switching transition. Additionally, it is important to estimated voltage under SC fault for accurate detection. For this purpose, Finite Element Analysis (FEA) tool is required to solve and analyze the complex geometry of PCB. In this design, ANSYS Maxwell 3D tool is used for identifying PCB characteristics.

First of all, a symbolic view of PCB layout is shown in Fig. 5. The returning current path is placed to underneath of top copper layer so that the power loop inductance could be minimized. Also, an induced voltage on a portion of return path is sensed, which is defined as the sense loop. Moreover, a simplified geometry of these two loops can be modeled as given in Fig. 6. The current, which flows through the power loop, induces a voltage on the sense loop with a coupling factor of M_{PS}, as presented in (1). In order to identify the coupling factor, change rate of power loop current is used as control variable. According to Ampére's law (3) in quasi-static form, the current density, (2), creates a magnetic field ($\vec{B}$) which passes through the sense loop. The total flux linkage can be

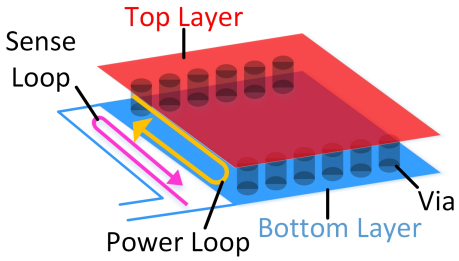

Fig. 5. A symbolic view of PCB layout for power loop and sense loop

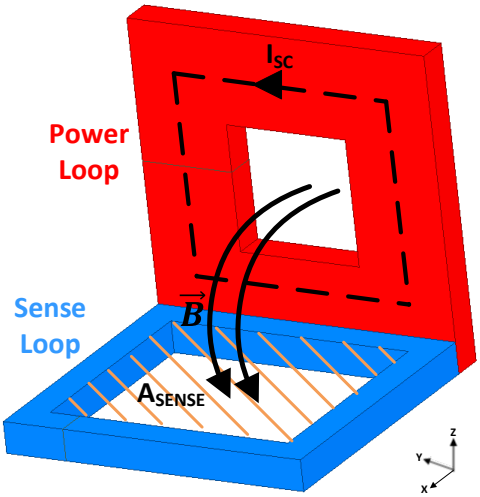

Fig. 6. A simplified model of PCB layout for power loop and sense loop

calculated based on Gauss's Law of Magnetism as in (4). Time derivative of total flux linkage within the loop area induces a voltage which is a result of Lenz's Law of Induction, (5).

$$\varepsilon = M_{PS}\frac{\partial i_{SC}}{\partial t} \tag{1}$$

$$i_{SC}(t) = \int_S \vec{J}.d\vec{S} \tag{2}$$

$$\mu_0 \oint_l \vec{B}.d\vec{l} = \int_S \vec{J}.d\vec{S} \tag{3}$$

$$\Psi = \int \vec{B}.d\vec{A} \tag{4}$$

$$\varepsilon = -\frac{\partial \Psi}{\partial t} \tag{5}$$

Similar to simplified model, the sensed voltage on the PCB can be calculated by estimating the total flux linkage in sense loop as shown in Fig. 7. According to FEA results, the power loop current induces voltage with a mutual coupling factor, M_{PS}, of 0.18 nH. Also, the self inductance of power loop layout is 0.6 nH which is low enough to guarantee safe operation.

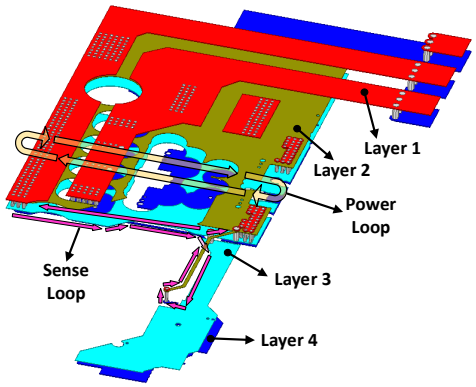

Fig. 7. Layout view for power loop and sense loop where layer orders are given from top layer (Layer 1) to bottom layer (Layer 4)

Fig. 8. Experimental setup for SC protection tests

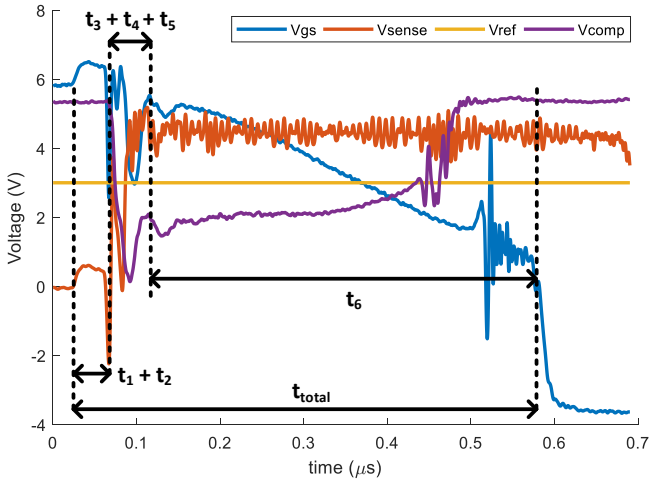

Fig. 9. Timing waveform of SC protection mechanism where V_{gs} is the gate-source voltage of bottom switch, V_{sense} is the induced voltage on PCB layout, V_{ref} is the threshold level of SC signal and V_{comp} is the output of comparator IC. (SUBJECT TO CHANGE)

TABLE I
DELAYS AND RELATED FACTORS

Time Interval	(ns)	Prolonging Factors	Expediting Factors
t_1	40	Loop Inductance Filter Components	Bus Voltage Decoupling Capacitance
t_2	5	Comparator Delay	-
Detection	45	-	-
t_3	16	Isolator Delay	-
t_4	17	Interrupt Latency	DSP Clock Speed
t_5	16	Isolator Delay	-
Turn-off Start	94	-	-
t_6	460	Base Resistor	BJT Gain
Total	554	-	-

IV. Experimental Results

The half-bridge board is tested in a configuration as given in Fig. 8. A digital signal processor, TMS320F28379D, with 200 MHz clock speed is used for generating PWM signals and for applying short-circuit protection. Experiments are organized to show capability of SC protection mechanism and switching performance of half-bridge board.

As shown in Fig. 9, SC fault is detected in 45 ns and the transistors are completely turned off in less than 550 ns with soft turn-off. The induced voltage under SC fault increased up to X V. Therefore, SC current increased with a slope of X A/ns. Delay intervals in SC timing waveform are affected from several factors positively or negatively as given in Table I. In order to minimize short-circuit protection duration, a fast comparator IC and and a fast digital isolator IC are required. Even though main time consumption belongs to soft turn-off mechanism, the SC current decreases gradually with time and soft turn-off is a must for operation safety. A comparison result is shown in Fig. 10. For a hard turn-off situation, the voltage on GaN HEMT increases up to 115 V under 40 VDC input which clearly indicates the risk for higher level of input voltages. On the contrary, when a soft turn-off is applied the voltage on GaN HEMT does not increase more than 80 volts and it ensures a transition in safe-operating-area limits.

Lastly, double pulse test (DPT) results are shown in Fig. 11. Transistors are switched with 20 Ω and 2 Ω turn-on and turn-off gate resistances, respectively. Whenever the control switch is turned-on, gate-source voltage of synchronous switch is charged via Miller capacitance. As shown in Fig. 11, the gate-source voltage is charged up to -1.9 V which stays lower than the threshold level, 1.7 V. This is a result of optimized and decoupled power loop and gate loop layouts.

Experimental results show that a proper power loop design is achievable for parallel connected transistors without sacrificing the reliability. SC fault can be detected in a very short amount of time and SC current can be brought under control in a period less than 100 ns.

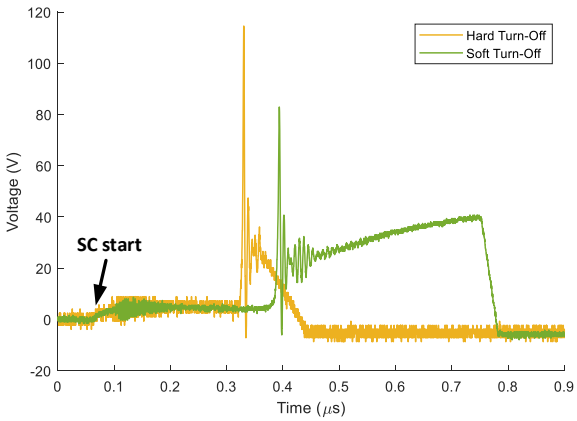

Fig. 10. Bottom side transistor drain-source voltages for hard and soft turn-off situations under 40 VDC

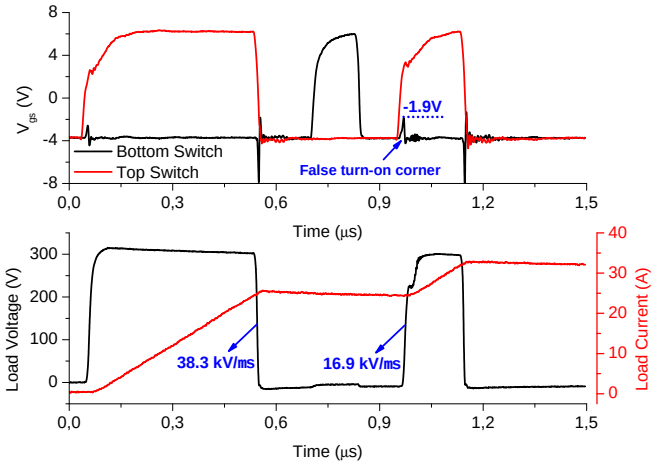

Fig. 11. Double Pulse Test (DPT) waveforms where V_{gs} stands for gate-source voltage of bottom transistor, V_{sw} is the switching node voltage which is also the load voltage.

V. Conclusion

In this paper, a short-circuit protection method based on layout inductance is applied on a parallel switch half-bridge. Short circuit protection mechanism is able to detect the fault in 45 ns. After detecting the fault, a soft turn-off process is initiated to keep transistor in safe-operating-area. Short circuit fault is completely removed in 550 ns. Moreover, experimental results show that proposed method does not distort power loop or gate loop layouts. As a result of optimized power and gate loops, gate voltage is always below the maximum level, 10 V, for high state and it is not distorted by miller capacitance during the switching for low state. The parallel half-bridge design increases current capability and the proposed board can be adapted to many applications with its short-circuit protection ability.

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