ORTA DOĞU TEKNİK ÜNİVERSİTESİ
MIDDLE EAST TECHNICAL UNIVERSITY

CHARACTERIZATION OF GAN TRANSISTORS AND DEVELOPMENT OF BI-DIRECTIONAL DC/DC CONVERTER WITH HALF-BRIDGE HAVING SHORT CIRCUIT PROTECTION FOR PARALLEL SWITCHES

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MSc Thesis Presentation
Advisor: Assist. Prof. Dr. Ozan Keysan
METU, EEE
09.09.2020

Layout

- Introduction
  - A game changer: GaN power transistors
  - Focus of thesis
- Transistor characterization
  - Input charge
  - Output capacitance
- Switching characteristics
- Half-bridge design
  - Layout optimization
  - Short-circuit protection
  - Thermal design
- Bi-directional DC/DC converter design
  - Design specifications
  - Experimental results
- Remarks and Conclusion

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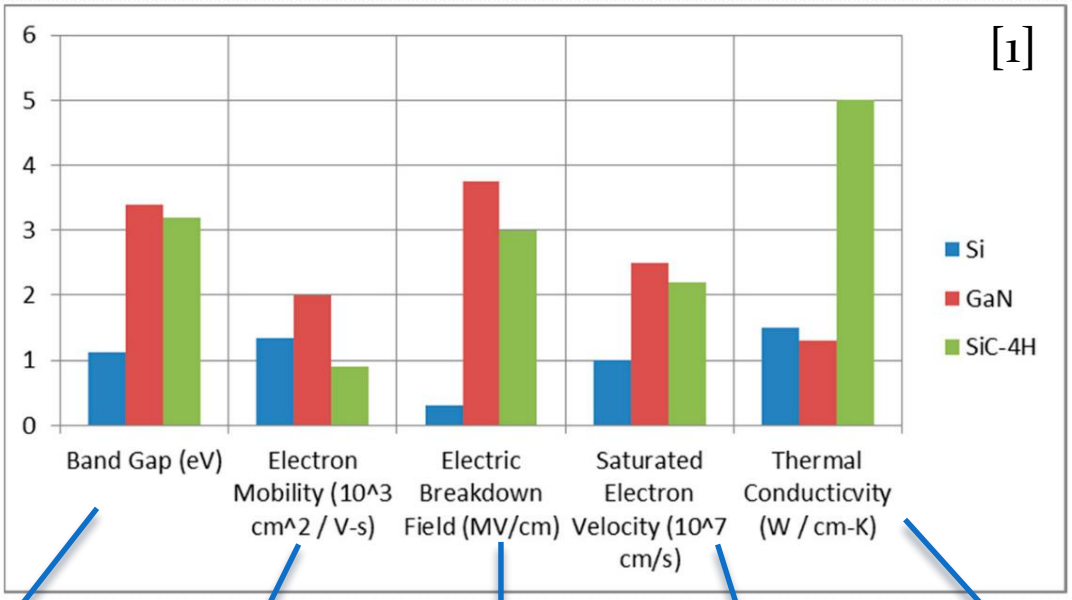
Why is GaN a Game Changer?

Comparison of Si, SiC and GaN materials



Smaller package size	Higher conductivity	Compact solutions	Higher Switch. Freq.	Better cooling
↓	↓	↓	↓	↓
Lower parasitics	Lower cond. losses	Low volume applications	Small passive components	Small cooling components

[1] C. T. Ma and Z. H. Gu, "Review of GaN HEMT applications in power converters over 500 W," *Electron.*, vol. 8, no. 12, 2019.

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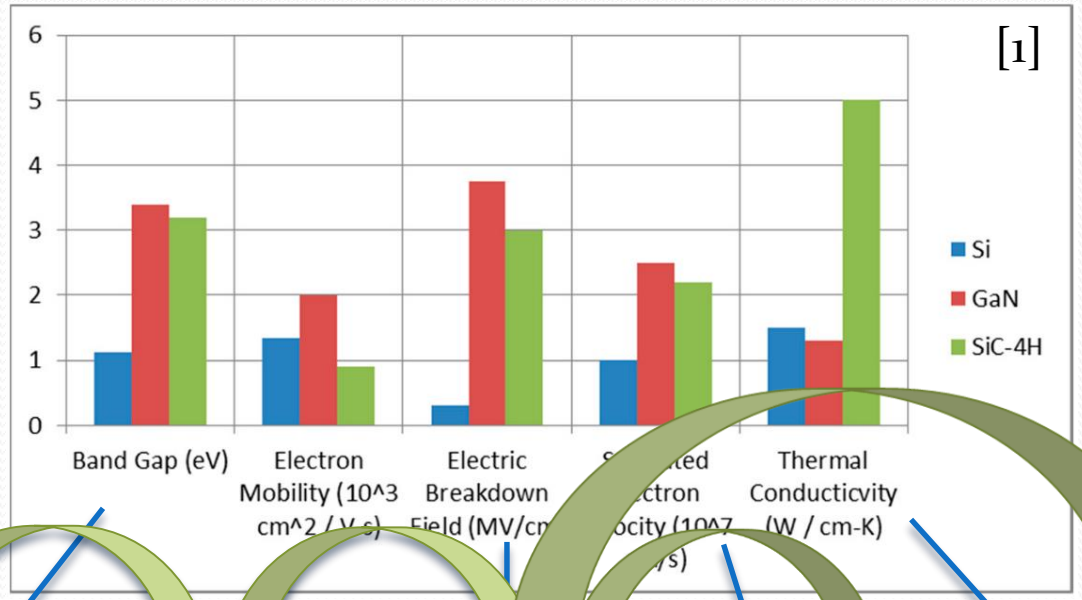

Smaller package size → Lower parasitics

Higher conductivity → Lower cond. losses

Compact solutions → Low volume applications

Higher Switch. Freq. → Small passive components

Better cooling → Small cooling components

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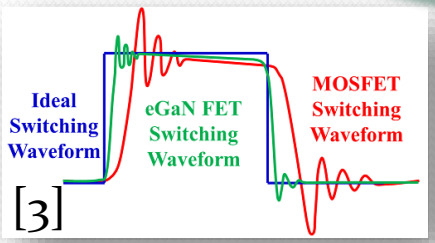
Focus of Thesis

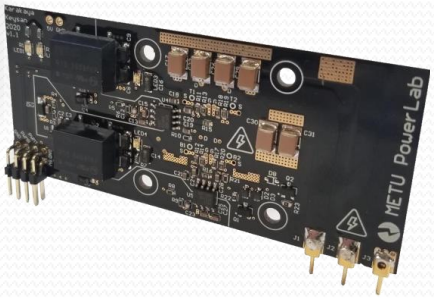
- A perspective from device level to system level

Device

[2]
Characterization
Experimental Results

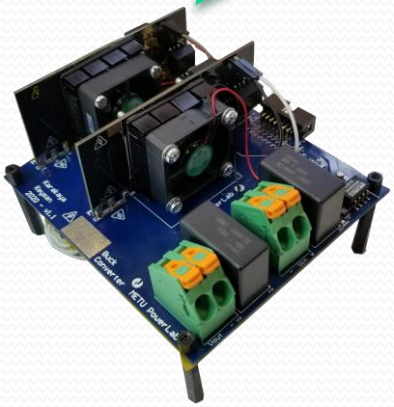


Switching Performance
Simulation Results



Half-bridge design
Experimental Results

System



DC/DC converter design
Experimental Results

[2] https://gansystems.com/gan-transistors/gs66508t/
[3] https://www.eeweb.com/how-to-gan-egan-fets-in-high-performance-class-d-audio-amplifiers/

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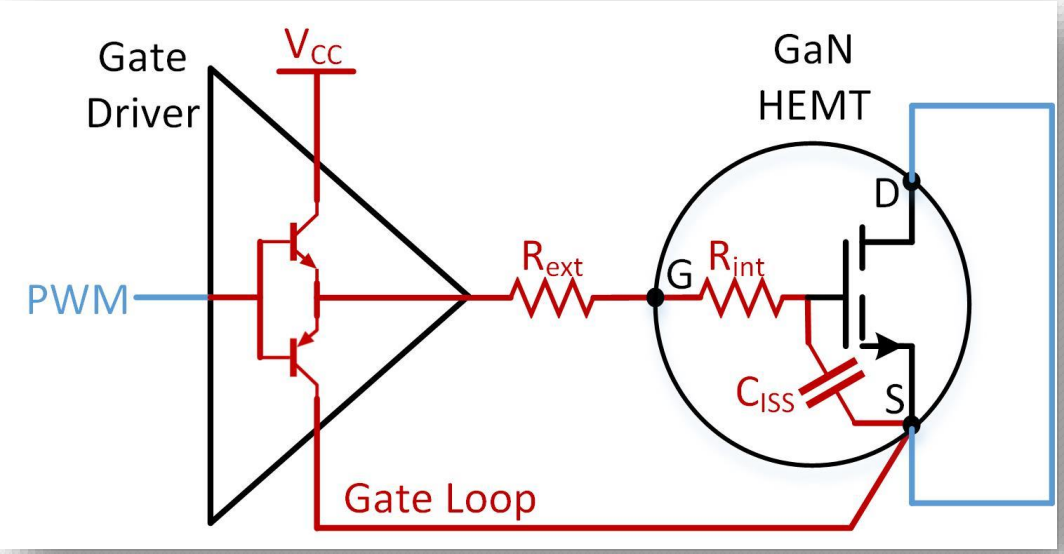
Characterization – Input Charge



Gate loss mechanism

$$P_G = P_{GD} + P_{R,ext} + P_{TR} \quad (1)$$

$$P_G = Q_G(V_{on} - V_{off})f_{sw} \quad (2)$$

$$Q_G = \int_{V_{off}}^{V_{on}} C_{ISS}(v)dv \quad (3)$$

Amount of gate charge determines how much energy has to be stored in the gate capacitance.

→ Is the gate charge the same for hard-switching and soft-switching?

Characterization – Estimating Gate Loss

Method - 1

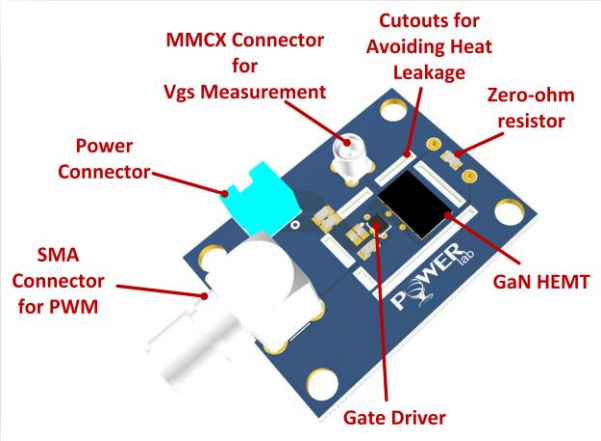
Datasheet

Take the gate charge data from datasheet

	GS66508T
Q_G	6.1 nC | V_{GS} = 0 to 6 V | V_{DS} = 400 V

Method - 2

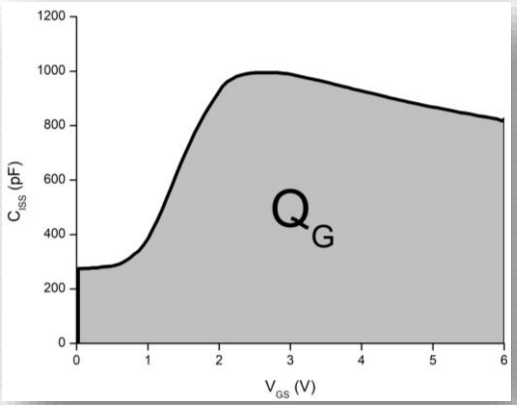
Thermal calibration



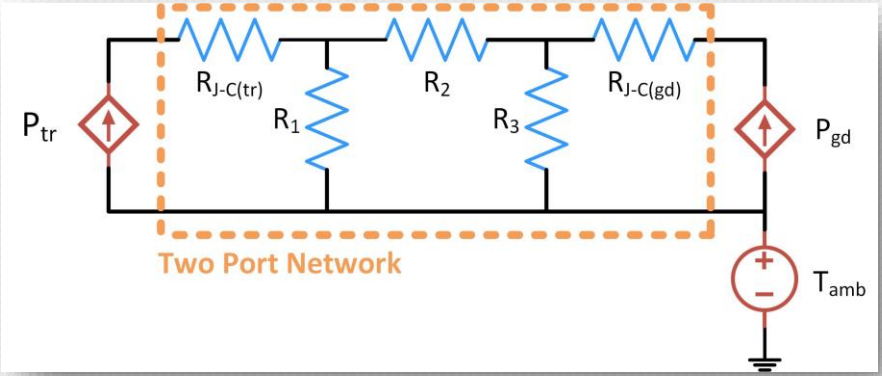
Gate charge characterization board

Method - 3

Impedance analyzer

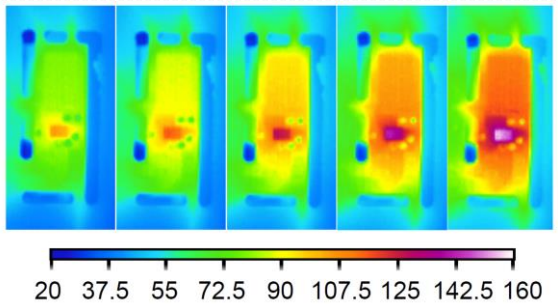


Measured gate charge

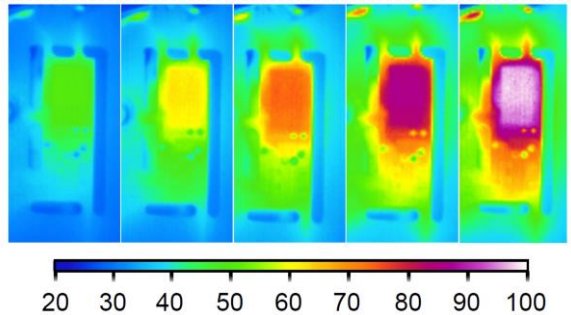


Thermal network

Characterization – Estimating Gate Loss



Gate driver causes loss

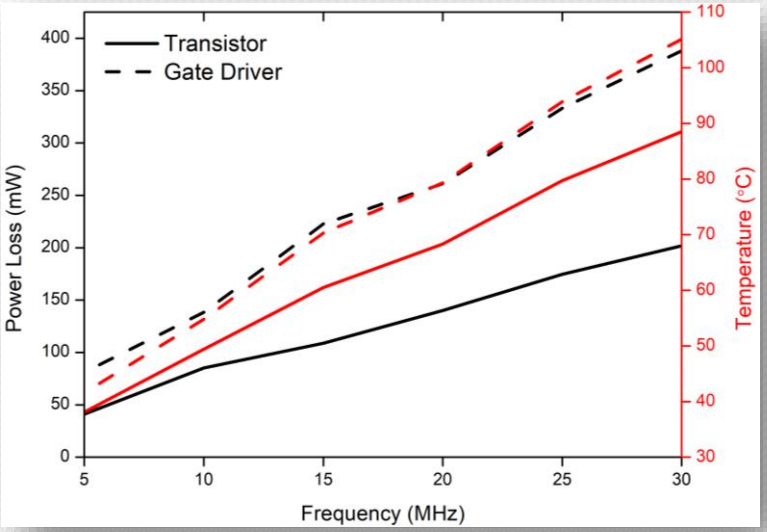


Transistor causes loss

$$\begin{bmatrix} \Delta T_{tr} \\ \Delta T_{gd} \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} * \begin{bmatrix} P_{tr} \\ P_{gd} \end{bmatrix} \quad (4)$$

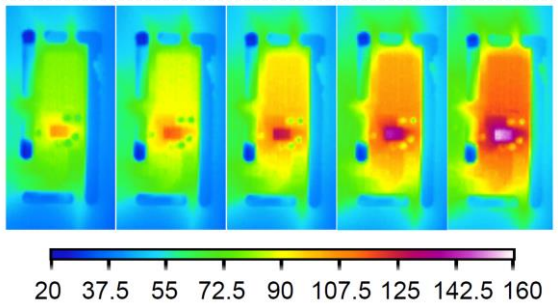
Inverted Matrix

$$\begin{bmatrix} P_{tr} \\ P_{gd} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{21} \\ G_{21} & G_{22} \end{bmatrix} * \begin{bmatrix} \Delta T_{tr} \\ \Delta T_{gd} \end{bmatrix} \quad (5)$$



Gate loss

Characterization – Estimating Gate Loss



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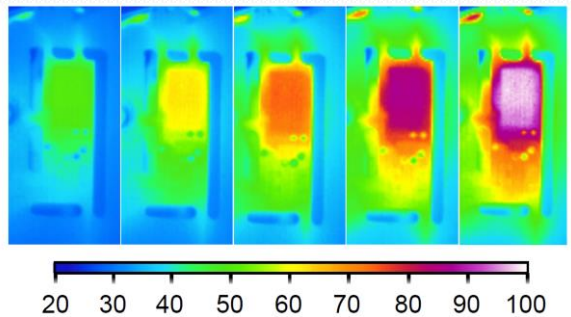

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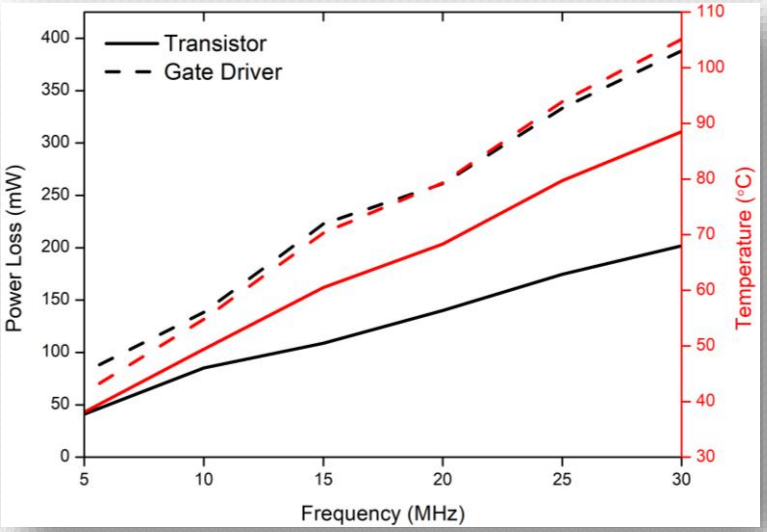
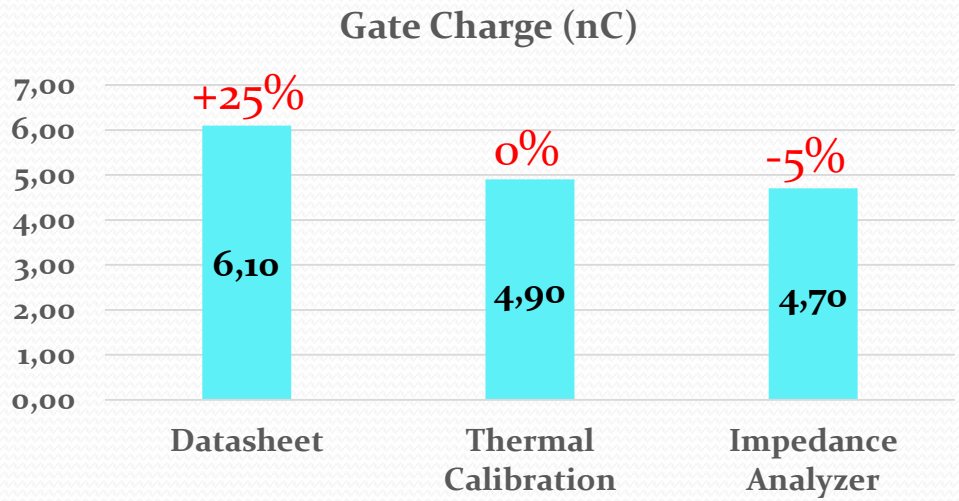


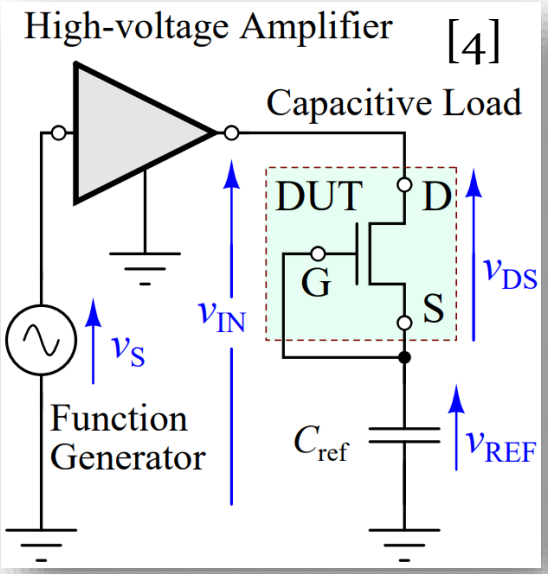
Gate loss



Gate charge deviates 25% for soft switching

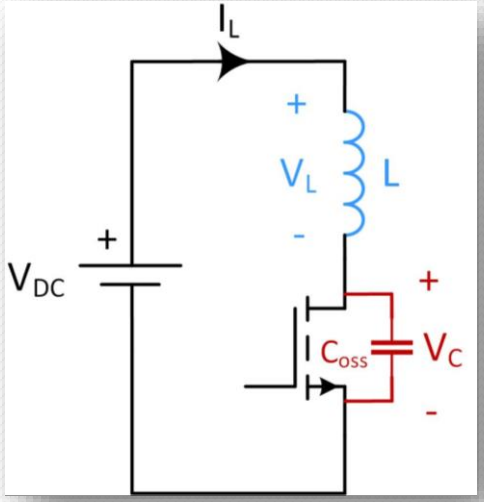
Characterization – Output Capacitance

Sawyer – Tower Method

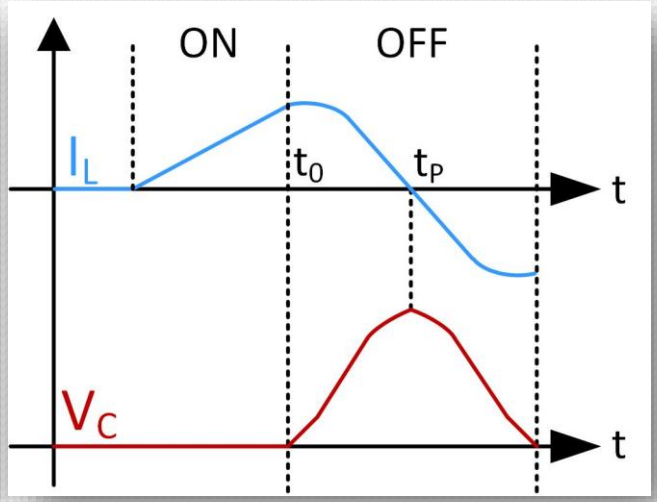


Circuit

Nonlinear Resonance Method



Circuit



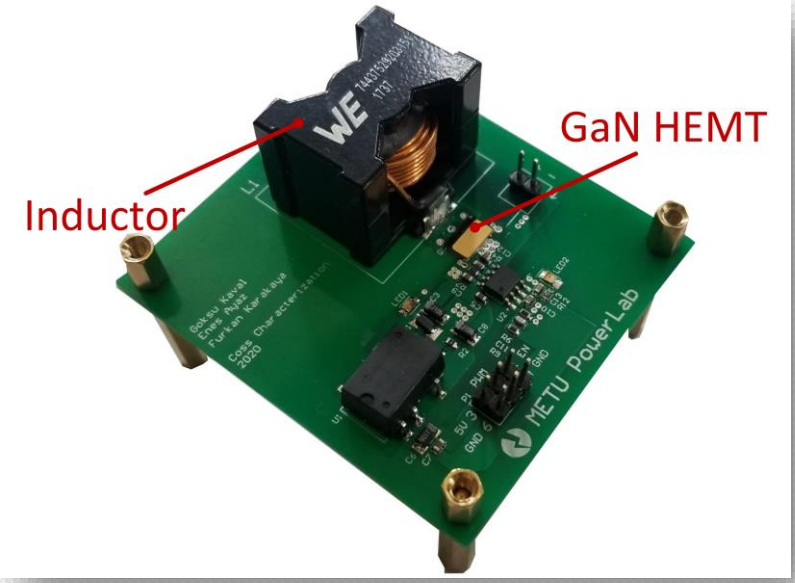
Waveform

[4] N. Perera *et al.*, "Analysis of Large-Signal Output Capacitance of Transistors using Sawyer–Tower Circuit," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6777, no. c, pp. 1–1, 2020.

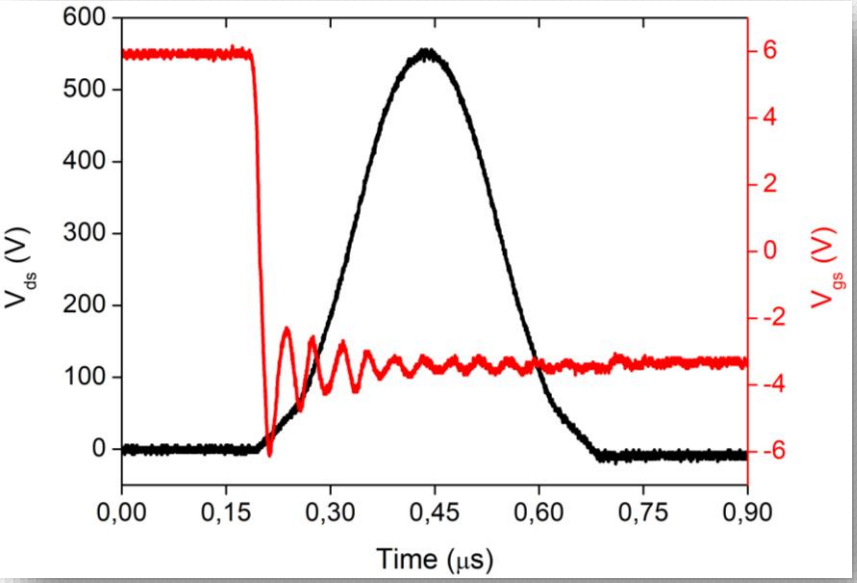
Characterization – Output Capacitance

$$C_{oss}(V_C) = \frac{\int_{t_o}^{t_p} V_C(t)dt - \int_{t_o}^{t} V_C(t)dt}{L\frac{d(V_C(t))}{dt}} \quad (6)$$

In order to characterize output capacitance of GaN HEMT, measurement of resonant voltage is enough

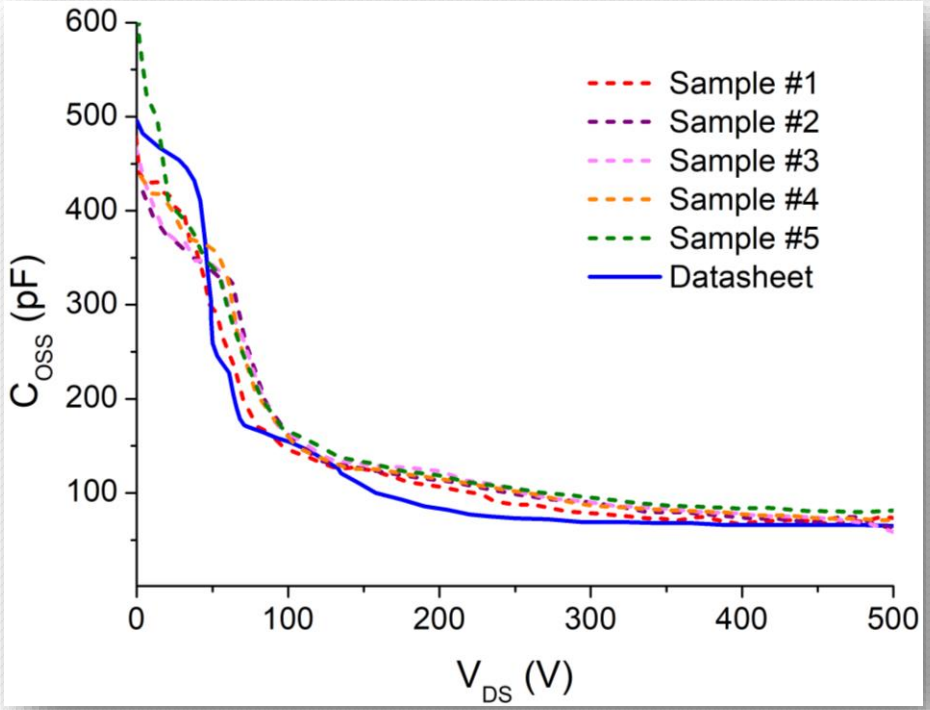


Characterization PCB

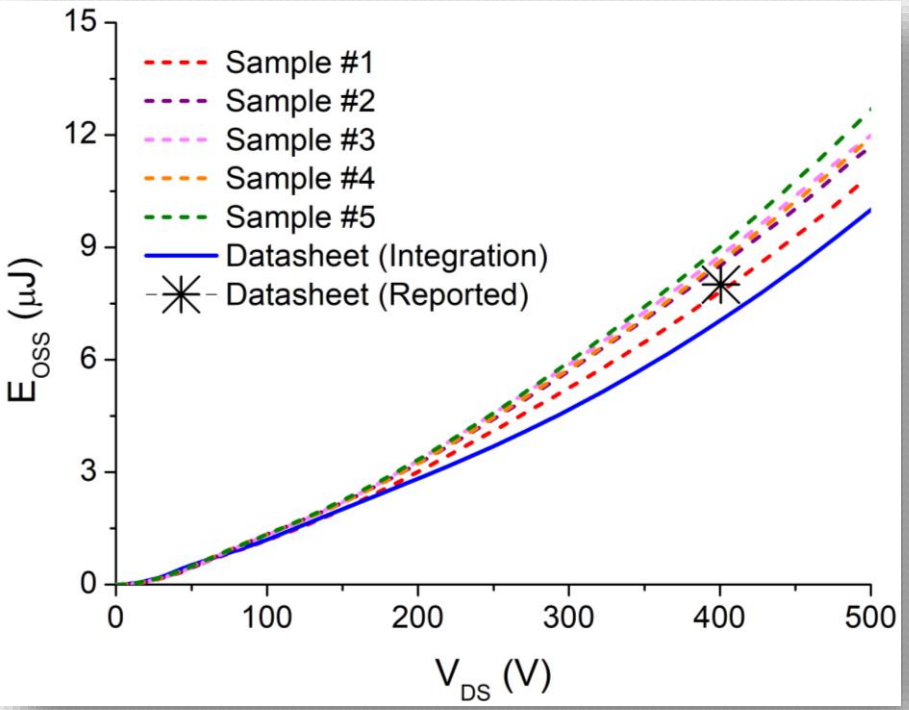


Oscilloscope waveform

Characterization – Output Capacitance



C_{OSS} vs V_{DS}



E_{OSS} vs V_{DS}

$$E_{OSS}(V) = \int_0^{V_{DS}} V C_{OSS}(V) dV \qquad (7)$$

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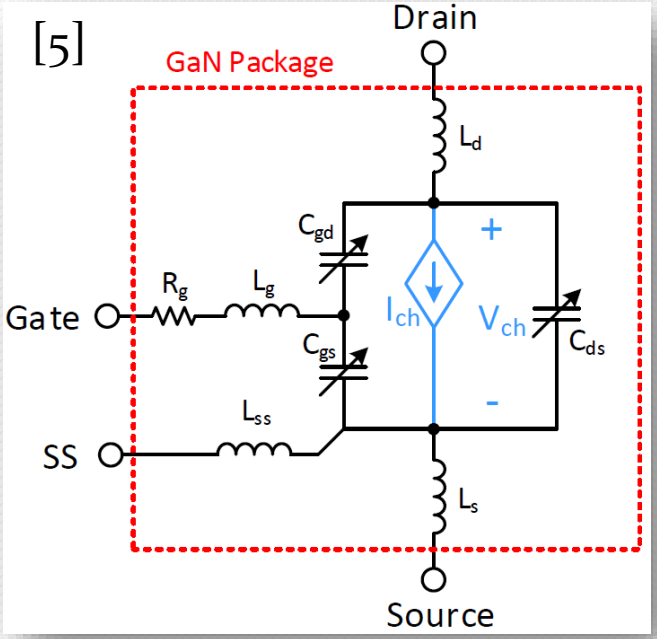
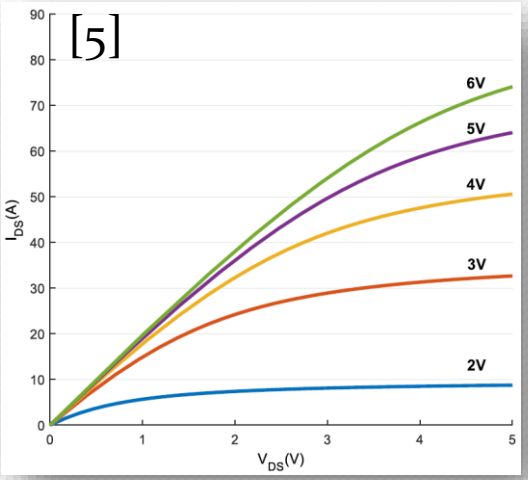
Switching Characteristics - Modeling

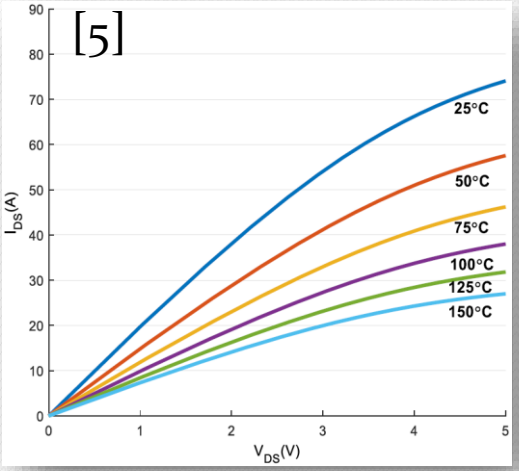


Transistor model

$$I_{ds} = K_1(T)\ln\left(1+e^{\frac{V_{gs}-V_{th}}{K_2}}\right)\frac{V_{ds}}{1+\max(K_3+K_4(V_{gs}+K_5),K_6)V_{ds}} \quad (8)$$



Forward conduction



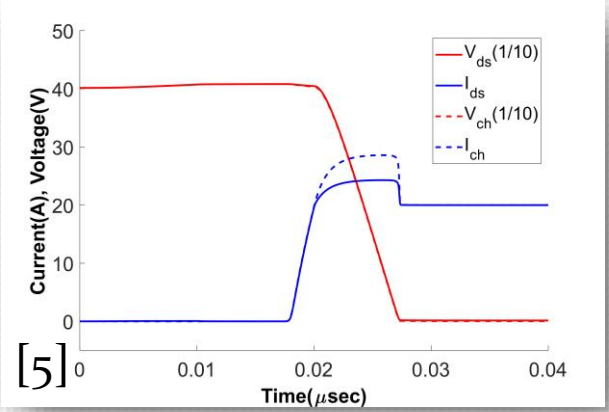
Temperature effect

Compatible with datasheet curves

[5] F. Karakaya, M. Ugur, and O. Keysan, "Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors," 2018, pp. 1–10.

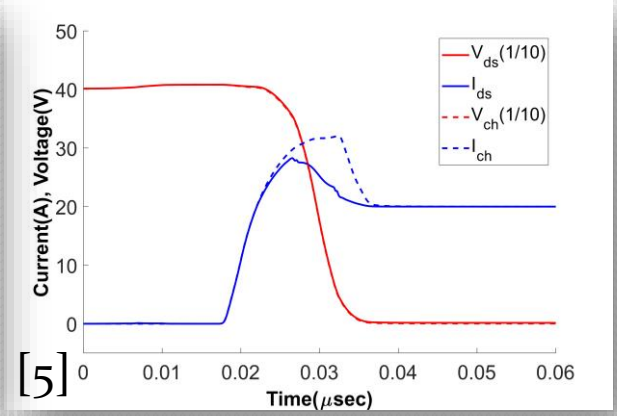
Switching Characteristics – Model Comparison

Model - 1



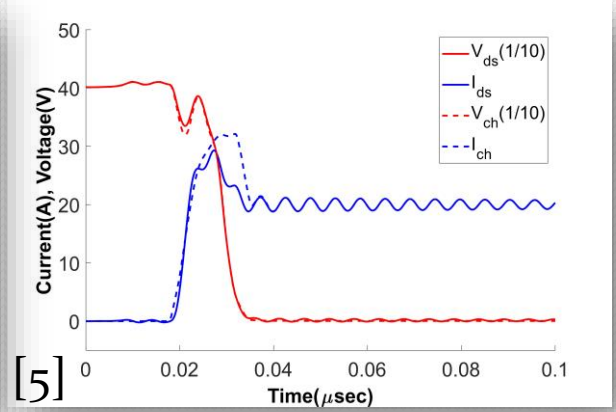
- Fixed capacitances
- Non-modeled inductances

Model - 2



- Variable capacitances
- Non-modeled inductances

Model - 3

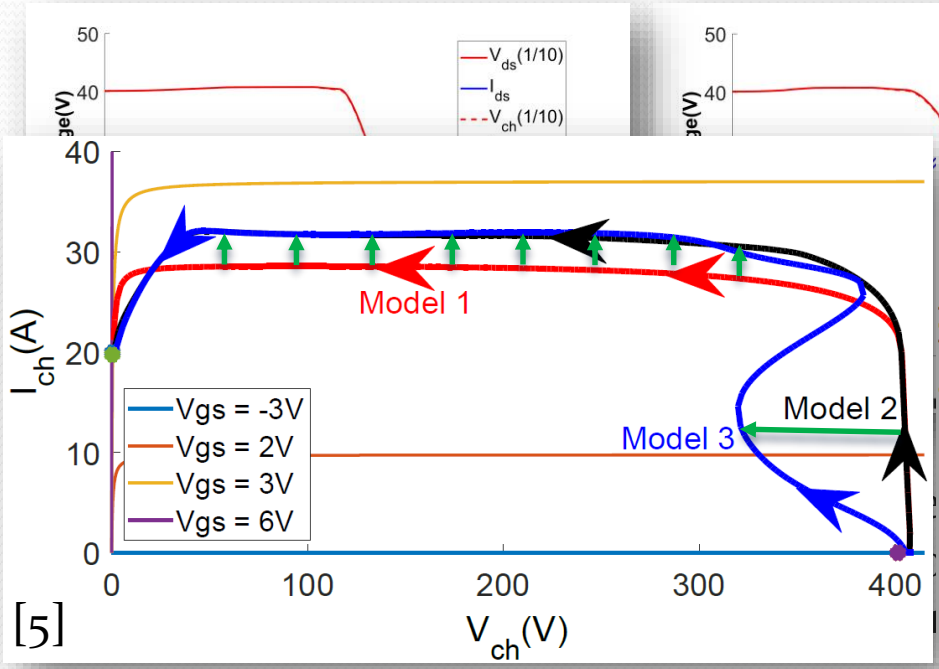


- Variable capacitances
- Modeled inductances

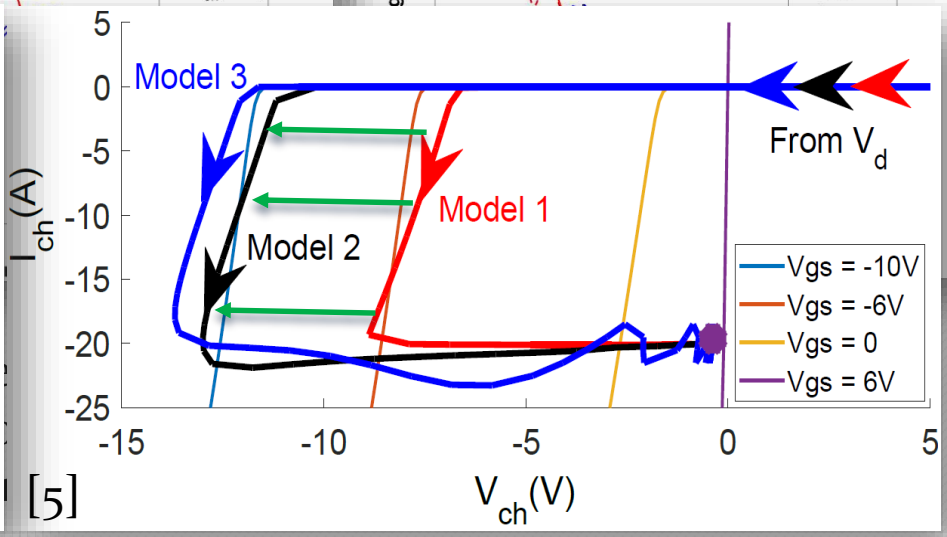
[5] F. Karakaya, M. Ugur, and O. Keysan, "Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors," 2018, pp. 1–10.

Switching Characteristics – Model Comparison

Model - 1 | Model - 2 | Model - 3



Forward conduction



Reverse conduction

[5] F. Karakaya, M. Ugur, and O. Keysan, "Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors," 2018, pp. 1–10.

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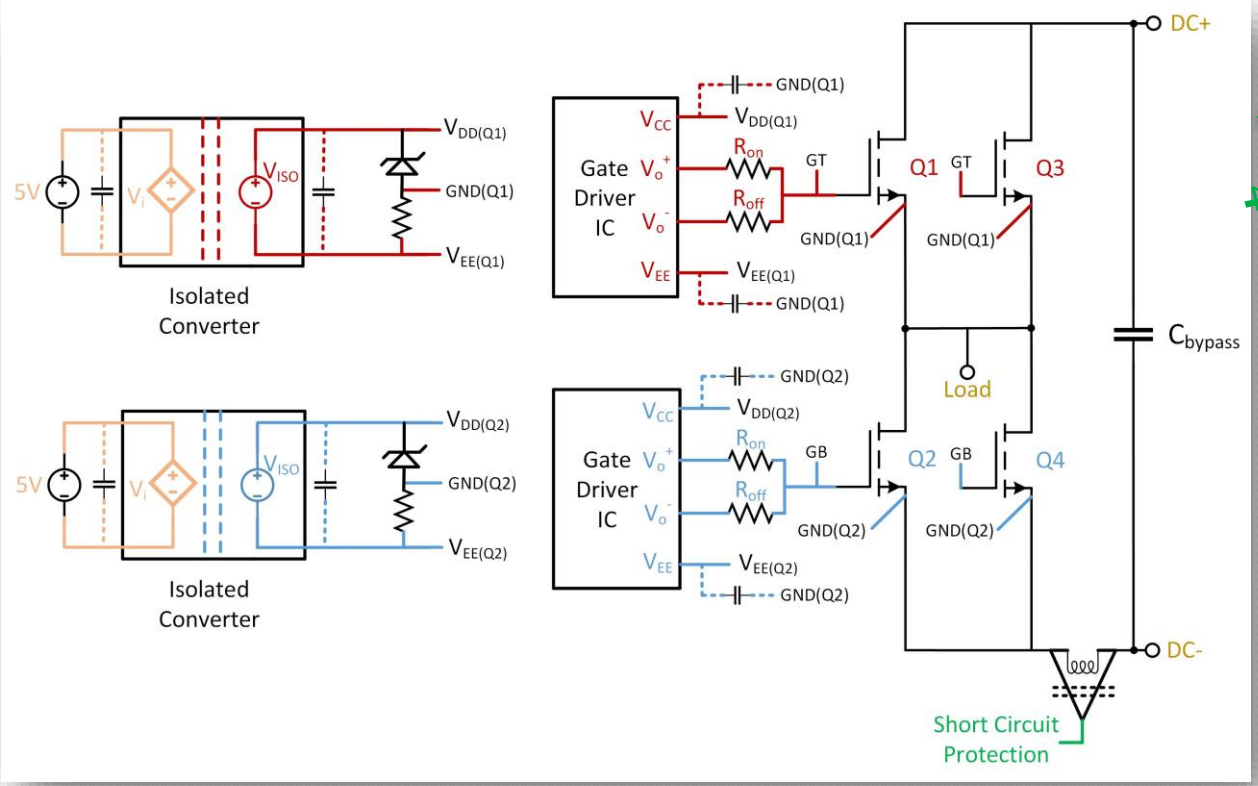
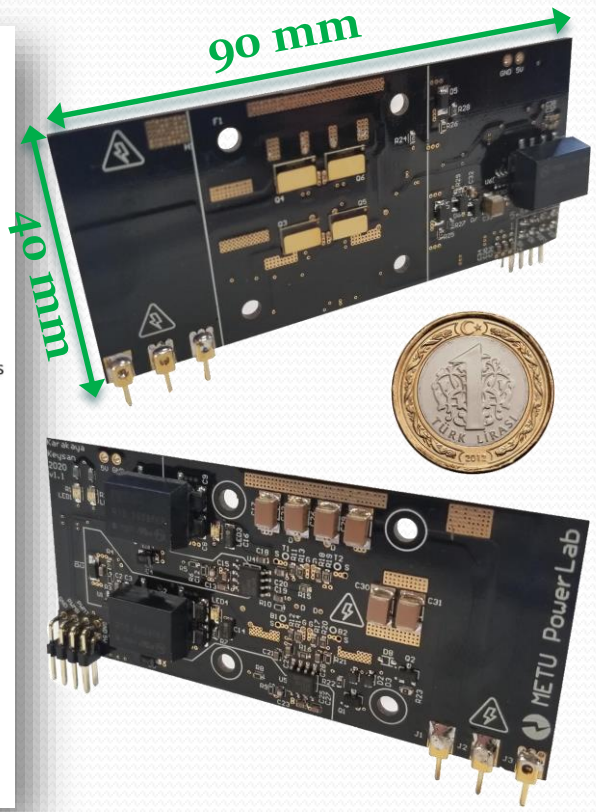
Half-bridge



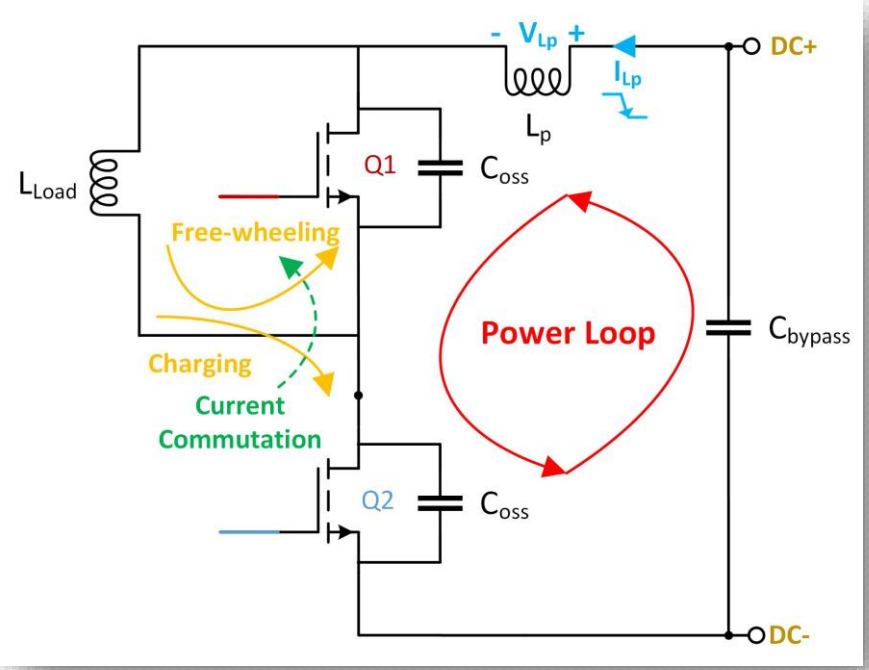
Half-bridge scheme



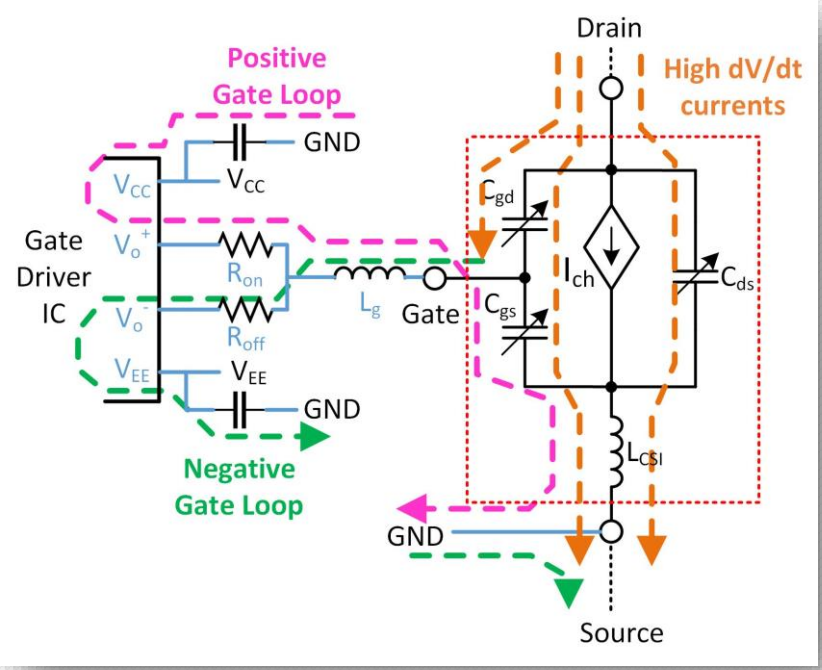
Half-bridge view

Half-bridge – Layout

Power Loop



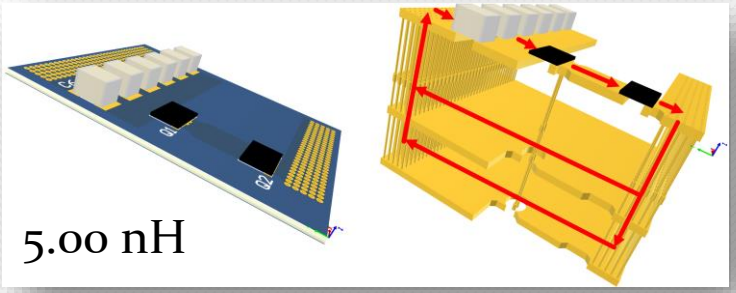
Gate Loop



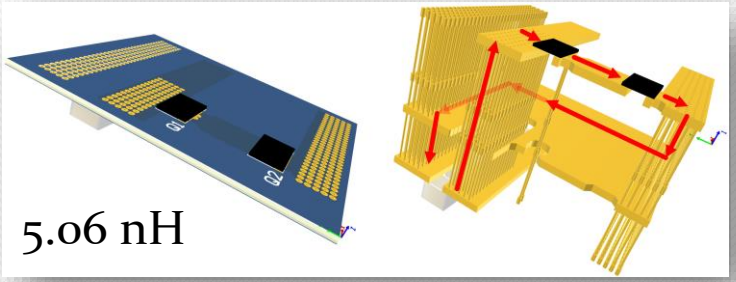
Half-bridge – Layout

Power Loop

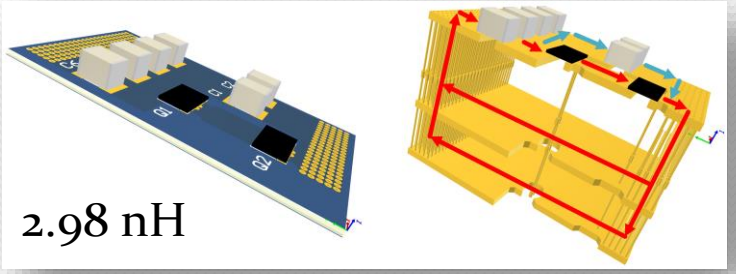
(a)



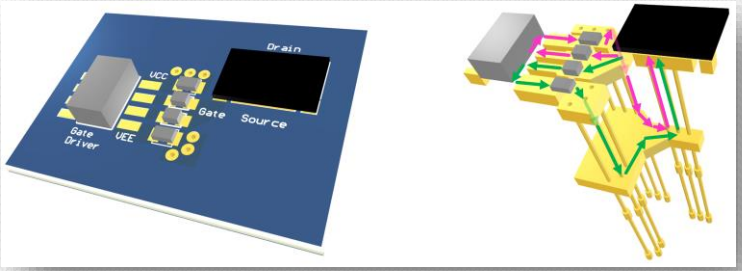
(b)



(c)



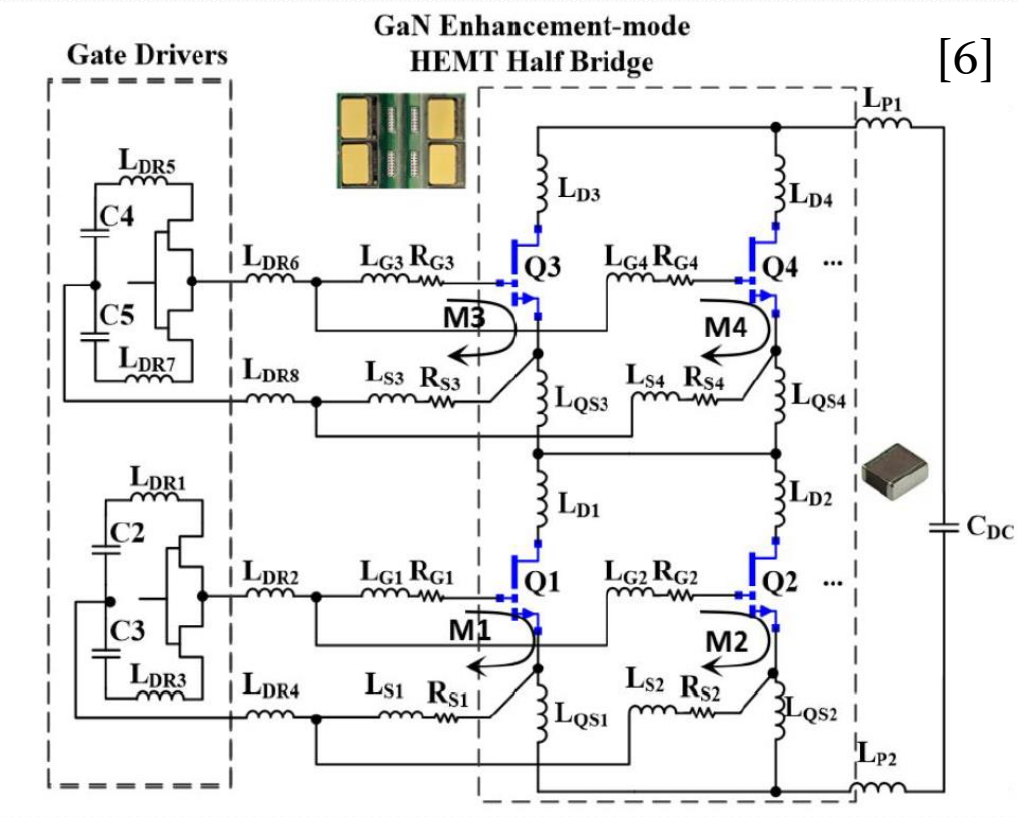
Gate Loop



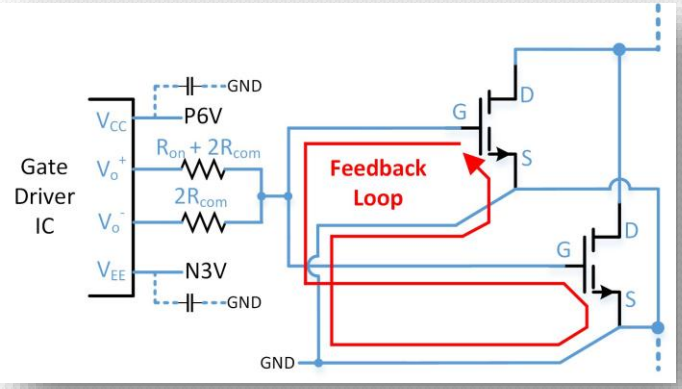
0.88 nH
Positive Gate Loop

0.93 nH
Negative Gate Loop

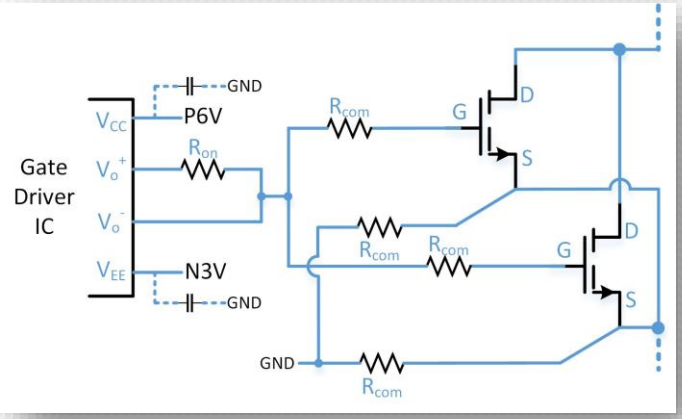
Half-bridge – Device Paralleling



Parasitic inductances for parallel operation



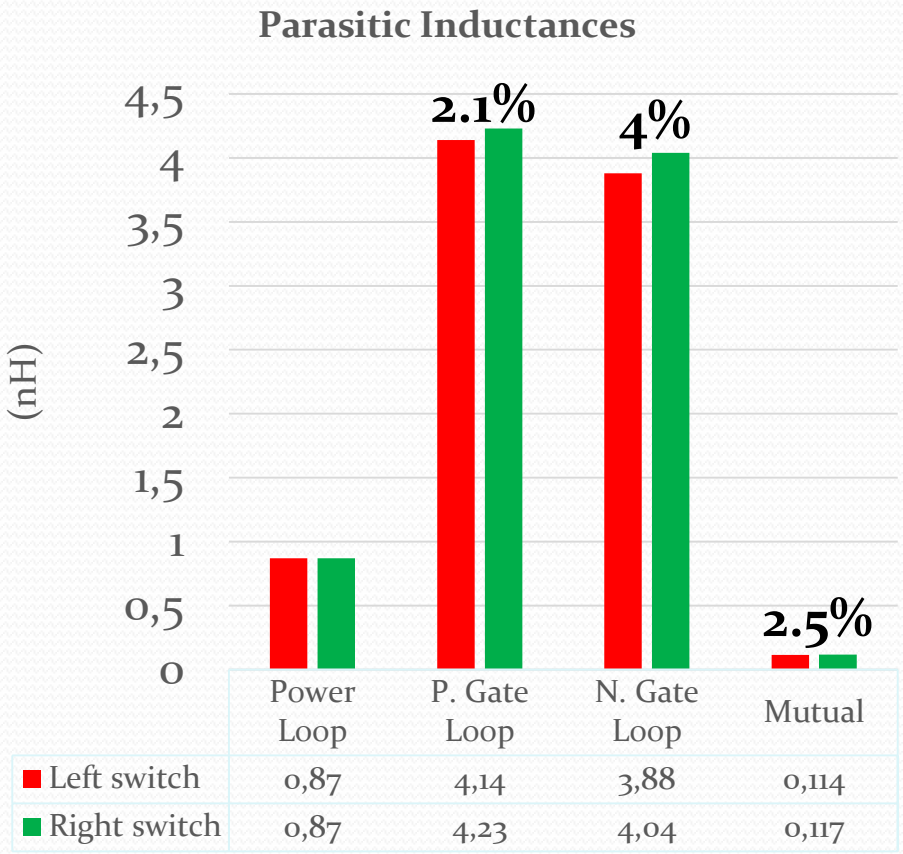
Improvement in Gate Loop



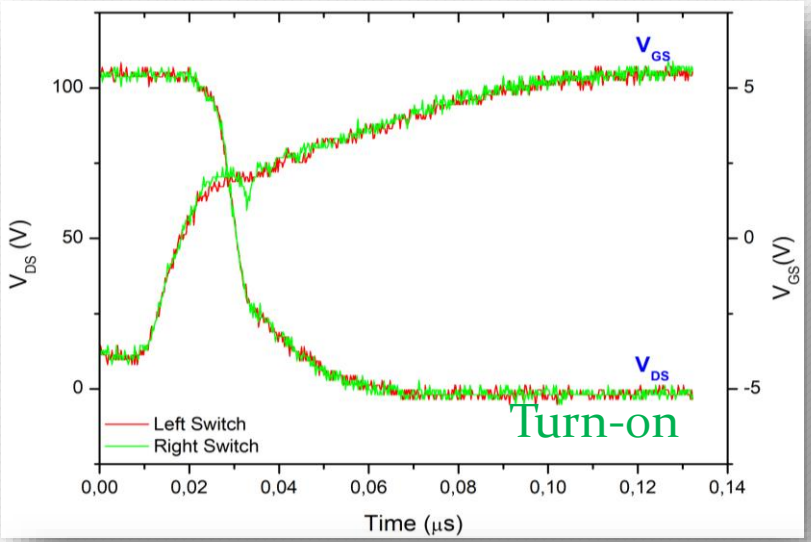
Gate driver circuit

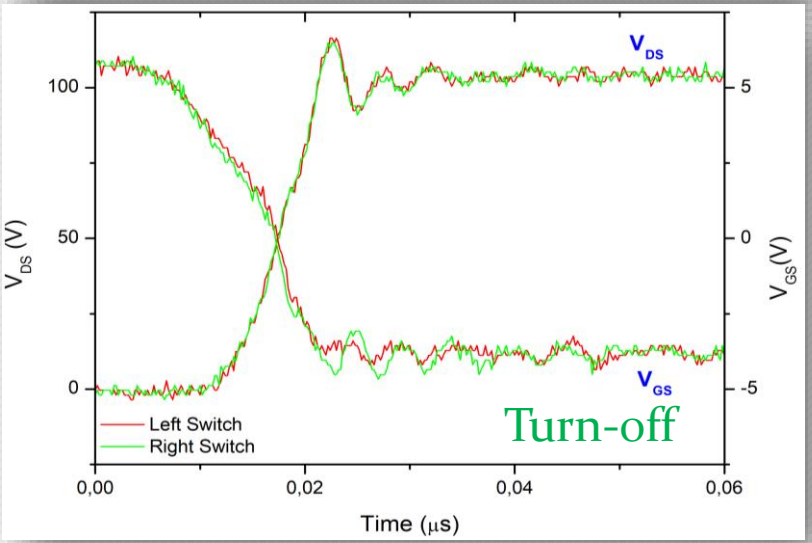
[6] J. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW-100kW systems," Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, pp. 3049–3056, 2017

Half-bridge – Device Paralleling



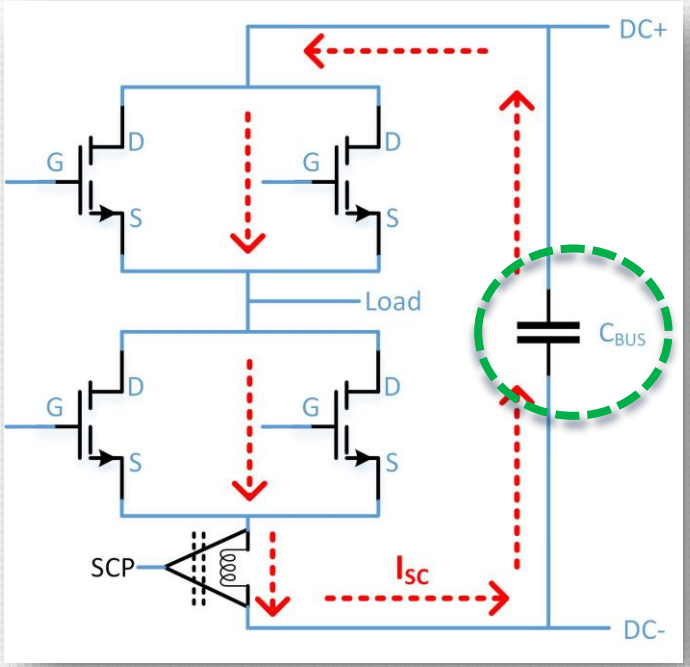
Similar parasitics for parallel connected switches



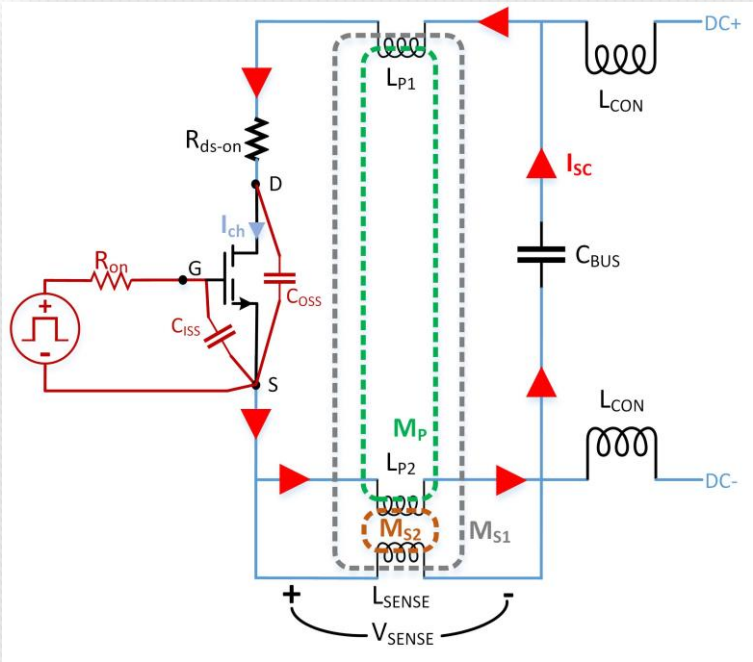


Switching Waveforms

Half-bridge – Short Circuit (SC) Protection



SC current path



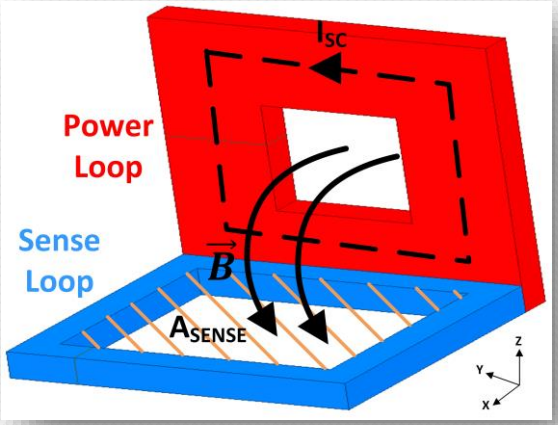
Dynamics of SC protection

SC current is supplied by the power loop capacitors!

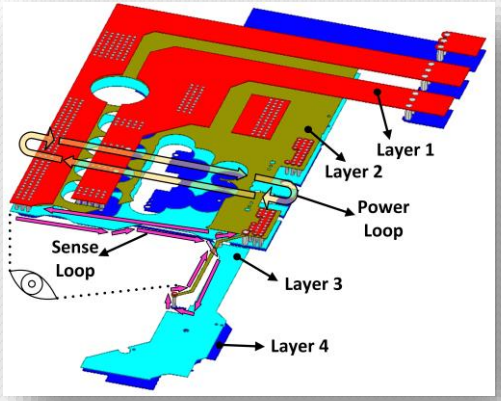
$$L_P = L_{P1} + L_{P2} + 2M_P \quad (9)$$

$$M_{PS} = M_{S2} - M_{S1} \quad (10)$$

Half-bridge – SC Protection: Detection



Simplified Model



FEA Model

How does SC current induce a voltage?

$$\epsilon = M_{PS}\frac{\partial i_{sc}}{\partial t} \quad (11)$$

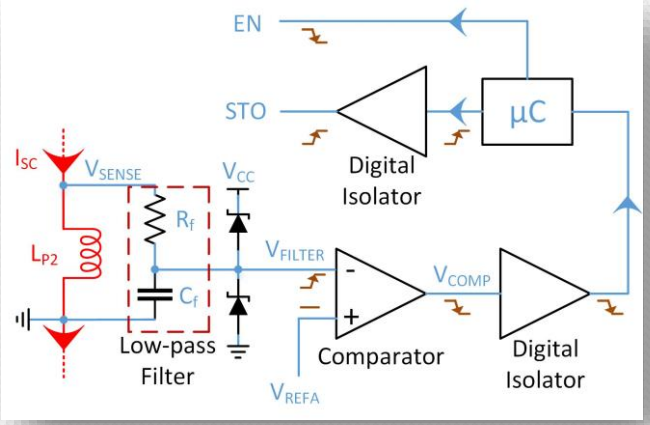
$$i_{sc}(t) = \int_S \vec{J}.d\vec{S} \quad (12)$$

$$\mu_o \oint_l \vec{B}.d\vec{l} = \int_S \vec{J}.d\vec{S} \quad (13)$$

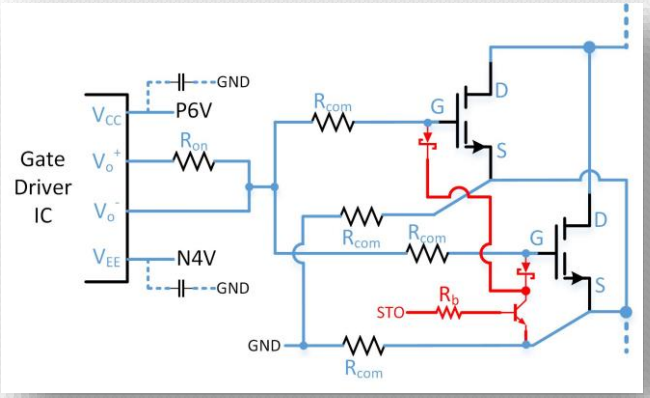
$$\Psi = \int \vec{B}.d\vec{A} \quad (14)$$

$$\epsilon = -\frac{\partial \Psi}{\partial t} \quad (15)$$

Mutual coupling is 0.87 nH

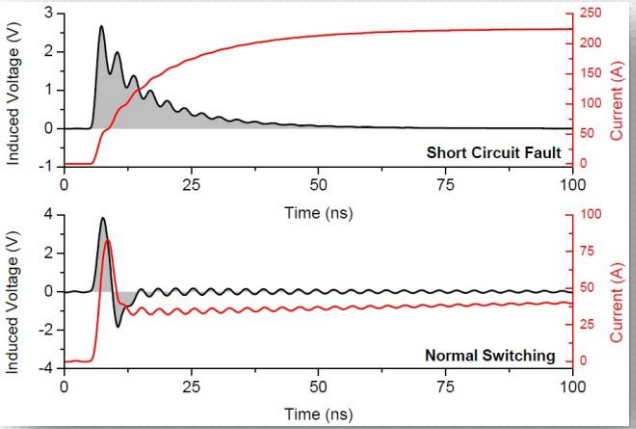


SC detection



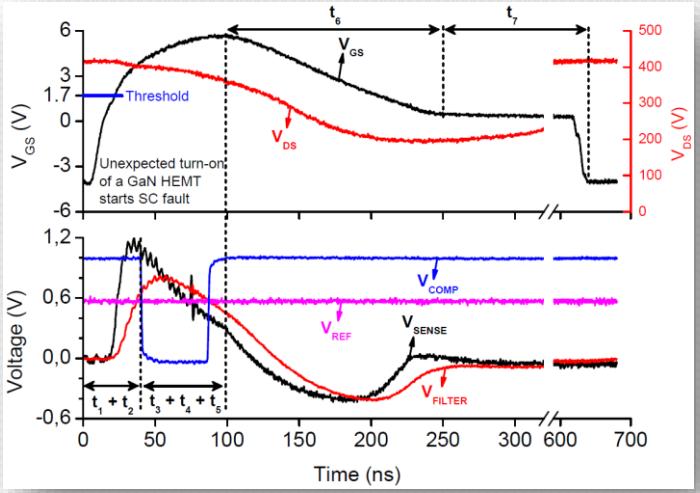
Gate driver modification

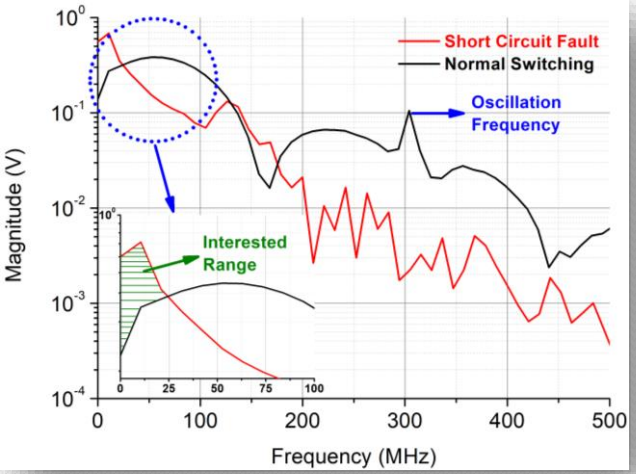
Half-bridge – SC Protection: Experiments



Waveform (simulation)

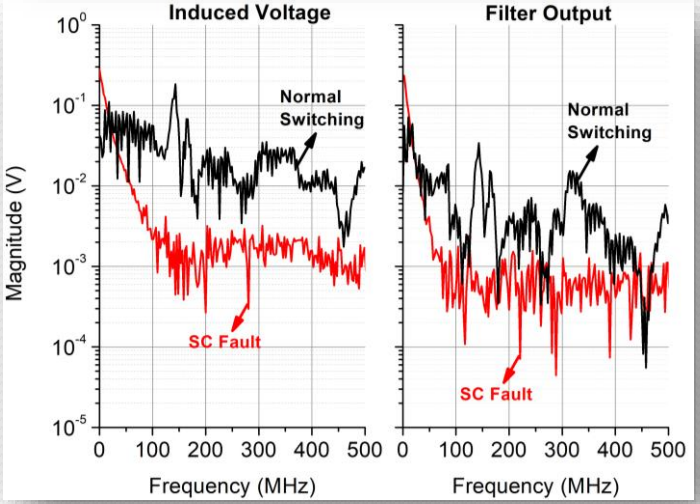
Experiment





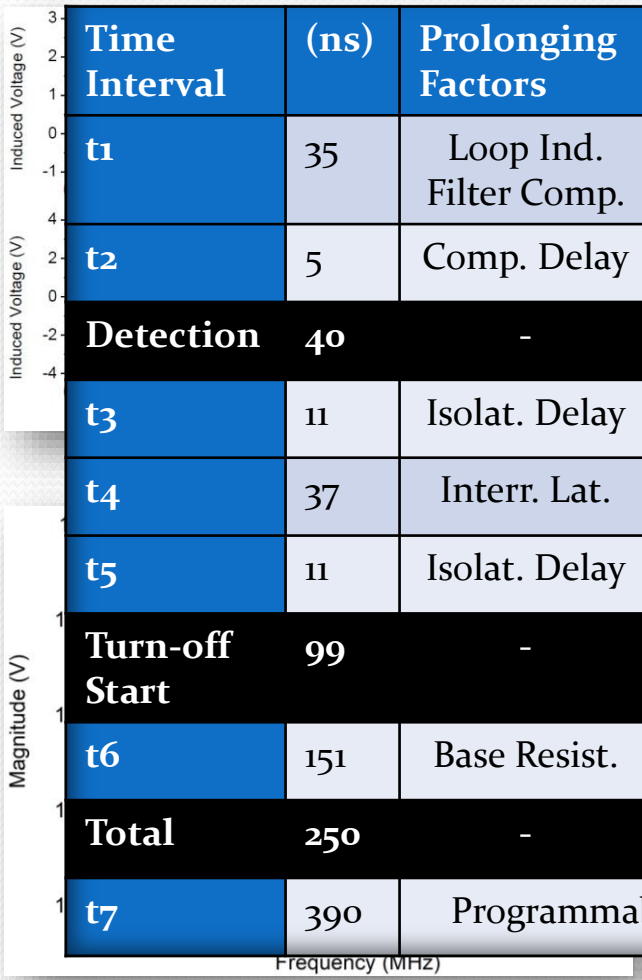
FFT (simulation)

Experiment

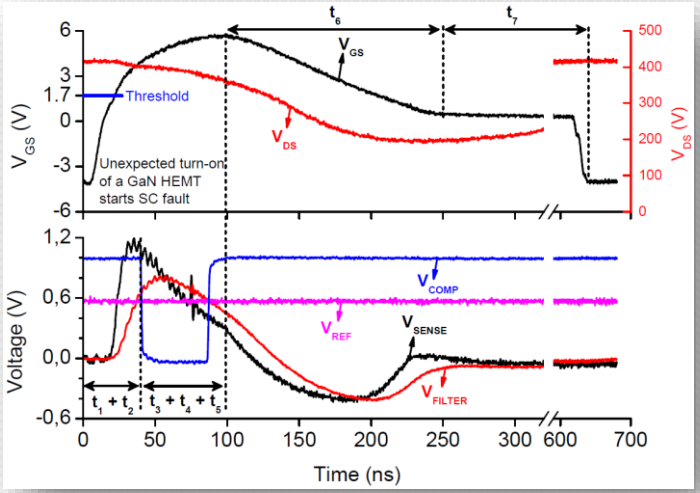


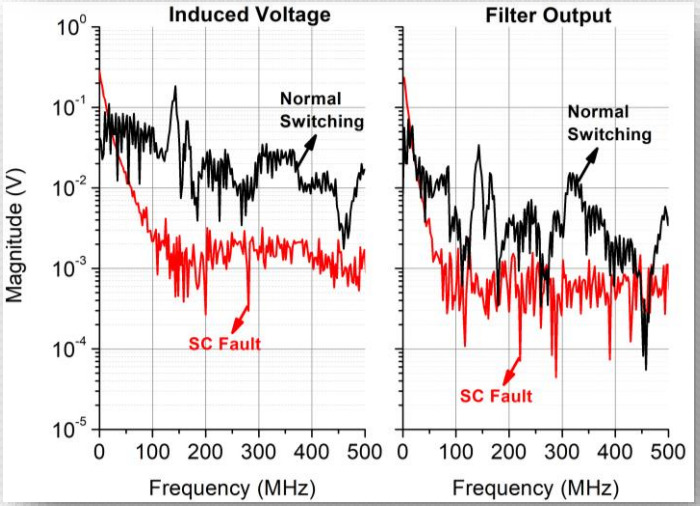
Half-bridge – SC Protection: Experiments

Time Interval	(ns)	Prolonging Factors	Expediting Factors
t1	35	Loop Ind. Filter Comp.	Bus Capac.
t2	5	Comp. Delay	-
Detection	40	-	-
t3	11	Isolat. Delay	-
t4	37	Interr. Lat.	DSP Speed
t5	11	Isolat. Delay	-
Turn-off Start	99	-	-
t6	151	Base Resist.	BJT Gain
Total	250	-	-
t7	390	Programmable Duration	

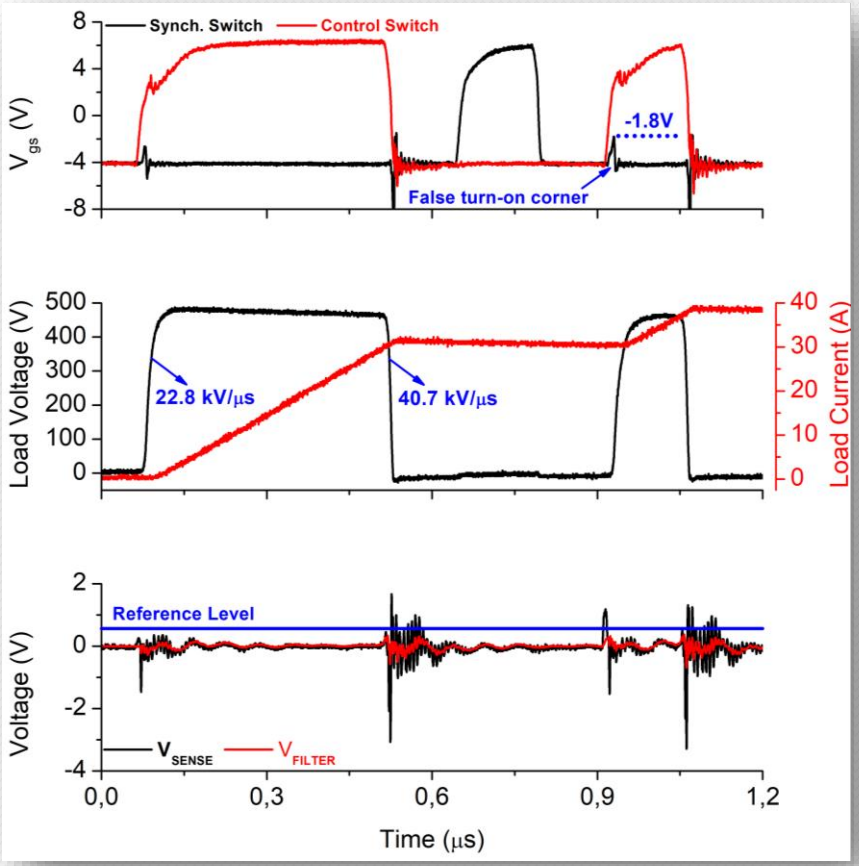


FFT (simulation)

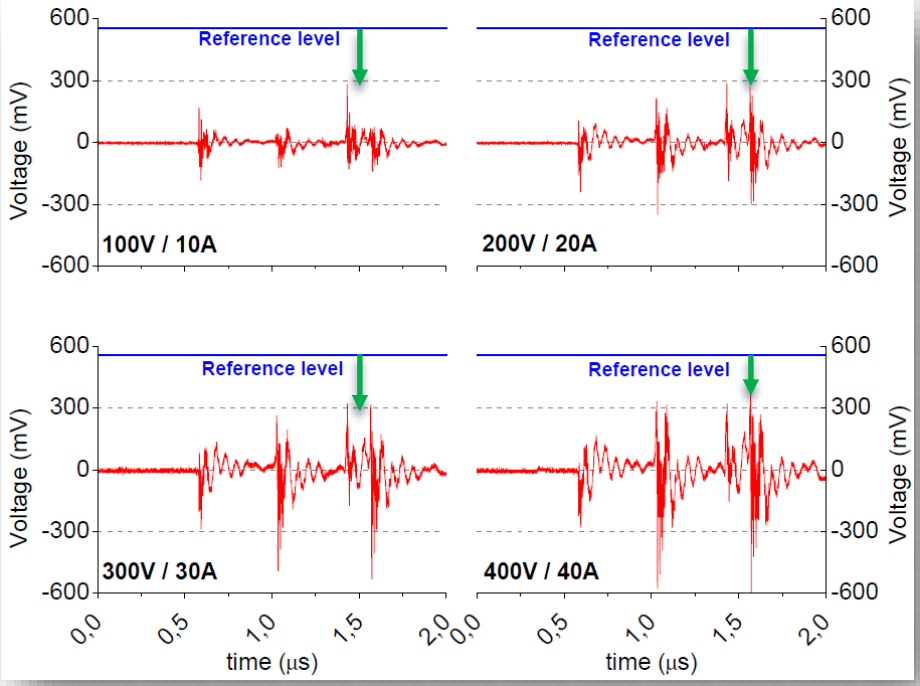




Half-bridge –SC Protection: Noise Immunity



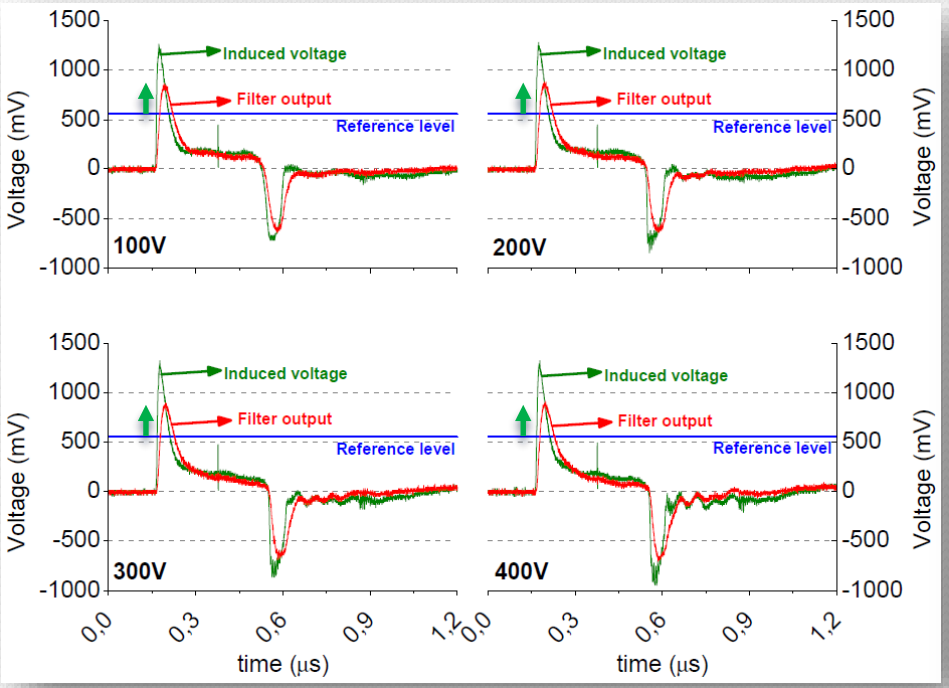
Double pulse test (DPT)



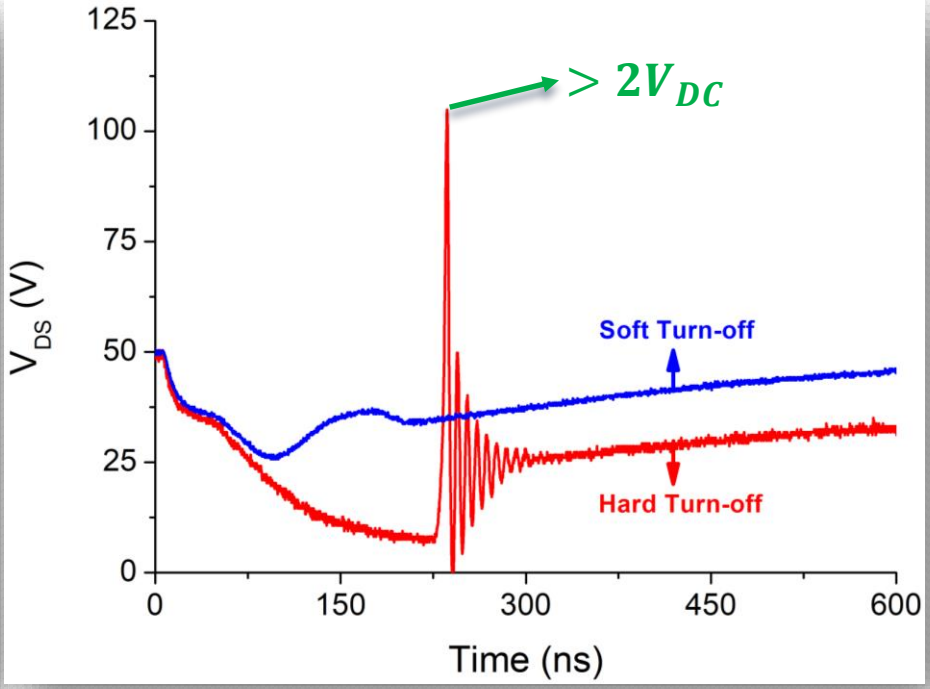
Induced voltage for DPTs

Always below the threshold

Half-bridge – SC Protection: Operation Range



SC tests

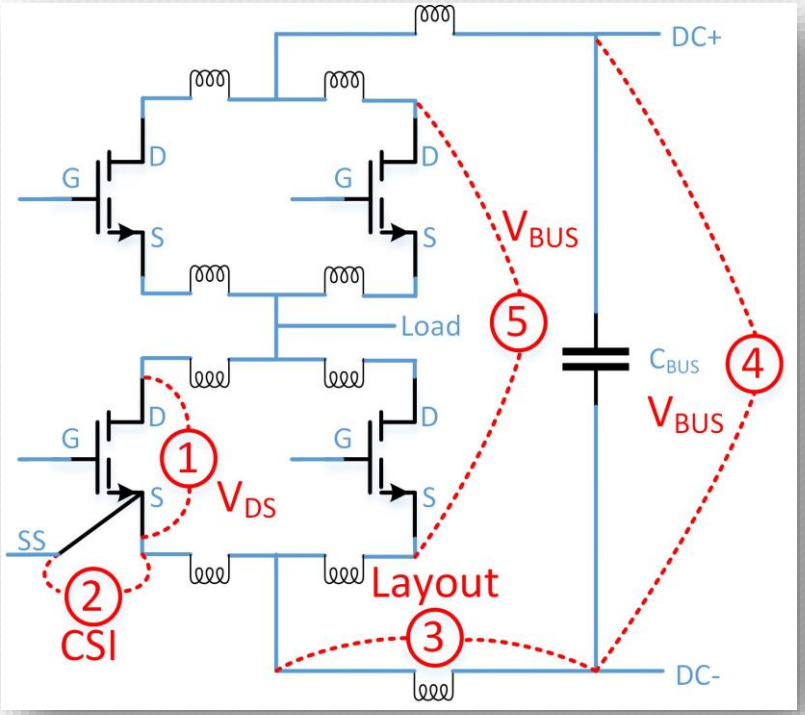


Effect of soft turn-off

Always above the threshold

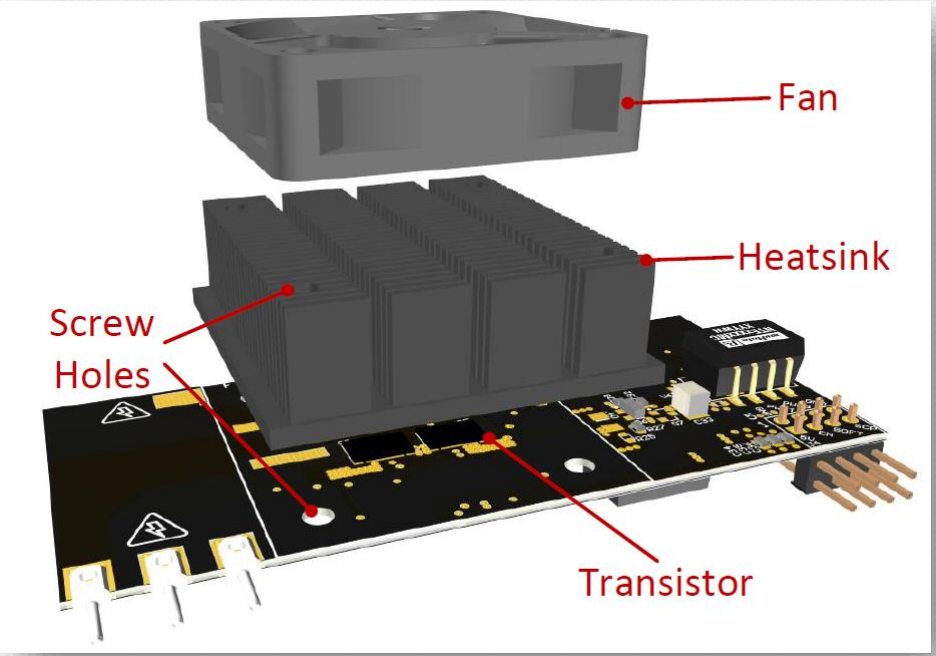
Half-bridge –SC Protection: Comparison

Study	STO Activ.	Sense	Device	Conf.
Hou et al. (2019)	70 ns	V_{DS} (1)	GaN HEMT	Single
Sun et al. (2018)	80 ns	CSI (2)	SiC	Single
Alemdar et al. (2019)	80 ns	Layout (3)	GaN HEMT	Single
Hou et al. (2018)	85 ns	V_{DS} (1)	GaN HEMT	Single
Awwad et al. (2015)	90 ns	Layout (3)	SiC	Single
This study (2020)	99 ns	Layout (3)	GaN HEMT	Parallel
Lyu et al. (2020)	200 ns	V_{BUS} (4)	GaN HEMT	Single
Wang et al. (2019)	224 ns	V_{BUS} (5)	GaN GIT	Single

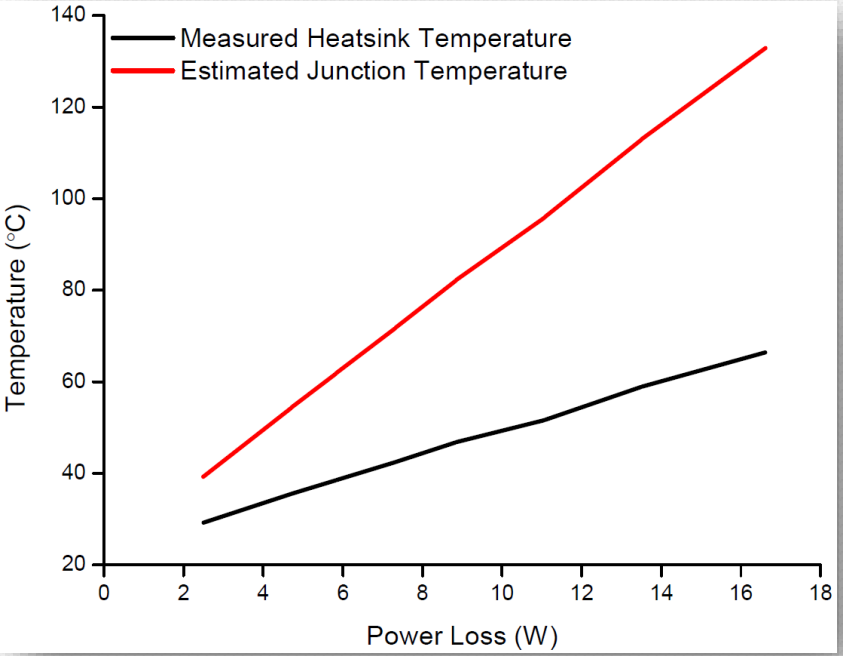


Different SC fault sense options

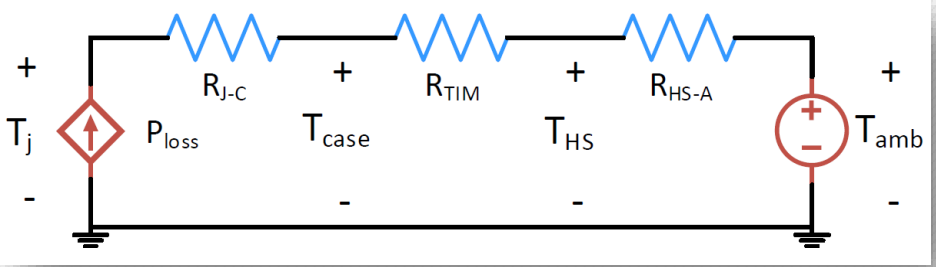
Half-bridge – Thermal Design



Mounting of cooling components



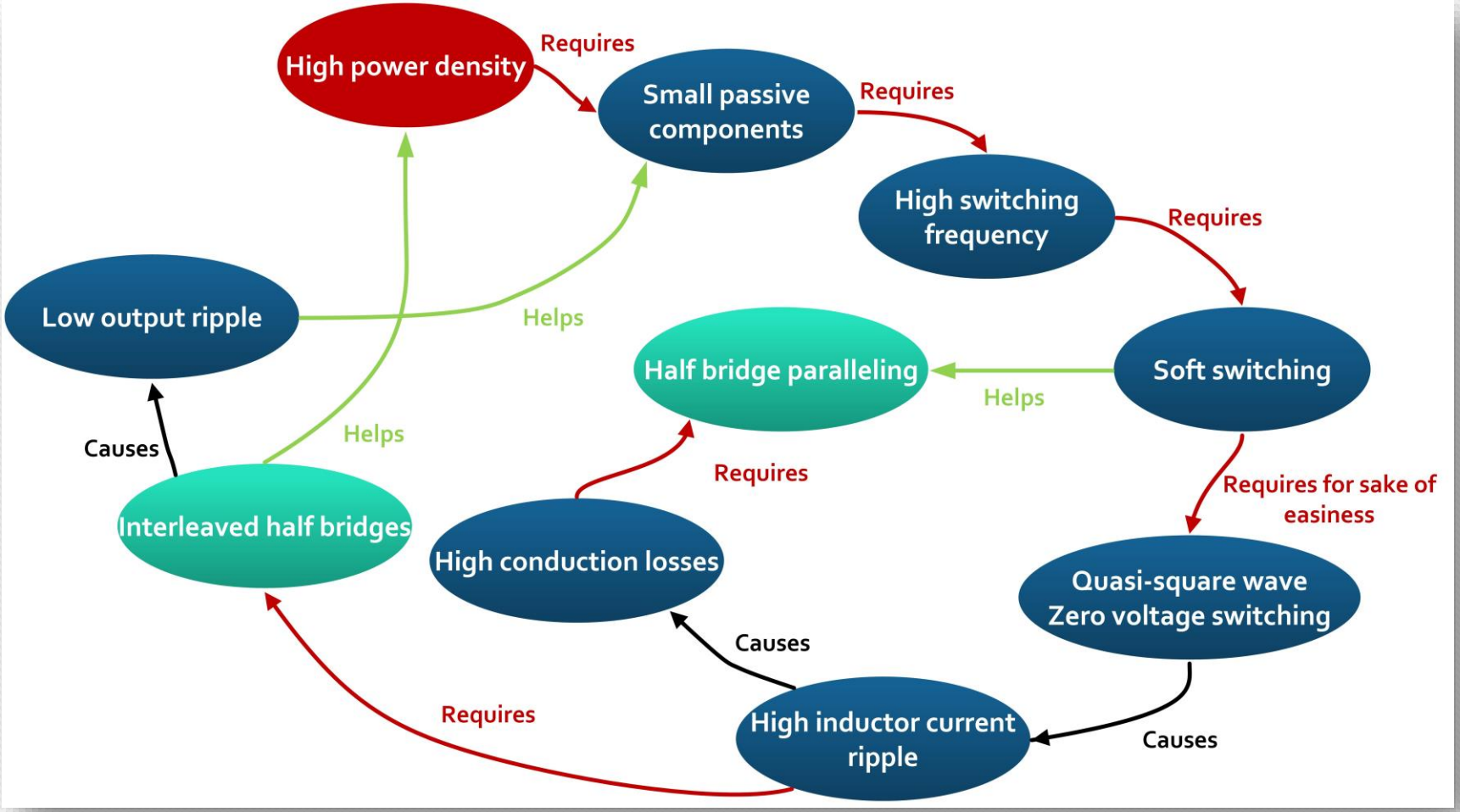
Thermal experiment results



Layout

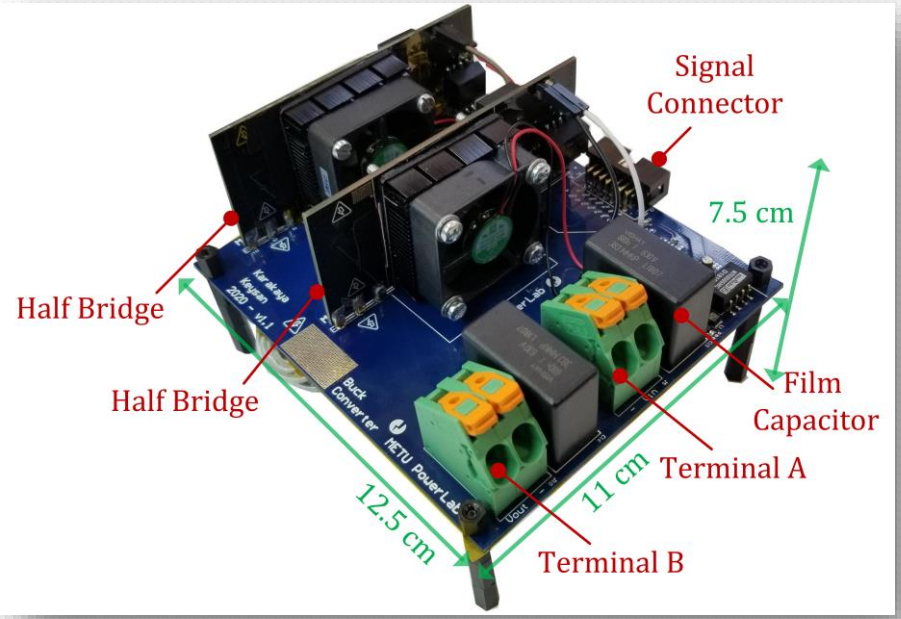
- Introduction
  - A game changer: GaN power transistors
  - Focus of thesis
- Transistor characterization
  - Input charge
  - Output capacitance
- Switching characteristics
- Half-bridge design
  - Layout optimization
  - Short-circuit protection
  - Thermal design
- Bi-directional DC/DC converter design
  - Design specifications
  - Experimental results
- Remarks and Conclusion

DC/DC Converter – Design Considerations



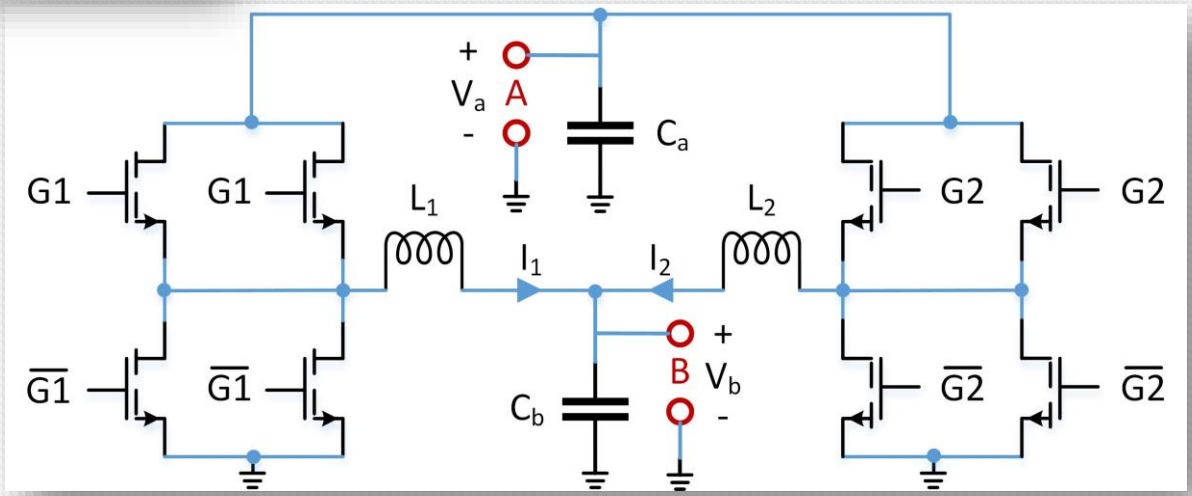
Logic diagram of converter design

DC/DC Converter – Design Considerations

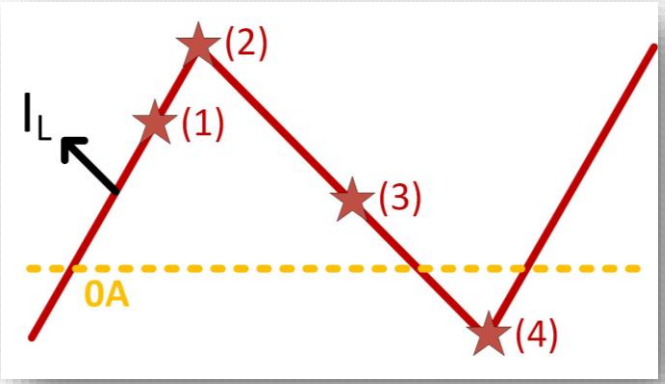


Converter

Converter Scheme



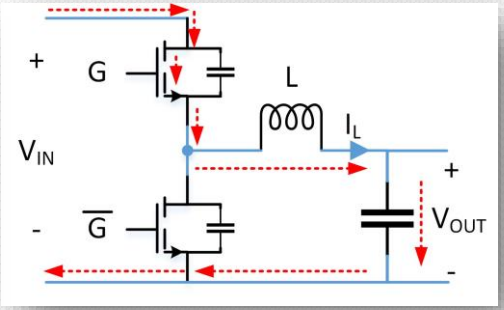
DC/DC Converter – QSW ZVS



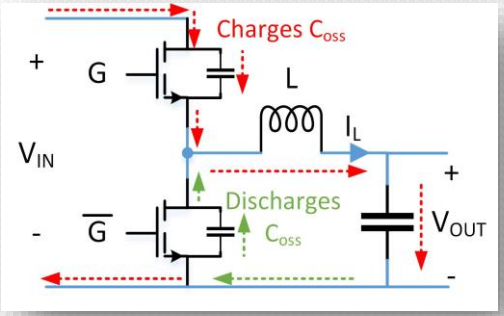
Inductor Current

$$I_{L-min} < 0$$

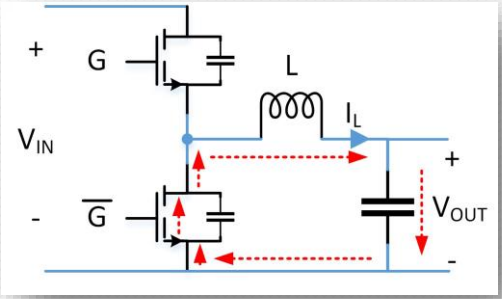
$$I_{L-pp} > 2 * \overline{I_L}$$



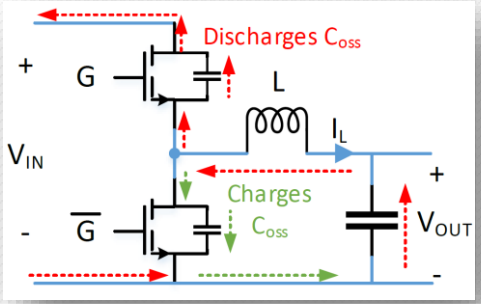
Moment (1)



Moment (2)



Moment (3)

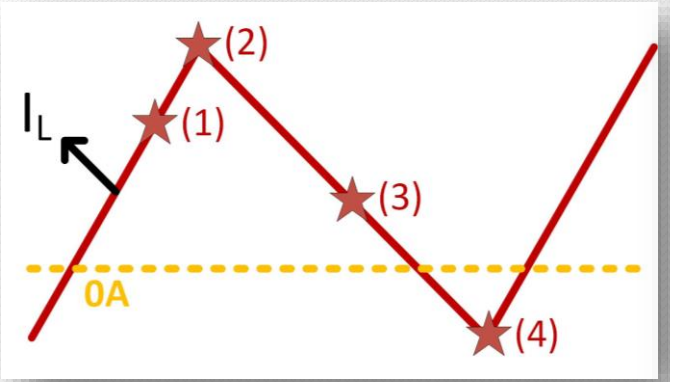


Moment (4)

Required dead-time can be calculated for moment (4)

$$t_{dead}\hat{I}_{L,neg} = 4C_{OSS}V_{DC} \quad (16)$$

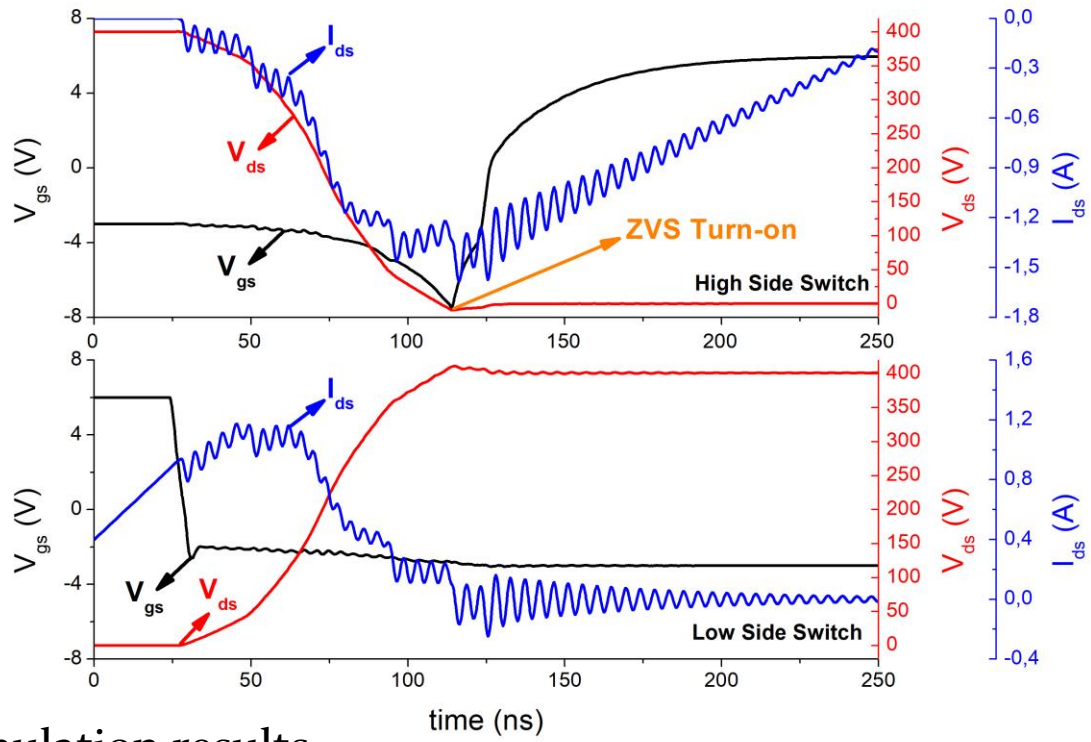
DC/DC Converter – QSW ZVS



Inductor Current

$$I_{L-min} < 0$$

$$I_{L-pp} > 2 * \overline{I_L}$$



Simulation results

Required dead-time can be calculated for moment (4)

$$t_{dead}\hat{I}_{L,neg} = 4C_{OSS}V_{DC} \quad (16)$$

DC/DC Converter – Operating Conditions and Interleaving

Operating condition

	Buck Mode	Boost Mode
Vin	400 V	270 V
Vout	270 V	400 V
Duty Cycle	0.675	0.323
Iout	20 A	13.5 A
Pout	5.4 kW	

Inductor parameters

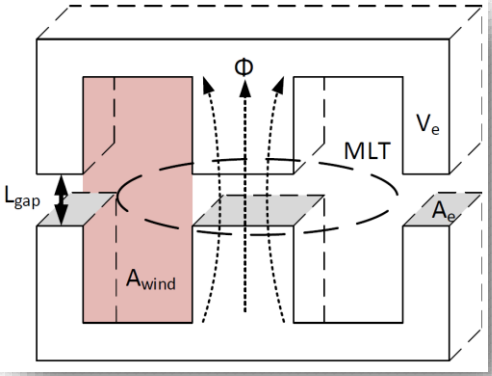
Inductance	6.8 µH
Frequency	450 kHz
Average current	10 A
Ripple Current	28 App

Main loss source on the inductor

Comparison interleaved bridge number

	Buck	Boost		
Bridge Number	$\frac{\Delta I_{cap}}{\Delta I_L}$		kW/br.	$\frac{\Delta I_L}{\overline{I_L}}$
1	1	1	5,4	2,4
2	0,515	0,521	2,7	2,8
3	0,037	0,045	1,8	3,2
4	0,235	0,228	1,35	3,6
5	0,21	0,209	1,08	4
Best	Better	Not Bad	Bad	Worse

DC/DC Converter – Inductor Design



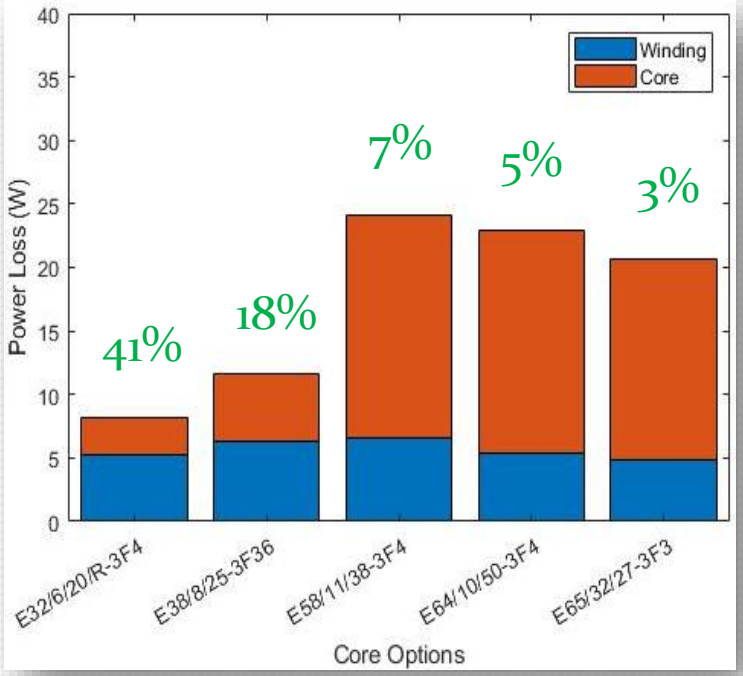
Definitions

$$R_{dc} = \frac{\rho N(MLT)}{A_{wire}} \quad (17)$$

$$P_{dc} = I_{avg}^2 R_{dc} \quad (18)$$

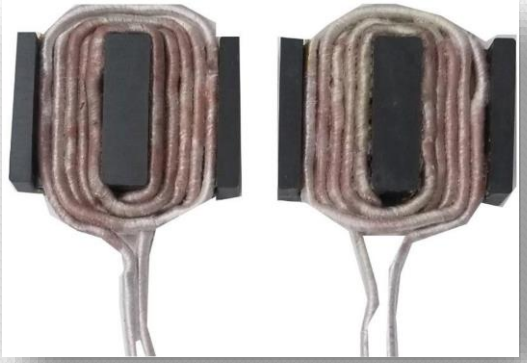
$$P_{ac} = I_{rms}^2 R_{ac} \quad (19)$$

$$P_{core} = P_{sp}(B_{ac}, f)V_e \quad (20)$$



Inductor design comparison

$$P_{ind} = P_{dc} + P_{ac} + P_c \quad (21)$$



Open view

Closed view

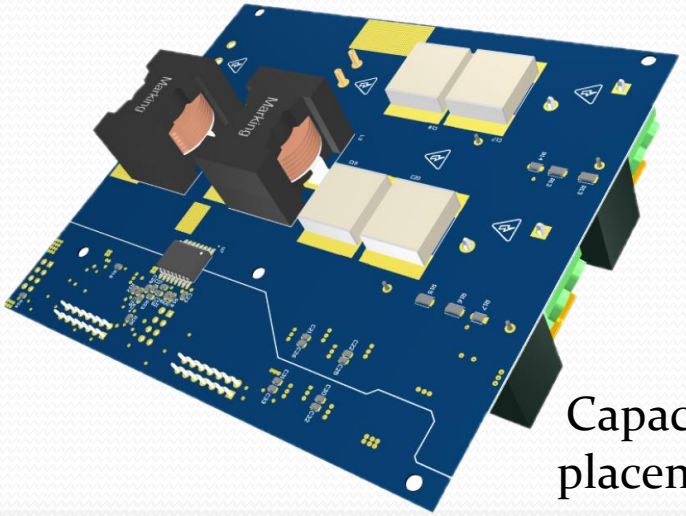
DC/DC Converter – Capacitor Selection

$$C = \frac{\Delta I}{8\Delta V(2f_{sw})} \quad (22)$$

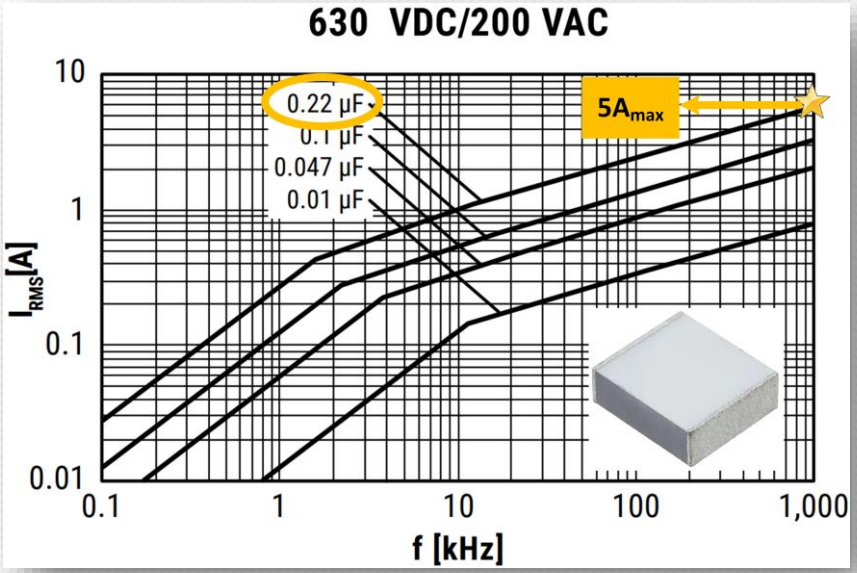
$$C > 690\ nF \rightarrow \frac{\Delta V}{V_o} < 1\% \quad (23)$$

$$I_{cap} = 7.8\ A_{rms}\ at\ 900kHz \quad (24)$$

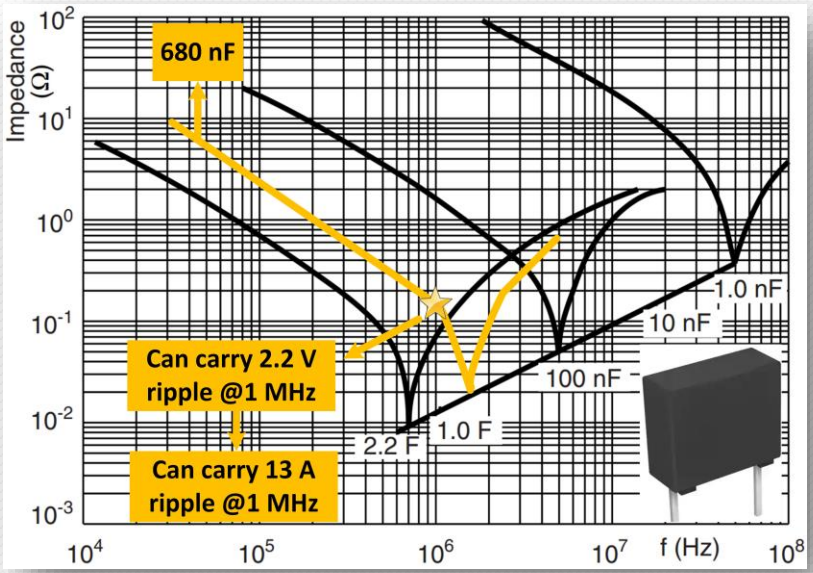
$$C_{total} = 2 * 0{,}22\mu F + 0{,}68\mu F = 1{,}12\mu F \quad (25)$$



Capacitor placement

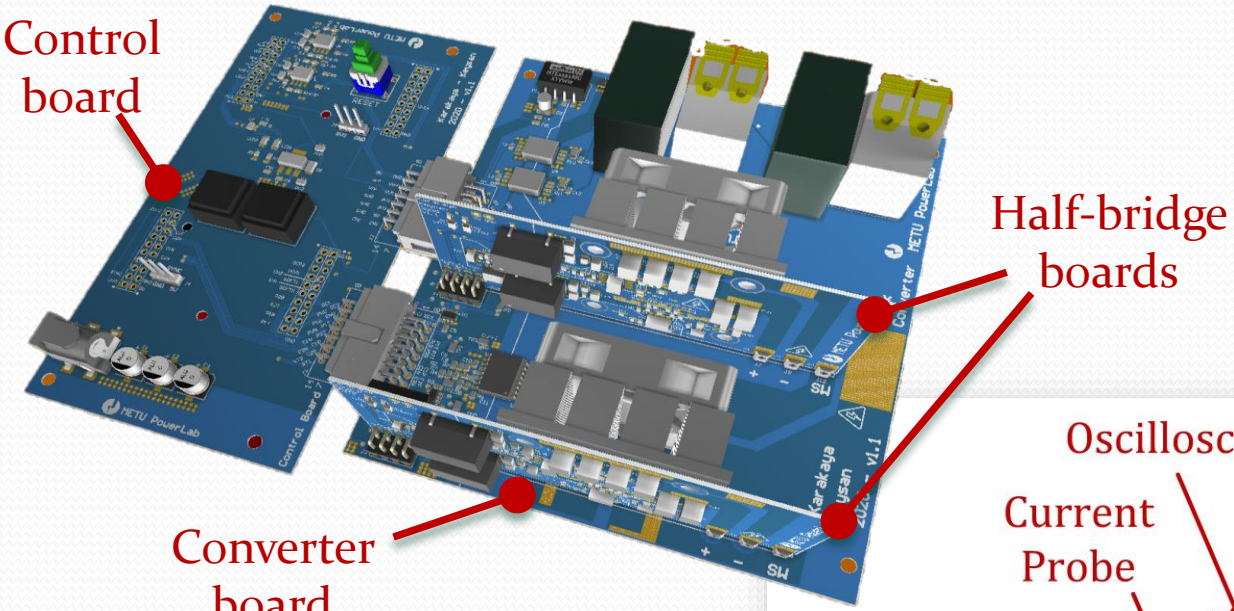


Frequency resp. of SMD cap

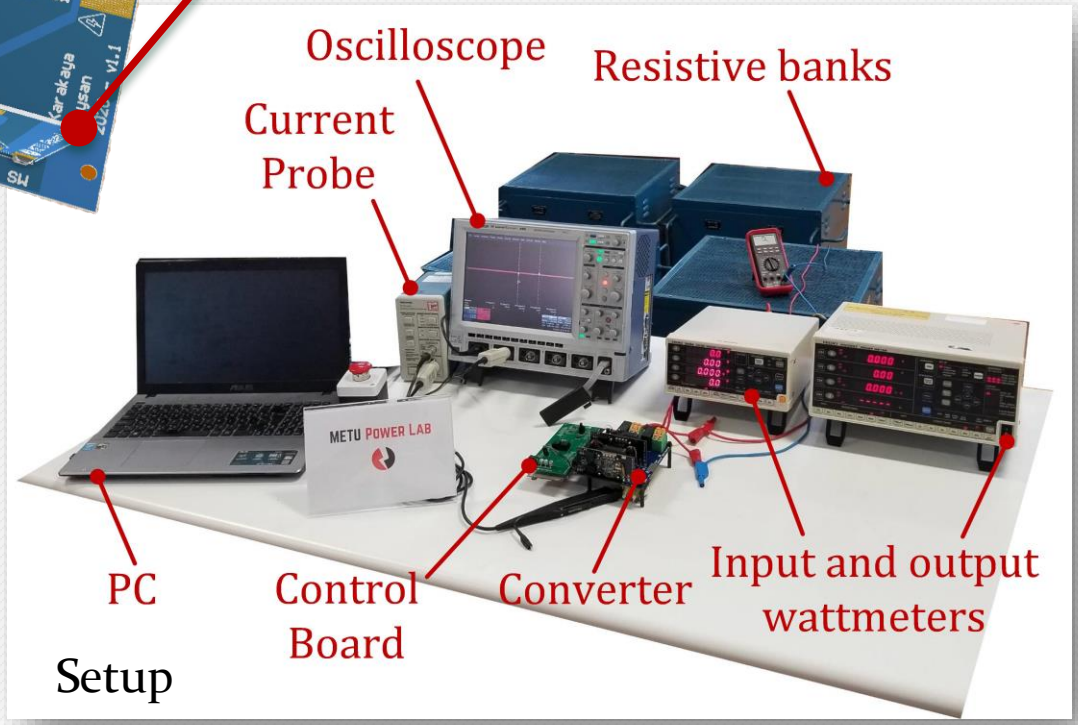


Frequency resp. of TH cap

DC/DC Converter – Setup

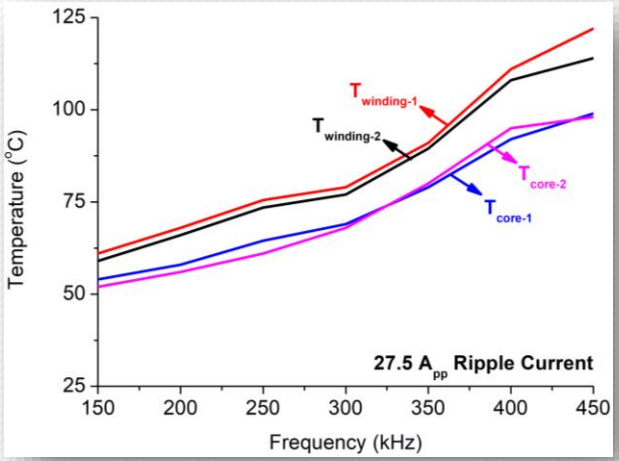


Connection of boards

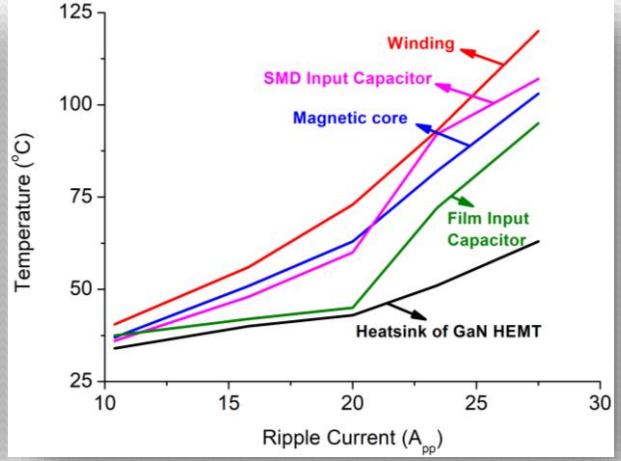


Setup

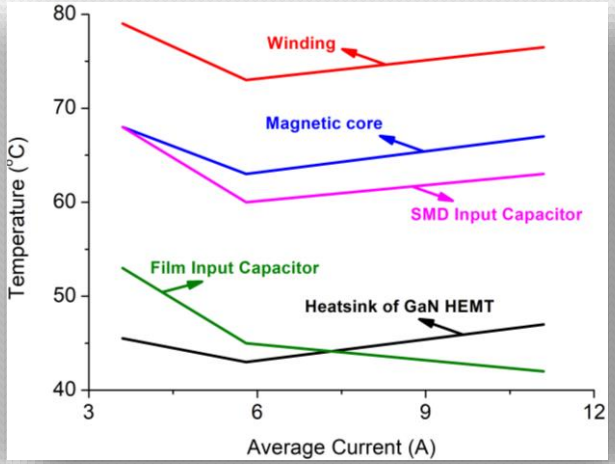
DC/DC Converter – Thermal Tests



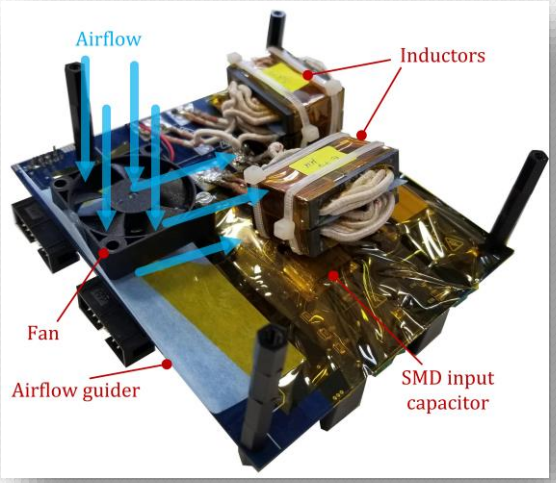
Varying frequency



Varying ripple



Varying average

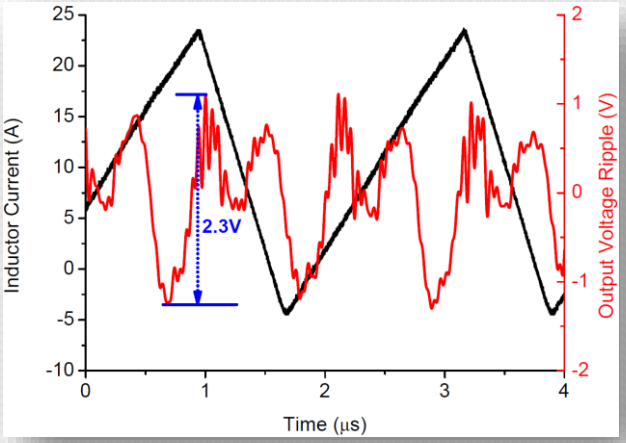


Bottom side view

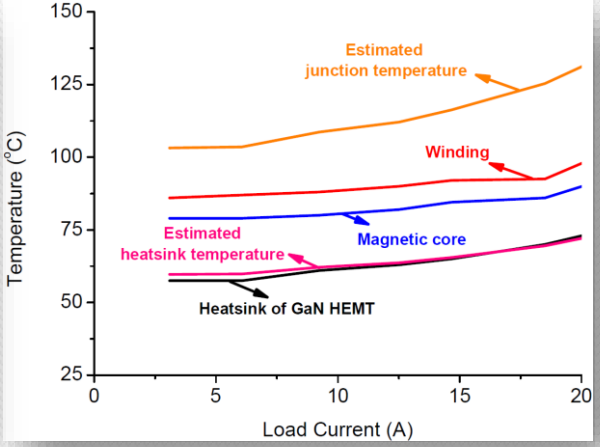
	Without fan	With fan
Winding	131 °C	86 °C
Core	119 °C	79 °C
SMD cap.	112 °C	60 °C
Film cap.	49,5 °C	44 °C
Heat sink	59 °C	57,5 °C

DC/DC Converter – Buck and Boost Modes

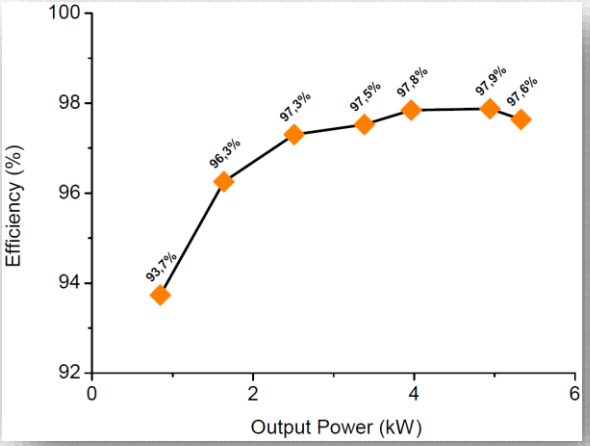
Buck Operation



Output Voltage

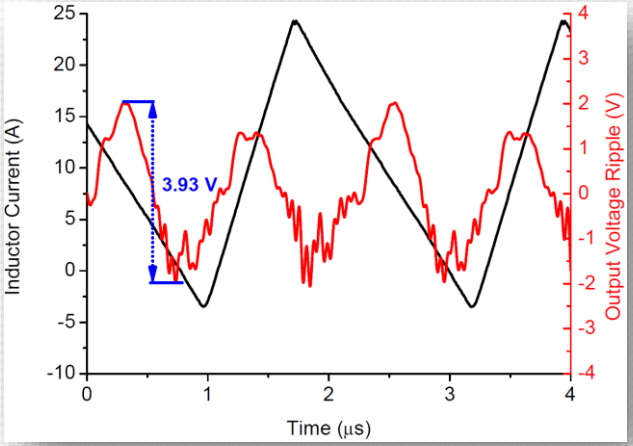


Temperature

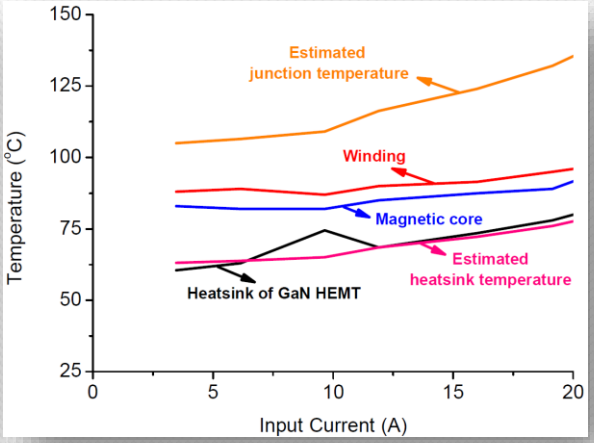


Efficiency

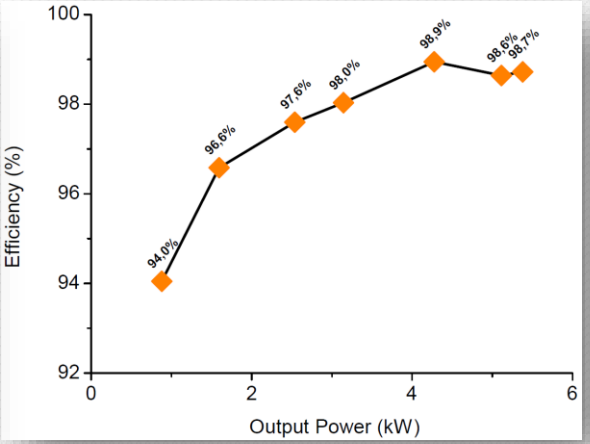
Boost Operation



Output Voltage

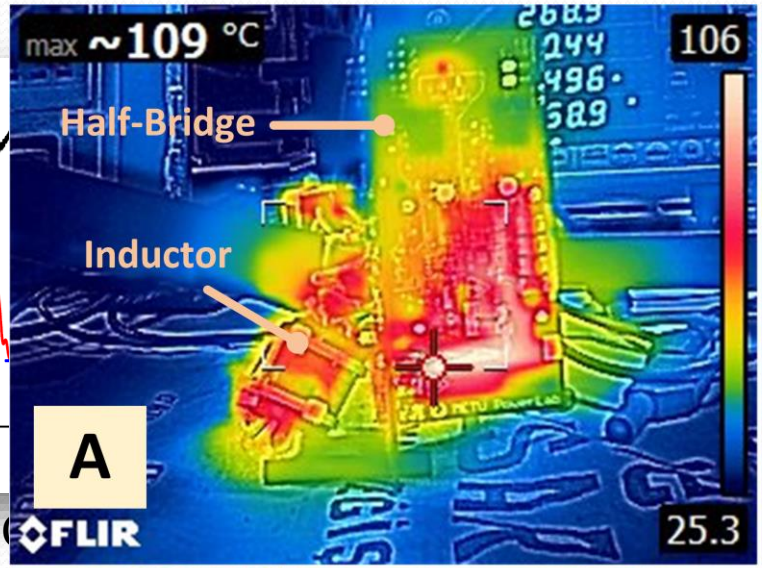


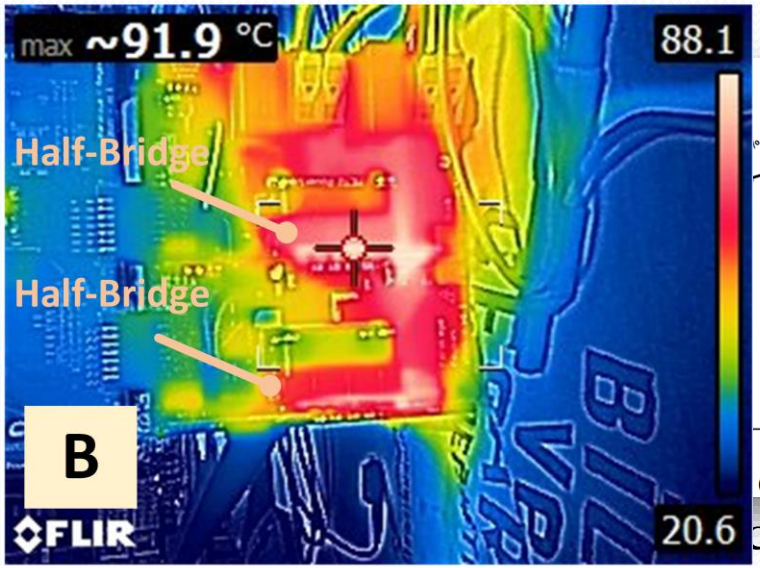
Temperature

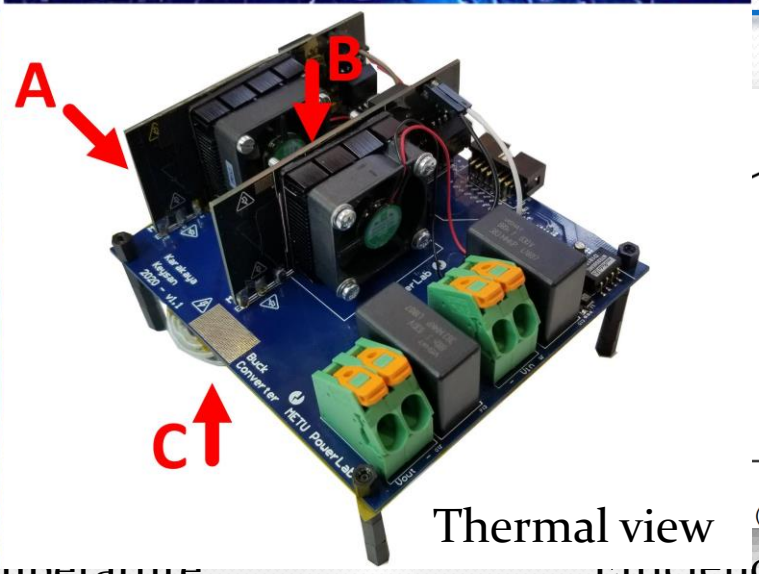


Efficiency

DC/DC Converter – Buck and Boost Modes

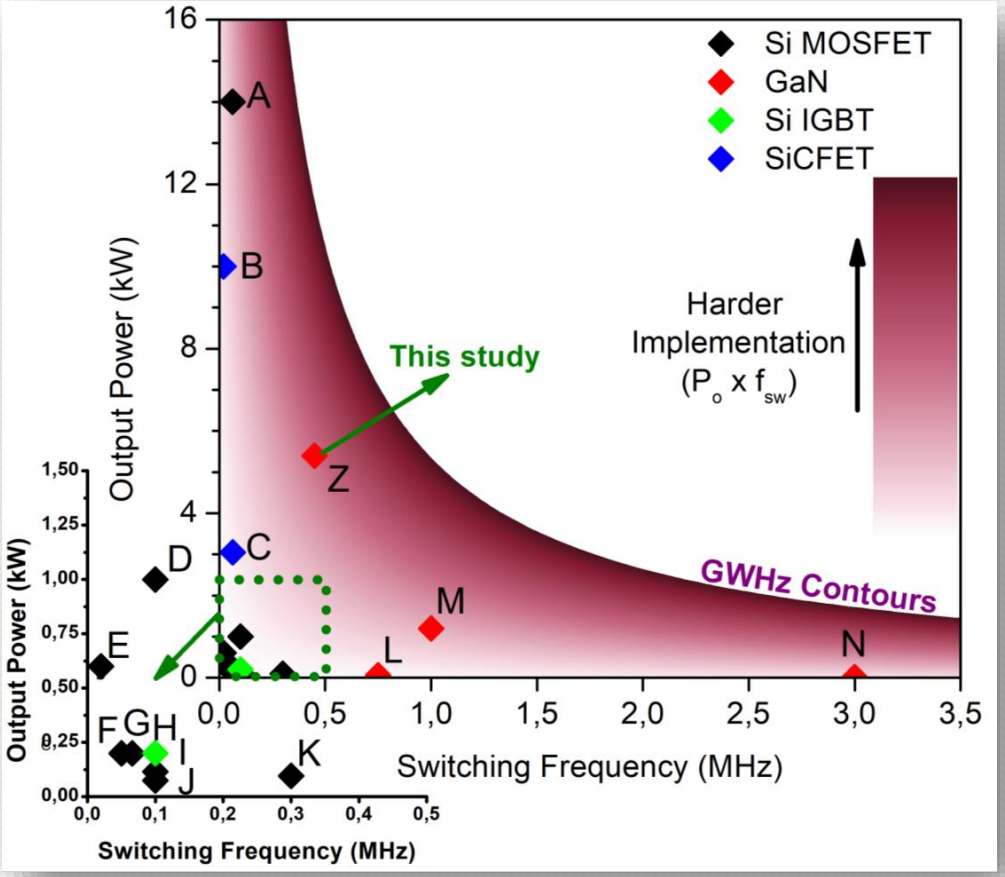






Thermal view

DC/DC Converter – Comparison



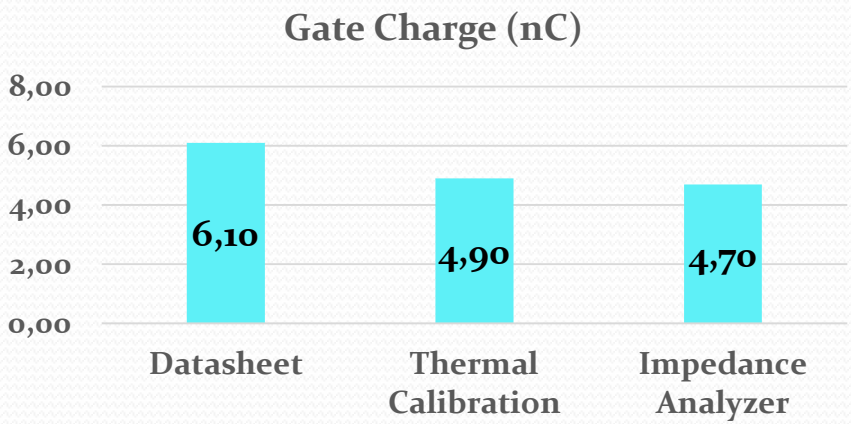
Comparison of proposed converters

Study	Po	fsw	Device
A	14 kW	66 kHz	Si MOSFET
B	10 kW	20 kHz	SiCFET
C	3.05 kW	64 kHz	SiCFET
D	1 kW	100 kHz	Si MOSFET
E	600 W	20 kHz	Si MOSFET
F	200 W	50 kHz	Si MOSFET
G	200 W	66 kHz	Si MOSFET
H	200 W	100 kHz	Si IGBT
I	115 W	100 kHz	Si MOSFET
J	75 W	100 kHz	Si MOSFET
K	96 W	300 kHz	Si MOSFET
L	60 W	750 kHz	GaN
M	1.2 kW	1 MHz	GaN
N	20 W	3 MHz	GaN
Z	5.4 kW	450 kHz	GaN

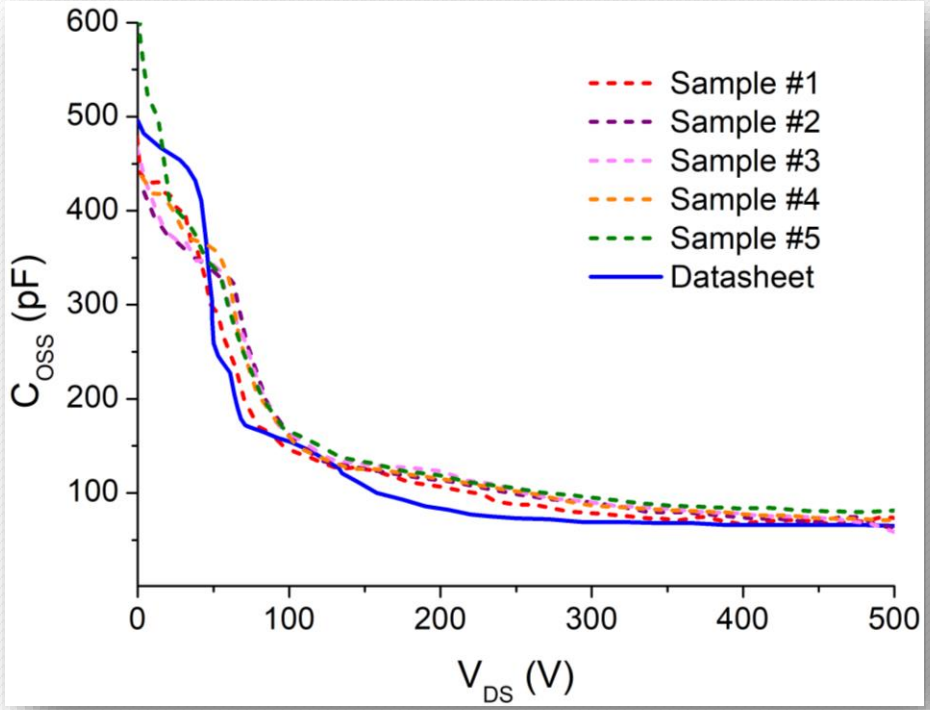
Layout

- Introduction
  - A game changer: GaN power transistors
  - Focus of thesis
- Transistor characterization
  - Input charge
  - Output capacitance
- Switching characteristics
- Half-bridge design
  - Layout optimization
  - Short-circuit protection
  - Thermal design
- Bi-directional DC/DC converter design
  - Design specifications
  - Experimental results
- Remarks and Conclusion

Remarks and Conclusion – Device

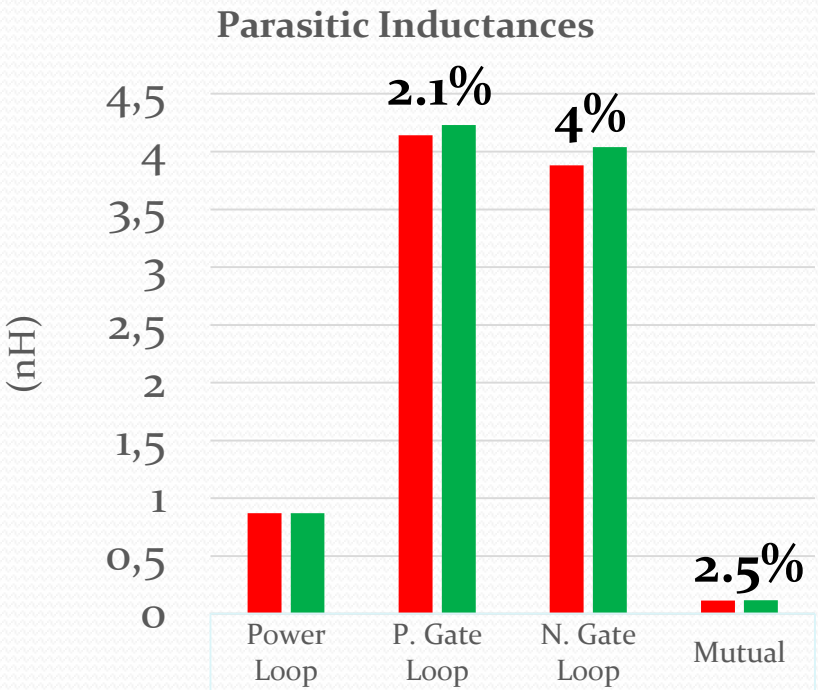


Gate charge characterization



Output capacitance characterization

Remarks and Conclusion – Half-bridge



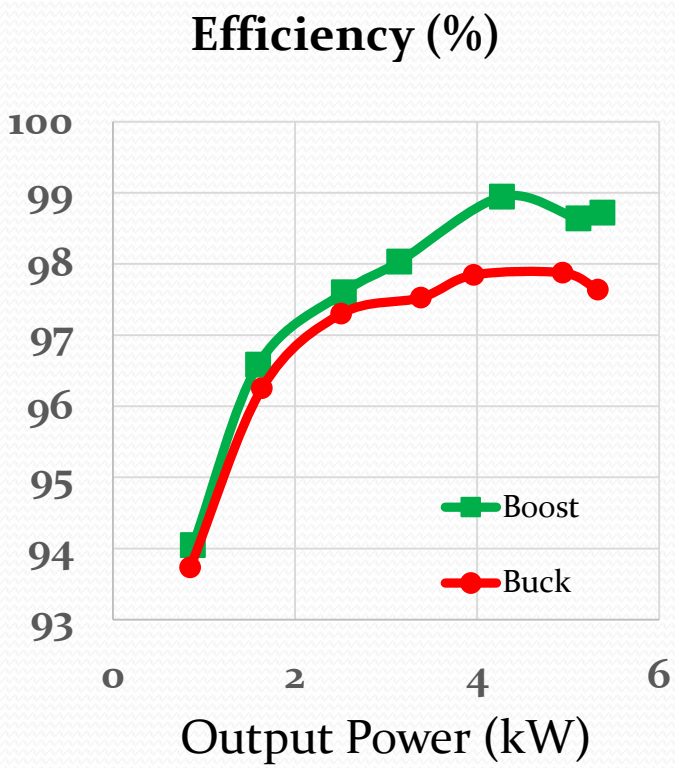
	Power Loop	P. Gate Loop	N. Gate Loop	Mutual
Left switch	0,87	4,14	3,88	0,114
Right switch	0,87	4,23	4,04	0,117

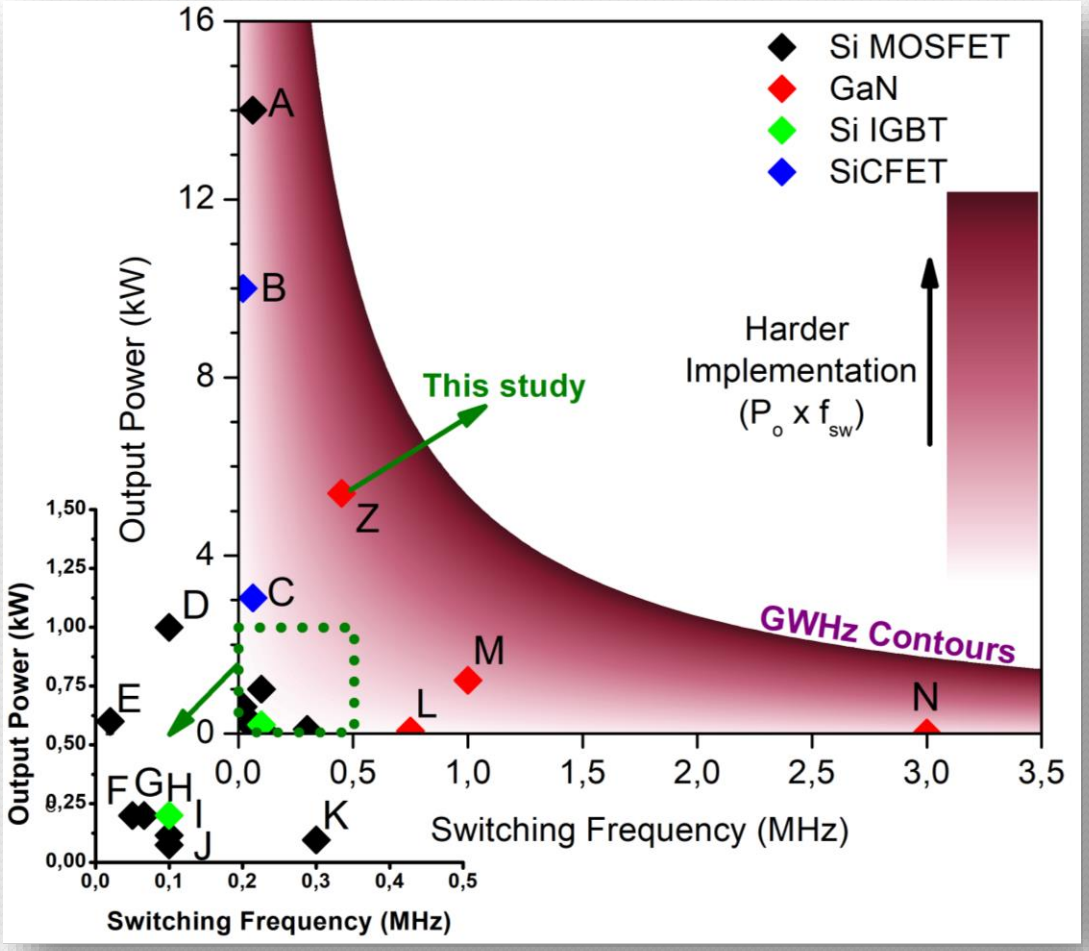
Layout design

Study	STO Activ.	Sense	Device	Conf.
Hou et al.	70 ns	V_{DS} (1)	GaN HEMT	Single
Sun et al.	80 ns	CSI (2)	SiC	Single
Alemdar et al.	80 ns	Layout (3)	GaN HEMT	Single
Hou et al.	85 ns	V_{DS} (1)	GaN HEMT	Single
Awwad et al.	90 ns	Layout (3)	SiC	Single
This study	99 ns	Layout (3)	GaN HEMT	Parallel
Lyu et al.	200 ns	V_{BUS} (4)	GaN HEMT	Single
Wang et al.	224 ns	V_{BUS} (5)	GaN GIT	Single

Short circuit protection

Remarks and Conclusion – Converter





Comparison of reported converters

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[5] F. Karakaya, M. Ugur, and O. Keysan, "Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors," 2018, pp. 1–10.
[6] J. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW-100kW systems," Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, pp. 3049–3056, 2017

Thank you for your attention.