PCB Layout Based Short-Circuit Protection Scheme for GaN HEMTs

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***Abstract*—Gallium Nitride Enhancement-Mode High Electron Mobility Transistors (GaN HEMTs) are superior to other power transistors in terms of efficiency, package size and switching speed which leads to increased power density in power converter applications. However, GaN HEMTs have much shorter short-circuit withstand time compared to the conventional devices, which is limited to several hundred nanoseconds. Therefore, reliable and fast protection solutions are required to protect GaN HEMTs from fatal over-current failures. In this paper, a novel short-circuit (SC) protection scheme based on fault current sensing by using Printed Circuit Board (PCB) layout parasitics is proposed. The proposed scheme uses the voltage drop on the parasitic inductance of the PCB trace to detect very intense high slew rate SC faults. In addition, the voltage drop on the parasitic resistance of the PCB trace is utilized to detect relatively slow over-current (OC) faults. Once a fault is detected, a soft turn-off mechanism is initiated by the proposed circuit to turn-off devices gradually to eliminate over-voltage breakdown risk. The proposed circuit is verified by both SPICE simulations and hardware implementation. The experimental results show that both SC and OC faults can be detected and GaN HEMTs can be protected. The total operation duration for the circuit is 370 ns during a SC fault. The SC fault can be detected within 30 ns and the soft turn-off mechanism is initiated within 80 ns to terminate the SC current flowing through the GaN HEMTs within 290 ns.**

***Index Terms*—GaN HEMT, gallium nitride, short-circuit protection, over-current protection, fault**

I. Introduction

The wide band-gap devices are strong candidates to meet the power density and efficiency requirements of today's commercial products [1]. Especially, the Gallium-Nitride (GaN) based power semiconductor devices are superior to Silicon (Si) and Silicon-Carbide (SiC) in terms of lower on-state resistance and higher switching speed [2]. However, due to increased switching speed, the GaN based circuits are more susceptible to noises and false turn-on faults [3]. In addition, due to fast switching capability, high amount of short-circuit (SC) current can flow through GaN HEMTs in the order of nanoseconds after a fault occurs.

With a typical maintenance time of 200 ns [4], a SC detection and protection circuit is required to act quickly in a reliable manner to protect GaN HEMTs. The most common method is the desaturation technique, where the voltage between the drain and source terminals is sensed [5]. However, this technique increases the equivalent output capacitance which leads to higher switching losses and relatively long settling time [6]–[8]. Another technique is sensing the voltage across the parasitic inductance at the source pin of a device [9] which is incapable of detecting the fault under low di/dt conditions such as Fault Under Load (FUL) type of short circuits. Current shunts which are cascaded to GaN HEMTs [8] are not applicable because adding components on the power loop increases the layout inductance and power losses. In [6], a protection method is proposed that uses steady-state nonzero gate current of GaN gate injection transistors (GITs), but it is not applicable for HEMTs due their voltage-driven gate structure as stated in [7]. Lastly, a two-stage protection circuitry, where a soft-turn off and hard turn-off are both available, is proposed in [7]. Similar to desaturation technique, the increased output capacitance and complicated reference voltage selection due to the temperature-dependent saturation current [6] are the weakest points of this technique.

In this paper, a novel SC protection scheme based on fault current sensing is proposed. The current flowing through the GaN HEMTs during SC or OC fault is sensed by utilizing some part of the PCB trace as a current sense impedance. The sensed signal is processed by a signal processing stage to generate the fault trigger signal which alerts the digital controller of the converter circuit to initiate soft turn-off mechanism. Then, the devices are turned off gradually to prevent over-voltage breakdown failures. The proposed method is capable of detecting both intense SC faults like a shoot-through and load over-current type faults.

The rest of the paper is organized as follows. Section II describes the proposed protection scheme and its operating principle. Section III presents design considerations related to PCB trace based current sense, signal processing stage and gate driver structure. In Section IV, circuit implementation and experimental results are given to verify the proposed method. Section V gives the conclusion.

II. Protection Scheme and Operating Principle

As shown in Fig. 1, the protection scheme has three building blocks, namely, the PCB based current sense impedance, the signal processing stage, and the soft turn-off block, which is implemented in the gate driver circuit. The micro-controller (μC) and the isolated gate drivers, which are already employed

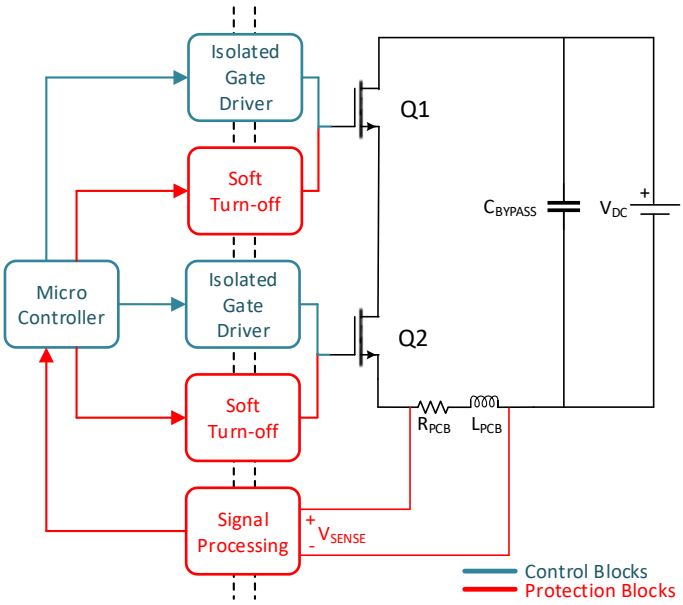


Fig. 1: The main block diagram of SC protection method.

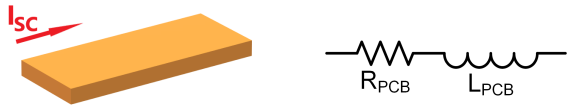
for the converter operation, are also utilized to implement the proposed scheme.

In this method, the induced voltage created by the short-circuit current (I_{SC}) on a portion of the power loop is sensed to detect faults. Due to the parasitic inductance (L_{PCB}) and copper resistance (R_{PCB}) of the PCB trace, the sensed voltage, V_{SENSE}, has inductive and resistive components as given in (1);

$$V_{SENSE} = R_{PCB} I_{SC} + L_{PCB} \frac{\partial I_{SC}}{\partial t} \tag{1}$$

The voltage on the PCB trace deviates greatly from its nominal operation level under a fault. The inductive part is sensitive to high slew rate current transitions and it becomes more dominant when SC fault current flows. On the other hand, the voltage drop on the resistive part can be used to detect relatively low slew rate current flows when the inductive part can be eliminated properly.

The V_{SENSE} is filtered out at the input of the signal processing stage with two different R-C networks to detect SC and OC faults. For the SC faults, a R-C network is used solely to filter out noise. On the other hand, for OC faults, a different R-C network is used as a phase compensation network in order to capture the purely resistive voltage drop on the PCB sense trace. Then, the output voltages of these R-C networks are compared with a threshold level to generate a fault trigger signal that is used to alert the μC to protect the GaN HEMTs. Once the μC receives the fault trigger signal, it initiates the soft turn-off mechanism, which is implemented in the gate driver circuit. The stored charge in the input capacitance of the GaN HEMTs are discharged slowly in order to prevent them from over-voltage breakdown. In the next section, some critical design considerations are provided in detail.



(a) (b)

Fig. 2: The geometry (a) and equivalent circuit model (b) of the sense trace.

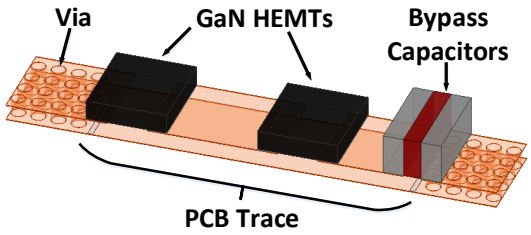


Fig. 3: The layout of the half bridge.

III. Design Considerations

A. PCB Based Current Sense

PCB traces of power converters consists of parasitic resistances, self and mutual inductances, and self and mutual capacitances. As mentioned before, some part of the PCB trace, namely, a flat conductor is used as a current sensor in the protection circuit to sense fault currents. The geometry of the sense trace and its equivalent circuit model are presented in Fig. 2. For the sake of simplicity, mutual inductances and all capacitances are neglected in the model. Therefore, the equivalent impedance of the sense trace can be represented in the form of (2);

$$Z_{TRACE} = R_{PCB} + j\omega L_{PCB} \tag{2}$$

In order to achieve improved efficiency, faster switching speeds, and reduced device voltage overshoot, PCB layout design is very critical for GaN HEMTs. Therefore, the effect of the current sense trace on the circuit layout should be kept minimum. For that purpose, return path of the power loop, which is implemented on the bottom layer, is selected as the current sense trace as shown in Fig. 3. The current flow paths under SC and OC faults are shown in Fig. 4. The current flows

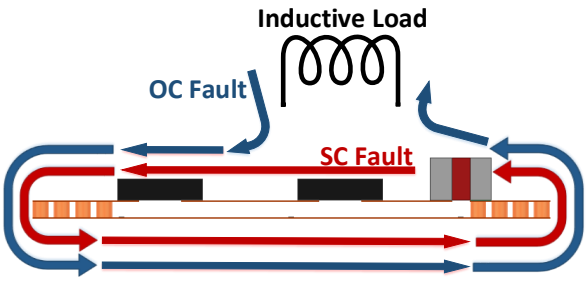


Fig. 4: Current flow paths under faults.

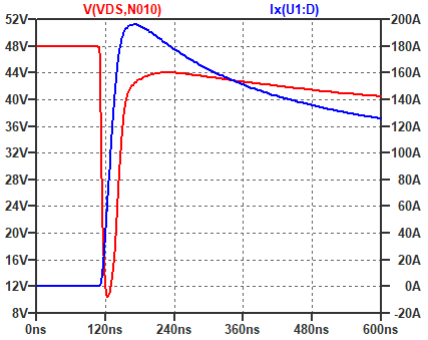


Fig. 5: SC fault simulation results without protection; red: V_{DS} of Q_2, blue: I_{DS} of Q_2.

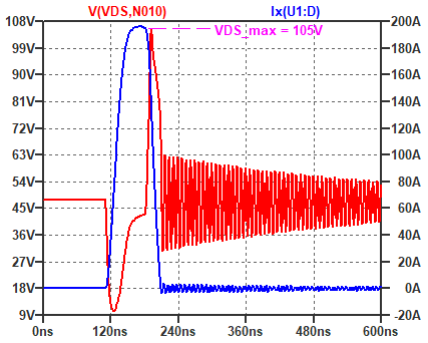


Fig. 6: SC fault simulation results with hard turn-off protection; red: V_{DS} of Q_2, blue: I_{DS} of Q_2.

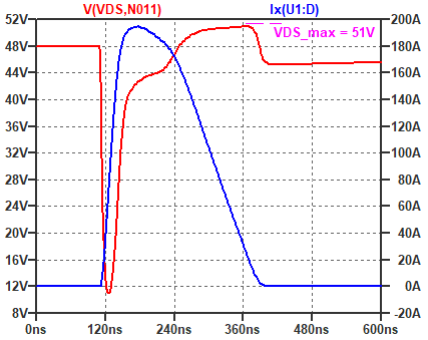


Fig. 7: SC fault simulation results with soft turn-off protection; red: V_{DS} of Q_2, blue: I_{DS} of Q_2.

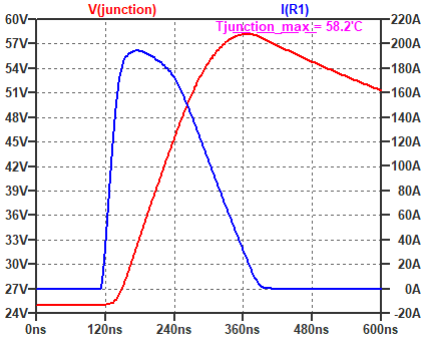


Fig. 8: SC fault simulation results with soft turn-off protection; red: junction temperature of Q_2, blue: I_{DS} of Q_2.

through all of the power loop under a SC fault. For an OC fault, the current flows through one of the transistors and the inductive load. Therefore, it is essential to locate current sense trace properly on the power loop to ensure that fault current will flow through it for each fault type.

In order to investigate the performance of the proposed scheme, SPICE simulations are performed by LTspice. The half-bridge circuit with GaN HEMTs, shown in Fig. 3, is modelled. In addition to component models, PCB layout parasitics are also implemented into the simulation model. The power loop and the PCB sense trace inductances and resistances are obtained by finite element analysis using Ansys Q3D Extractor. The total resistance and inductance of the power loop is 2.74 mΩ (for DC) and 4.96 nH (for 50 MHz) respectively.

Fig. 5 indicates a SC fault situation without protection where Q_2 is turned on while Q_1 is already on. As shown in Fig. 5, the drain current of Q_2 rises dramatically. In Fig. 6, the protection is achieved by the hard turn-off of Q_2. In other words, the device is turned off by the gate driver circuit when the drain current is relatively high. Therefore, due to the existence of parasitic inductances in the circuit, the high di/dt leads to a voltage overshoot on the device, which could break down the device. In Fig. 7, instead of hard turn-off, soft turn-off is applied to the fault, where the gate to source voltage is decreased by using additional components in the gate driver circuit. Thus, relatively low voltage overshoot can be achieved. The device junction temperature rise should be limited to an acceptable value when soft turn-off protection is applied. Fig. 8 represents the relative junction temperature rise during the soft turn-off protection where the case temperature is taken as 25°C.

The voltage drop on the PCB sense trace during a SC fault with soft turn-off protection is shown in Fig. 9. L_{PCB} leads to a voltage spike while the SC current rises. Then, the voltage drop becomes negative during the soft turn-off instant. This voltage is used by the signal processing stage to detect the SC fault. Fig. 10 indicates a OC fault situation with soft turn-off protection where Q_2 is turned off while the load current is rising gradually. Fig. 11 shows the voltage drop on the PCB sense trace. The sense voltage is not proper to use to detect OC faults. The voltage drop across the L_{PCB}, V_{L-PCB}, and the voltage drop across the R_{PCB}, V_{R-PCB}, are shown separately in Fig. 12. It is clear that, instead of V_{SENSE}, purely resistive voltage drop on the R_{PCB} can be used to detect the fault current. In the next section, how these signals are used to detect SC and OC faults are addressed in detail.

B. Signal Processing Stage

A signal processing stage is used to process V_{SENSE} to generate the fault trigger signal, V_{TRIG}. This stage includes two R-C networks, a non-inverting amplifier, two comparator circuits, and a digital isolator as shown in Fig. 13.

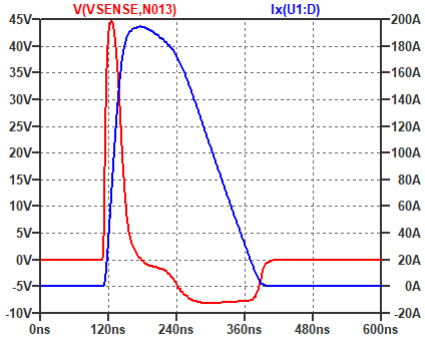


Fig. 9: SC fault simulation results with soft turn-off protection; red: V_{SENSE}, blue: I_{DS} of Q_2.

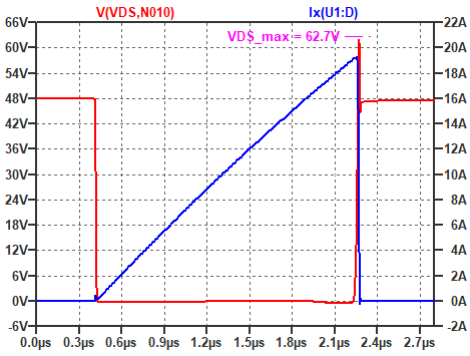


Fig. 10: OC fault simulation results with soft turn-off protection; red: V_{DS} of Q_2, blue: I_{DS} of Q_2.

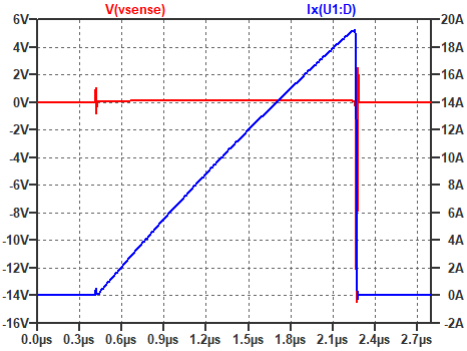
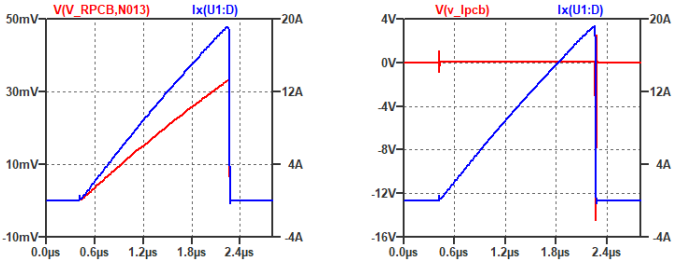


Fig. 11: OC fault simulation results with soft turn-off protection; red: V_{SENSE}, blue: I_{DS} of Q_2.



(a) (b)

Fig. 12: OC fault simulation results with soft turn-off protection: (a) red: V_{R-PCB}, blue: I_{DS} of Q_2; (b) red: V_{L-PCB}, blue: I_{DS} of Q_2.

As previously mentioned, different R-C networks are required for SC and OC faults. The Part A of the signal processing stage is adjusted to utilize V_{SENSE} to detect high slew rate SC current. R_A and C_A are used for filtering. Schottky diodes are used to clamp the positive and negative voltage spikes on the V_{SENSE} to not to destruct the circuit components. The signal processing stage has its own isolated power supply to not to be affected from the ground oscillations occurring during faults. This is the reason why a digital isolator is employed between the signal processing stage and the μC.

The Part B is designed for OC fault detection. R_B and C_B filters the V_{SENSE} to provide the true resistive voltage drop, V_{TRV}, to the input of the non-inverting amplifier, G. During the fault, I_{SC} and V_{SENSE} are greater than zero. The Laplace transformation expressions of I_{SC} and V_{SENSE} can represented as i_{SC}(s) and v_{SENSE}(s) respectively. v_{TRV}(s) is derived in (3). Also, time constants τ_1 and τ_2 are defined in (4) and (5) respectively. To precisely capture the resistive voltage drop on the sense resistor, R_B and C_B parameters should be properly selected. When τ_1 is made equal to τ_2, then (6) can be derived. As a result, V_{TRV}(t)=R_{PCB}*I_{SC}(t) can be obtained from (6) by means of inverse Laplace transformation. Thus, V_{TRV} can be amplified and used by the comparator B to detect OC fault current.

$$v_{TRV}(s) = \frac{R_{PCB}(1 + sL_{PCB}/R_{PCB})}{1 + sR_BC_B} * i_{SC}(s) \quad (3)$$

$$\tau_1 = L_{PCB}/R_{PCB} \quad (4)$$

$$\tau_2 = R_BC_B \quad (5)$$

$$v_{TRV}(s) = R_{PCB} * i_{SC}(s) \quad (6)$$

The R_{PCB} is small in magnitude, and thus, V_{TRV} has a small amplitude. Therefore, an amplifier is required to amplify the signal up to a comparable level, V_{AMP}. This is the reason why Part B circuit is not proper to detect SC faults. High slew rate SC current results in very high frequency V_{TRV}. It is difficult to amplify such a high frequency signal. A very high gainbandwidth product amplifier will be required for this purpose which is not cost-effective. Outputs of the comparators are connected through diodes to implement an OR logic, which is used to generate fault trigger signal for both SC and OC faults.

The most critical design consideration for the Part B is the operating temperature of the PCB sense trace, which impacts directly the R_{PCB} parameter. The resistivity of copper increases as the temperature increases. The normalized R_{PCB}

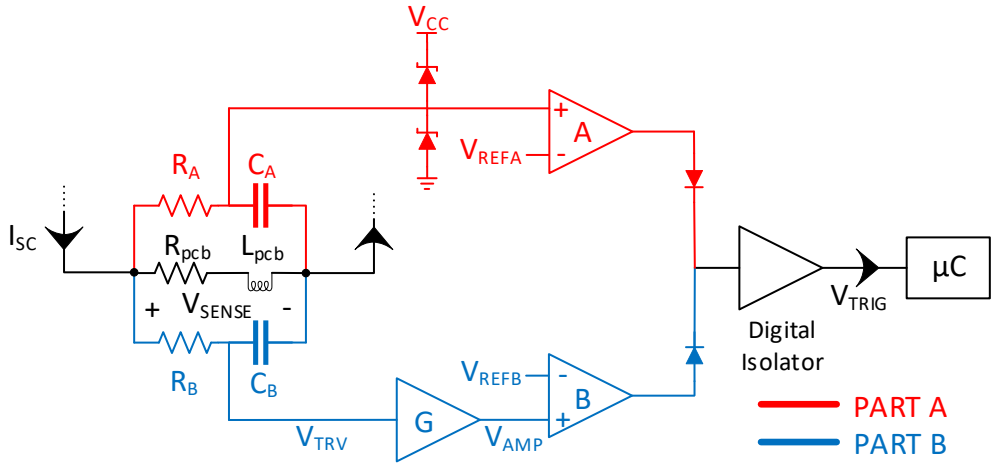


Fig. 13: Signal processing stage.

value varies from 0.75 to 1.3 when the operating temperature varies from -40°C to 100°C, as shown in Fig. 15. This means τ_1 decreases as the temperature increases. In order to keep τ_2 equal to τ_1, temperature compensation has to be realized in the R_B-C_B network. Otherwise, the circuit can not operate properly over the full operating temperature range.

To achieve temperature compensation, a simple method is to let the R_B value decrease as the temperature increases. For this purpose, instead of a single fixed resistor, a resistor network employing a negative temperature coefficient (NTC) thermistor R_{NTC} and two fixed value resistors R_1 and R_2 are used as R_B in the network as shown in Fig. 14. NTC thermistors are made from a mixture of metal oxides which gives them a negative electrical resistance versus temperature relationship. The resistance of an NTC thermistor can be calculated by (7) where $R_{NTC-ref}$ is the resistance of the thermistor at the reference temperature of 298.15 K, β is the material constant, and T is the temperature in K. Then, the equivalent R_B value, R_{B-EQ}, appearing in the network can be represented by (8).

$$R_{NTC} = R_{NTC-ref} e^{(\beta(\frac{1}{T} - \frac{1}{298.15}))} \tag{7}$$

$$R_{B-EQ} = \frac{R_{NTC}R_1 + R_{NTC}R_2 + R_1R_2}{R_{NTC}R_2} \tag{8}$$

The R_{B-EQ} value decreases as the temperature increases as shown in Fig. 15. From (4) and (5), in order to achieve temperature compensation, the product of R_{B-EQ} and R_{PCB} should be kept constant over the full operating temperature range. Fig. 15 shows implementation of the temperature compensation with maximum error of 5%. In order to achieve the best possible compensation, the NTC thermistor should be the same temperature as the PCB track sense impedance. Thus, they should be placed in close proximity in the PCB layout.

C. Gate Driver Design

An isolated gate driver with two outputs (on and off) is implemented separately for each transistor. The gate driver can

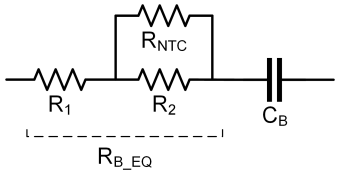


Fig. 14: Implementation of R_{B-EQ}.

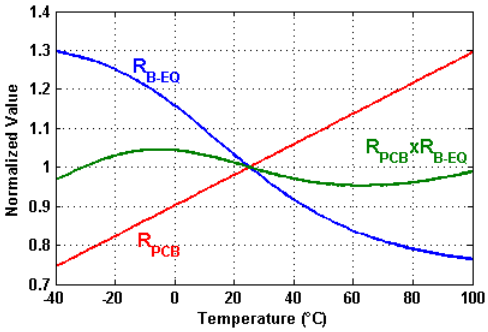


Fig. 15: Temperature compensation implementation in R_B-C_B network.

turn-on and turn-off the transistor in a fast and hard manner. A hard turn-off which stops the SC current immediately might cause failure of transistors due to over-voltage. Therefore, a soft turn-off structure is also implemented for each transistor. The resulting gate driver design is shown in Fig. 16.

After detection of a fault, the μC initiates the soft turn-off mechanism by turning the BJT on. The BJT starts to discharge the stored energy in the input capacitance of the GaN HEMTs and the speed of discharge can be adjusted by a base resistor, R_{ST}. Decreasing the gate-source voltage of the transistor decreases the conductivity of transistor channel. Finally, the device becomes completely turned off. It should be noted that the BJT decreases the gate-source voltage while

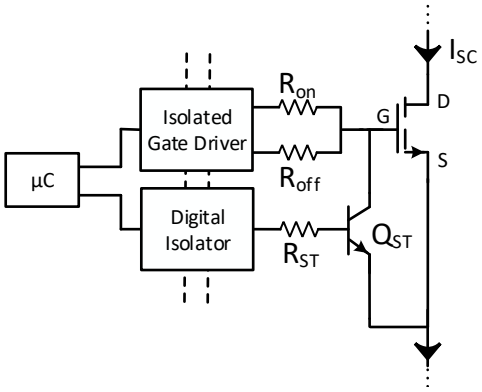


Fig. 16: Gate driver structure including soft turn-off mechanism.

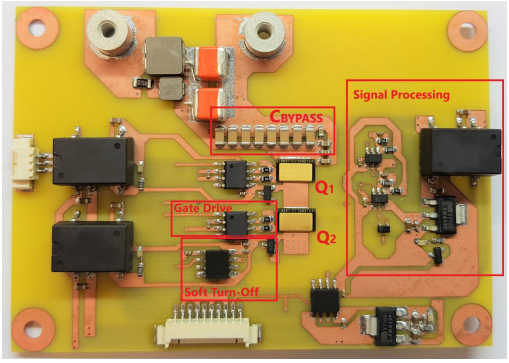


Fig. 17: Half-bridge prototype, top layer.

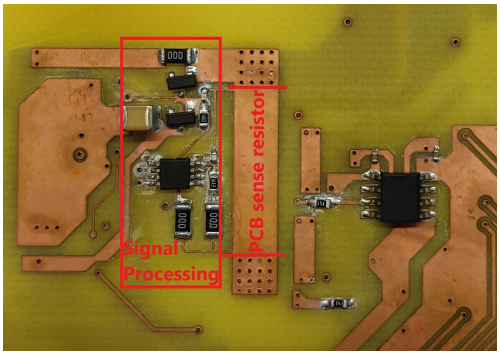


Fig. 18: Half-bridge prototype, bottom layer.

the gate driver output is still high. Therefore, the selected BJT should have sufficient forward gain to decrease the voltage at its collector node below the transistor's gate threshold limit.

Even though using a BJT in parallel with gate-source terminals increases the input capacitance of the transistor slightly, it is easy to tune switching timings by varying turn-on and turn-off resistances.

IV. Circuit Implementation and Experimental Results

A half-bridge prototype, which is shown in Fig. 17, was built to verify the proposed short-circuit protection scheme. The DC input voltage is 48V for the half-bridge. Simplified PCB layout of the power loop is shown in Fig. 3. The GaN HEMTs are chosen to be GS61008T, V_{DS} = 100V and R_{DS-ON} = 7 mΩ, from GaN Systems. Gate drive voltage is determined as 0V/+6V. As described previously, a single sided PCB design is applied for the power loop and the sense impedance is realized on the power loop return path, in other words, on the bottom layer, which is shown in Fig. 18. Kelvin connection is used to transfer the voltage across the sense impedance to the signal processing stage. The dimensions of the sense trace are 4.57 mm x 16.26 mm x 35 μm. Then, R_{PCB} and L_{PCB} are equal to 1.72 mΩ (for DC) and 6.7 nH (for 50 MHz) respectively. It should be noted that even though the power loop is longer than the PCB sense trace, its total inductance, which is obtained as 4.96nH, is lower because of the mutual inductances on the power loop.

In order to implement the soft turn-off mechanism, ZXTN19020 BJT from Diodes Inc. is employed in the gate driver circuit. In order to generate the control signals, TM4C1294 μC EVM from Texas Instruments is utilized. Four output signals, namely, two gate drive signals and two soft turn-off signals are generated to control the half-bridge. Also, one fault trigger input signal is used to detect faults. The clock frequency is set to be 120MHz.

The SC fault test waveforms are shown in Fig. 19 and Fig. 20. In Fig. 19, CH2 represents the voltage drop across the PCB sense trace, V_{SENSE}, and CH4 shows the fault trigger signal, V_{TRIG}, generated by the signal processing stage. The circuit detects the SC fault in 30 ns and sets the SC trigger signal to logic high level, 3.3V. The SC current slew rate can be calculated as 3.7 A/ns at the beginning of the fault where SC current rises almost linearly. The peak value of the SC current can be estimated as 70.7A from the CH2 waveform, which has almost the same trend with the simulation result shown in Fig. 9. The SC fault current was not measured directly in order to not add any probe inside the power loop.

In Fig. 20, CH2 represents the drain to source voltage of Q_2 and CH3 represents the gate to source voltage of Q_2 during the SC fault. Also, CH4 captures the fault trigger signal waveform. As shown in Fig. 20, due to the SC fault, the drain to source voltage decreases down to 16V and also there exists an overshoot in the gate to source voltage, the peak value is 7.2V. Once the μC receives the SC trigger signal, it activates the soft turn-off mechanism to protect the GaN HEMTs. The total circuit operation lasts almost 370 ns. The gate to source voltage of Q_2 decreases gradually after soft turn-off is initiated. Soft turn-off lasts almost 290 ns and the BJT used in the gate driver circuit terminates the SC current by turning off the GaN HEMTs.

The OC fault test waveforms are shown in Fig. 21. For this case, OC fault current is measured by CH1 and CH4 captures the fault trigger signal waveform. CH3 represents the output voltage of the current sense amplifier, V_{AMP}, which is used to detect the OC fault. The limit is set to be 18A for the load current. As shown in Fig. 21, the OC current slew rate is almost 3.4 A/μs. Once the current is higher than the limit

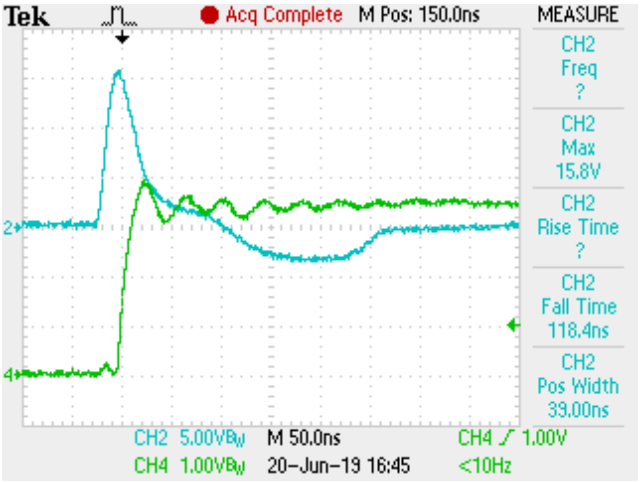


Fig. 19: SC fault protection experimental waveforms; CH2: V_{SENSE}, CH4: V_{TRIG}.

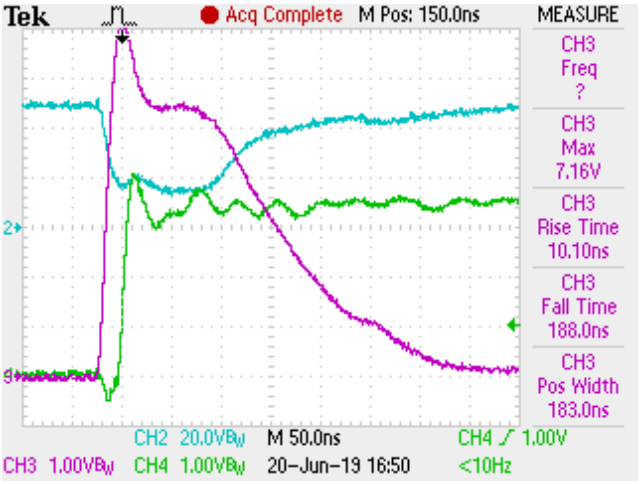


Fig. 20: SC fault protection experimental waveforms; CH2: V_{DS} of Q_2, CH3: V_{GS} of Q_2, CH4: V_{TRIG}.

value, the protection circuit terminates the current flow by turning off the GaN HEMTs with the help of the soft turn-off mechanism.

V. Conclusion

This paper presents a fast and effective short-circuit detection and protection scheme for both intense SC faults and relatively slow OC faults. Basically, the proposed circuit uses the voltage drop on the PCB layout parasitics as a sense signal to detect the faults. Therefore, it can be applied to any power converter circuit by designing PCB layout properly. The proposed scheme employs a PCB based current sense impedance, a signal processing stage, and a soft turn-off mechanism to protect GaN HEMTs from catastrophic over-current failures. Simulation and hardware implementation results are provided to verify the proposed circuit, which has fast response (SC detection within 30 ns), high current range (no limitation from PCB trace), and low power loss (no additional conduction

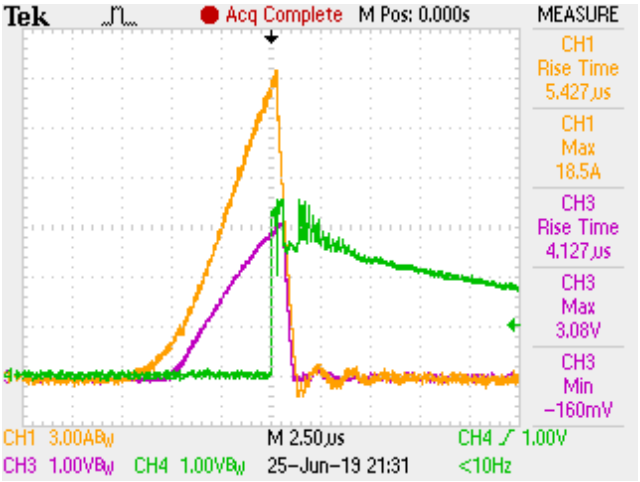


Fig. 21: OC fault protection experimental waveforms; CH1: I_{DS} of Q_2, CH3: V_{AMP}, CH4: V_{TRIG}.

loss from current sensing PCB trace which is already used for circuit connection). It is clear that the proposed circuit is able to protect the GaN HEMTs from SC and OC faults.

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