

Dear Prof. Joseph Olorunfemi Ojo,  
Tennessee Tech University, USA  
Editor-in-Chief,  
IEEE Journal of Emerging and Selected Topics in Power Electronics

14/12/2020

We would like to resubmit the enclosed manuscript entitled “*Layout Based Ultra-Fast Short-Circuit Protection Technique for Parallel Connected GaN HEMTs*,” which we wish to be considered for publication in IEEE Journal of Emerging and Selected Topics in Power Electronics. The paper is renovated and improved in the lights of previous supportive and helpful reviews. The practical perspective of the applied method is investigated and the flexibility of the proposed short-circuit protection method is highlighted. The novelty of the paper is sensing the induced voltage on the layout for detection of short-circuit fault for parallel connected GaN HEMTs, which is not studied enough for GaN HEMTs in the literature.

We would like to highlight the improvements in this paper. For this purpose, the new content is highlighted in the main text and the helpful comments of the reviewers are addressed in the following pages.

We deeply appreciate your consideration of our manuscript. If you have any queries, please don't hesitate to contact us.

Kind regards,  
Dr. Ozan Keysan

## Author's Response to Reviewer 1's Comments

**Authors:** Thank you very much for your precious time and efforts invested in improving this paper. Your insightful advice is very much appreciated. We have addressed all your concerns, which greatly improved the quality of our paper.

### Reviewer 1's comments:

#### Comment 1:

*Though the SCP using parasitic loop inductance is clearly discussed, which can be similar with previously reported SCP using inductance and  $di/dt$ , this paper does not demonstrate enough significance for the proposed method.*

#### Author's Response:

Thanks for your comment. The last paragraph of Section V is modified to highlight the significance of the proposed method.

#### Comment 2:

*SCP though the proposed is complicated, which requires a modelling of layout for every other engineer on their PCB. From the updated results, it seems the relative loop inductance to other parasitics can be varying from design to design, and this leaves the proposed method unpractical for others to apply.*

#### Author's Response:

Thanks for your comment. The practical concerns are addressed in Section V. The mutual coupling sensitivity to layout change were analyzed by FEA tools and the results are presented in Fig. 17. A test procedure which eliminates the necessity of a layout modelling is described in Section V.

#### Comment 3:

*Meanwhile, the necessity of this method on GaN sensing, especially on paralleled GaN devices, is not clear or strong enough. Thanks.*

#### Author's Response:

Thanks for your comment. The advantages of the proposed method for parallel GaN devices is additionally discussed in the last paragraph of Section V.

## **Author's Response to Reviewer 2's Comments**

**Authors:** Thank you very much for your precious time and efforts invested in improving this paper.

**Reviewer 2's comments:**

**General comments:**

*The authors have answered all my questions.*

### **Author's Response to Reviewer 3's Comments**

**Authors:** Thank you very much for your precious time and efforts invested in improving this paper.

**Reviewer 3's comments:**

**General comments:**

*All the concerns have been well addressed.*

## Author's Response to Reviewer 4's Comments

**Authors:** Thank you very much for your precious time and efforts invested in improving this paper. Your insightful advice is very much appreciated. We have addressed all your concerns, which greatly improved the quality of our paper.

### Reviewer 4's comments:

#### General comments:

*Thanks for the effort from authors. The paper is much improved. However, I still have several questions:*

#### Author's Response:

Thanks for your comments. The paper was revised according to your suggestions as follows:

#### Comment 1:

*1. For de-sat type protection, I don't believe it obtain "the response speed is twice of the layout based protection technique", and de-sat method can be applied to each individual paralleled GaN HEMT, which means it is more safe than just control the overall two paralleled GaN devices.*

#### Author's Response:

Thanks for your comments. The **sixth paragraph of Section VI** was revisited to give a better explanation for comparison of de-sat and layout methods. Usage of the de-sat method for each individual paralleled GaN HEMT is discussed in **the sixth paragraph of Section VI** as well.

#### Comment 2:

*2. The layout parasitics can have boards-to-boards or design-to-design variations. Does it mean each time engineers do the layout and they need to extract the board parasitics and then tune the detection circuit to proper triggering value?*

#### Author's Response:

Thanks for your comments. The board-to-board or design-to-design variation range of the mutual coupling was investigated by FEA tools. The results are presented in **Fig. 17** and discussed in **Section V**. An experimental procedure for tuning the threshold level of the short-circuit protection circuit without extracting the layout parasitics is explained in **Section V** as well.