Effects of Parasitics

Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} L_{D1-4}	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{s1}-L_{s4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
L_{QS1-6}	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	