PCB Layout Based Short-Circuit Fault Detection Circuit for GaN HEMTs

Abstract: Gallium Nitride Enhancement-Mode High Electron Mobility Transistors (GaN E-HEMTs) are superior to other power transistors in terms of efficiency, package size and switching speed which leads to increased power density; however, their reliability is a concern for the end-user products. Due to high switching speed capability, high amount of short-circuit (SC) current can flow in the order of nanoseconds after a fault occurs. In this paper, a SC fault detection method based on PCB layout is proposed to eliminate the risk of over-current breakdown. The experiment results show that SC current can be detected by the proposed method which can be used to protect the GaN E-HEMTs from SC faults.

1 Introduction

The wide band-gap devices are strong candidates to meet the power density and efficiency requirements of today's commercial products [1]. Especially, the Gallium-Nitride (GaN) based power semiconductor devices are superior to Silicon (Si) and Silicon-Carbide (SiC), in terms of lower on-state resistance and higher switching speed [2]. However, due to increased switching speed, the system will be more susceptible to noises and false turn-on faults [3]. With a typical maintenance time of 200ns, [4], a SC detection circuit is required to act quickly in a reliable manner.

The most common method is the desaturation technique, where the voltage across the drain-source terminals are sensed [5]. However, this technique increases output capacitance which leads to higher switching losses and relatively long settling time [6–8]. Another technique is sensing the voltage across a portion of loop inductance on the layout [9] which has low performance under low dI/dt conditions such as Fault Under Load (FUL) type of short circuits. Current shunts which are cascaded on GaN HEMTs [8] are not applicable because adding component on the power loop increases the layout inductance. In [6], a protection method is proposed that uses steady-state nonzero gate current of GaN gate injection transistors (GITs), but it is not applicable for HEMTs due their voltage-driven gate structure as stated in [7]. Lastly, a two-stage protection circuitry, where a soft-turn off and hard turn-off are both available, is proposed in [7]. Similar to desaturation technique, the increased output capacitance and complicated reference voltage selection due to the temperature-dependent saturation current [6] are the weakest points of this technique.

In this paper, a novel SC protection scheme by utilizing Printed Circuit Board (PCB) path as

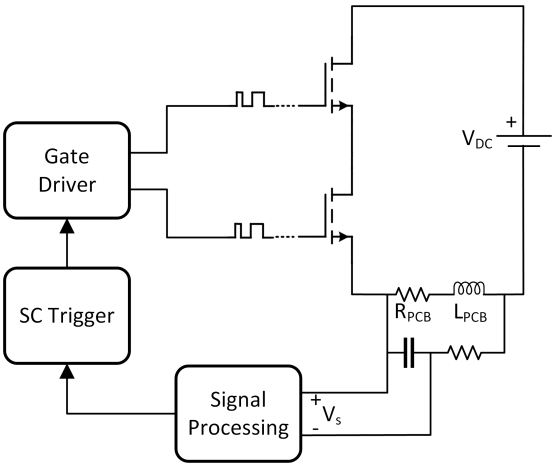

Fig. 1: Main Block Diagram

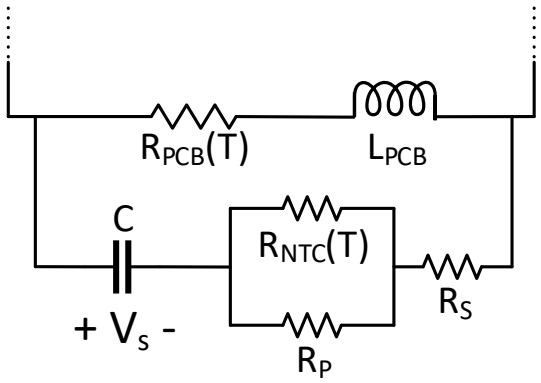

Fig. 2: R-C Network Circuit

a current sense resistor is proposed. The sensed signal is processed by an analog circuit to generate the SC trigger signal which turns off the device by triggering the digital controller IC.

2 Operating Principle of Proposed SC Detection Circuit

The proposed circuit is shown in Fig.1. The SC trigger signal is generated based on the sensed current I_{SC} flowing through the current sense resistor, R_{PCB}. The building blocks of the circuit are PCB current sense resistor, external filtering R-C network, the signal processing stage and the digital controller. I_{SC} is sensed by using the R_{PCB} which is the self resistance of the PCB track. At low operating frequencies, the PCB track can be modelled as a purely resistive element. However, during the SC fault, the current rises too rapidly; that is, the equivalent frequency is very high. Therefore, the self-inductance, L_{PCB}, which can be modelled as in series with the resistance of the copper trace, becomes the dominant part. Therefore, the sensed voltage across the PCB resistor deviates greatly from the original current waveform. In order to measure the current properly, the voltage drop across L_{PCB} has to be compensated. For this purpose, a simple low pass R-C network is used. The voltage drop across the R_{PCB} is filtered and the purely resistive voltage drop is used as the input signal for the signal processing stage.

As a summary, the proposed circuit protects the switching devices from overcurrent faults. Some part of the PCB track which is already used in circuit connection is utilized for the sense operation. Therefore, power loop inductance and resistance are not increased, so there is no additional switching or conduction losses.

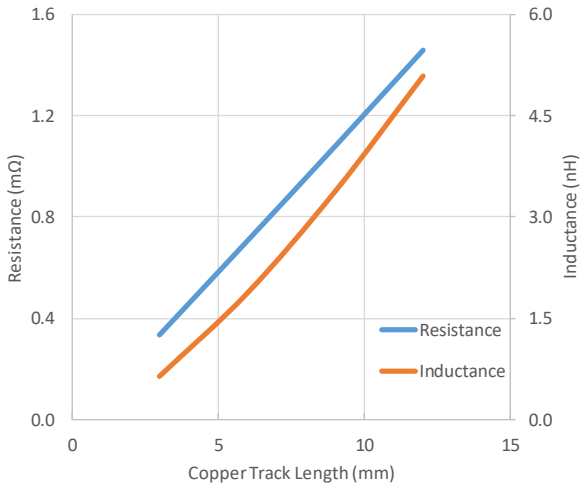

Fig. 3: PCB parasitics vs track length graph

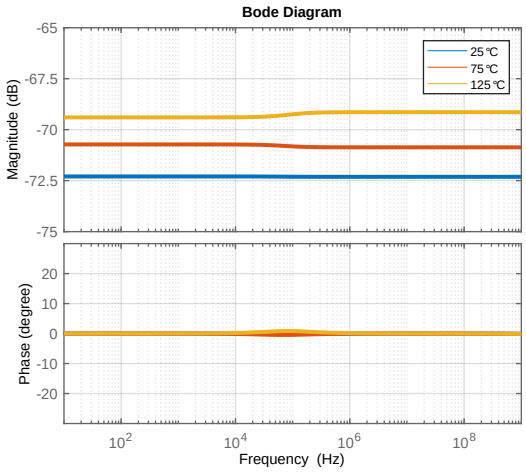

Fig. 4: Bode Plot of SC Current to Sense Voltage Transfer Function for Different Operating Temperatures

3 Design Considerations and Circuit Implementation

3.1 PCB Based Current Sense Resistor

As mentioned before, some part of the existing PCB track is used as a current sense resistor in the driving circuit to eliminate extra conduction loss due to additional components. The equivalent impedance of the sense resistor can be represented in the form of (1). It is clear that ωL_{PCB} parameter becomes more dominant as frequency of the current increases which is the case for a SC fault. FastHenry2 simulation tool is used to analyze how R_{PCB} and L_{PCB} parameters change with different width (w), length (l), and thickness (t). For a 35 μm thickness and 5 mm width PCB layer the results are presented for different track lengths in Fig. 3.

$$Z_{PCB} = R_{PCB} + j\omega L_{PCB} \tag{1}$$

3.2 R-C Network

The most critical design consideration for the low pass R-C network is the operating temperature of the sense resistor, which directly impacts the R_{PCB} resistance. The normalized R_{PCB} varies from 0.9 to 1.5 when the operating temperature varies from -40°C to 100°C, which means electrical time constant of PCB track (L_{PCB}/R_{PCB}) decreases as the temperature increases. In order to keep the time constant of R-C network ($C * R_{eq}$) equal to the PCB track time constant, temperature

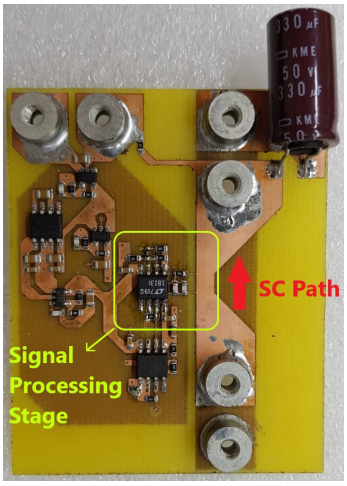

Fig. 5: Physical Implementation of SC Protection Method

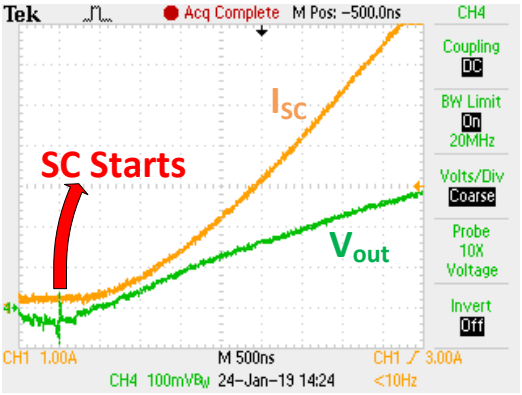

Fig. 6: Experimental result showing short circuit current and output voltage of signal processing block

compensation has to be realized in the low pass R-C network to maintain proper operation over the full temperature range.

$$R_{eq} = \frac{R_{NTC}R_s + R_{NTC}R_p + R_sR_p}{R_{NTC} + R_p} \tag{2}$$

$$\frac{d}{dT}R_{PCB} = -\frac{d}{dT}R_{eq} \tag{3}$$

It is difficult to design a compensation network that exactly satisfies (3) due to tolerances of components. However, the mismatch can be minimized by using Negative Temperature Coefficient (NTC) thermistor to achieve the best possible temperature change as shown in Fig. 2. As shown in the bode plot, Fig. 4, the gain (G) is constant over a wide range of frequency which is an advantage. Furthermore, the gain changes in small amplitude with temperature.

In order to verify the proposed method, a SC current measurement prototype without GaNFETs is implemented as shown in Fig. 5. This prototype includes PCB sense resistor, R-C compensation network and the signal processing stage. The dimensions of the sense resistor are 3 mm x 3 mm x 35 μm. Then, R_{PCB} is equal to 1.7 mΩ and L_{PCB} is equal to 840 pH. In R-C network, R_{eq} and C are selected as 2.21 kΩ and 200 pF. The short-circuit test result for the prototype is shown in Fig. 6. It is observed that the output voltage of signal processing block, V_{out}, can be used to measure the SC current flowing through the PCB sense resistor. For this experiment, the slew rate of SC current is 2.5 A/μs. It is clear that in order to measure higher slew rate SC current, high

bandwidth op-amp is required for signal processing. In the final prototype, V_{out} will be compared with a reference level to generate SC trigger signal.

4 Conclusion

In this study, a novel SC protection method is proposed and first version of prototype is demonstrated. It is shown that PCB track can be used to measure the SC current flowing through the circuit. In order to utilize the PCB track for sense operation, a R-C network is required, where the temperature compensation is achieved. To amplify the sensed voltage across the R-C network, a high bandwidth amplifier circuit is required.

In the final paper, the proposed method will be implemented with all blocks including a GaN-FET half-bridge. It will be shown that the proposed method is able to protect the GaNFETs from high slew rate SC current.

References

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