GaN Enhancement-mode Gate Drivers HEMT Half Bridge $\sum_{P_1}^{L_{P_1}}$ L_{DR5} L_{D3} L_{D4} $L_{G3}R_{G3}$ $L_{G4}R_{G4}$ L_{DR6} Q3 $L_{ m DR7}$ L_{DR8} L_{S3} R_{S3} L_{S4} R_{S4} L_{QS4} L_{QS3} $\stackrel{L_{DR1}}{\sim}$ $\langle L_{D2} \rangle$ L_{D1} $+ C_{DG}$ $L_{G1}R_{G1}$ $L_{G2}R_{G2}$ L_{DR2} Q1 M1 M2 L_{S2} R_{S2} L_{DR3} L_{S1} R_{S1} L_{DR4} L_{QS2} L_{QS1} \mathbf{L}_{P2}

Effects of Parasitics

[Parameter	Description	Effect	Priority	Design Rules
ос	LP1,LP2 LD1-4	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
	LDR1-LDR8		Increase Vgs ringing and overshoot	Medium	Smaller the better
	LG1-LG4 Ls1-Ls4	Gate drive loop inductance	Increase Vgs ringing and overshoot, Susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
	M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
	LQS1-6	Quasi-common source inductance	Feedback the difference of di/dt to Vgs, Balance current sharing Potentially cause gate oscillation	Extremely High	