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Space vector based modulation scheme for reducing capacitor RMS current in three-level diode-clamped inverter

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ABSTRACT

The DC capacitor is an important component in a voltage source inverter. The RMS current flowing through the capacitor determines the capacitor size and losses. The losses, in turn, influence the capacitor life. This paper proposes a space vector based modulation strategy for reducing the capacitor RMS current in a three-level diode-clamped inverter. An analytical closed-form expression is derived for the DC capacitor RMS current with the proposed PWM strategy. The analytical expression is validated through simulations and also experimentally. Theoretical and experimental results are presented, comparing the proposed strategy with conventional space vector PWM (CSVPWM). It is shown that the proposed strategy reduces the capacitor RMS current significantly at high modulation indices and high power factors.

1. Introduction

Three-level neutral-point clamped (NPC) inverters [1] are being increasingly used these days [2]. Among the various power converter topologies for high power application, NPC inverter is the most widely used in the medium voltage range [3]. Design guidelines for the construction and control of NPC inverters have been presented in [2]. The usefulness of NPC topology to low-voltage applications has been studied rigorously [4]. The NPC inverters have been found to be beneficial, compared to two-level inverters, in grid-connected converter, conventional motor drives and permanent magnet motor drives, operating at high switching frequencies [4]. These have also been used successfully in renewable energy applications [5]. These are also useful in reactive power compensation and active-power filtering in single phase [6] and three-phase applications [7].

Pulse width modulation is used for controlling the devices in an NPC inverter [8]. Mainly, there are three types of pulse width modulation strategies – carrier based PWM, space vector based PWM (SVPWM) and selective harmonic elimination based PWM (SHEPWM) [3]. A hybrid PWM method using SVPWM and SHEPWM has been used to reduce the harmonic content in load current [9]. SHEPWM is essentially an off-line or a stored waveform PWM method, which leads to huge transients under dynamic conditions. Hence, only carrier-based and space vector based PWM schemes are mainly used for real-time generation of PWM waveform. Also, any carrier based strategy can be viewed as an equivalent SVPWM based strategy [10]. Many carrier-based and space-vector based pulse width modulation (PWM) methods for the NPC inverter employ the three nearest voltage vectors (TNV) to synthesize the reference vector [11]. An algorithm to determine the location of the voltage reference vector is discussed in [12]. A computationally fast method to synthesize the reference vector using the three nearest vectors is presented in [13]. A fractal approach to generate TNV based PWM is presented in [14]. TNV based continuous and discontinuous modulation schemes have been presented in [15]. The three nearest vector (TNV) PWM methods have the advantage of low harmonic distortion in the line current, compared to non-TNV methods [16,11]. The most popular TNV based PWM method is the conventional space vector pulse width modulation (CSVPWM) scheme. Switching strategies which apply the three nearest vectors in different sequences, instead of the traditional CSVPWM sequence, have been proposed in [16]. These novel sequences lead to lower THD in the load current than CSVPWM at high modulation indices [16].

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CSVPWM in a three-level NPC inverter causes neutral-point voltage imbalance in the DC-link capacitor at high modulation indices [17]. A modified TNV based method to reduce the neutral-point unbalance problem has been proposed in [18]. A combination of TNV and three nearest virtual vectors has been used to address the neutral-point unbalance problem [19]. More work has been reported on the use of non-TNV PWM methods (which do not use the three nearest vectors) for DC capacitor voltage balancing [20]. A hybrid combination of TNV and non-TNV methods has been used for reducing the DC-capacitor voltage balancing in [17,21]. A carrier based non-TNV strategy for reducing the neutral-point imbalance has been presented in [22]. Non-TNV methods have also been used for common-mode voltage reduction [23]. Thus, while the TNV methods result in good waveform quality in the AC side, the non-TNV methods appear to lead to performance improvement in the DC-side. This paper explores the possibility of developing a non-TNV PWM scheme to reduce the current stress on the DC capacitor in an NPC inverter.

The capacitor RMS current determines the size, and thereby, the cost of the capacitor [24]. Further, the RMS capacitor current is directly related to the power loss in a capacitor [25]. The heating causes acceleration of chemical changes in the oxide layer and electrolyte, and also electrolyte vapour leakage through the capacitor end seal [24,26]. This increases the equivalent series resistance (ESR) of the capacitor over its operating life. When the ESR exceeds the maximum recommended value, the capacitor needs to be replaced [26,27]. Thus, the capacitor RMS current also plays a significant role in the lifetime of the DC capacitor. This paper proposes a space vector based non-TNV PWM scheme for reducing capacitor RMS current in a three-level inverter.

Harmonic analysis of the DC capacitor current in a two-level inverter using the convolution of load current and switching function of the switch in frequency domain has been presented in [28]. In [29], double Fourier series has been used for the harmonic analysis of capacitor current in a two-level inverter. Evaluation of capacitor RMS current [25,30] and theoretical evaluation of capacitor loss [31] have also been reported for a two-level inverter. The effect of modulation signal on the capacitor RMS current and capacitor voltage ripple in a two-level inverter has also been studied [32]. Harmonic analysis of capacitor current in a three-level inverter using the convolution method has been proposed in [28]. Analytical estimation of the capacitor RMS current in a sinusoidally modulated three-level inverter has been reported in [33,34]. In this paper, an analytical closed-form expression is derived for the RMS value of the DC capacitor current in an NPC inverter, modulated with the proposed PWM scheme. The capacitor RMS current is expressed as a function of modulation index V_{ref} and power factor angle ϕ. The analytical expression is validated experimentally on a 3-kVA three-level inverter. Theoretical, simulation and experimental results are presented, to compare the RMS values of the capacitor current with CSVPWM and the proposed PWM at different operating conditions. The analytical, simulated and experimental results show significant reduction in capacitor RMS current with the proposed PWM scheme over CSVPWM scheme at high power factors and high modulation indices.

2. Proposed PWM scheme

A three-level diode-clamped inverter is shown in Fig. 1. The inverter states and voltage vectors of the three-level inverter are shown in Fig. 2. The vectors $\mathbf{V}_1$,$\mathbf{V}_2$,$\mathbf{V}_3$,$\mathbf{V}_4$,$\mathbf{V}_5$ and $\mathbf{V}_6$ are called long vectors; $\mathbf{V}_7$, $\mathbf{V}_8$, $\mathbf{V}_9$, $\mathbf{V}_{10}$, $\mathbf{V}_{11}$ and $\mathbf{V}_{12}$ are short vectors; $\mathbf{V}_{13}$, $\mathbf{V}_{14}$, $\mathbf{V}_{15}$, $\mathbf{V}_{16}$, $\mathbf{V}_{17}$ and $\mathbf{V}_{18}$ are medium vectors; $\mathbf{V}_0$ is the zero vector. All vectors are normalized with respect to V_{dc}. A sector is defined here as the spatial region between two medium vectors.

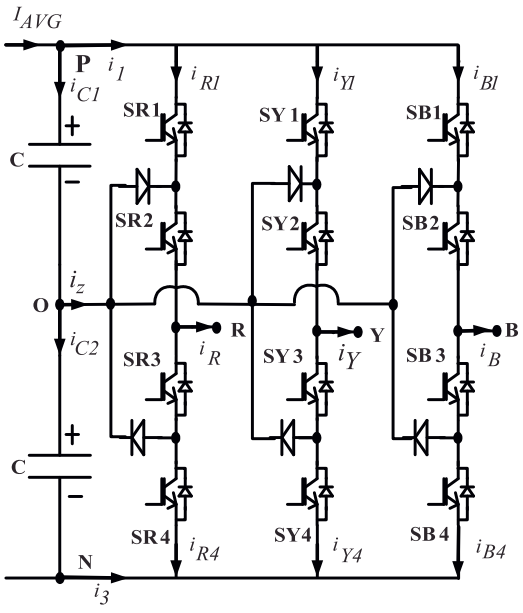

Fig. 1. Three-level three-phase diode-clamped inverter.

Many PWM schemes generate the reference vector by the time-averaging of the three nearest vectors (TNV) as discussed in Section 1 [11–16]. The three nearest vectors would be $\mathbf{V}_7$, $\mathbf{V}_1$ and $\mathbf{V}_{13}$ for both the reference vectors $\mathbf{V}_{ref1}$ and $\mathbf{V}_{ref2}$ shown in Fig. 3.

However, the proposed PWM scheme employs two adjacent medium vectors (say $\mathbf{V}_{13}$ and $\mathbf{V}_{18}$) and the null vector $\mathbf{V}_0$, if the tip of the reference vector falls within the triangle formed by the two medium vectors and the line joining their tips (e.g. $\mathbf{V}_{ref1}$ in Fig. 3) [23]. This is termed as "sequence-1". The dwell times of $\mathbf{V}_0$, $\mathbf{V}_{13}$ and $\mathbf{V}_{18}$ are calculated as shown in (1), where T_s is the subcycle duration. The expressions for dwell times of the three voltage vectors used in "sequence 1" are given in Table 1, considering sectors I and II (see Fig. 2). Here, the angle α of

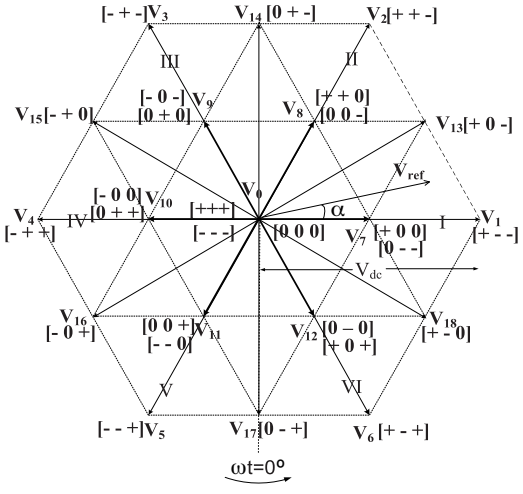

Fig. 2. Voltage vectors of a three-level inverer. I, II, III, IV, V and VI are sectors.

Table 1
Dwell times of voltage vectors in sectors I and II for sequence 1.

Sector	State	Vector	Dwell time expression	Dwell time
I	000	$\mathbf{V}_0$	$\left(1-\frac{4}{3}V_{ref}\cos(\alpha)\right)\times T_s$	T_0
I	+0−	$\mathbf{V}_{13}$	$\left(\left(\frac{2}{3}V_{ref}\cos(\alpha)\right)+\left(\frac{2}{\sqrt{3}}V_{ref}\sin(\alpha)\right)\right)\times T_s$	T_{13}
I	+−0	$\mathbf{V}_{18}$	$\left(\left(\frac{2}{3}V_{ref}\cos(\alpha)\right)-\left(\frac{2}{\sqrt{3}}V_{ref}\sin(\alpha)\right)\right)\times T_s$	T_{18}
II	000	$\mathbf{V}_0$	$\left(1-\left(\frac{2}{3}V_{ref}\cos(\alpha)\right)-\left(\frac{2}{\sqrt{3}}V_{ref}\sin(\alpha)\right)\right)\times T_s$	T_0
II	0+ −	$\mathbf{V}_{14}$	$\frac{4}{3}V_{ref}\cos(\alpha)\times T_s$	T_{14}
II	+0−	$\mathbf{V}_{13}$	$\left(\left(\frac{2}{\sqrt{3}}V_{ref}\sin(\alpha)\right)-\left(\frac{2}{3}V_{ref}\cos(\alpha)\right)\right)\times T_s$	T_{13}

the reference vector is measured from the long voltage vector $\mathbf{V}_1$.

$$
\begin{aligned}
&V_{ref1}T_s = V_0T_0 + V_{13}T_{13} + V_{18}T_{18}\\
&T_0 = \left[1-\frac{4}{3}V_{ref1}\cos(\alpha)\right]\times T_s\\
&T_{13} = \left[\frac{2}{3}V_{ref1}\cos(\alpha)+\frac{2}{\sqrt{3}}V_{ref1}\sin(\alpha)\right]\times T_s\\
&T_{18} = \left[\frac{2}{3}V_{ref1}\cos(\alpha)-\frac{2}{\sqrt{3}}V_{ref1}\sin(\alpha)\right]\times T_s
\end{aligned}
\tag{1}
$$

If the tip of the reference vector falls within the triangle formed by the tips of the two medium vectors (say $\mathbf{V}_{13}$ and $\mathbf{V}_{18}$) and a long vector (say $\mathbf{V}_1$) as in case of $\mathbf{V}_{ref2}$ in Fig. 3, the vectors $\mathbf{V}_1$, $\mathbf{V}_{13}$ and $\mathbf{V}_{18}$ are applied for dwell times T_1, T_{13} and T_{18}, respectively. These dwell times can be computed as shown in (2). Such a sequence is termed as "sequence 2". Expressions for the dwell times of the vectors used in the "sequence 2" in sectors I and II are given in Table 2. Here again, the angle α is measured with respect to the long voltage vector V_1.

$$
\begin{aligned}
&V_{ref2}T_s = V_1T_1 + V_{13}T_{13} + V_{18}T_{18}\\
&T_1 = [-3+4V_{ref2}\cos(\alpha)]\times T_s\\
&T_{13} = \left[2-2V_{ref2}\cos(\alpha)+\frac{2}{\sqrt{3}}V_{ref2}\sin(\alpha)\right]\times T_s\\
&T_{18} = \left[2-2V_{ref2}\cos(\alpha)-\frac{2}{\sqrt{3}}V_{ref2}\sin(\alpha)\right]\times T_s
\end{aligned}
\tag{2}
$$

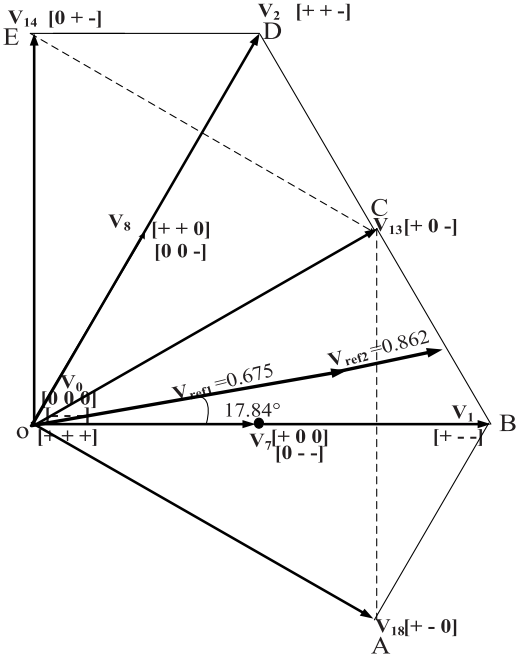

Fig. 3. Illustration of the reference vectors in sector I on the space vector plane.

The influence of the switching sequences on the capacitor current is discussed in Sections 3 and 4. Simulation and experimental results are also presented, comparing the proposed PWM and CSVPWM schemes.

3. Instantaneous capacitor current

In this section, the instantaneous DC-link capacitor current in an NPC inverter is analyzed and is expressed in terms of load current and switching functions of the top devices in the inverter legs. The instantaneous capacitor currents, pertaining to CSVPWM and the proposed PWM, are compared at different operating conditions through simulations and experiments.

3.1. Analysis

The instantaneous dc link currents i_1 and i_3 in Fig. 1 are given by the following equations:

$$
\begin{aligned}
i_1 &= S_{R1}i_R + S_{Y1}i_Y + S_{B1}i_B\\
i_3 &= S_{R4}i_R + S_{Y4}i_Y + S_{B4}i_B
\end{aligned}
\tag{3}
$$

where S_{R1}, S_{Y1} and S_{B1} are the switching functions of the top devices in the R, Y and B phases, respectively. If $S_{R1}=1$, for example, then the R-phase top device (S_{R1}) is 'ON'; this also means that the R-phase pole voltage v_{R0} equals $V_{DC}/2$. If the switching function $S_{R1}=0$, then the top device is 'OFF'; the pole voltage v_{R0} is either 0 or $-(V_{DC}/2)$. Similarly, S_{R4}, S_{Y4} and S_{B4} are the switching functions of the bottom devices in the R, Y and B phase legs, respectively. Ignoring the harmonic components, the three-phase load currents i_R, i_Y and i_B can be expressed as:

$$
\begin{aligned}
i_R &= I_N\sin(\theta-\phi)\\
i_Y &= I_N\sin\left(\theta-\frac{2\pi}{3}-\phi\right)\\
i_B &= I_N\sin\left(\theta+\frac{2\pi}{3}-\phi\right)
\end{aligned}
\tag{4}
$$

where I_N is the peak value of fundamental current, θ is the fundamental angle, and ϕ is the fundamental power factor angle.

When the inverter state +0−, +− − or +0− is applied, the DC link current i_1 equals i_R. When the null state 000 is applied, i_1 is zero. Considering $\mathbf{V}_{ref1}$, the dc link current over a sub-cycle for the sequences (+00, +0−, +− −, 0− −) and (+−0, +0−, 000) are as shown in Fig. 4(a) and (b), respectively. Similarly, for $\mathbf{V}_{ref2}$, the DC-link current is illustrated in Fig. 5(a) and (b) for the two PWM methods. The current through the top DC-link capacitor is the difference between the instantaneous DC-link current (i_1) and the average DC-link current I_{AVG} as shown by (5).

$$
i_{C1} = i_1 - I_{AVG} \tag{5}
$$

Table 2
Dwell times of voltage vectors in sectors I and II for sequence 2.

Sector	State	Vector	Dwell time expression	Dwell time
I	+– –	$\mathbf{V}_1$	$(-3+(4V_{ref}\cos(\alpha)))\times T_s$	T_1
I	+0–	$\mathbf{V}_{13}$	$\left(2-(2V_{ref}\cos(\alpha))+\left(\frac{2}{\sqrt{3}}V_{ref}\sin(\alpha)\right)\right)\times T_s$	T_{13}
I	+– 0	$\mathbf{V}_{18}$	$\left(2-(2V_{ref}\cos(\alpha))-\left(\frac{2}{\sqrt{3}}V_{ref}\sin(\alpha)\right)\right)\times T_s$	T_{18}
II	++ –	$\mathbf{V}_2$	$((2V_{ref}\cos(\alpha))-3+(2\sqrt{3}V_{ref}\sin(\alpha)))\times T_s$	T_2
II	0+ –	$\mathbf{V}_{14}$	$(2-(1.154V_{ref}\sin(\alpha))-(2V_{ref}\cos(\alpha)))\times T_s$	T_{14}
II	+0–	$\mathbf{V}_{13}$	$\left(2-\left(\frac{4}{\sqrt{3}}V_{ref}\sin(\alpha)\right)\right)\times T_s$	T_{13}

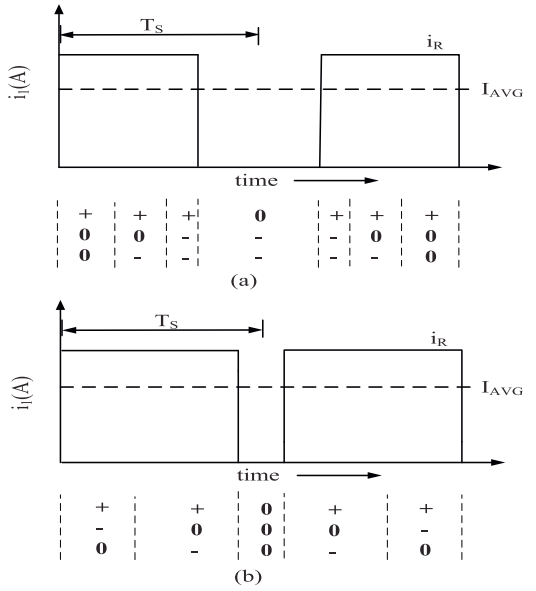

Fig. 4. Instantaneous DC link current in a switching cycle for V_{ref}0.675 for (a) CSVPWM scheme and (b) new modulation scheme (sequence-1), considering unity power factor.

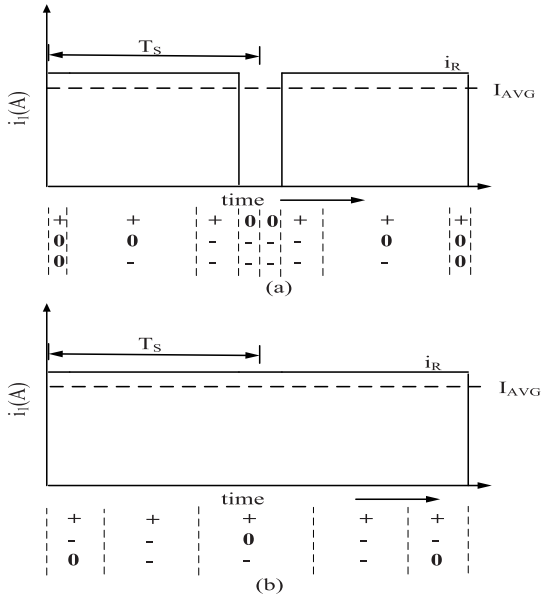

Fig. 5. Instantaneous DC link current in a switching cycle for V_{ref} = 0.866 for (a) CSVPWM scheme and (b) new modulation scheme (sequence-2), considering unity power factor.

where I_{AVG} can be obtained from the input–output power balance of the inverter as follows:

$$I_{AVG} = V_{ref} I_N \cos(\phi) \tag{6}$$

The instantaneous DC-link current i_1 and the average DC-link current I_{AVG} are shown in solid and dashed lines, respectively, in Figs. 4 and 5. The peak value of capacitor current is $-I_{AVG}$ in case of CSVPWM, but is much lower in case of the proposed PWM as seen from Fig. 5. When V_{ref} < 0.75, though the peak capacitor current is $-I_{AVG}$ for both the schemes, the duration for which the peak current flows is lower for the proposed PWM scheme than CSVPWM scheme as can be seen from Fig. 4.

3.2. Simulation results

The new modulation technique as well as CSVPWM technique are first compared through simulation studies using MATLAB SIMULINK. The load is modeled as a three-phase current sink. The sampling frequency is 3.2 kHz. The gating pulses to the *R*-phase top switch, the *R*-phase load current and the capacitor current are shown for CSVPWM and the new modulation schemes at V_{ref} = 0.825, I_N = 5A and ϕ = 45° (lag) in Fig. 6(a) and (b), respectively. As seen, there is a reduction in the number of switching-frequency pulses in Fig. 6(b) compared to (a). But there is a marginal increase in the capacitor RMS current in Fig. 6(b). Similar waveforms for ϕ = 10° (lag) are presented in Fig. 6(c) and (d). In this case, the number of ripple frequency pulses is reduced and the capacitor RMS current is also reduced with the proposed PWM.

Simulated waveforms at the same power factor angles of 45° (lag) and 10° (lag) as in Fig. 6, but at a different modulation index of V_{ref} = 0.675, are presented in Fig. 7. At this modulation index also, there is a reduction in capacitor current for ϕ = 10° (lag) with the proposed PWM. Hence, it can be said that the proposed modulation scheme reduces the capacitor RMS current at high power factors. Further study on capacitor RMS is presented in Section 4.

Simulations are carried out to study the instantaneous capacitor current during transient conditions as well. When the load is suddenly changed from 15 A peak to 5 A peak, the instantaneous capacitor current for CSVPWM and the proposed PWM are as given in Fig. 8(a) and (b), respectively. From the figure it can be seen that the transient response in the capacitor current is pretty much smooth for both the schemes. It takes one line cycle roughly for the capacitor current to settle down to the new operating condition.

Apart from linear loads, a three-phase non-linear load which draws three-phase quasi-square wave currents from the inverter is also considered. Fig. 9(a) and (b) shows the instantaneous capacitor current for the non-linear load with CSVPWM and the new modulation scheme, respectively. The power factor of the fundamental component of the quasi-square wave is unity, and the modulation index is V_{ref} = 0.825. As seen, the capacitor current pulses are of the same amplitude, but there is a reduction in the number of switching-frequency pulses in the capacitor current with the new modulation scheme, compared to the CSVPWM scheme. However,

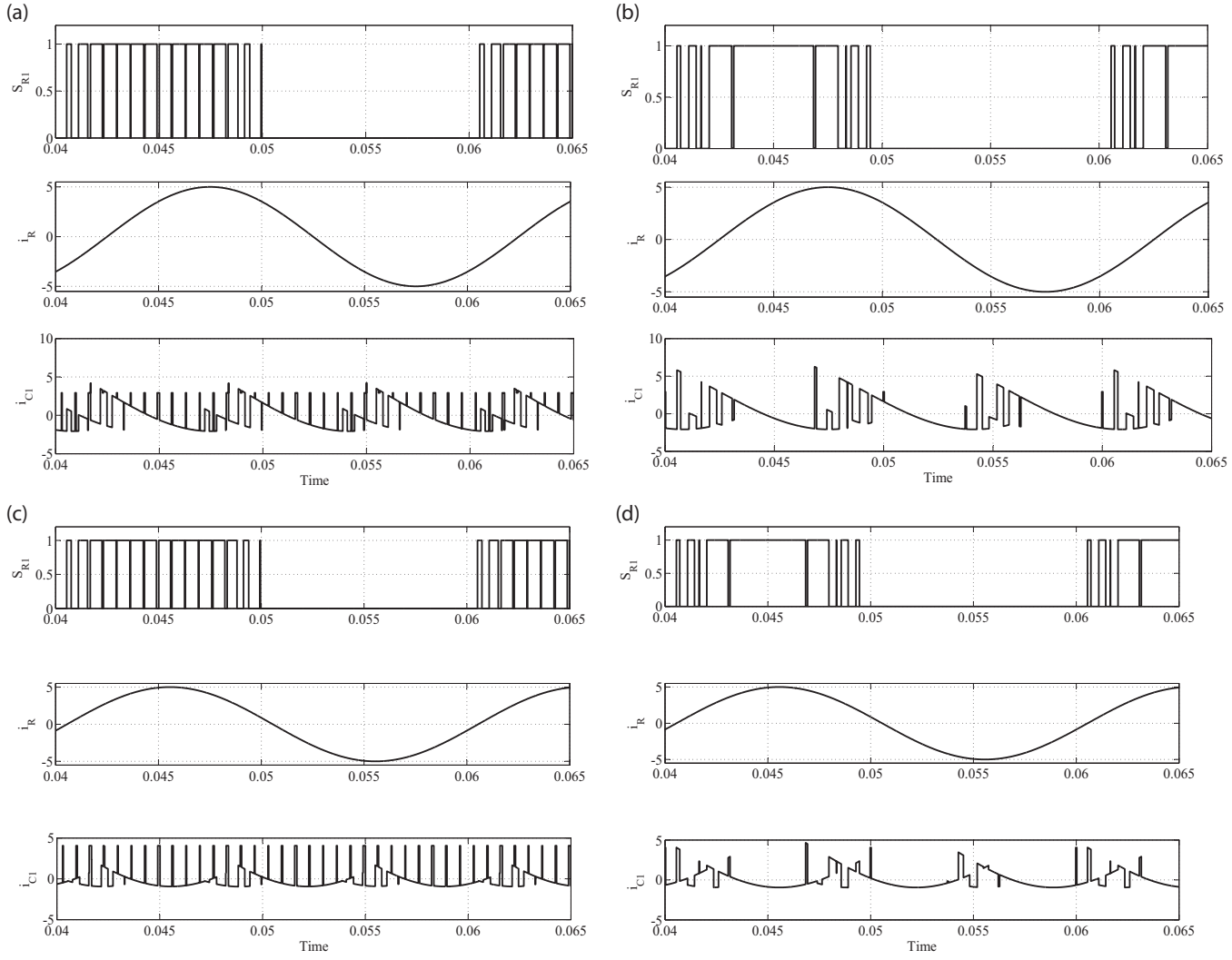

Fig. 6. Simulated waveforms of pulses for top switch, load current and capacitor current for (a) CSVPWM scheme V_{ref} = 0.825 and ϕ = 45° (lag). (b) New PWM scheme V_{ref} = 0.825 and ϕ = 45° (lag). (c) CSVPWM scheme V_{ref} = 0.825 and ϕ = 10° (lag). (d) New PWM scheme V_{ref} = 0.825 and ϕ = 10° (lag). The respective RMS values of the capacitor current are (a) 1.69 A, (b) 1.98 A, (c) 1.41 A, (d) 1.18 A.

the RMS value of the capacitor current are found to be comparable for the two methods.

Also, a similar simulation study is carried out for another nonlinear load, consisting of a three-phase diode bridge rectifier with an output filter capacitor of 1000 μF and a load resistance of 20 Ω. The modulation index V_{ref} = 0.825. The results of the simulation study are presented in Fig. 10. As seen, the fundamental power factor of the load current is unity. The number of switching frequency pulses in the capacitor current waveform is reduced as earlier. Once again, the capacitor RMS current is almost the same for both the PWM schemes.

3.3. Experimental results

The experimental setup is a 3 kVA MOSFET-based three-level inverter, controlled using a dSPIC30F4011 based digital controller [35]. The MOSFETs used are irfp460 and the clamping diode are mur860. The DC-capacitor consists of two sets of three 470 μF, 450 V capacitors connected in parallel. These two sets of parallel-connected capacitors are connected in series. The point of series connection forms the DC neutral point. The load consists of a constant inductance of 24.5 mH and a 100 Ω variable rheostat per phase. By varying the resistance, the power factor angle is varied. The DC source is Agilent 6035 A (0–500 V, 0–5 A, 1000 W) programmable power supply. The load current is maintained constant at 5A, irrespective of modulation index and power factor angle, by varying the DC bus voltage. The sampling frequency is 3.2 kHz as in case of simulation studies. The capacitor current is measured using a Fluke-1400S probe.

Experimental results, corresponding to the simulation results in Figs. 6 and 7, are presented in Figs. 11 and 12, respectively. The simulation and experimental results closely tally with each other. The RMS value of the capacitor current with the new modulation scheme is higher than that with the CSVPWM scheme at a power factor angle of 45° (lag), as is seen from Figs. 11(a,b) and 12(a,b). On the other hand, at a power factor angle of 10° (lag), the capacitor RMS current is reduced with the proposed PWM, as shown by Figs. 11(c,d) and 12(c,d). Thus, the experimental results confirm the reduction in capacitor RMS current at high power factors with the proposed method.

4. RMS capacitor current

Based on the expressions for the instantaneous capacitor current in the previous section, an analytical expression is derived for the capacitor RMS current, pertaining to the proposed PWM

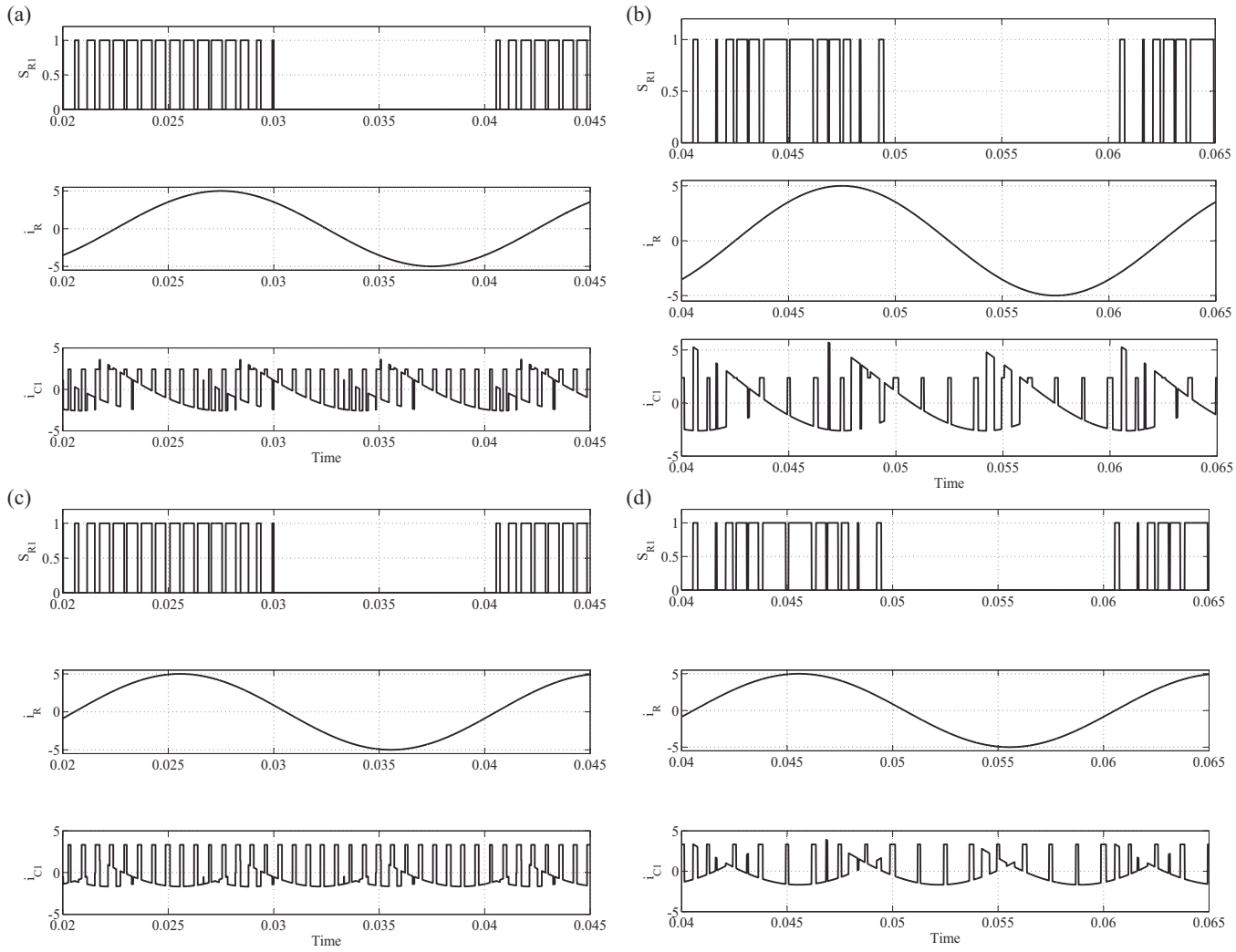

Fig. 7. Simulated waveforms of pulses for top switch, load current and capacitor current for (a) CSVPWM scheme $V_{ref} = 0.675$ and $\phi = 45^\circ$ (lag). (b) New PWM scheme $V_{ref} = 0.675$ and $\phi = 45^\circ$ (lag). (c) CSVPWM scheme $V_{ref} = 0.675$ and $\phi = 10^\circ$ (lag). (d) New PWM scheme $V_{ref} = 0.675$ and $\phi = 10^\circ$ (lag). The respective RMS values of the capacitor current are (a) 1.89 A, (b) 2.24 A, (c) 2.02 A, (d) 1.92 A.

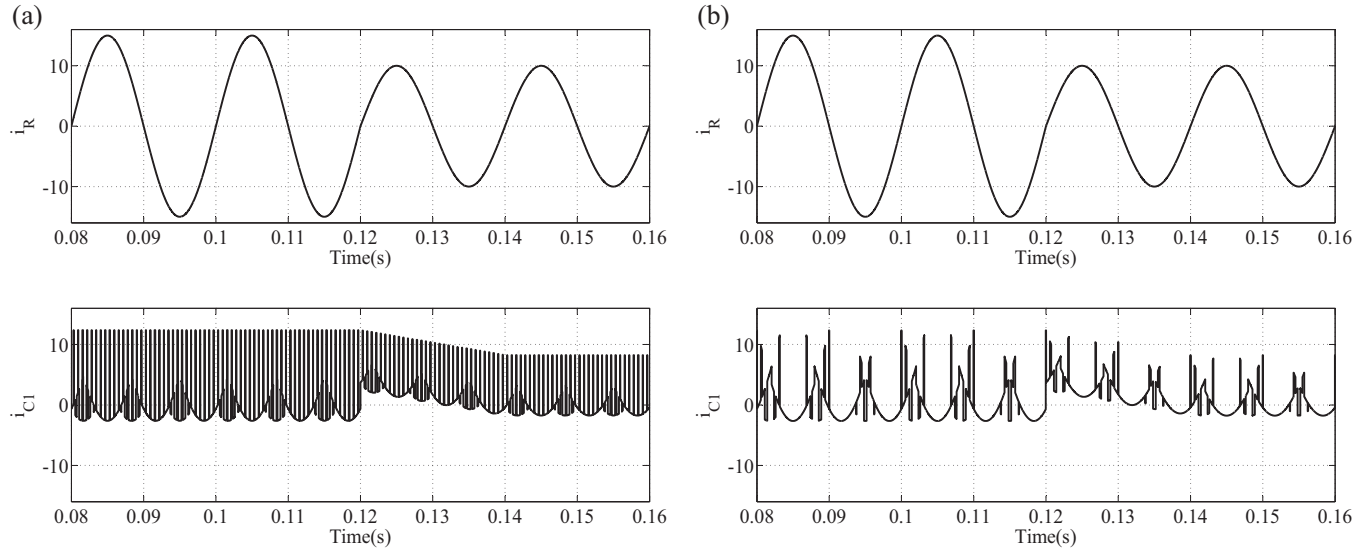

Fig. 8. Simulated waveforms of the instantaneous capacitor current for a sudden change in load current from 15 A to 5 A (peak) in case of (a) CSVPWM scheme and (b) new modulation scheme.

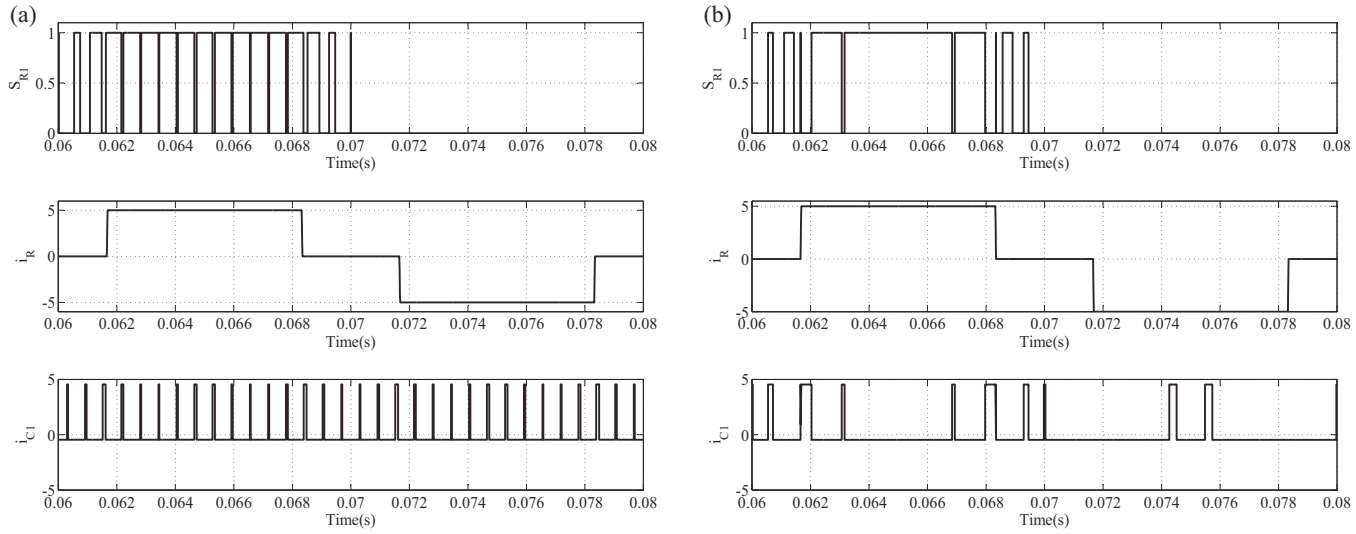

Fig. 9. Simulated waveforms of pulses of top switch, load current and capacitor current when the load is a non-linear quasi square wave current of amplitude 5 A for (a) CSVPWM scheme and (b) new modulation scheme. The capacitor RMS currents are (a) 1.43 A and (b) 1.45 A.

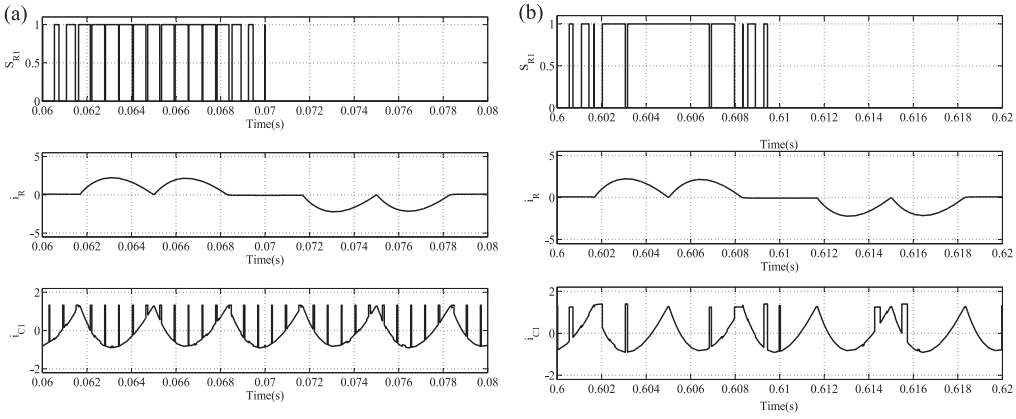

Fig. 10. Simulated waveforms of pulses of top switch, load current and capacitor current when the load is a rectifier with a filter capacitor for (a) CSVPWM scheme and (b) new modulation scheme. The capacitor RMS currents are (a) 0.75 A and (b) 0.75 A.

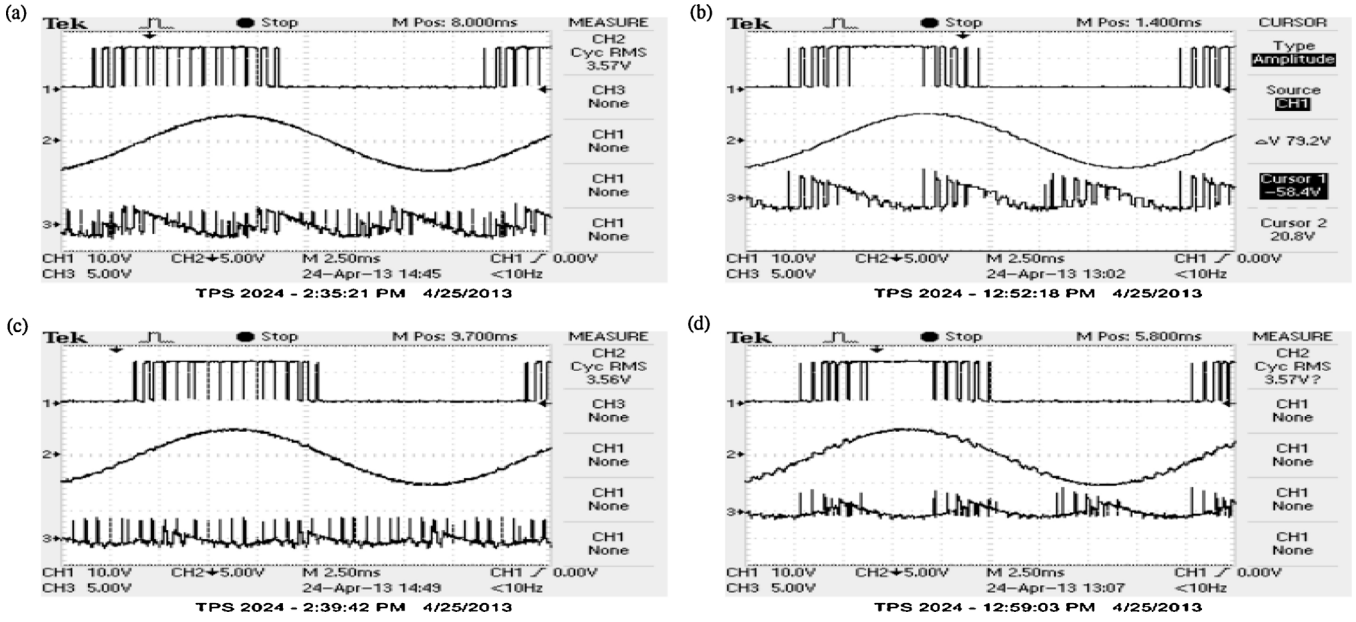

Fig. 11. Measured switching pulses for top switch (trace 1), the load current (trace 2) and the capacitor current (trace 3) for (a) CSVPWM scheme for $\phi = 45^\circ$ (lag) and $V_{ref} = 0.825$. (b) New modulation scheme for $\phi = 45^\circ$ (lag) and $V_{ref} = 0.825$. (c) CSVPWM scheme for $\phi = 10^\circ$ (lag) and $V_{ref} = 0.825$. (d) New modulation scheme for $\phi = 10^\circ$ (lag) and $V_{ref} = 0.825$. The respective RMS values of the capacitor current is (a) 1.70 A, (b) 1.95 A, (c) 1.30 A, (d) 1.12 A.

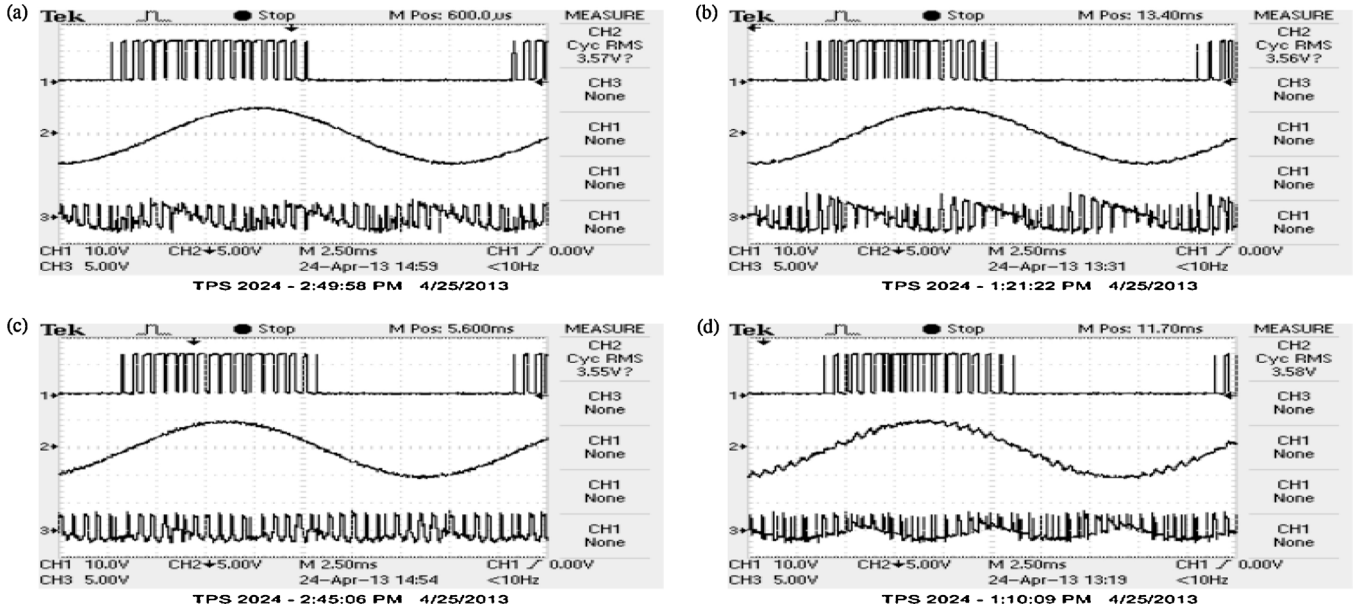

Fig. 12. Measured switching pulses for top switch (trace 1), the load current (trace 2) and the capacitor current(trace 3) for (a) CSVPWM scheme for $\phi = 45^\circ$ (lag) and V_{ref} 0.675. (b) New modulation scheme for $\phi = 45^\circ$ (lag) and $V_{ref} = 0.675$. (c) CSVPWM scheme for $\phi = 10^\circ$ (lag) and $V_{ref} = 0.675$. (d) New modulation scheme for $\phi = 10^\circ$ (lag) and $V_{ref} = 0.675$. The respective RMS values of the capacitor current is (a) 1.90 A, (b) 2.15 A, (c) 1.92 A, (d) 1.74 A.

method. The analytical expression is validated through simulations and experiments. The RMS values of capacitor current, pertaining to CSVPWM and the proposed PWM, are compared at various operating conditions based on simulations and actual measurements.

4.1. Analysis

A discussion on the instantaneous DC-link current is given in Section 3. The average and RMS values of the DC-link current over a switching cycle are designated as $i_{1,avg}$ and $i_{1,rms}$, respectively. The average value of the DC-link current over a fundamental cycle (i.e. I_{AVG}) and the RMS value of the DC-link current over a fundamental cycle ($I_{1,RMS}$), can be obtained using $i_{1,avg}$ and $i_{1,rms}$ as shown in (7).

$$I_{AVG} = \frac{1}{2\pi}\int_0^{2\pi}(i_{1,avg})d\theta$$
$$I_{1,RMS}^2 = \frac{1}{2\pi}\int_0^{2\pi}(i_{1,rms}^2)d\theta \tag{7}$$

Further, the capacitor current has a periodicity of 120° at the fundamental frequency as can be seen from Fig. 6 and 7 [4,34]. Hence it is sufficient to choose any two sectors for evaluation of the capacitor RMS current. Hence, sectors I and II are considered here for the derivation. Therefore, I_{AVG} and $I_{1,RMS}$ reduce to the following equations:

$$I_{AVG} = \frac{3}{2\pi}\int_{\pi/3}^{\pi}(i_{1,avg})d\theta$$
$$I_{1,RMS}^2 = \frac{3}{2\pi}\int_{\pi/3}^{\pi}(i_{1,rms}^2)d\theta \tag{8}$$

Both $i_{1,avg}$ and $i_{1,RMS}$ depend on the spatial region in which the reference vector falls. The expressions for $i_{1,avg}$ and $i_{1,rms}^2$ for the spatial regions OAC, ABC, OCE and CDE in Fig. 3 are tabulated in Table 3.

When $V_{ref} < 0.75$, the reference vector sweeps through the triangle OAC in sector I and the triangle OCE in sector II. Hence $I_{1,AVG}$ and $I_{1,RMS}$ can be evaluated as shown below:

$$I_{AVG} = \frac{3}{2\pi}\left(\int_{\pi/3}^{2\pi/3}(i_{1,avg,OAC})d\theta + \int_{2\pi/3}^{\pi}(i_{1,avg,OCE})d\theta\right)$$
$$I_{1,RMS}^2 = \frac{3}{2\pi}\left(\int_{\pi/3}^{2\pi/3}(i_{1,rms,OAC}^2)d\theta + \int_{2\pi/3}^{\pi}(i_{1,rms,OCE}^2)d\theta\right) \tag{9}$$

Table 3
Expressions for switching-cycle-average and switching-cycle-RMS DC-link current in sectors I and II.

Vertices	V_{ref}	θ	$i_{1,avg}$	$i_{1,rms}^2$
OAC	$0 < V_{ref} < 0.75$	$\frac{\pi}{3} < \theta < \frac{2\pi}{3}$	$\frac{1}{T_s}(i_R(T_{13}+T_{18}))$	$\frac{1}{T_s}(i_R^2(T_{13}+T_{18}))$
OAC	$0.75 < V_{ref} < 0.866$	$\frac{\pi}{3} < \theta < \frac{\pi}{2} - x$	$\frac{1}{T_s}(i_R(T_{13}+T_{18}))$	$\frac{1}{T_s}(i_R^2(T_{13}+T_{18}))$
OAC	$0.75 < V_{ref} < 0.866$	$\frac{\pi}{2} + x < \theta < \frac{2\pi}{3}$	$\frac{1}{T_s}(i_R(T_{13}+T_{18}))$	$\frac{1}{T_s}(i_R^2(T_{13}+T_{18}))$
ABC	$0.75 < V_{ref} < 0.866$	$\frac{\pi}{2} - x < \theta < \frac{\pi}{2} + \cos^{-1}x$	$\frac{1}{T_s}(i_R(T_1+T_{13}+T_{18}))$	$\frac{1}{T_s}(i_R^2(T_1+T_{13}+T_{18}))$
OCE	$0 < V_{ref} < 0.75$	$\frac{2\pi}{3} < \theta < \pi$	$\frac{1}{T_s}(i_Y T_{14} + i_R T_{13})$	$\frac{1}{T_s}(i_Y^2 T_{14} + i_R^2 T_{13})$
OCE	$0.75 < V_{ref} < 0.866$	$\frac{2\pi}{3} < \theta < \frac{5\pi}{6} - x$	$\frac{1}{T_s}(i_Y T_{14} + i_R T_{13})$	$\frac{1}{T_s}(i_Y^2 T_{14} + i_R^2 T_{13})$
OCE	$0.75 < V_{ref} < 0.866$	$\frac{5\pi}{6} + x < \theta < \pi$	$\frac{1}{T_s}(i_Y T_{14} + i_R T_{13})$	$\frac{1}{T_s}(i_Y^2 T_{14} + i_R^2 T_{13})$
CDE	$0.75 < V_{ref} < 0.866$	$\frac{5\pi}{6} - x < \theta < \frac{5\pi}{6} + \cos^{-1}x$	$\frac{1}{T_s}(i_Y T_{14} + i_B T_2 + i_R T_{13})$	$\frac{1}{T_s}(i_Y^2 T_{14} + i_B^2 T_2 + i_R^2 T_{13})$

Considering the expressions for $i_{1,avg}$ and $i^2_{1,rms}$ for the spatial regions OAC and OCE in Table 3, the final expressions for $I_{1,AVG}$ and $I^2_{1,RMS}$ for $V_{ref} < 0.75$ can be obtained as shown in (10).

$$I_{AVG} = V_{ref} I_N \cos(\phi) \quad 0 < V_{ref} < 0.75$$
$$I^2_{1,RMS} = V_{ref} I^2_N \left(\frac{2}{\pi} + \frac{2\cos(2\phi)}{3\pi}\right) \quad 0 < V_{ref} < 0.75 \tag{10}$$

Now, when the reference vector V_{ref} is greater than 0.75, the tip of the reference vector passes through the triangles OAC and ABC in sector I. Similarly, it sweeps through triangles OCE and CDE in sector II. Hence $I_{1,AVG}$ and $I^2_{1,RMS}$ can be evaluated as shown in (11). The ranges of fundamental angle for which the reference vector lies in the different triangles are given in Table 3.

$$I_{AVG} = \frac{3}{2\pi}\left(\int_{\pi/3}^{\pi/2-x} i_{1,avg,OAC}\,d\theta + \int_{\pi/2-x}^{\pi/2+x} i_{1,avg,ABC}\,d\theta + \int_{\pi/2+x}^{2\pi/3} i_{1,avg,OAC}\,d\theta + \int_{2\pi/3}^{5\pi/6-x} i_{1,avg,OCE}\,d\theta + \int_{5\pi/6-x}^{5\pi/6+x} i_{1,avg,CDE}\,d\theta + \int_{5\pi/6+x}^{\pi} i_{1,avg,OCE}\,d\theta\right)$$
$$I^2_{1,RMS} = \frac{3}{2\pi}\left(\int_{\pi/3}^{\pi/2-x} i^2_{1,rms,OAC}\,d\theta + \int_{\pi/2-x}^{\pi/2+x} i^2_{1,rms,ABC}\,d\theta + \int_{\pi/2+x}^{2\pi/3} i^2_{1,rms,OAC}\,d\theta + \int_{2\pi/3}^{5\pi/6-x} i^2_{1,rms,OCE}\,d\theta + \int_{5\pi/6-x}^{5\pi/6+x} i^2_{1,rms,CDE}\,d\theta + \int_{5\pi/6+x}^{\pi} i^2_{1,rms,OCE}\,d\theta\right) \tag{11}$$

Here $x = \cos^{-1}(3/4V_{ref})$. The expressions for $i_{1,avg}$ and $i^2_{1,rms}$ for the four spatial regions (i.e. OAC, ABC, OCE and CDE) are given in Table 3. Using these expressions, closed-form expressions can be derived for $I_{1,AVG}$ and $I_{1,RMS}$ as shown in (12).

$$I_{AVG} = V_{ref} I_N \cos(\phi) \quad 0.75 < V_{ref} < 0.866$$
$$\begin{aligned} I^2_{1,RMS} = \frac{3}{2\pi}[&V_{ref} I^2_N[4/3 + 11/18\cos(2\phi) - 8/3\sin(x) \\ &+ 4/9\sin(3x + 2\phi) + 4/3\sin(x + 2\phi) + 4/9\sin(3x - 2\phi) \\ &+ 4/3\sin(x - 2\phi)] + I^2_N[2x - \sin(2x - 2\phi) \\ &- \sin(2x + 2\phi)]] \quad 0.75 < V_{ref} < 0.866 \end{aligned} \tag{12}$$

The DC link current has an average component as well as ripple component. Assuming that the entire ripple component of i_1 flows through the capacitor, the RMS current through the capacitor I_{C1} can be obtained as shown below.

$$I_{C1} = \sqrt{I^2_{1,RMS} - I^2_{AVG}} \tag{13}$$

The capacitor RMS current, normalized with respect to the peak load current I_N, is shown plotted against V_{ref} for lagging power factor angles 0°, 10°, 18° and 45° for CSVPWM and the new modulation scheme in Fig. 13(a)–(d), respectively. From the plots one can see that the new scheme reduces the capacitor RMS current at power factor angles of 0°, 10° and 18° compared to CSVPWM scheme. On the other hand, the capacitor RMS current at $\phi = 45°$ with the proposed PWM is higher than that with CSVPWM. It can be seen that the RMS capacitor current with the proposed scheme is lower than that with CSVPWM for $\phi < 30°$. Also, the reduction in capacitor RMS current with the new modulation scheme as compared with CSVPWM scheme decreases with decrease in V_{ref}.

In order to study the dependency of RMS value of capacitor current with V_{ref} and power factor angle, a plot of normalized capacitor RMS current with respect to V_{ref} at four different power factor angles of 0°, 30°, 60° and 90° for CSVPWM is given in Fig. 14(a). Similar plot for the new modulation scheme is given in Fig. 14(b). From the figure, it can be seen that at low power factors, the capacitor RMS current increases with V_{ref} in the entire modulation range. However, at high power factors, the capacitor RMS current increases with V_{ref} upto a certain value of V_{ref}, and then stars decreasing with further increase in V_{ref}. This is true for both the modulationschemes. Also from the Fig. 14(b), it can be seen that the capacitor RMS current increases with increase in power factor for both the schemes upto a particular V_{ref}, which is around 0.75 in the case of CSVPWM and around 0.5 in the case of new modulation scheme. After this point the capacitor RMS current decreases with increase in power factor.

From Eqs. (10) and (12), it can be seen that the capacitor *rms* current depends on value of the power factor; it does not depend on whether the power factor is leading or lagging. For example, the capacitor RMS current is the same for a power factor angle of 10° (lag) as well as 10°(lead). Simulation studies on the capacitor RMS current are carried out, and the results are given in the following section.

4.2. Simulation results

A simulation study is carried out in MATLAB simulink platform, as detailed in Section 3.2. The load is modeled as a purely sinusoidal current sink as before. The RMS value of the capacitor current is determined at various power factors, both lagging and leading. The results are given in Table 5. From the data it can be seen that the capacitor RMS current does not depend on the lagging and leading nature of the load. Also, the simulated values of the capacitor RMS current in Table 5 tally with the analytically evaluated values of capacitor RMS current in Fig. 13.

4.3. Experimental results

The experimental set up is the same as that described in Section 3.3. The load current is maintained at 5 A by varying the DC-bus voltage. The modulation index is varied from $V_{ref} = 0.3$ to $V_{ref} = 0.825$ in steps of 0.075. The practical plots of normalized capacitor RMS current for the new modulation scheme and for CSVPWM at different modulation indices are shown in Fig. 15(a)–(d) for power factor angles of 0°, 10°, 18° and 45°, respectively. The plots show a direct agreement with the analytical results presented in Fig. 13, and the simulation results presented in Table 4.

5. Total harmonic distortion of load current

The load current THD is measured for CSVPWM and the proposed PWM schemes at different modulation indices and power factor angles. The measured values are tabulated in Table 6. As seen from the table, the proposed scheme leads to higher distortion than the CSVPWM scheme. This certainly implies increase in copper losses in the line-side elements. However, reduction in capacitor current signifies not only reduction in capacitor losses, but also increase in capacitor life time.

6. Evaluation of device conduction and switching losses

The conduction loss P_c and the switching loss P_s in the NPC inverter under various operating conditions are evaluated, considering both CSVPWM and the new modulation schemes. The results are shown tabulated in Table 4 for comparison.

The conduction loss in a MOSFET (i.e. $P_{c,m}$) is evaluated using the RMS current through the MOSFET (i.e. $I_{D,RMS}$) and the on-state resistance of the device (i.e. r_{DS}) as shown in (14) [36,37]. The diode

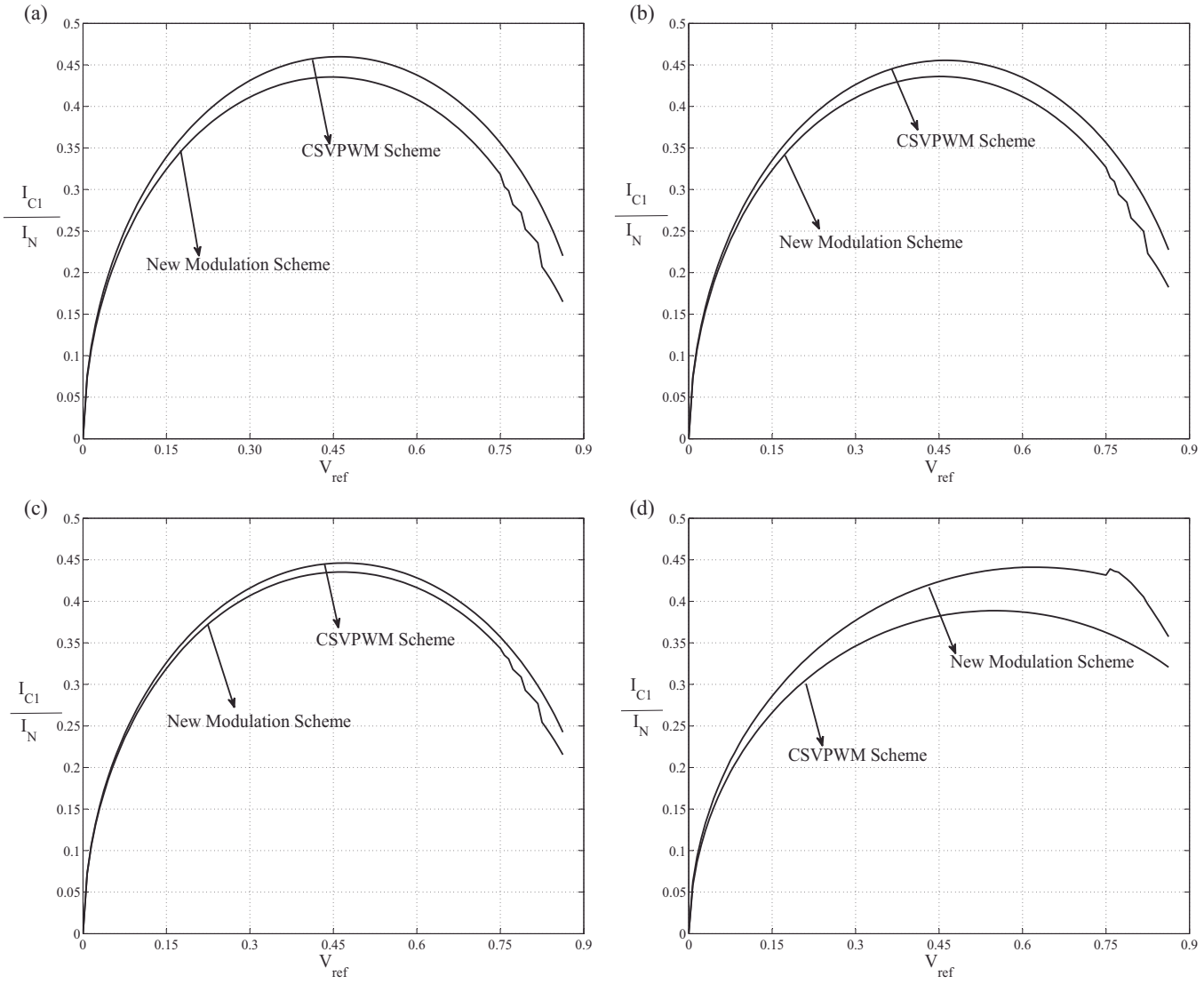

Fig. 13. Analytically evaluated normalized capacitor RMS current with CSVPWM and the new modulation scheme at (a) $\phi = 0^\circ$ (lag), (b) $\phi = 10^\circ$ (lag), (c) $\phi = 18^\circ$ (lag), (d) $\phi = 45^\circ$ (lag).

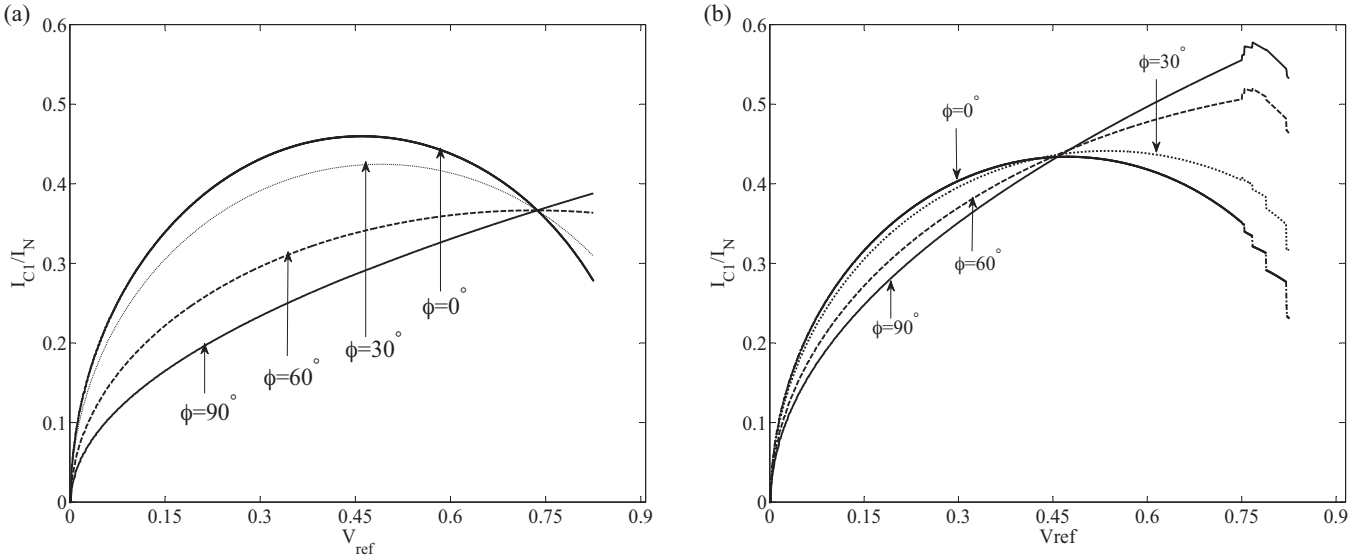

Fig. 14. Variation of normalized capacitor RMS current against V_{ref} at different angles of 0°, 30°, 60° and 90° for (a) CSVPWM scheme and (b) new modulation scheme.

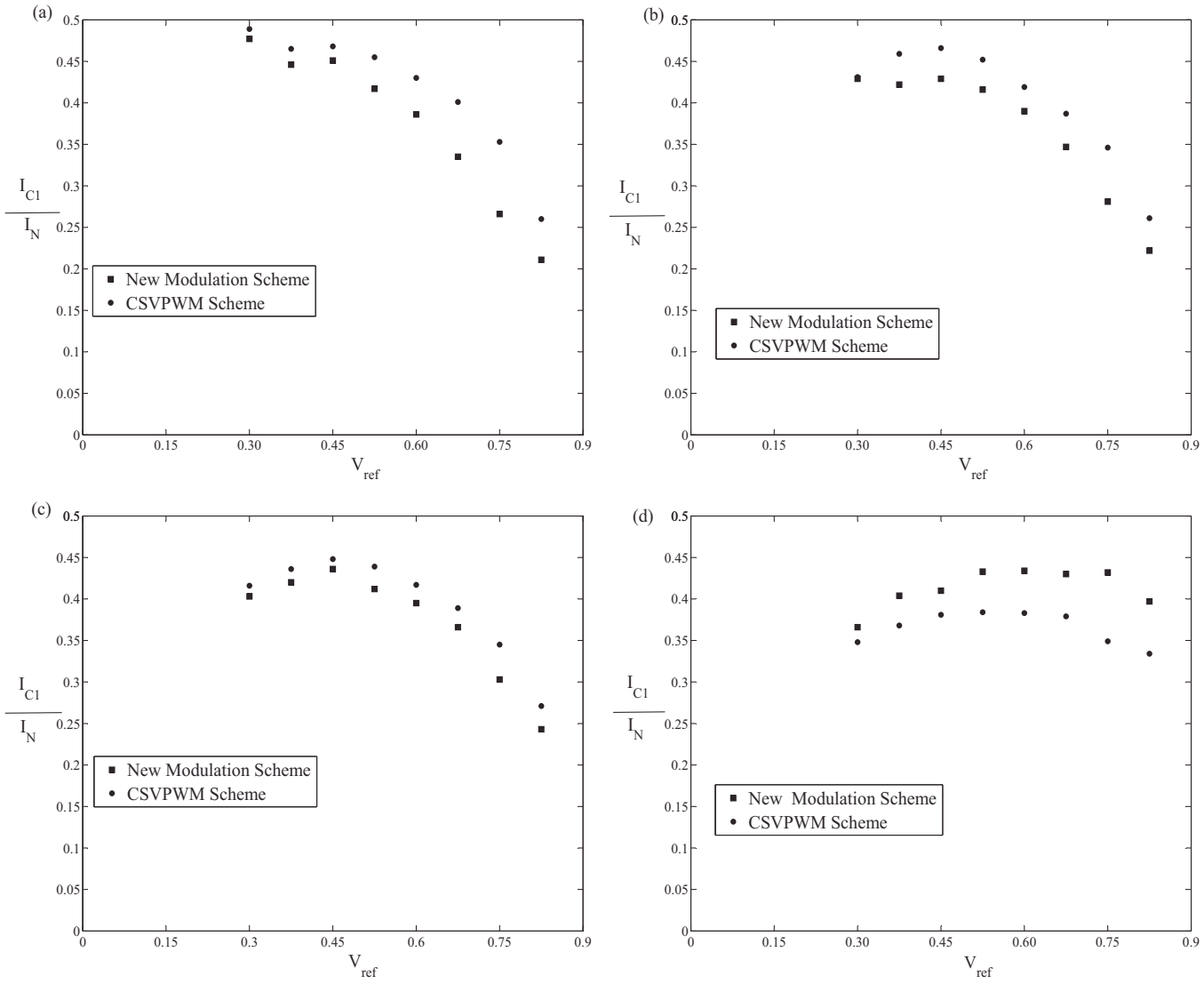

Fig. 15. Measured values of normalized capacitor RMS current with CSVPWM and new modulation scheme at (a) $\phi = 0^\circ$ (lag), (b) $\phi = 10^\circ$ (lag), (c) $\phi = 18^\circ$ (lag), (d)$\phi = 45^\circ$ (lag).

is modeled as a series combination of a fixed voltage drop v_D and a resistance r_D [36,38]. Hence, the conduction loss in a diode ($P_{c,d}$) is evaluated based on the average current through the diode ($I_{D1,avg}$) and the rms current through the diode ($I_{D1,RMS}$) as shown in (14) [36]

The conduction losses in the 12 MOSFETS, 12 anti-parallel diodes and 6 clamping diodes are all added to obtain the total conduction loss P_c in the NPC inverter.

$$P_{c,m} = I_{D,RMS}^2 r_{DS}$$
$$P_{c,d} = v_D I_{D1,avg} + I_{D1,RMS}^2 r_D \quad (14)$$

The turn 'ON' switching energy loss (E_{ON}) and turn 'OFF' switching energy loss (E_{OFF}) in the MOSFET are calculated as shown in (15). Here, t_{ON} and t_{OFF} are the switching 'ON' time and switching 'OFF' time, respectively of the MOSFET [36,37].

$$E_{ON,M} = \frac{V_{DC}}{4} i_D t_{ON}$$
$$E_{OFF,M} = \frac{V_{DC}}{4} i_D t_{OFF} \quad (15)$$

For each MOSFET, E_{ON} and E_{OFF} during each turn-on and turn-off interval, respectively, are summed up over a fundamental

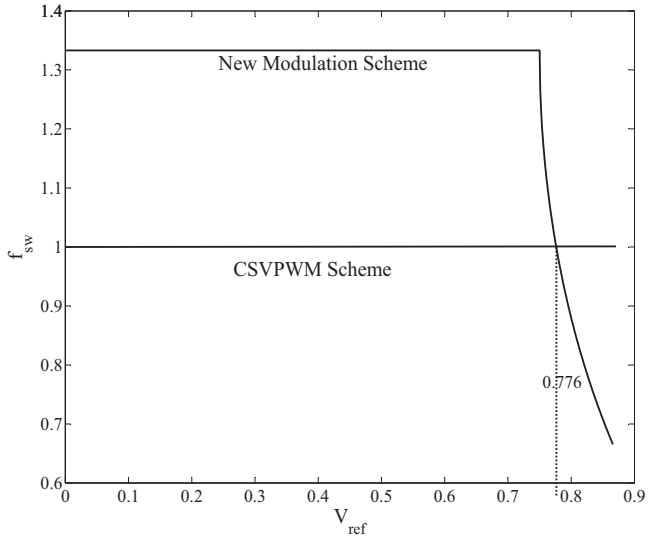

Fig. 16. Normalized average switching frequency against V_{ref} for the proposed modulation scheme and CSVPWM scheme.

Table 4
Conduction loss, switching loss of the inverter using the new modulation scheme and CSVPWM scheme.

V_{ref}	Power factor	Input power (w)	Conduction loss (w)		Switching loss (w)	
			New scheme	CSVPWM	New scheme	CSVPWM
0.825	1	2475	21.26	21.48	10.24	13.51
0.825	0.966	2390	21.48	21.71	11.01	14.28
0.825	0.866	2144	22.03	22.37	11.81	15.06
0.825	0.707	1751	22.89	23.36	12.61	15.84
0.75	1	2250	21.69	21.61	16.64	13.51
0.75	0.966	2173	21.85	21.85	17.41	14.28
0.75	0.866	1949	22.26	22.52	18.18	15.06
0.75	0.707	1591	22.92	23.49	18.95	15.84
0.675	1	2025	21.99	21.74	16.64	13.51
0.675	0.966	1956	22.15	21.98	17.41	14.28
0.675	0.866	1754	22.52	22.68	18.18	15.06
0.675	0.707	1432	23.11	23.63	18.95	15.84
0.6	1	1800	22.30	22.23	16.64	13.51
0.6	0.966	1738	22.44	22.40	17.41	14.28
0.6	0.866	1554	22.77	22.95	18.18	15.06
0.6	0.707	1273	23.30	23.76	18.95	15.84
0.525	1	1575	22.61	22.33	16.64	13.51
0.525	0.966	1521	22.74	22.49	17.41	14.28
0.525	0.866	1364	23.03	23.00	18.18	15.06
0.525	0.707	1114	23.49	23.75	18.95	15.84
0.45	1	1350	22.91	22.33	16.64	13.51
0.45	0.966	1304	23.03	22.48	17.41	14.28
0.45	0.866	1169	23.29	22.96	18.18	15.06
0.45	0.707	955	23.68	23.75	18.95	15.84

Table 5
Simulated values of capacitor RMS current with the new modulation scheme for different operating conditions.

V_{ref}	$\phi = 45^\circ$		$\phi = 30^\circ$		$\phi = 18^\circ$		$\phi = 10^\circ$	
	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead
0.267	1.8329	1.8311	1.9024	1.9009	1.9438	1.9428	1.961	1.9604
0.375	1.9802	1.9791	2.0267	2.0258	2.0547	2.0541	2.0665	2.0661
0.450	2.0911	2.0905	2.1048	2.1044	2.1132	2.1129	2.1168	2.1166
0.525	2.1704	2.1705	2.1412	2.1412	2.1230	2.1230	2.1152	2.1152
0.6	2.2217	2.2223	2.1379	2.1384	2.0846	2.0850	2.0616	2.0618
0.675	2.2473	2.2483	2.0951	2.0960	1.9957	1.9964	1.9521	1.9524
0.75	2.2482	2.2497	2.0107	2.0121	1.8495	1.8405	1.7767	1.7774
0.825	2.2248	2.2269	1.8798	1.8819	1.6316	1.6332	1.5141	1.5151

cycle. These summed up values are given by $E_{ON,total}$ and $E_{OFF,total}$, respectively. The net average switching loss in the MOSFET in a fundamental cycle ($P_{s,m}$) is given by (16), where T_f is the fundamental time period.

$$P_{s,m} = \frac{E_{ON,total} + E_{OFF_total}}{T_f} \tag{16}$$

The reverse recovery energy loss ($E_{RR,D}$) in a diode is calculated as shown in (17), where Q_{rr} is the reverse recovery charge in the diode, V_{DD} is the voltage across the diode [36,37]. For each diode, the reverse recovery energy during each turn-on interval of the MOSFET is accumulated over the line-cycle to get the total reverse recovery loss ($E_{RR,total}$). This is divided by the fundamental cycle time to obtain the diode reverse recovery loss $P_{RR,D}$ as shown below:

$$E_{RR,D} = Q_{rr} V_{DD}$$
$$P_{RR,D} = \frac{E_{RR,total}}{T_f} \tag{17}$$

The switching loss in the MOSFETS and the reverse recovery losses in the diodes are summed up to obtain the total switching loss in the inverter as shown:

$$P_s = P_{s,m} + P_{RR,D} \tag{18}$$

It can be seen from Table 4 that the conduction losses due to both the schemes are comparable. But the switching loss with CSVPWM

Table 6
Measured load current THD values for CSVPWM and new modulation scheme.

V_{ref}	$\phi = 45^\circ$ (lag)		$\phi = 30^\circ$ (lag)		$\phi = 18^\circ$ (lag)		$\phi = 10^\circ$ (lag)		$\phi = 0^\circ$ (lag)	
	CSVPWM	New scheme	CSVPWM	New scheme	CSVPWM	New scheme	CSVPWM	New scheme	CSVPWM	New scheme
0.825	0.0346	0.0524	0.0352	0.0385	0.0414	0.0438	0.0498	0.0522	0.0777	0.1311
0.750	0.0458	0.0329	0.0486	0.0487	0.0553	0.0655	0.0570	0.0912	0.1019	0.1667
0.675	0.0190	0.0378	0.0233	0.0535	0.0324	0.0776	0.0441	0.1108	0.0838	0.1970
0.600	0.0205	0.0445	0.0251	0.0648	0.0328	0.900	0.0450	0.1296	0.0870	0.2338
0.525	0.0205	0.0496	0.0251	0.0733	0.0320	0.1061	0.0462	0.1526	0.0789	0.2797
0.450	0.0220	0.0570	0.0289	0.0854	0.0378	0.1238	0.0513	0.1785	0.0984	0.3088
0.375	0.0292	0.0633	0.0382	0.0993	0.0495	0.1415	0.0765	0.2021	0.1381	0.3575
0.300	0.0346	0.0707	0.0493	0.1053	0.0758	0.1592	0.0992	0.2316	0.1964	0.4192

is lower than that with the proposed scheme for $V_{ref} < 0.75$. However, the proposed scheme leads to reduced switching loss for $V_{ref} > 0.75$, compared to CSVPWM.

The difference in the switching losses of the two PWM methods is on account of the difference in the average switching frequency of the two methods, as illustrated by Fig. 16. With CSVPWM, each phase switches once in a subcycle, and there are three switchings per subcycle. However, with the proposed PWM, there are four switchings per subcycle when sequence 1 is used, and two switching per subcycle when the sequence 2 is employed (see Section 2). Hence, the normalized switching frequency of the new PWM scheme (i.e. ratio of the average switching frequency of the proposed PWM to the switching frequency of CSVPWM) varies with modulation index V_{ref} as shown in Fig. 16.

7. Conclusion

A space vector based modulation scheme for reducing the capacitor RMS current in a three-level diode-clamped inverter is proposed. The proposed method is a non-three nearest vector (non-TNV) PWM method. An analytical closed-form expression is derived for the capacitor RMS current with the proposed PWM scheme. The capacitor RMS current is expressed as a function of modulation index, peak fundamental current and power factor angle. This analytical expression is validated through simulations and also experimentally at a number of operating conditions. Simulation and experimental results demonstrate the reduction in capacitor RMS current at high power factors with the proposed PWM method. It is shown that the proposed scheme is particularly effective in reducing the capacitor RMS current at medium to high modulation indices. Thus, the work brings out another possible benefit of non-nearest three vector PWM methods, namely reduction of capacitor RMS current in a three-level inverter.

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