Novel Switching Sequences for a Space-Vector-Modulated Three-Level Inverter

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***Abstract*—A three-level inverter produces six active vectors, each of normalized magnitudes 1, 0.866, and 0.5, besides a zero vector. The vectors of relative length 0.5 are termed *pivot vectors*. The three nearest voltage vectors are usually used to synthesize the reference vector. In most continuous pulsewidth-modulation (PWM) schemes, the switching sequence begins from a pivot vector and ends with the same pivot vector. Thus, the pivot vector is applied twice in a subcycle or half-carrier cycle. This paper proposes and investigates alternative switching sequences, which use the pivot vector only once but employ one of the other two vectors twice within the subcycle. The total harmonic distortion (THD) in the fundamental line current pertaining to these novel sequences is studied theoretically as well as experimentally over the whole range of modulation. Compared with centered space vector PWM, two of the proposed sequences lead to reduced THD at high modulation indices at a given average switching frequency.**

***Index Terms*—Harmonic analysis, harmonic distortion, multilevel inverter, neutral-point clamped (NPC) inverter, pulsewidth modulation, space vector, stator flux ripple, voltage source inverter.**

I. Introduction

NOWADAYS, three-level voltage source inverters (3LVSIs) are increasingly employed for dc–ac power conversion. A three-level neutral-point clamped (NPC) inverter, shown in Fig. 1, has numerous advantages over a conventional two-level voltage source inverter (2LVSI) [1]–[8]. One of the advantages is the improved output waveform quality or reduction in total harmonic distortion (THD) in the line current, compared with that of a 2LVSI, under similar operating conditions [2]–[4]. With devices of the same voltage rating, a 3LVSI can handle a dc bus voltage roughly twice that of a 2LVSI. Hence, this topology is favored in medium-voltage applications [5]–[7]. It also provides better performance in terms of semiconductor losses, filtering arrangement, and common-mode voltages than a two-level converter in low-voltage applications with medium to high switching frequencies [2].

After its introduction around 1980 [8], [9], the multilevel inverter has been an active subject for research, particularly in the recent years [1]–[7]. There has also been extensive research on pulsewidth-modulation (PWM) methods for a multilevel inverter [8]–[30].

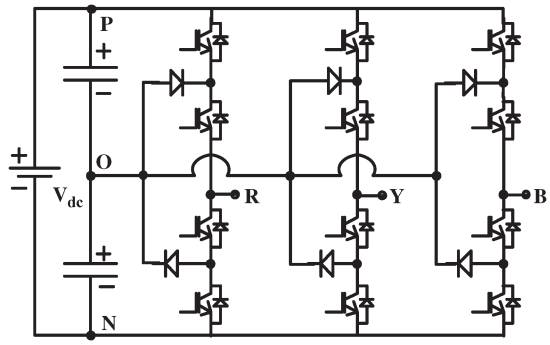

Fig. 1. Diode-clamped three-level inverter.

Selective harmonic elimination PWM (SHEPWM) [8] and simple uniform PWM [9] are among the earliest PWM methods used for an NPC inverter. Subsequently, considerable research has been carried out on SHEPWM for multilevel converters [8], [10], [11]. With uniform PWM, the voltage pulses are of uniform width over a line cycle [9]. In sinusoidal PWM (SPWM), the widths of the voltage pulses are modulated in a sinusoidal fashion over the fundamental cycle to achieve good spectral properties [12]–[14], [28]–[30].

Usually, in sinusoidal PWM, three-phase sinusoidal reference signals are compared against two level-shifted carriers. These two carriers could be either in phase or in phase opposition, leading to in-phase SPWM (IPSPWM) and phase opposition SPWM (POSPWM), respectively [12], [14]. Third harmonic or zero-sequence components are added to the three-phase sinusoidal modulating signals to achieve better utilization of dc bus and superior waveform quality [15], [16]. Centered space vector PWM (CSVPWM) [17]–[24], [27]–[30] has gained popularity as it offers higher dc bus utilization and lower harmonic distortion in line current than sinusoidal PWM. Recently, discontinuous or bus-clamping modulation techniques have been proposed for multilevel inverters [25]–[27]. These further reduce the harmonic distortion in line current at high modulation indices at the same average switching frequency [27].

All the aforementioned methods are essentially extensions of corresponding PWM techniques for a two-level inverter [31]–[42]. All continuous and discontinuous modulation schemes for a 2LVSI, in turn, are on account of the redundancy in application of the zero vector in the inverter (Fig. 2) [33]–[35]. The zero vector ($\mathbf{E_0}$) can be applied either using the zero state $---(0)$ or the zero state $+++(7)$, as seen in Fig. 2[31],

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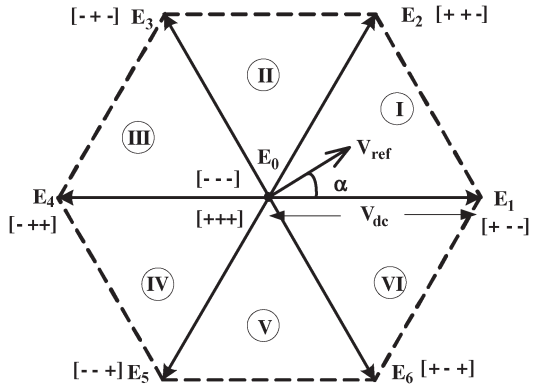

Fig. 2. Vector diagram of a 2LVSI. I, II, II, IV, V, and VI are sectors.

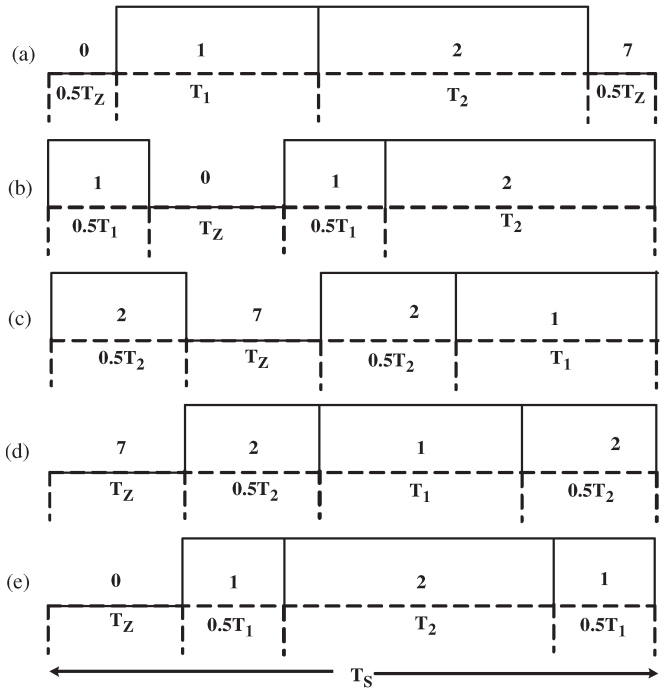

Fig. 3. Switching sequences for a two-level inverter.

[32]. In continuous modulation methods, both the zero states are used; the inverter state changes in a sequence starting from one zero state (say $---$ or 0) and ending with the other zero state ($+++$ or 7) in a subcycle [33]–[35]. In case of CSVPWM, the two zero states are applied for an equal duration of time, as shown in Fig. 3(a). For the reference vector shown in Fig. 2, active vectors 1 and 2 are applied for duration T_1 and T_2, respectively, as given by

$$T_1 = \frac{V_{\text{ref}}}{V_{\text{dc}}} \frac{\sin(60^\circ - \alpha)}{\sin(60^\circ)} T_s$$

$$T_2 = \frac{V_{\text{ref}}}{V_{\text{dc}}} \frac{\sin(\alpha)}{\sin(60^\circ)} T_s$$

$$T_Z = T_s - (T_1 + T_2). \tag{1}$$

In case of discontinuous PWM methods, only one zero state ($---$ or $+++$) is applied for the entire T_{Z} in a subcycle or half-carrier cycle [40]–[44].

In conventional sequence 0127, all three phases switch once in a subcycle. Alternative switching sequences, where one phase switches twice, another switches once, and the third phase is clamped in a subcycle (T_{s}), have been proposed and investigated recently for a two-level inverter [36]–[42]. These are termed *double-switching clamping sequences* and are shown in Fig. 3(b)–(e). While all these sequences use only one zero state, these apply one of the active states (closer to the zero state used) twice in a subcycle as seen from Fig. 3(b)–(e). Any one of these sequences (for example, 0121) and its reversed version (for example, 1210) can be used in alternate subcycles. With such sequences, the total number of switchings per subcycle is the same as that of CSVPWM, namely, three [33]–[42].

At the same average switching frequency, sequences 7212 and 0121 have been shown to reduce the line current THD by about 40% close to maximum modulation index [33], [34]. Sequences 1012 and 2721 have been shown to reduce the pulsating torque in motor drives [40]. Appropriate selection and combination of such sequences have resulted in reduced switching loss in a two-level inverter [39]. Such sequences have also been employed in interleaved PWM converters to reduce line current ripple [41].

This paper proposes and investigates novel switching sequences for a three-level inverter, which are equivalent to the sequences 1012, 2721, 0121, and 7212 for a two-level inverter. Limited results pertaining to sequences 0121 and 7212 were presented in a conference publication [24]. Detailed analysis and results pertaining to all four sequences are presented here.

The construction of double-switching clamping sequences for a three-level inverter is explained in detail in Section II. While producing the same reference vector, these alternative switching sequences considerably influence the line current ripple. The proposed sequences are analyzed in terms of rms current ripple and inverter switching loss in Sections III and IV, respectively. The current ripple analysis is validated through extensive experimental study over a wide range of modulation on a constant voltage to frequency (V/f) induction motor drive in Section V. It is shown that two of the proposed sequences reduce the THD in the line current by around 30% at high modulation indices, compared with CSVPWM; another sequence results in reduced current ripple at lower modulation indices (fundamental frequencies below 12 Hz). The conclusions are presented in Section VI.

II. Switching Sequence for a Three-Level Inverter

The alternative switching sequences for a two-level inverter, discussed in the previous section, are on account of the redundancy in zero vector and multiple application of active states [36]–[42]. In this section, the redundancies in a three-level inverter are discussed first. Appropriate switching sequences are constructed subsequently.

A. Redundancy in a Three-Level Inverter

Redundancy implies availability of multiple inverter states to produce a given voltage vector in a voltage source converter.

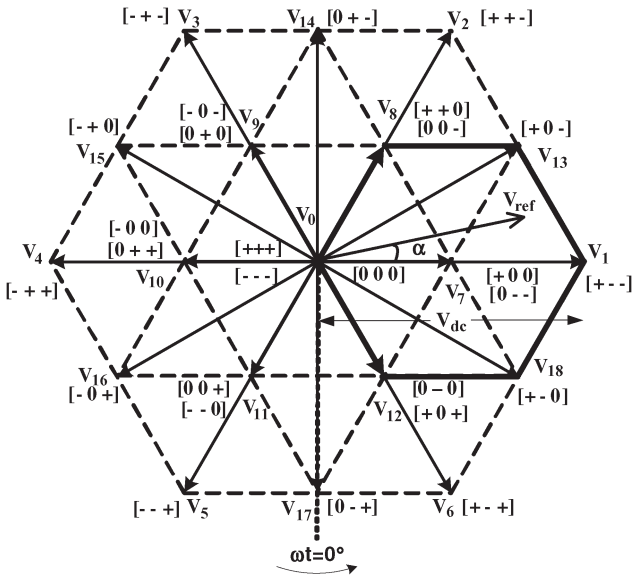

Fig. 4. Voltage vector diagram of a three-level inverter.

In an NPC inverter, there is redundancy in zero vector $\mathbf{V_0}$ and also in vectors of magnitude 0.5 $V_{\rm dc}$ ($\mathbf{V_7}$ to $\mathbf{V_{12}}$), as seen in Fig. 4. The zero vector ($\mathbf{V_0}$) can be produced using any one of the three zero states ($+++$, 000, and $---$). Similarly, each of the vectors of magnitude 0.5 $V_{\rm dc}$ ($\mathbf{V_7}$ to $\mathbf{V_{12}}$) can be applied using one of two corresponding states. For example, the vector $\mathbf{V_7}$ has two corresponding states, namely $+00$ and $0--$, as shown in Fig. 4. In most continuous modulation methods for a three-level inverter, the switching sequence starts from one such state and ends with the other state [14], [17], [19], [20], [24]. Hence, these two states are termed *pivot states*, and the corresponding voltage vector is called *pivot vector* [17], [19], [20].

Three voltage vectors, closest to the commanded reference vector $\mathbf{V_{ref}}$, are usually used to synthesize $\mathbf{V_{ref}}$ in a subcycle [17]–[20]. For the reference vector $\mathbf{V_{ref}}$ shown in Fig. 4, voltage vectors $\mathbf{V_7}$, $\mathbf{V_1}$, and $\mathbf{V_{13}}$ are usually used [17]–[20]. POSPWM is a notable exception in this regard, where $\mathbf{V_0}$, $\mathbf{V_7}$, $\mathbf{V_{13}}$, and $\mathbf{V_1}$ are applied to synthesize the $\mathbf{V_{ref}}$ shown; the switching sequence is $(000, +00, +0-, +--)$ or its time-reversed version $(+--, +0-, +00, 000)$[14]. Understandably, since all vectors used are not close to $\mathbf{V_{ref}}$, the harmonic distortion in line current is higher with POSPWM than with IPSPWM [14].

When three closest vectors are used, the zero vector ($\mathbf{V_0}$) is one of them only if the tip of $\mathbf{V_{ref}}$ falls within the inner hexagon, formed by the tips of pivot vectors $\mathbf{V_7}$ to $\mathbf{V_{12}}$. For the reference vector angle α shown in Fig. 4, the pivot vector $\mathbf{V_7}$ is one of the closest vectors for any realizable length $V_{\rm ref}$. Thus, the zero vector is applied only at low modulation indices, while a pivot vector is used at low as well as high modulation indices.

Since a pivot vector is used at all modulation indices and also the switching sequence typically begins from and ends with the pivot vector, the role of pivot vector in a 3LVSI is similar to that of zero vector in case of a 2LVSI. This has led to the widespread practice of controlling a three-level inverter as an equivalent two-level inverter [17], [20], [24], [25]. During such control, a phase switches only between positive dc bus (P) and dc bus midpoint (O) during its positive half cycle and only between "O" and negative dc bus (N) during its negative half cycle. Hence, all the three-phases are never concurrently connected to the dc rail "P." Similarly, all three phases are also never connected to the negative dc bus "N" at the same time. Thus, the zero states $+++$ and $---$ never get employed; only the zero state 000 is used to apply the null vector $\mathbf{V_0}$.

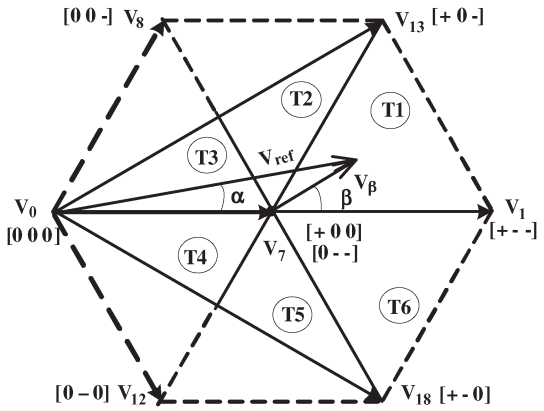

Fig. 5. Vector diagram of the equivalent two-level inverter in the first hextant.

To the authors' knowledge, the earliest attempt to investigate switching sequences based on redundancy and multiple application of states for a 3LVSI is found in [19]. Due to the redundancy in zero vector, more switching sequences are possible in the inner hexagon, formed by tips of vectors $\mathbf{V_7}$ to $\mathbf{V_{12}}$ [19]. Since this paper focuses on sequences for a 3LVSI controlled as an equivalent 2LVSI, the redundancy in zero vector $\mathbf{V_0}$ is not utilized here. Novel switching sequences are constructed based on the redundancy in pivot vector and the possibility of multiple application of inverter states in the following section.

B. Novel Switching Sequences

The reference vector $\mathbf{V_{ref}}$ for a three-level inverter, shown in Fig. 4, is reproduced in Fig. 5. The nearest pivot vector $\mathbf{V_7}$ can be subtracted from $\mathbf{V_{ref}}$ to obtain the reference vector $(V_\beta \angle \beta)$ corresponding to the equivalent two-level inverter, as shown in Fig. 5. The equivalent reference vector ($\mathbf{V_\beta}$) can be synthesized by applying the voltage vectors $\mathbf{V_1}$, $\mathbf{V_{13}}$, and $\mathbf{V_7}$ for durations T_1, T_2, and $T_{\rm Z}$, respectively. The dwell times can be calculated in a fashion similar to that of a two-level inverter, as shown in the following:

$$T_1 = \frac{V_\beta}{0.5V_{\rm dc}} \frac{\sin(60^\circ - \beta)}{\sin(60^\circ)} T_s$$

$$T_2 = \frac{V_\beta}{0.5V_{\rm dc}} \frac{\sin(\beta)}{\sin(60^\circ)} T_s$$

$$T_Z = T_s - (T_1 + T_2). \tag{2}$$

Most continuous PWM schemes such as IPSPWM and CSVPWM apply the pivot vector $\mathbf{V_7}$ through both pivot states ($0--$ and $+00$); the switching sequence is ($0--$,

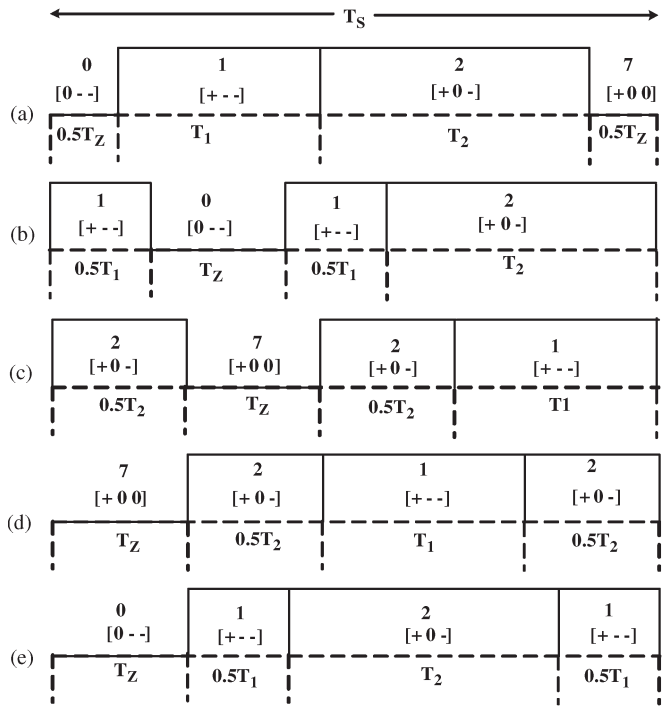

Fig. 6. Switching sequences for a three-level inverter.

$+--, +0-, +00)$ or its reversed version, i.e., $(+00, +0-, +--, 0--)$ [14], [17]. The pivot vector time T_Z is divided unequally between two pivot states in IPSPWM [14]. The dwell times of the two pivot states are equal in the case of CSVPWM [17], [24]. Only one pivot state is applied for the entire pivot vector time in discontinuous PWM methods [25], [26], e.g., $(0--, +--, +0-)$. This results in clamping of one of the phases to one of the dc rails, e.g., B-phase to negative dc rail [25], [26]. Thus, various existing PWM schemes essentially differ in the apportioning of the pivot vector time between the two pivot states.

This paper proposes alternative switching sequences, shown in Fig. 6(b)–(e), for the reference vector $\mathbf{V_{ref}}$ in Fig. 5. These sequences use only one pivot state for the entire pivot vector time T_Z, while apply one of the other two states twice for a total duration as given by (2). A transition between the pivot state used and the state applied twice requires switching of only one phase between adjacent voltage levels (between "P" and "O" or between "O" and "N"). If the state $+--$ is used twice, then the pivot state employed is $0--$ as seen from Fig. 6(b) and (e). On the other hand, if the state $+0-$ is applied twice, the pivot state $+00$ is employed for the entire duration T_Z, as shown in Fig. 6(c) and (d).

In the sequence $(+--, 0--, +--, +0-)$ shown in Fig. 6(b), R-phase switches twice while B-phase remains clamped. In the case of sequence $(+0-, +00, +0-, +--)$ in Fig. 6(c), B-phase switches twice in a subcycle with R-phase remaining clamped. In both cases, Y-phase switches once. On the other hand, sequences $(+00, +0-, +--, +0-)$ and $(0--, +--, +0-, +--)$, shown in Fig. 6(d) and (e), respectively, involve double switching of Y-phase. R-phase is clamped to the positive dc bus with the former, while B-phase is clamped to the negative dc bus in the case of the latter. With such sequences, the total number of switchings per subcycle is three as in CSVPWM, as shown in Fig. 6(a).

TABLE I
ZERO AND ACTIVE STATES OF THE EQUIVALENT TWO-LEVEL INVERTER

Hex no.	Range of angle, ωt	Pivot vector, equivalent zero states	Equivalent active states
1	60° < ωt ≤ 120°	$\mathbf{V_7}$ (0--, +00)	000, 0-0, +-0, +--, +0-, 00-
2	120° < ωt ≤ 180°	$\mathbf{V_8}$ (++0, 00-)	000, +00, +0-, ++-, 0+-, 0+0
3	180° < ωt ≤ 240°	$\mathbf{V_9}$ (-0-, 0+0)	000, 00-, 0+-, -+-, -+0, -00
4	240° < ωt ≤ 300°	$\mathbf{V_{10}}$ (0++, -00)	000, 0+0, -0+, -++, -0+, 00+
5	300° < ωt ≤ 360°	$\mathbf{V_{11}}$ (--0, 00+)	000, -00, -0+, --+, 0-+, 0-0
6	0° < ωt ≤ 60°	$\mathbf{V_{12}}$ (+0+, 0-0)	000, 00+, 0-+, +-+, +-0, +00

In all the proposed sequences, only one phase switches for a state transition. Furthermore, a phase switches only between adjacent voltage to keep the voltage stress and device losses low. These sequences are valid in the spatial region, bounded by the tips of vectors $\mathbf{V_7}$, $\mathbf{V_1}$, and $\mathbf{V_{13}}$. These are generalized for the whole spatial region, bounded by the tips of vectors $\mathbf{V_1}$ to $\mathbf{V_6}$, in the following section.

C. Generalization of Switching Sequences

The polarities of the three-phase fundamental voltages divide a line cycle into six hextants. These are defined mathematically in terms of the fundamental angle ωt in Table I, where $\omega t = 0^\circ$ corresponds to the positive zero-crossing of R-phase fundamental voltage (see Fig. 4). Pivot vector $\mathbf{V_7}$ to $\mathbf{V_{12}}$, respectively, act as the equivalent zero vectors in the six hextants. Hexagons of side 0.5 V_{dc}, centered around the tips of the respective pivot vectors, represent the equivalent two-level inverter in the six hextants. The hexagon, pertaining to the first hextant, is shown in Fig. 4; this is reproduced in Fig. 5. The equivalent zero states (pivot states) and the six equivalent active states, corresponding to all six hexagons, are tabulated in Table I.

In any given hextant, the nearest pivot vector $\mathbf{V_{PN}}$ (i.e., the pivot vector corresponding to the given hextant) is subtracted from the reference vector $\mathbf{V_{ref}}$ to obtain the equivalent reference vector $\mathbf{V_\beta}$ for the conceptual two-level inverter, as shown in the following:

$$\mathbf{V_\beta} = \mathbf{V_{ref}} - \mathbf{V_{PN}} = V_\beta \angle \beta. \tag{3}$$

Based on the angle (β) of the equivalent reference vector, each hexagon (for example, hexagon 1) is divided into six triangles, as shown in Fig. 5 and listed in Table II.

For each hexagon, the two pivot states are designated as equivalent zero state 0 and equivalent zero state 7, as indicated in Table III. For each hexagon and triangle, the generalized states 1 and 2 are as listed in the same table. In any given triangle, the generalized state 1 is closer to the generalized zero state; the generalized state 2 is closer to the generalized zero state 7. In terms of the generalized states, the five sequences in

TABLE II
TRIANGLE IDENTIFICATION BASED ON ANGLE β

Triangle no, T	Range of angle, β
1	$0° < \beta \leq 60°$
2	$60° < \beta \leq 120°$
3	$120° < \beta \leq 180°$
4	$180° < \beta \leq 240°$
5	$240° < \beta \leq 300°$
6	$300° < \beta \leq 360°$

TABLE III
GENERALIZED STATES OF THE EQUIVALENT TWO-LEVEL INVERTER

Hex no	Tri. No,T	State-0	State-1	State-2	State-7
1	1	0--	+--	+0-	+00
	2		00-	+0-	
	3		00-	000	
	4		0-0	000	
	5		0-0	+-0	
	6		+--	+-0	
2	1	++0	++-	0+-	00-
	2		0+0	0+-	
	3		0+0	000	
	4		+00	000	
	5		+00	+0-	
	6		++-	+0-	
3	1	-0-	-+-	-+0	0+0
	2		-00	-+0	
	3		-00	000	
	4		00-	000	
	5		00-	0+-	
	6		-+-	0+-	
4	1	0++	-++	-0+	-00
	2		00+	-0+	
	3		00+	000	
	4		0+0	000	
	5		0+0	-+0	
	6		-++	-+0	
5	1	--0	--+	0-+	00+
	2		0-0	0-+	
	3		0-0	000	
	4		-00	000	
	5		-00	-0+	
	6		--+	-0+	
6	1	+0+	+-+	+-0	0-0
	2		+00	+-0	
	3		+00	000	
	4		00+	000	
	5		00+	0-+	
	6		+-+	0-+	

Fig. 6 can be designated as 0127, 1012, 2721, 7212, and 0121, respectively.

Table IV lists the generalized switching sequences and the corresponding actual switching sequences for triangles T1 to T3 in hexagon 1. Based on the definition of generalized states in Table III, the actual switching sequence corresponding to a given generalized sequence can similarly be determined in any triangle and any hexagon.

As in the case of discontinuous PWM, the four novel sequences clamp every phase to one of the dc rails over certain intervals in the line cycle. The difference here is that one of the other two phases switches at twice the nominal switching frequency in these intervals. Thus, these sequences result in

TABLE IV
GENERALIZED AND ACTUAL SWITCHING SEQUENCES IN HEXAGON I

Sl. No.	Generalized Sequence	Actual switching sequences		
		Triangle T1	Triangle T2	Triangle T3
1	0127	(0--, +--, +0-, +00)	(0--, 00-, +0-, +00)	(0--, 00-, 000, +00)
2	1012	(+--, 0--, +--, +0-)	(00-, 0--, 00-, +0-)	(00-, 0--, 00-, 000)
3	2721	(+0-, +00, +0-, +--)	(+0-, +00, +0-, 00-)	(000, +00, 000, 00-)
4	7212	(+00, +0-, +--, +0-)	(+00, +0-, 00-, +0-)	(+00, 000, 00-, 000)
5	0121	(0--, +--, +0-, +--)	(0--, 00-, +0-, 00-)	(0--, 00-, 000, 00-)

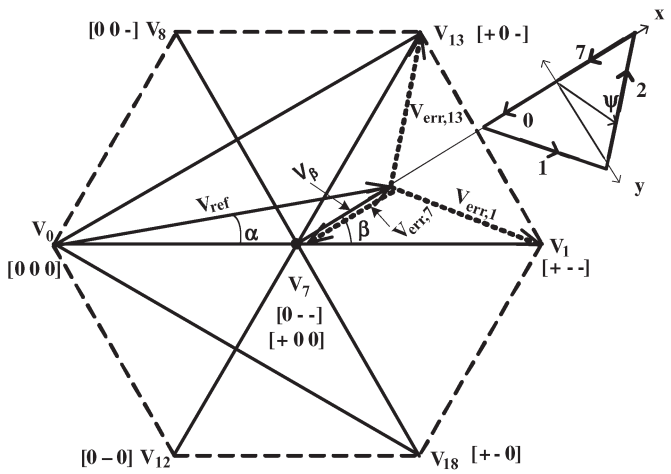

Fig. 7. Error voltage vectors corresponding to equivalent active vector 1 ($\mathbf{V_1}$), equivalent active vector 2 ($\mathbf{V_{13}}$), equivalent zero vector ($\mathbf{V_7}$), and stator flux ripple vector for sequence 0127.

certain redistribution of the "local" switching frequency over a line cycle. The "local" switching frequency of a phase is zero in certain intervals of the fundamental cycle, while it is twice the nominal switching frequency in certain other regions. This has been discussed in considerable detail in the context of a two-level inverter in [39]. The intent of this paper is to investigate the effect of such redistribution of the "local" switching frequency on the line current distortion at a given average switching frequency in a three-level inverter.

III. ANALYSIS OF CURRENT RIPPLE

As it is widely known, the line current ripple in a PWM inverter-fed motor drive is caused by the instantaneous error between the applied voltage and the reference voltage [33]–[35], [39]–[44]. Fig. 7 shows the error voltage vectors, corresponding to the applied voltage vectors $\mathbf{V_1}$, $\mathbf{V_{13}}$, and $\mathbf{V_7}$ for a reference vector $\mathbf{V_{ref}} = 0.7\ \mathrm{V_{dc}}\angle 10°$. The error voltage vectors can be expressed as

$$\begin{aligned} \boldsymbol{V}_{\mathbf{err},\mathbf{1}} &= \boldsymbol{V}_{\mathbf{1}} - \boldsymbol{V}_{\mathbf{ref}} = \boldsymbol{V}_{\mathbf{1}} - (\boldsymbol{V}_{\boldsymbol{\beta}} + \boldsymbol{V}_{\mathbf{7}}) \\ \boldsymbol{V}_{\mathbf{err},\mathbf{13}} &= \boldsymbol{V}_{\mathbf{13}} - \boldsymbol{V}_{\mathbf{ref}} = \boldsymbol{V}_{\mathbf{13}} - (\boldsymbol{V}_{\boldsymbol{\beta}} + \boldsymbol{V}_{\mathbf{7}}) \\ \boldsymbol{V}_{\mathbf{err},\mathbf{7}} &= \boldsymbol{V}_{\mathbf{7}} - \boldsymbol{V}_{\mathbf{ref}} = -\boldsymbol{V}_{\boldsymbol{\beta}}. \end{aligned} \tag{4}$$

The time integral of the error voltage vector is defined as the "stator flux ripple vector" [38]–[42].

When sequence $(0--, +--, +0-, +00)$, i.e., sequence 0127, is employed, the trajectory of the tip of the stator flux ripple vector $(\boldsymbol{\Psi})$ is triangular, as shown in Fig. 7. The stator flux ripple vector can be resolved along two orthogonal axes. In a two-level inverter, the two orthogonal axes are chosen such that one of them (q-axis) coincides with the reference vector $\mathbf{V_{ref}}$ [38]–[42]. Here, one of the orthogonal axes (x-axis) is aligned with the reference vector $\mathbf{V}_{\boldsymbol{\beta}}$ of the equivalent two-level inverter, as shown in Fig. 7. The y-axis is perpendicular to the x-axis as shown. This choice of axes simplifies calculation and is similar to the q-axis and d-axis in the analysis of PWM for a two-level inverter [38]–[42].

The sides of the triangular trajectory correspond to the three vectors (active vector 1, active vector 2, and zero vector). These are equal to $\mathbf{V_{err,1}}T_1$, $\mathbf{V_{err,2}}T_2$, and $\mathbf{V_{err,Z}}T_Z$. The x-axis components of the three sides are X_1, X_2, and X_Z, respectively, as defined in the following:

$$X_1 = [0.5V_{\rm dc}\cos(\beta) - V_\beta]\,T_1$$

$$X_2 = [0.5V_{\rm dc}\cos(60^\circ - \beta) - V_\beta]\,T_2$$

$$X_Z = -V_\beta T_Z. \tag{5a}$$

The side $\mathrm{V_{err,Z}}T_Z$ has no component along the y-axis. The projection of the other two sides of the triangle on the y-axis is given by Y defined as follows:

$$Y = 0.5V_{\rm dc}\sin(\beta)T_1 = 0.5V_{\rm dc}\sin(60^\circ - \beta)T_2. \tag{5b}$$

The x- and y-axis components of the flux ripple vector are shown in terms of X_1, X_2, X_Z, and Y in Fig. 8(a). The mean square values of ψ_x and ψ_y over the subcycle corresponding to sequence 0127 ($F^2_{x,0127}$ and $F^2_{y,0127}$, respectively) can be computed following the procedure detailed in [24] and [42]. These two quantities can be added up to obtain the mean square value of the total stator flux ripple over the subcycle corresponding to sequence 0127 as shown

$$F^2_{0127} = F^2_{x,0127} + F^2_{y,0127}. \tag{6}$$

Fig. 8(b)–(e) shows the trajectories of the tips of the stator flux ripple vectors, corresponding to sequences 1012, 2721, 0121, and 7212, for the same reference vector shown in Fig. 7. It is seen that the trajectory of the tip of the stator flux ripple vector is "doubly triangular" for these sequences. The corresponding x- and y-axis components are also shown in Fig. 8(b)–(e). The mean square value of the stator flux ripple over a subcycle corresponding to these four sequences $F^2_{\rm SEQ}$ (SEQ = 1012, 2721, 0121, and 7212) can be evaluated in a fashion similar to F^2_{0127}.

The rms value of stator flux ripple over a sector is normalized with respect to the fundamental flux ψ_1 to obtain the total rms harmonic distortion factor based on stator flux ripple $(F_{\rm DIST})$ as defined in

$$F_{\rm DIST} = \frac{1}{\psi_1}\sqrt{\frac{3}{\pi}\int_0^{\pi/3} F^2_{\rm SEQ}\,da}, \qquad \psi_1 = \frac{V_{\rm ref}}{2\pi f_1}. \tag{7}$$

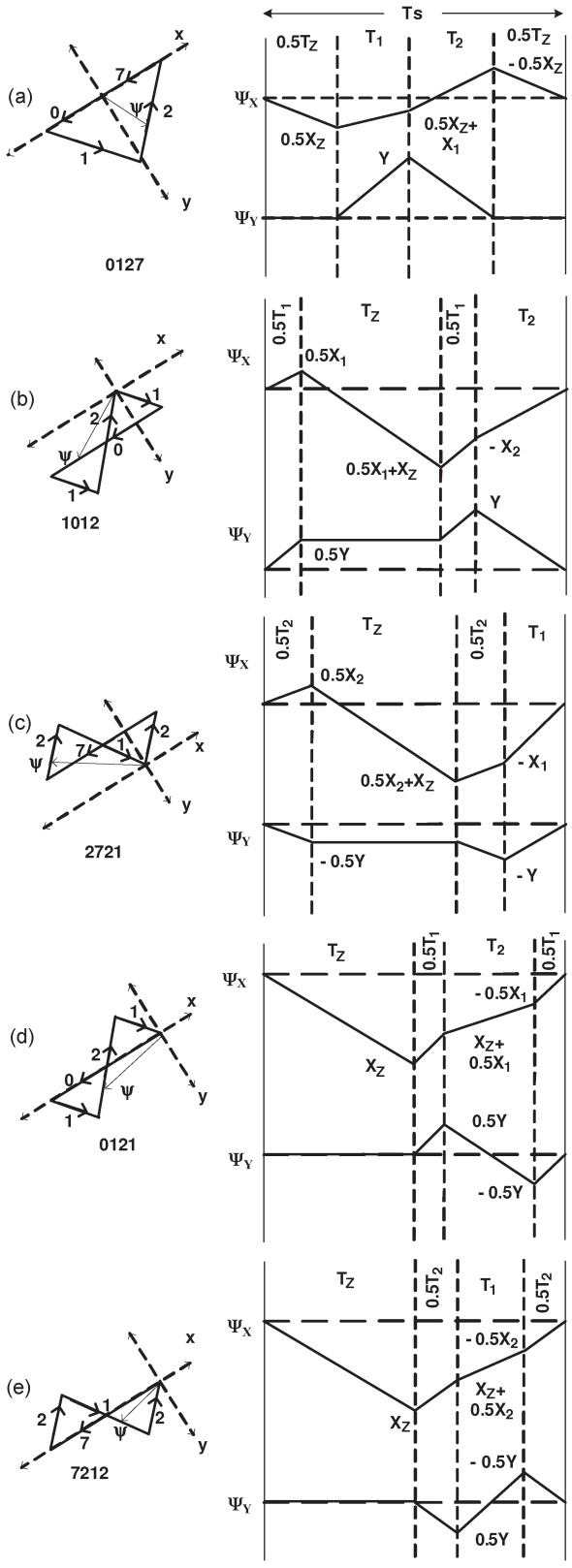

Fig. 8. Stator flux ripple vector over a subcycle corresponding to different sequences for a given reference vector. $\mathbf{V_{ref}} = 0.7\ \mathrm{V_{dc}}\angle 10^\circ$.

The total rms line current ripple can be calculated using the analytically evaluated $F_{\rm DIST}$, which is independent of machine parameters [35], [42]–[44].

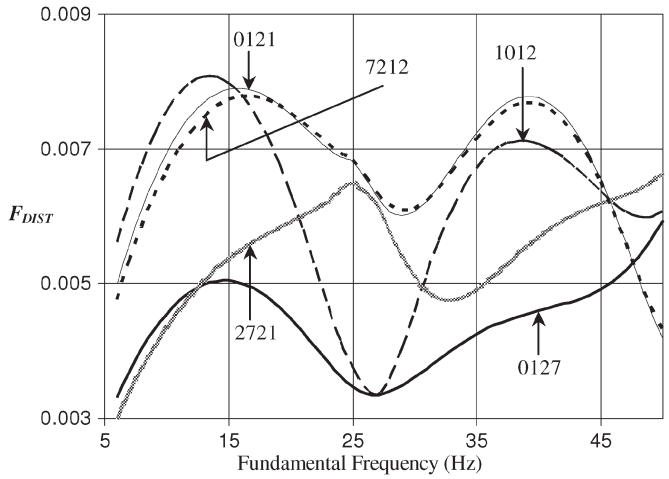

Fig. 9. Analytically evaluated harmonic distortion factor corresponding to the sequences 0127, 1012, 2721, 7212, and 0121.

Fig. 9 shows a theoretical comparison of the harmonic distortion $(F_{\rm DIST})$ pertaining to the five sequences, assuming the voltage to frequency ratio (V/f) to be fixed at its rated value. The figure indicates a significant reduction in current ripple at high frequency range (47.5–50 Hz) due to sequences 0121 and 7212. The percentage improvement in THD in line current due to sequence 7212 is about 25% and that due to sequence 0121 is close to 30% at full modulation index of the linear modulation zone. These two sequences result in comparable distortion in line current throughout the frequency range. It is also observed that sequence 2721 results in lower THD than the conventional sequence 0127 at low frequency range (less than 12 Hz). In the frequency range of 12–47.5 Hz, the conventional sequence 0127 results in the lowest THD. The line current THD due to sequence 1012 is comparable with that due to sequence 0127 over a small frequency range between 26 and 28 Hz.

The analysis in terms of stator flux ripple is validated experimentally by measuring the line current THD at various fundamental frequencies for the different sequences in Section V.

IV. Analysis of Switching Loss

The normalized switching loss $(P_{\rm SW,SEQ})$ pertaining to a given sequence (SEQ) (i.e., ratio of switching loss due to the given sequence to that due to conventional sequence 0127) can be evaluated as

$$P_{\rm SW,SEQ} = \frac{1}{2}\int_{\phi}^{\pi+\phi} n_{\rm ph}\,|\sin(\omega t+\varphi)|\,d(\omega t) \qquad (8)$$

where $n_{\rm ph}$ is the number of switching per phase per subcycle and ϕ is the phase angle between the line-side (ac-side) fundamental voltage and fundamental current [39].

Fig. 10 shows the normalized switching loss corresponding to different sequences over the entire power factor angle at full modulation index $(V_{\rm ref} = 0.866\ {\rm V_{dc}})$. As seen from the figure, the switching loss due to sequence 7212 is the lowest at high power factors (>0.8); the reduction in switching loss is about 35% over sequence 0127 at power factors close to unity. Compared with sequence 0127, sequence 1012 reduces the switching loss at low power factors, while sequences 0121 and 7212 lead to reduced loss at high power factors.

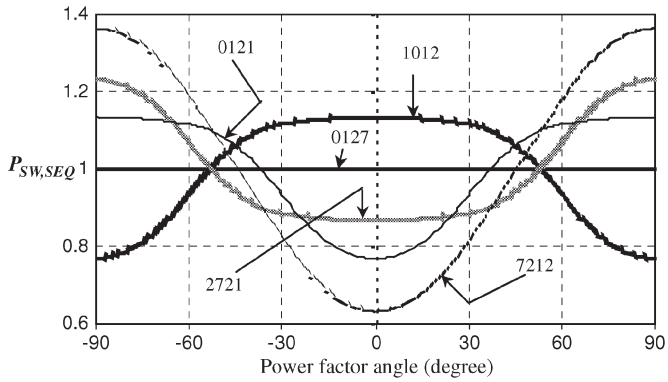

Fig. 10. Analytically evaluated normalized switching loss at $V_{\rm ref} = 0.866$, corresponding to various sequences.

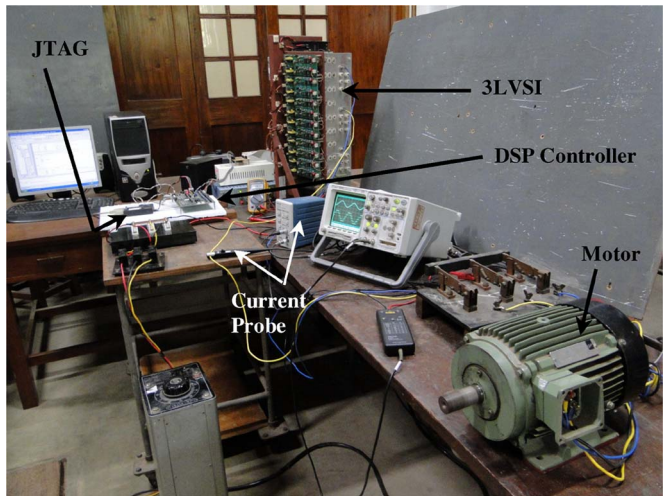

Fig. 11. Experimental setup.

V. Experimental Results

The conventional sequence and the four proposed sequences are evaluated on a 10-kVA IGBT-based inverter-fed 2.2-kW 415-V 50-Hz induction motor drive with constant volts per hertz (V/f) control. The dc bus voltage is 600 V. The PWM techniques are implemented on a TMS320LF2407A DSP controller [45]. A photograph of the experimental setup is shown in Fig. 11.

Fig. 12 shows the harmonic spectrum of the line voltage at a fundamental frequency of 50 Hz and an average switching frequency of 1.5 kHz corresponding to sequence 0127. It is seen that the sidebands are around 1.5 and 3 kHz. The dominant harmonic components are around 1.5 kHz.

Fig. 13–16 show the measured harmonic spectra of line voltage waveforms corresponding to novel sequences 1021, 2721, 7212, and 0121, respectively, at the same fundamental frequency and average switching frequency as those in Fig. 12. In the harmonic spectra corresponding to sequences 1012 and 2721, the dominant harmonic components are around 1.5 kHz. When sequences 7212 and 0121 are considered, there are

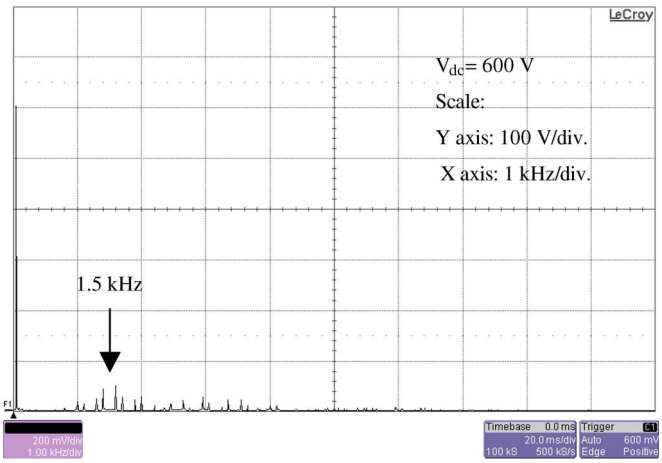

Fig. 12. Measured harmonic spectra of line voltage at 50 Hz with sequence 0127.

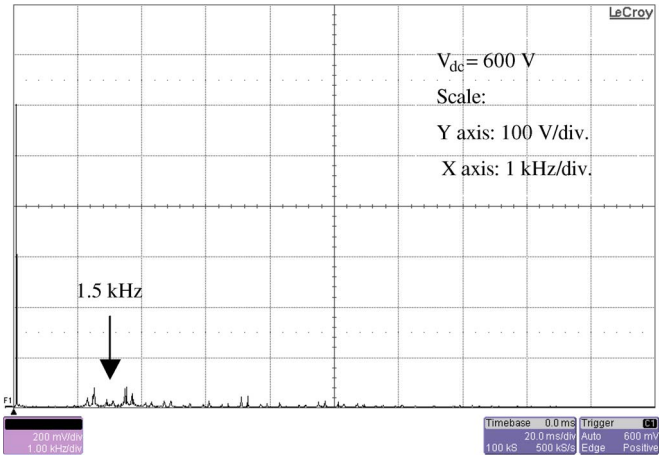

Fig. 13. Measured harmonic spectra of line voltage at 50 Hz with sequence 1012.

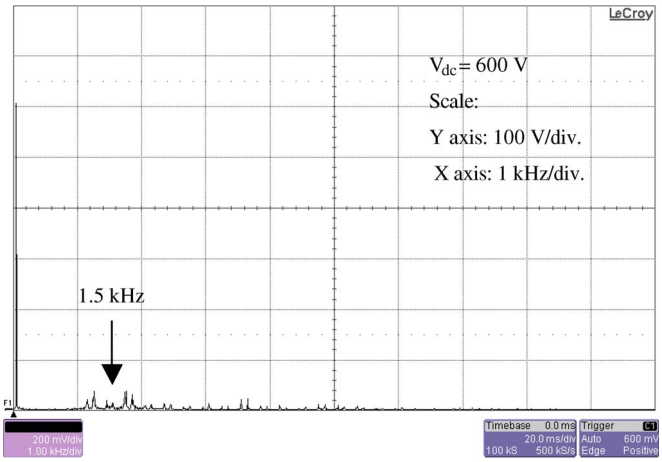

Fig. 14. Measured harmonic spectra of line voltage at 50 Hz with sequence 2721.

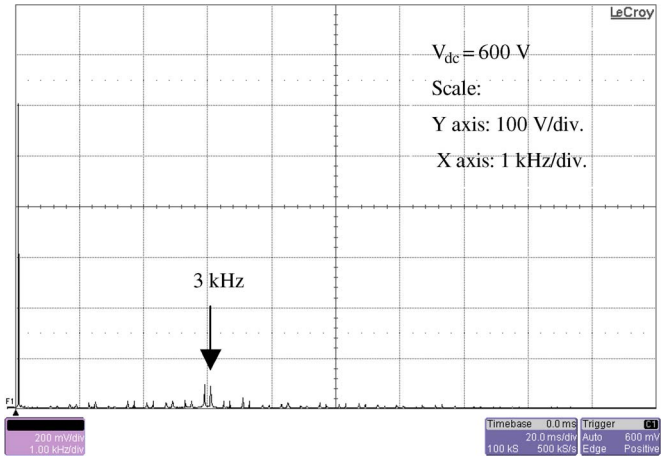

Fig. 15. Measured harmonic spectra of line voltage at 50 Hz with sequence 7212.

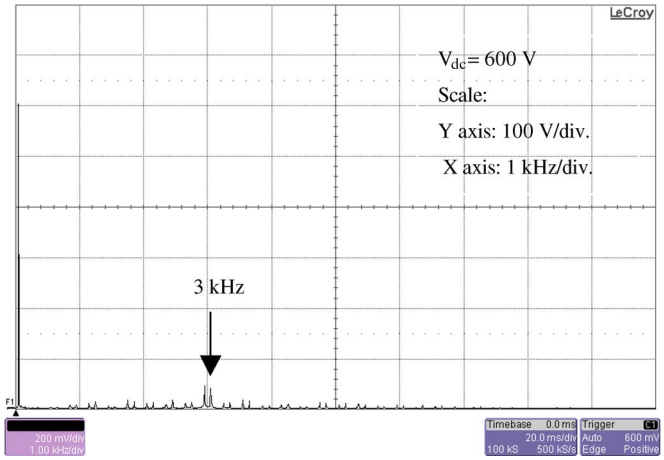

Fig. 16. Measured harmonic spectra of line voltage at 50 Hz with sequence 0121.

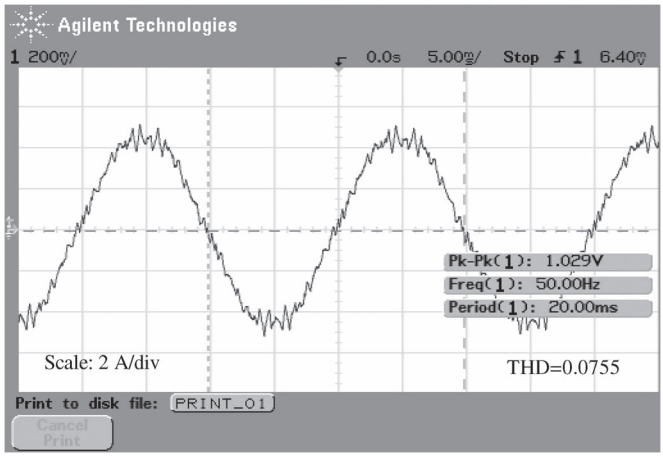

Fig. 17. Measured line current waveform at 50 Hz with sequence 0127.

no significant harmonic components around 1.5 kHz, as seen from Figs. 15 and 16. The dominant harmonic components are around 3 kHz instead. Since the dominant harmonic voltages are at higher frequencies, these are effectively filtered by the motor leakage inductance. Hence, sequences 0121 and 7212 result in lower values of line current THD than the other sequences at $V_{\rm ref} = 0.866\ V_{\rm dc}$ as brought out by the measured line current waveforms, shown in Fig. 17–21.

The THD factor of the no-load current $(I_{\rm THD})$ is defined as

$$I_{\rm THD} = \frac{1}{I_1}\sqrt{\sum_{n\neq 1} I_n^2} \tag{9}$$

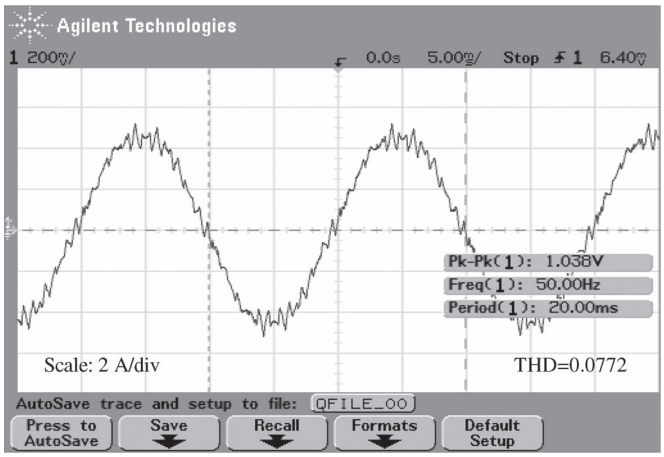

Fig. 18. Measured line current waveform at 50 Hz with sequence 1012.

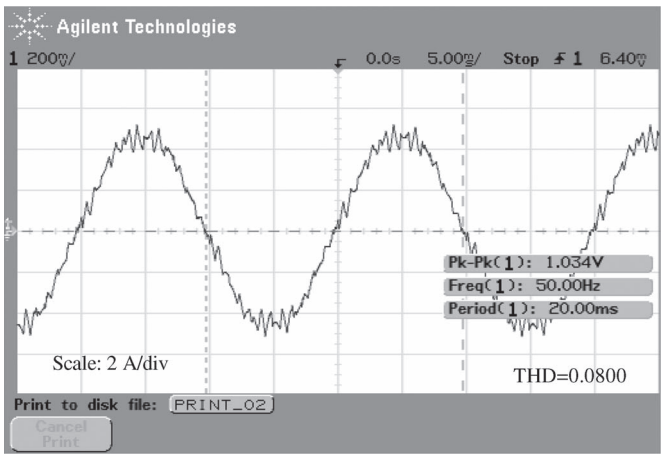

Fig. 19. Measured line current waveform at 50 Hz with sequence 2721.

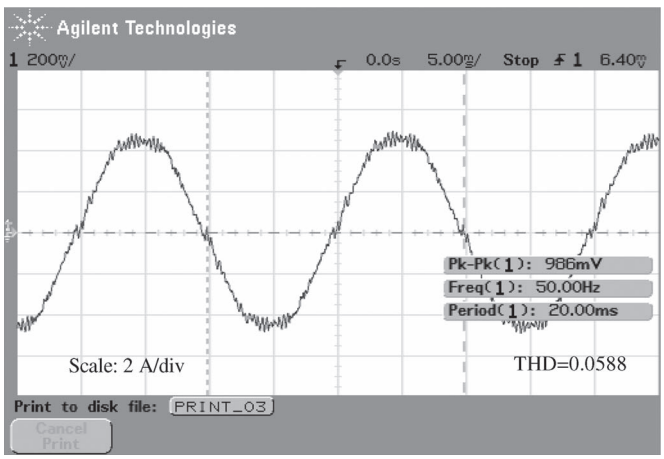

Fig. 20. Measured line current waveform at 50 Hz with sequence 7212.

where I_1 is the rms value of fundamental current at no load and I_n is the rms value of the nth harmonic current [42].

As seen from Fig. 17–21, while the measured $I_{\rm THD}$ values for sequences 1012 (Fig. 18) and 2721 (Fig. 19) are slightly higher than that for sequence 0127 (Fig. 17), those for sequences 7212 (Fig. 20) and 0121 (Fig. 21) are substantially lower than that for sequence 0127. The ripple current varies over the fundamental cycle. The worst-case peak–peak ripple is

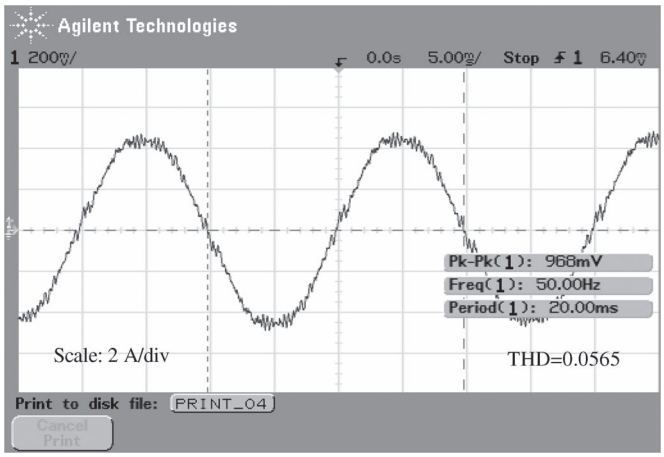

Fig. 21. Measured line current waveform at 50 Hz with sequence 0121.

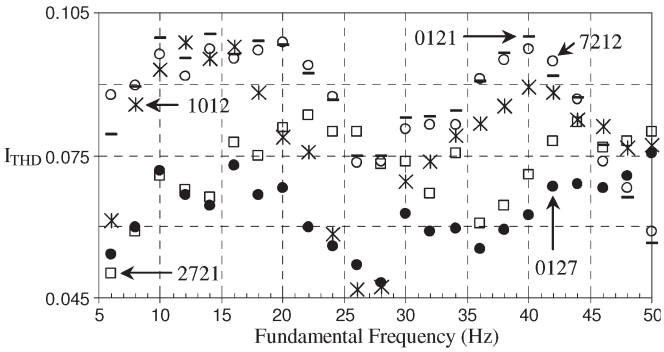

Fig. 22. Measured values of THD in line current corresponding to the five sequences.

observed close to the peak of fundamental current in Fig. 17. Clearly, the peak–peak values of current ripple in Figs. 20 and 21 are much lower than those in Fig. 17–19.

This can be understood from the study of stator flux ripple presented in Section III. It can be seen from Fig. 8 that the y-axis ripple would be more dominant than the x-axis ripple for $V_{\rm ref}$ close to 0.866 $V_{\rm dc}$. Sequences 7212 and 0121 have more transitions between the equivalent active states 1 and 2. These result in a much reduced y-axis ripple as can be seen from Fig. 8(d) and (e). Hence, the rms current ripple is lower with sequences 7212 and 0121 than with sequence 0127 at such high modulation indices. The experimental values of THD factor of the no-load current $(I_{\rm THD})$ due to the switching sequences 0121, 7212, and 0127 validate this. The relative values of measured $I_{\rm THD}$ agree with those of the analytically evaluated $F_{\rm DIST}$.

The measured $I_{\rm THD}$ values corresponding to sequence 0127 at various fundamental frequencies are shown in thick circular dots in Fig. 22. A fifth degree polynomial curve fitting is done on these measured values; this curve is shown in Fig. 23. The experimental $I_{\rm THD}$ curve agrees reasonably well with the corresponding theoretical $F_{\rm DIST}$ curve in Fig. 9. Similarly, the measured $I_{\rm THD}$ values corresponding to other sequences 1012, 2721, 7212, and 0121 are also plotted against fundamental frequency in Fig. 22. Polynomial curve fits are done as before and shown in Fig. 23. One could find the nature of these experimental $I_{\rm THD}$ curves matching reasonably well

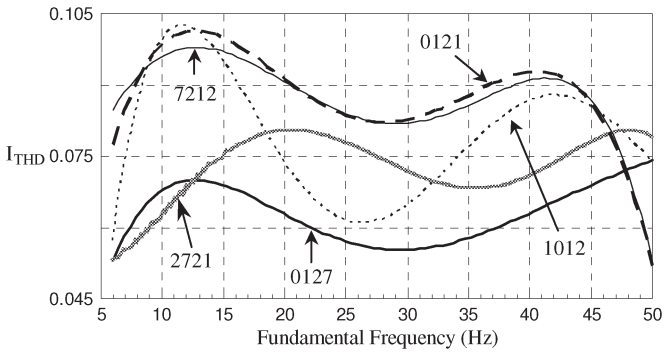

Fig. 23. Curves fitted on measured THD values corresponding to the five sequences.

with the theoretical F_{DIST} curves in Fig. 9. These experimental results confirm that the total rms harmonic distortion in the line current can indeed be analyzed in terms of F_{DIST} theoretically (despite the simplifying assumptions involved in the evaluation of F_{DIST} [42]–[44]). At least, this is valid for the frequency range considered, namely, 10%–100% of the base frequency.

Thus, the analytical as well as experimental results show that sequences 0121 and 7212 lead to substantial reduction in THD close to the base frequency (50 Hz). Also, the sequence 2721 leads to marginal improvement in THD at fundamental frequencies below 12 Hz.

Furthermore, under the experimental conditions, the peak–peak variation in the dc midpoint potential is observed to be around 3 V with the conventional sequence 0127. The corresponding figure is between 3.5 and 4.5 V with the proposed sequences. Thus, there is a marginal increase in the dc neutral voltage shift with the proposed sequences. Further research is required on the effect of these switching sequences on dc voltage unbalance and possible methods for mitigating the unbalance.

VI. Conclusion

Four novel switching sequences for a space-vector-modulated three-level inverter, controlled effectively as a two-level inverter, have been proposed and evaluated. These switching sequences exploit the redundancy in pivot vector and the possibility of multiple application of an inverter state in a subcycle. The maximum line voltage obtainable for a given dc bus voltage with any of these sequences is as high as that of centered space vector modulation.

The harmonic distortion pertaining to the proposed sequences is analyzed based on the notion of stator flux ripple. The proposed sequences are also evaluated experimentally on a 2.2-kW induction motor drive and compared with CSVPWM over a wide range of modulation. The theoretical and experimental investigations demonstrate the superior performance of two of the proposed sequences (0121 and 7212) close to the rated speed of the drive. These sequences reduce the line current THD by 25%–30% at a given average switching frequency at rated speed, compared with the conventional sequence 0127. Also, sequence 2721 yields a marginal reduction in line current distortion at fundamental frequencies less than 12 Hz. Hence, a PWM technique can be proposed where sequence 0121 or 7212 can be employed at fundamental frequencies of 48 Hz and above, conventional sequence (0127) can be used in the fundamental frequency range between 48 and 12 Hz, and sequence 2721 is used below 12 Hz.

A theoretical study on switching loss at full modulation index shows that the sequences 0121 and 7212 reduce the loss at high power factors, sequence 1012 leads to reduced switching loss at low power factors, and sequence 2721 is the best in terms of switching loss at certain intermediate power factors.

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