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Design and Analysis Three Phase Three Level Diode-Clamped Grid Connected Inverter

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Abstract

Abstract — In general, Multi-level converter has been utilized widely in many applications, especially in renewable energy aspects. This is because of the associations in high power, medium switch voltage and lower output total harmonics distortion. In this article, the multi-level converter was constructed as a 2 kW output power of the 3 phase 3 level diode clamped grid connected inverter. The proposed multi-level inverter uses a carrier based space vector pulse width modulation scheme in order to produces the desired output voltage. The scheme is the modulation of three identical reference signals, which is 120° phase shifted to each other comparing to a 10 kHz triangular signal. These reference signals comprise of some harmonics in order to generate a space vector PWM signal for switches in the inverter. A Phase Lock Loop (PLL) is utilized together with the controller in order to phase and frequency locking between the voltage at the point of common connection (PCC) and voltage at the grid system. After the proposed inverter connected to the grid system, it can be injected the inverter current into grid system by using the appropriated PI (proportional-integrator) controller within the control scheme. However, L-C low-pass filter is also utilized at the inverter output for reducing harmonic contents. It results to reducing the output harmonic contents. In which, the value of THDv at PCC is less than 5 %.

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Keywords: Multi-level Inverter, Grid Connected, Phase Lock Loop, NPC

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1. Introduction

Electrical energy that flows from the renewable energy source into the grid system depends on the limitation of the storage systems and efficiency of the inverter. The utilization of the topologies of the grid inverter depends on the type of such renewable energy source [1]. However, the applications of sources in grid system such as photovoltaic, fuel cell or wind turbines are affected in design and operation of that grid network [2]. Multi-level inverters are suitable for high voltage and high power application because of less harmonic spectrum output voltage that results into a better synchronization [7].

In this article, the diode-clamped topology is used in three phase three level grid connected inverter. However, various strategies of modulation techniques and control schemes are implemented in multi-level diode-clamped grid connected inverter system. The SVPWM (space vector PWM) is a popular modulation technique for providing an appropriate output voltage waveform of such multi-level inverters [3]. In order to synchronize the inverter's output to the grid system at PCC, the frequency and phase of PCC voltage are detected by phase lock loop (PLL). The system in this aspect is simulated using MATLAB/Simulink program. The control scheme of the grid connected inverter is shown in Figure 1.

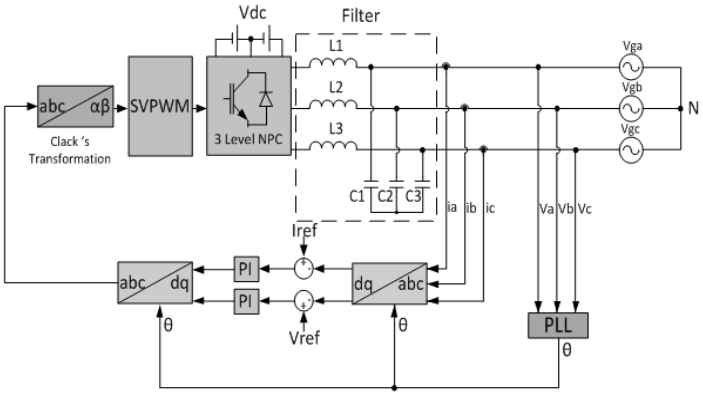

Fig. 1 Control scheme of the grid connected inverter

2. System Descriptions

2.1. Three-Level Diode-Clamped Inverter Topology

The 3 phase 3-level diode-clamped inverter in this paper that shown in Figure 2 came from the neutral point converters (NPC) topology, which was proposed by Nabae, Takahashi, and Akagi in 1981 [2].

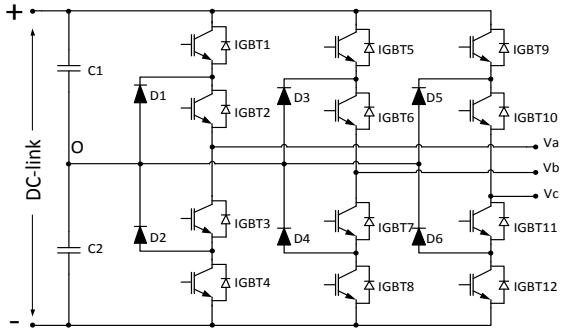

Fig. 2 Three Phase Three Level Diode-Clamped Inverter

From figure 2, each phase of the inverter shared the DC-link supply. At the center of each phase is also connected to the common point of the series capacitors. There are 6 clamped diodes that connected between the center of couple power switches (upper and lower couple sets) in each phase to the common point of the DC-link as seen in Figure 2. It yields to the power switching voltage is limited to VDC/2.

2.2. Control scheme of the system

Figure 1 shows the control scheme of the overall grid connected inverter, which consists of grid synchronization and current control. In the developed system. A carrier-based SVPWM modulation technique [3] is utilized in this aspect in order to provide a appropriate switching pattern for better output sinusoidal voltage waveform. However, this technique is collaborated with the d-q synchronous reference frame control scheme in order to operate the system for grid synchronization and the current control. The algorithm of overall control scheme is as following. When the PLL has detected the frequency and phase from grid system, the phase angle is used to be a reference for the two-phase transformation (abc→dq). These independent parts of signal will be controlled via the PI controller, which are act as current and voltage control, respectively. The controlled signals will be re-transformed into 3 phase control signals (dq → abc), and then transformed to be a proper controlling signals using a Park's transformation. These control signals are suitable to use as a reference signal for the carrier-based SVPWM technique. The reference signal for such technique utilized in this paper is shown in Figure 4.

The relation between 3 phase control signals (abc) to d-q axis and α-β axis can be expresses in the equations as follows. The illustration of a two-axis is shown in Figure 3, it has 6 sections and 8 voltage vectors, each vector runs from (0 0 0) to (1 1 1). Due to voltage vector V_0 and V_7 are at origin and then there are 6 sectors and 6 voltage vectors.

$$\begin{bmatrix} Vd \\ Vq \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \tag{2}$$

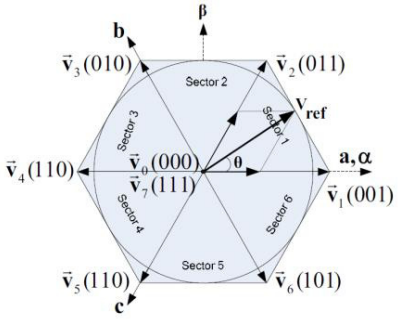

Fig. 3 The illustration of two axis voltage vector

A traditional carrier-based PWM modulation technique is well-known and worldwide in various applications in power electronic areas. Carrier-based SVPWM is one of the implementation of such traditional modulation technique [5]. Carrier-based SVPWM technique has an advantage on its efficient implementation without any sector determination.

The illustrated SVPWM modulation technique in this paper is shown in Figure 5 (all 3 phases). By this technique, the control signals for the 4 power switches (in phase A) are exhibited as shown in Figure 6.

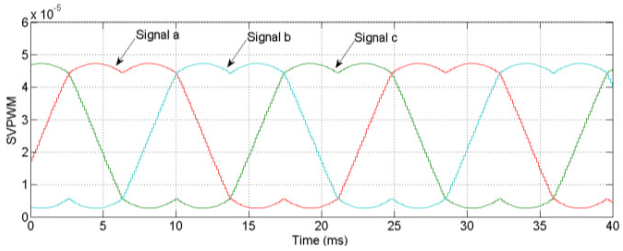

Fig. 4 The reference signals for carrier-based SVPWM

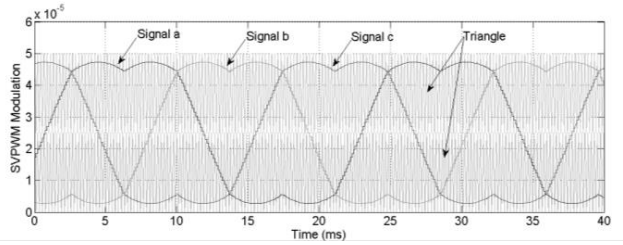

Fig. 5 Modulation technique of carrier-based SVPWM

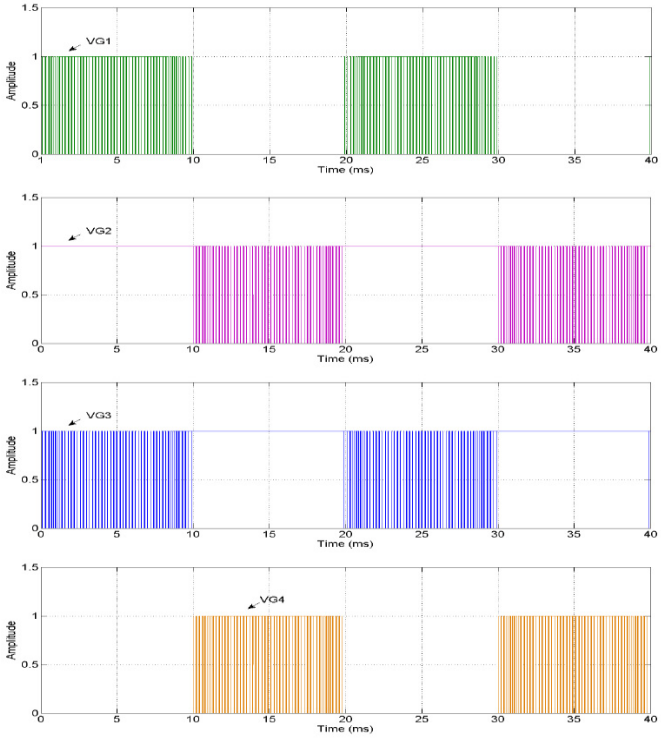

Fig. 6 Example of control signals for phase A (for 4 power switches)

3. Simulation model and results

Simulink model of power circuit of 3 phase 3 level diode-clamped grid connected inverter is shown in Figure 7. The simulation parameters of the proposed system are given in Table 1.

Table 1. Simulation parameters of the proposed system

Parameters	Specification
Output power (Pout)	2 kW
DC-link voltage	600V
Filter inductance (L)	8mH
Filter capacitors (C)	10uF
ESR of Filter capacitor (R)	32Ω
Phase voltage (V)	220V
Frequency of grid system (f)	50Hz
Capacitors at DC-link	4800x2
Switching frequency (f_{sw})	10kHz

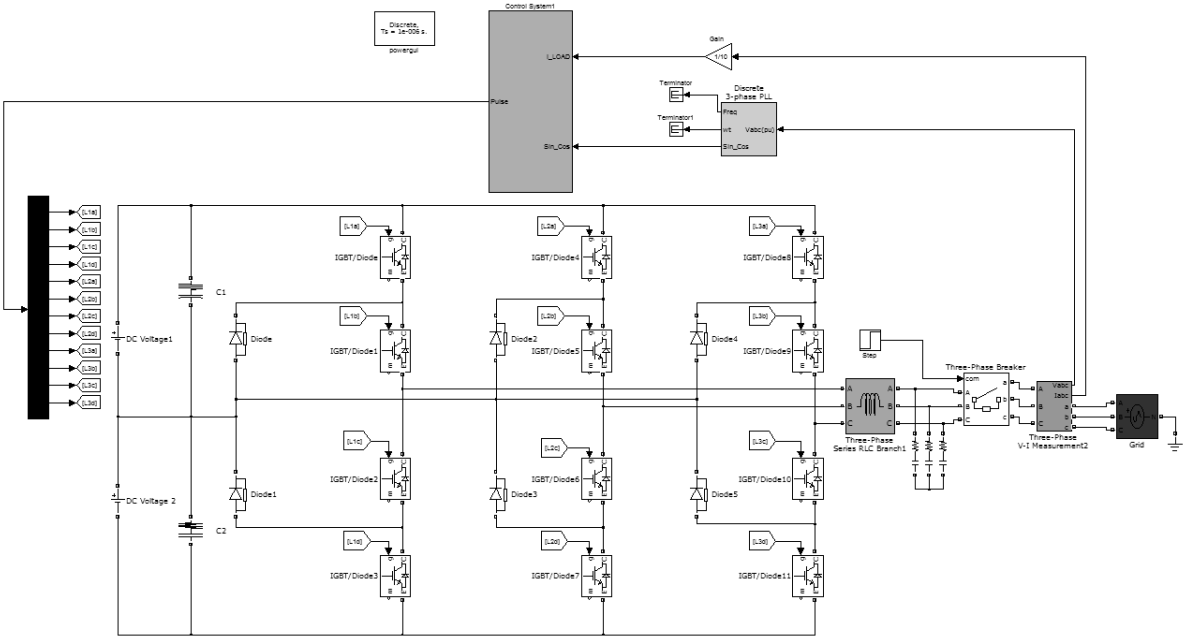

Fig. 7 The Simulink model of the proposed 3 phase 3 level diode clamped grid connected inverter

From the simulation model in Figure 7, the output line voltages from the proposed inverter are shown in Figure 8. These line voltages are un-filtering. After the reducing of high frequency harmonics by passing through the low-pass LC filter, these voltages will be shaved as sinusoidal waveform.

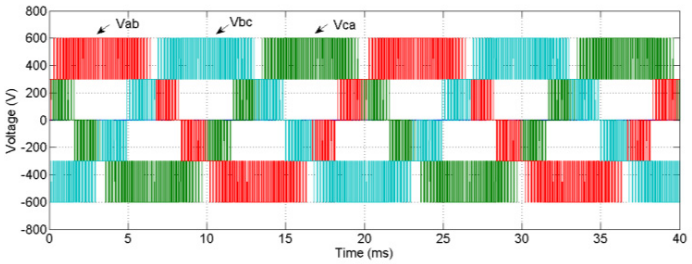

Fig. 8 Output voltage for three phase three level NPC

However, the proposed grid inverter will provides the currents into grid system. From the simulation result, phase current waveforms at PCC that flow from inverter to grid are shown in Figure 9. It can be observed that it has low harmonics distortion. The percentage of harmonic contents is that the comparing to its fundamental frequency content (at 50 Hz). This means that the current waveform and its percentage of harmonics content are shown in Figure 10, respectively. The total harmonic distortion (THD) of the grid current is approximately 2.26%, in which, it is smaller than 5%, which is the recommendation of the IEEE Std. 929-2000 [6].

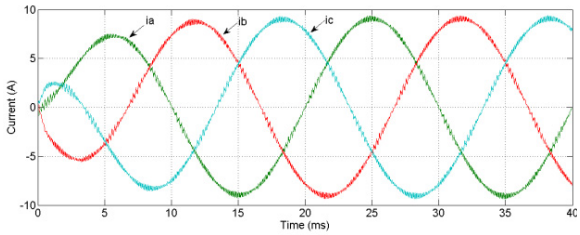

Fig. 9 Currents waveforms from the proposed grid connected inverter

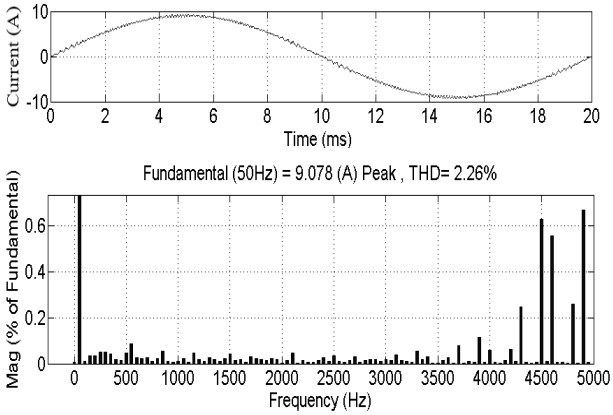

Fig. 10 Total harmonic distortion of grid current (THD

4. Conclusion

In this article, the simulation of the 3 phase 3 level diode-clamped grid connected inverter is done using the MATLAB/Simulink program. The proposed grid inverter has a mandated power rating on 2 kW, 220/380V at PCC and 600 V at DC-link. There are 12 power switches in the 3 phase 3 level diode clamped inverter. The proposed carrier-based SVPWM techniques provides a better performance of voltage and grid current waveform at the PCC. However, L-C filter is also associated to ensures the sinusoidal waveform of both voltage and current. By the adjustment of PI controller in the control scheme, the energy can be transferred from inverter. In which, the THDi of grid current is at 2.26 % within the IEEE Std. 929-2000 limit.

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