A Novel SVPWM Strategy Considering DC-link Balancing for a Multi-level Voltage Source Inverter

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Abstract-**This paper proposes a novel SVPWM (space vector pulse width modulation) strategy for a multi-level voltage source inverter. This strategy is easily implemented as SPWM (sinusoidal pulse width modulation) and has the same DC-link voltage utilization as general SVPWM. The method to keep the voltage balancing of DC-link is also proposed by the analysis of DC-link voltage fluctuation. The usefulness of the proposed SVPWM is verified through the simulation.**

I. INTRODUCTION

To realize high power, high efficiency DC-AC conversion, numerous multi-level inverter topologies such as diode clamped configuration, flying capacitor configuration and H-bridge configuration inverter have been proposed together with suitable control scheme [1]-[3]. The main advantages offered by these inverters can be summarized as follows.

- Achieving higher voltage rating by synthesizing a lot of lower partial DC voltage source.
- Solving voltage-sharing problem of series connected power devices.
- Reducing THD in output voltage waveform.
- Reducing EMI problems by decreasing switching dv/dt stress.

Especially, in the field of high power variable speed application like traction and steel mill system, DCICs (diode clamped inverter configurations) have been widely used. The DCICs were derived from neutral-point-clamped inverter given by Nabae [1]. After that time, DCMLIs (diode clamped multi-level inverter) were developed [4], [5].

As the technique to control the inverter, pulse width modulation is established as a standard of nowadays. Many PWM strategies have been researched and proposed. In these PWMs, the space vector PWM has excellent DC-link voltage utilization and low current ripple. The sine-triangle PWM is widely employed in an application because of easy implementation [6]. Many papers using SVPWM in diode clamped three-level inverter have been published. However, it is very difficult to employ those SVPWMs in DCMLICs because of complex implementation algorithm with 3 or 4 stages [7]. Moreover, DC-link voltage balancing, which is certainly under consideration to realize DCMLIs, adds an extra weight on difficulty in using SVPWM.

We proposed a novel SVPWM strategy for DCMLIs in this paper. It is easily implemented by introducing a new approach that SVPWM is equal to SPWM adding proper DC voltage offset. And, the analysis method of the link potential fluctuation by the reference voltage and phase current in the inverter is described. The DC-link voltage fluctuation can be controlled by this analysis method. The usefulness of the proposed SVPWM is verified through the simulation.

II. PRINCIPLE OF PROPOSED SVPWM

A. Problems of conventional SVPWM

In the SVPWM, generally, the reference voltage vector is realized on average basis by using nearest three vectors in order to minimize the harmonic components of the output line-to-line voltage. The duration of each voltage vector can be calculated by vector calculation [8]. It means that the change of reference voltage vector results in a different vector calculation and the location of the reference voltage vector has to be identified. In DCMLICs, the number of vector calculation equation, generally, is $3(N\text{-}1)^2$. And, these vector calculation equations have the terms of *sin/cos* function. Additionally, the duration of each voltage vector is not real on-off time of power device. Therefore, the duration of each voltage vector has to be converted into the real on-off time of power device [7].

B. Realization of novel SVPWM in two-level inverter

If a reference voltage vector V^* is placed on any region of space voltage presentation, each phase voltages V_{AS}', V_{BS}' and V_{CS}' (defined as "imaginary phase voltage") are derived from reference voltage vector Vd, Vq of the stationary reference frame d-q axis as shown Fig. 1 (a). The imaginary phase voltages are obtained by (1).

$$\begin{bmatrix} V_{AS}' \\ V_{BS}' \\ V_{CS}' \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & +\sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} |V^*|\cos\alpha (= V_q) \\ |V^*|\sin\alpha (= V_d) \end{bmatrix} \quad (1)$$

The imaginary phase voltages have the information of line-to-line voltages being seen by the load. The addition of a DC offset voltage (denoted as "V_{OFFSET}") to each imaginary

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phase voltage does not change this information. So, we can obtain the same reference voltage vector in the space voltage presentation by adding DC offset voltage to each imaginary phase voltage [9].

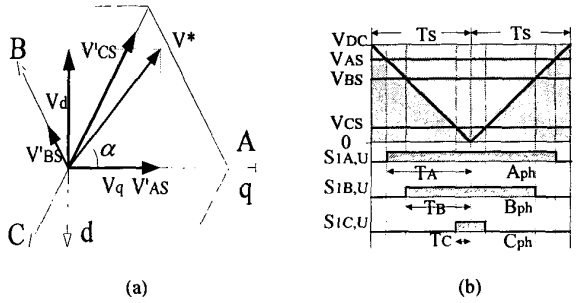


Fig. 1. Definition of imaginary phase voltages (a) and proposed space vector PWM (b) in two-level inverter.

Additionally, if all imaginary phase voltages with addition of a DC offset voltage are located from 0 to DC-link voltage, the instant, when all these imaginary phase voltages change from 0 to DC-link voltage or the contrary, is the same as that of real on-off time of switching devices. If each imaginary phase voltage with addition of a DC offset voltage is defined as effective phase voltage (denoted as "V_{AS}, V_{BS} and V_{CS}"), it can be written as (2).

$$\begin{aligned} V_{AS} &= V'_{AS} + V_{OFFSET} \\ V_{BS} &= V'_{BS} + V_{OFFSET} \\ V_{CS} &= V'_{CS} + V_{OFFSET} \end{aligned} \tag{2}$$

The changing instants of effective phase voltage (denoted as "T_A, T_B and T_C") and DC offset voltage are also expressed as (3) and (4).

$$\begin{aligned} T_A &= \frac{V_{AS}}{V_{DC}} \cdot T_S \\ T_B &= \frac{V_{BS}}{V_{DC}} \cdot T_S \\ T_C &= \frac{V_{CS}}{V_{DC}} \cdot T_S \end{aligned} \tag{3}$$

$$V_{OFFSET} = \frac{1}{2} \cdot (V_{DC} - V_{MAX} - V_{MIN}) \tag{4}$$

where, V_{DC} is DC-link voltage; V_{MAX}, V_{MIN} is a maximum, minimum voltage of imaginary phase voltages;

The addition of DC voltage offset makes imaginary phase voltages to have central value from 0 to V_{DC} as shown Fig. 1 (b). It means that this PWM method generates symmetrical switching pulse pattern and minimizes the ripple of phase currents. Practically, T_A, T_B and T_C can be easily obtained by comparing all effective phase voltages with the triangle waveform which has two times of sampling time Ts, the period of which is as shown Fig. 1 (b). This method is very close to sine-triangle PWM.

C. Realization of novel SVPWM in DCMLIs

In two-level inverter, the method to get effective voltage V_{XS} is that V_{DC} is generated during $V_{XS}/V_{DC} \cdot T_S$ of sampling time T_S and 0 is generated during the rest of sampling time T_S. However, in DCMLIs, the number of inverter phase voltages is N. Therefore, we can utilize many inverter phase voltages.

To explain extension of proposed SVPWM for DCMLIs, three-level inverter is taken as an example. Fig. 2 shows a schematic diagram of a three-level inverter. Each phase of this inverter consists of two clamping diodes, four main power devices and four freewheeling diodes. Table I shows the switching states of three-level inverter. Fig. 3 (a) shows the presentation of the space voltage vector. This space voltage vector consists of six regions. Each region can be divided into four smaller regions 1, 2, 3 and 4. Fig 3 (b) shows the space vector diagram of all switching states.

TABLE I
SWITCHING STATES IN THREE-LEVEL INVERTER (X=A,B,C)

Switching State	$S_{2X,U}$	$S_{1X,U}$	$S_{2X,L}$	$S_{1X,L}$	V_X
2	ON	ON	OFF	OFF	V_{DC}
1	OFF	ON	ON	OFF	$V_{DC}/2$
0	OFF	OFF	ON	ON	*0*

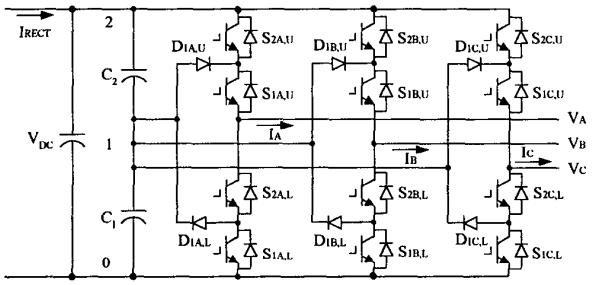


Fig. 2. Schematic diagram of a three-level inverter.

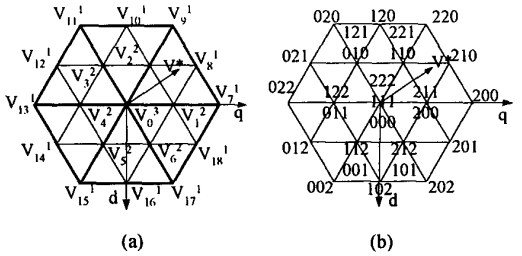


Fig. 3. Voltage vectors (a) and switching states (b) in space vector presentation of three-level inverter.

If a reference voltage vector is placed on the any region of vector space, all the imaginary phase voltages, DC offset voltage and effective phase voltages are obtained by (1), (2) and (4), respectively. To utilize three switching states, the region of DC-link voltage is divide into two parts. It is realized by introducing two triangle waveforms of $V_{DC}/2$ magnitude as shown Fig. 4.

Fig. 4 shows that the phase voltage V_{XS}, which is realized by introducing two triangle waveforms (indicated as solid-line), is equal to those realized by using only one triangle waveform (indicated as dashed-line). Fig. 4 (a) shows that V_{XS} is greater than one half of DC-link voltage ($V_{DC}/2$). Fig. 4 (b) is on the contrary. The symbols presented in Fig. 4 are as follows.

- T_{ON1} : on-time duration when one triangle waveform is used.
- T_{ON2} : on-time duration when two triangle waveforms are used.
- δ : time difference between T_{ON1} and T_{ON2}.

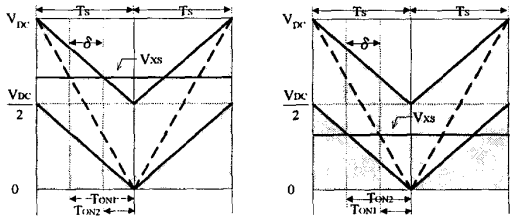


Fig. 4. Realization of phase voltage when $V_{XS}>V_{DC}/2$ (a) and $V_{XS}<V_{DC}/2$ in three-level inverter.

In Fig. 4 (a), T_S - T_{ON1} is equal to δ. The phase voltage V_{XS} is realized by the method that one half of DC-link voltage ($V_{DC}/2$) is generated during the ($2 \cdot \delta$) of sampling time T_S and DC-link voltage (V_{DC}) is generated during the rest time of sampling time ($T_S - 2 \cdot \delta$). On the contrary, in Fig 4 (b), T_{ON1} is equal to δ. Therefore, the phase voltage V_{XS} is realized by the method that zero voltage is generated during (T_S - 2 T_{ON1}) of sampling time and ($V_{DC}/2$) is generated during the rest of sampling time ($2 \cdot T_{ON1}$). The realization of the phase voltage V_{XS} can be represented as:

$$V_{XS} \geq \frac{V_{DC}}{2} \;:\; V_{DC} \cdot \left(\frac{T_{ON}-\delta}{T_S}\right) + \frac{V_{DC}}{2} \cdot \frac{2 \cdot \delta}{T_s}$$
$$V_{XS} \leq \frac{V_{DC}}{2} \;:\; \frac{V_{DC}}{2} \cdot \frac{2 \cdot T_{ON}}{T_s} \qquad (5)$$

The method to obtain real on-off time of power device also is similar to sine-triangle PWM for three-level inverter. The upper triangle waveform determines the real on-off instant of $S_{2X,U}$ (X=A,B,C) and lower triangle waveform determines the real on-off instant of $S_{1X,U}$. The relation of $S_{2X,U}$($S_{1X,U}$) and $S_{2X,L}$($S_{1X,L}$) is complement.

Fig. 5 shows the disposition of effective phase voltage and triangle waveforms in DCMLIs. The number of triangle waveform is N-1. The J-th triangle waveform determine the real on-off instant of $S_{JX,U}$ and $S_{JX,L}$ switching devices. Therefore, the output phase voltage changes from (J-1)$\cdot V_{DC}/(N$-1) to $J \cdot V_{DC}/(N$-1) or from $J \cdot V_{DC}/(N$-1) to (J-1)$\cdot V_{DC}/(N$-1). The direction change is obtained from the rising or falling sloop of the J-th triangle waveform [9].

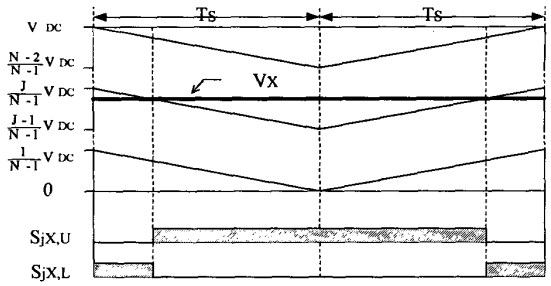


Fig. 5. Proposed space vector PWM in DCMLIs(X=A,B,C).

III. DC-LINK VOLTAGE CONTROL METHOD

A. Approach of DC-link voltage balancing

In DCMLIs, the DC-link voltage is divided by (N-1) capacitors and each capacitor is composed of series connection construction. If voltage unbalancing occurs between each capacitor, the power devices used in DCMLIs do not guarantee safe operation and the line-to-line output voltage waveform has many harmonic components. Therefore, the balancing of DC-link voltage is important function, which determines both the safety and efficiency of DCMLIs.

This unbalancing of DC-link voltage originates from the different charging or discharging time and path of each series-connected capacitor in according to switching state and load condition. If a reference voltage vector is placed on any region of space voltage presentation, the switching state and duration of itself corresponding to magnitude and direction of the reference voltage vector. This switching state makes a specific capacitor charge or discharge according to load condition. Therefore, the voltage of the specific capacitor increases or decreases.

In the standpoint of DC-link voltage balancing, the addition of DC offset voltage with a equal magnitude to each effective phase voltage obtained by (2) can change charging or discharging path and duration on capacitor. Therefore, in the proposed SVPWM, the fluctuation of DC-link voltage can be controlled by addition another DC offset voltage (denoted as "V_{BAL}") to effective phase voltage.

$$V_A = V_{AS} + V_{BAL} = V'_{AS} + V_{OFFSET} + V_{BAL}$$
$$V_B = V_{BS} + V_{BAL} = V'_{BS} + V_{OFFSET} + V_{BAL} \qquad (6)$$
$$V_C = V_{CS} + V_{BAL} = V'_{CS} + V_{OFFSET} + V_{BAL}$$

Fig. 6 shows that correlation between DC offset voltage and charging or discharging duration of capacitor in three-level inverter. In Fig. 6 (a), when DC offset voltage is zero, the switching state (110) results in the charging or discharging path through lower capacitor C_1. The switching

state (*211*) and (*221*) results in the charging or discharging path through upper capacitor C_2. When DC offset voltage is positive, T_{110} (duration of switching state (*110*)) decreases and T_{211}, T_{221} (duration of switching state (*221*), (*221*), respectively) increase as shown Fig. 6 (b). It means that the charging or discharging time of upper capacitor C_2 is longer than that of lower capacitor C_1. In Fig. 6 (c), on the contrary, when DC offset voltage is negative, the charging or discharging duration of lower capacitor C_1 is longer than that of upper capacitor.

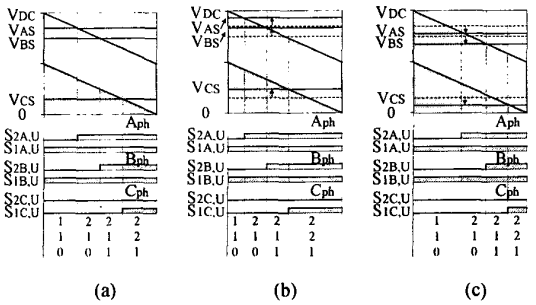


Fig. 6. Approach of DC-link balancing when V_{BAL}=0 (a) and V_{BAL}>0 (b) and V_{BAL}<0 (c) in three-level inverter.

Therefore, if each capacitor voltage and load condition is recognized, DC-link voltage can be balanced by adding or subtracting appreciate DC offset voltage. In this paper, DC offset can be obtained by modeling and analyzing which is suitable for proposed SVPWM as following section. This approach can be extended to DCMLIs.

B. Analysis of link potential fluctuation

To control link potential fluctuation, new analysis method that is suitable for proposed SVPWM is devised. Firstly, in the following analysis, it is assumed that sampling frequency is enough high as compared with fundamental output frequency. Therefore, the phase currents of the three-level inverter can be considered as constant during sampling time. This assumption becomes more reasonable due to inductive load of inverter.

Conceptually, the magnitude of effective phase voltages obtained (2) determines the time to flow the corresponding phase current of three-level inverter from or into each partial DC capacitors. For example, it is assumed that effective phase voltage of inverter arm *A* (denoted as V_A) is one half of overall DC-link voltage (V_{DC}/2) and phase current of inverter arm *A*, (denoted as I_A) flows from neutral points as shown in Fig. 2. The time to flow phase current I_A from capacitor C_1 and capacitor C_2 is one half of sampling time (T_S/2) and zero, respectively. Therefore, the flowing time of each capacitor (denoted as "$T_{C1,VA}$, $T_{C2,VA}$") can be written in terms of eta function (η (x)) as (7).

$$T_{C1C2,V_A} = T_S \, H_{C1C2,V_A} \tag{7}$$

where, $T_{C1C2,V_A} = [T_{C1,V_A} \quad T_{C2,V_A}]^T$;

$H_{C1C2,V_A} = [\eta(t_A) \quad \eta(t_A - 1)]^T$;

$t_A = \frac{2 \cdot V_A}{V_{DC}}$; $\eta(x) = \frac{1}{2}(|x| - |x-1| + 1)$;

If all the capacitance of each partial DC capacitors is *C*, the fluctuation of DC-link voltage caused by the current flowing from each partial dc capacitor during sampling time can be obtained as (8).

$$\Delta I_{C1C2,V_A} = I_A \, T_{C1C2,V_A} \tag{8}$$

where, $\Delta I_{C1C2,V_A} = [\Delta I_{C1,V_A} \quad \Delta I_{C2,V_A}]^T$;

$\Delta V_{C1C2,V_A} = \left(\frac{T_S}{C}\right) \Delta I_{C1C2,V_A}$;

Generally, it is assumed that effective phase voltages is obtained by (2) (denoted as "V_{AS}, V_{BS} and V_{CS}") and three phase currents (I_A, I_B and I_C) corresponding to effective phase voltages which flows from partial DC capacitor to load is as shown Fig. 2. It is also assumed that the load is balanced. The fluctuation of DC-link voltage on the each partial DC capacitors during sampling time can be written by superposition principle as (9).

$$\Delta V_{link,C1C2} = \left(\frac{T_S}{C}\right) H_{C1C2} \, I_{ABC} \tag{9}$$

where, $\Delta V_{link,C1C2} = [\Delta V_{link,C1} \quad \Delta V_{link,C1}]^T$;

$H_{C1C2} = \begin{bmatrix} \eta(t_A) & \eta(t_B) & \eta(t_C) \\ \eta(t_A - 1) & \eta(t_B - 1) & \eta(t_C - 1) \end{bmatrix}$;

$I_{ABC} = [I_A \quad I_B \quad I_C]^T$; $T_{A,B,C} = \frac{2 \cdot V_{A,B,C}}{V_{DC}}$;

The current of passive rectifier flows commonly into all partial DC capacitors to make the overall fluctuation of DC-link voltage zero. Therefore, rectifier current results in the fluctuation of DC-link voltage with the same magnitude on each partial DC capacitor as (10).

$$\Delta V_{rect,C1C2} = -\frac{1}{2} L \, \Delta V_{link,C1C2} \tag{10}$$

where, $\Delta V_{rect,C1C2} = [V_{rect,C1} \quad V_{rect,C2}]^T$; $L = \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$;

The overall fluctuation of DC-link voltage can be obtained as (11) by adding (9) and (10).

$$\Delta V_{C1C2} = \Delta V_{link,C1C2} + \Delta V_{rect,C1C2} \tag{11}$$

where, $\Delta V_{C1C2} = [\Delta V_{C1} \quad \Delta V_{C2}]^T$;

Knowing three phase currents I_A, I_B and I_C and effective phase voltages V_A, V_B and V_C, the overall fluctuation of DC-link voltage can be estimated by (12).

$$\begin{bmatrix}\Delta V_{C1}\\ \Delta V_{C2}\end{bmatrix}=\left(\frac{T_S^2}{C}\right)\begin{bmatrix}1/2 & 1\\ 1 & 1/2\end{bmatrix}\begin{bmatrix}\eta(t_A) & \eta(t_B) & \eta(t_B)\\ \eta(t_A-1) & \eta(t_B-1) & \eta(t_B-1)\end{bmatrix}\begin{bmatrix}I_A\\ I_B\\ I_C\end{bmatrix} \quad (12)$$

C. Realization of DC-link voltage control method

As mentioned above, in proposed space vector PWM, the addition of optimal voltage offset with a equal magnitude to each effective phase voltages obtained by (2) changes the path and duration to flow the phase currents from or into each partial DC capacitor. The best optimal voltage offset is the value to make the overall fluctuation of DC-link voltage estimated by (12) zero during sampling time of reference voltage vector. However, it needs difficult and complex process that mathematical optimal voltage offset is obtained through algebraically solving (12) due to eta function. Though mathematical optimal voltage offset can be obtained, it doesn't always valid. For example, sometimes, the summation value of voltage offset and effective phase voltages is not located from 0 to overall DC-link voltage. Therefore, this approach is not suitable for real implementation.

As alternative approach, the method that optimal voltage offset for only one of the two partial DC capacitors is chosen among prefixed voltage offset is devised. In this paper, only three prefixed voltage offsets, which are 0, $-(V_{DC}-V_{MAX})$ and $(V_{DC}-V_{MAX})$, are used for simplicity of calculation, where, V_{DC} is overall DC-link voltage; V_{MAX} is a maximum voltage of three phase reference voltages. Because each of these prefixed voltage offset makes fully different path and time to flow the phase current from or into each partial DC capacitors, they have enough influence to control DC-link voltage and they are valid to summation with effective phase voltages. In order to choose optimal voltage offset, we should know which is maximum capacitor voltage among two partial DC capacitor voltages. It seems to be desirable to guarantee the safe operating of power devices.

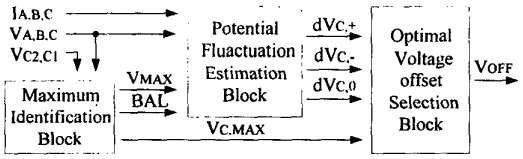


Fig. 7. Schematic diagram of proposed dc link voltage control.

Fig. 7 shows the schematic diagram of proposed DC-link voltage control method. The maximum effective phase voltage and maximum partial capacitor voltage are identified in maximum identification block. The maximum effective phase voltage is used to make prefixed voltage offsets and the maximum partial capacitor voltage is used to choose optimal voltage offset. The fluctuations of DC-link voltage according to each of prefixed voltage offsets can be estimated by (12) in the potential fluctuation estimation block. If the differences between each of two capacitor voltage and $V_{DC}/2$ are all less than a prefixed value, *BAL* signal is false. Then, optimal voltage offset becomes zero. Otherwise, optimal voltage offset, which makes the maximum fluctuation of partial DC capacitor suppressed, is selected in the optimal voltage offset selection block.

IV. Simulation Results

To verify the validity of the proposed SVPWM and control method of DC-link voltage, some simulations is archived by MATLAB/Simulink. Table II shows simulation condition. To certify the proposed method to keep the balancing of dc link voltage, unbalancing of DC-link voltage is made by charging lower capacitor C_1 with 4000A current at 1 second.

TABLE II
SIMULATION CONDITION.

Inverter	Ts	500[us]	C_{DC}	4000uF
Motor	Lr	0.0547[H]	Rr	0.2[Ω]
	Ls	0.0547[H]	Rs	1.26[Ω]
	Lm	0.05[H]	Jm	0.017 [kg ·m²]
	Power	3.7[kW]		
Computer System	CPU	P-166	Running Time	15[min]
	RAM	64MB		
Reference Speed [S]	0.0-0.5	0[rpm]	0.5-1.5	1500[rpm]
	1.5-2.0	-1500[rpm]	2.0-2.7	750[rpm]

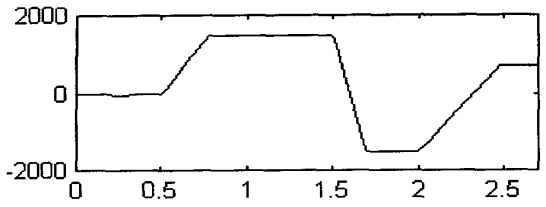
Fig. 8 and Fig. 9 show simulation results of the proposed SVPWM. Fig. 8 (a), (b), (c) and (d) present the steady-state waveforms of motor speed, phase current, line-to-line voltage and DC-link capacitor voltage in the three-level inverter respectively. By using the proposed method to keep the balancing of DC-link voltage, DC-link voltage keeps the balancing when the motor is accelerated or decelerated. Moreover, in spite of charging lower capacitor C_1 with 4000A current, voltage balancing is well adjusted. Fig. 9 (a) and (b) show the extended line-to-line voltage waveforms of two-level and three-level.

V. Conclusion

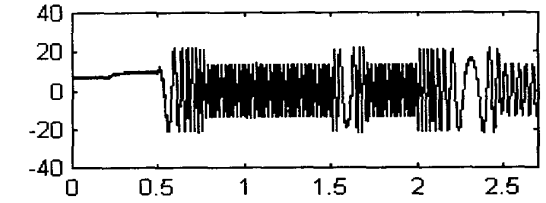
We proposed a novel SVPWM strategy considering DC-link voltage balancing for a diode clamped multi-level inverters in this paper. Because of using only absolute function and min-max sorting algorithm without sinusoidal function, they are easily implemented for digital controller. It is similar to SPWM and has the same DC-link voltage utilization as conventional SVPWM. In proposed PWM, the influence of the reference voltage and phase current about the fluctuation of DC-link voltage is analyzed. By this analysis, the method to keep the voltage balancing of series-connected dc partial capacitor is proposed.

The usefulness of the proposed SVPWM and DC-link voltage balancing method is verified through the simulation. They are suitable for a large capacity diode clamped multi-level inverter applied to variable speed drive of induction motor.

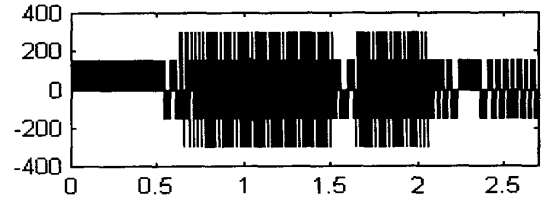
Theoretically, the proposed SVPWM and DC-link balancing method can be extended to DCMLIs. However, DCMLIs with more than four-level has another inherent problem of DC-link voltage balancing. When a modulation index is high, the voltage fluctuation of inner capacitors can not be controlled. Therefore, the method to solve it will have to be devised. In DCMLIs, if the modulation index is limited to low depth, the proposed PWM strategy and DC-link voltage balancing method will be able to be available.



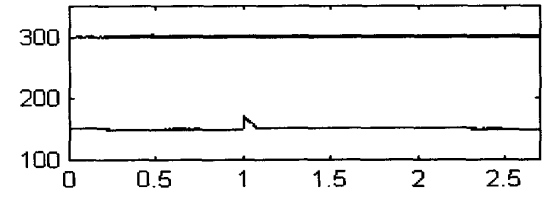
(a) Motor speed



(b) Phase current

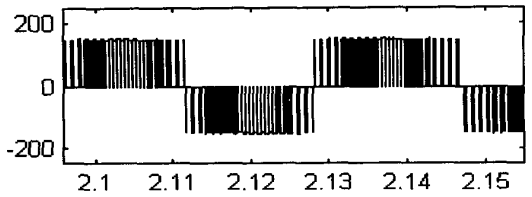


(c) Line-to-line voltage

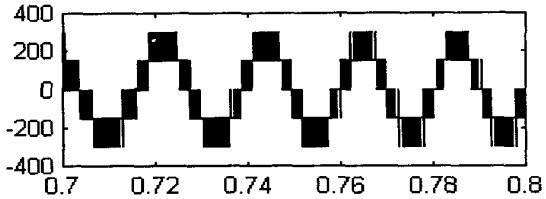


(d) DC-link capacitor bank voltage

Fig. 8. Simulated waveforms in three-level inverter.



(a) Line-to-line voltage in two-level region.



(b) Line-to-line voltage in three-level region.

Fig. 9. Extended line-to-line voltage in three-level inverter.

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