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Simulation Analysis of Three Level Diode Clamped Multilevel Inverter Fed PMSM Drive Using Carrier Based Space Vector Pulse Width Modulation (CB-SVPWM)

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Abstract

This paper proposes implementation of Three Level Diode-Clamped Multilevel inverter using IGBT's fed PMSM drive. The pulses for the inverters have been developed by using Carrier based Space Vector Pulse Width Modulation Technique (CB-SVPWM). Carrier based Space Vector Pulse Width Modulation Technique is most prominent PWM technique for three phase voltage source inverters for the control of Permanent Magnet Synchronous Motors. The output voltages, currents, torque & speed characteristics have studied for three-level inverters fed PMSM drive. It has observed three -level inverter with Carrier based Space Vector Pulse Width Modulation Technique (CB-SVPWM) can use more DC link voltage as compare to Space Vector Pulse Width Modulation Technique (SVPWM). and also CB-SVPWM Technique utilizes DC bus voltage more efficiently and generates less harmonics.

Peer-review under responsibility of the Organizing Committee of ICCCV 2016

Keywords: Permanent magnet synchronous motor (PMSM); diode clamped multilevel inverter(DCML); space vector pulse width modulation (SVPWM); carrier-based space vector pulse width modulation (CBSVPWM).

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1. Introduction

The most attractive applications of the Multilevel power conversion technology are in the medium- to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications. In general, multilevel power converters can be viewed as voltage synthesizers, in which the high

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output voltage is synthesized from many discrete smaller voltage levels. The selection of the best topology of multilevel inverter and the best control method for each given application are unspecified and is subject to different engineering tradeoffs. By concentrating on the DC/AC multilevel inverter power conversion technologies that do not require power regeneration, several attractive topological, modulation and power semiconductor device choices present themselves [1]-[4].

The highly developed multilevel inverter topologies are

- Diode Clamped
- Flying Capacitor
- Cascade Full Bridge

The Modulation strategies are classified as Fundamental Frequency Switching

- Pulse Width Modulation
- Sinusoidal Pulse Width Modulation (SPWM)
- Space Vector Pulse Width Modulation (SVPWM)
- Carrier Based Space Vector Pulse Width Modulation (CB-SVPWM)

In low power and low voltage drive applications ,the two-level inverter configuration has attracted attention where as in high power high performances voltage drive applications ,three-level inverter configuration has attracted more attention as compared to two-level inverter configuration . The objective of these two-level and three-level inverter configuration is to provide a three phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. The two-level inverter is consists of only one switching cell per phase but the three-level inverter has two switching cell per phase. Three level DCMLI is most favorable among the various multi level configuration. Using enough levels the multi-level inverter generates approximately a sinusoidal voltage waveform with very low harmonic distortion [2]-[6]. With the availability of high speed power semi conductor devices the harmonic contents of output voltage can be minimized or reduced significantly by switching techniques like Carrier Based space vector pulse width modulation (CB-SVPWM). Compared to the conventional SVPWM this method is simpler and avoids complex trigonometric calculations.

In this paper the analysis of three-level diode clamped multilevel inverters has simulated using IGBT's , pulses for the switches has simulated using CB-SVPWM technique and the output of these inverters are fed to Permanent Magnet Synchronous Motor. A Torque & Speed characteristic of PMSM has been studied [4].

2. Diode clamped multilevel inverter configuration

This circuit converts the available ac line voltage into required dc voltage for the Three level Diode clamped Inverter. It uses four diode D_1, D_2, D_3 and D_4 in bridge configuration as shown in fig.1 Diode bridge converts ac to dc. This dc voltage is not pure dc voltage but contains ac ripples in it. So capacitor is connected across the output of the bridge rectifier which filters out ac contained in the dc and gives almost pure dc voltage. Figure 1 shows the Power circuit of three level diode clamped inverter (DCMLI)

fed PMSM drive, where only one DC source Vd is needed. Two capacitors are used to split the DC voltage and provide a neutral point N. The inverter leg A is composed of four active switches Sa1, Sa2, Sa3 and Sa4 with two anti-parallel diodes D1 to D4.The switches are employed with 12 IGBT's .Switching states for three-level inverter are shown in Table I. For one leg operation of phase-A for a three-level diode clamped inverter, to have a output voltage of Vdc/2 the switches Sa1, Sa2 should conduct and to have –Vdc/2 voltage, the switches Sa3. Sa4 should conduct and to have output voltage as zero the switches Sa2, Sa3 should conduct. For each voltage level two switches should conduct at a time. The maximum output voltage in the output is half of the DC source.

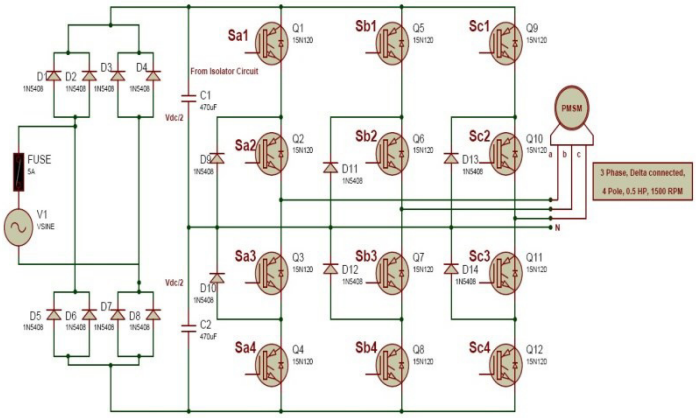

Fig. 1 Power circuit of three level diode clamped inverter (DCMLI) fed PMSM drive

Table 1. Switching sequences for three-level diode clamped inverter

Sector	Voltage Vector	Switching State											
		Sa1	Sa2	Sa3	Sa4	Sb1	Sb2	Sb3	Sb4	Sc1	Sc2	Sc3	Sc4
1	V1	1	1	0	0	0	0	1	1	0	0	1	1
2	V2	1	1	0	0	0	1	1	0	0	0	1	1
3	V3	1	1	0	0	1	1	0	0	0	0	1	1
4	V4	0	1	1	0	1	1	0	0	0	0	1	1
5	V5	0	0	1	1	1	1	0	0	0	0	1	1
6	V6	0	0	1	1	1	1	0	0	0	1	1	0
7	V7	0	0	1	1	1	1	0	0	1	1	0	0
8	V8	0	0	1	1	0	1	1	0	1	1	0	0
9	V9	0	0	1	1	0	0	1	1	1	1	0	0
10	V10	0	1	1	0	0	0	1	1	1	1	0	0
11	V11	1	1	0	0	0	0	1	1	1	1	0	0
12	V12	1	1	0	0	0	0	1	1	0	1	1	0

3. CB-SVPWM configuration for three-level inverter

Carrier based SVPWM allow fast and efficient implementation of SVPWM without sector determination. The technique is based on the duty ratio profiles that SVPWM exhibits By comparing the duty ratio profile with a higher frequency triangular carrier the pulses can be generated, based on the same arguments as the sinusoidal pulse width modulation.

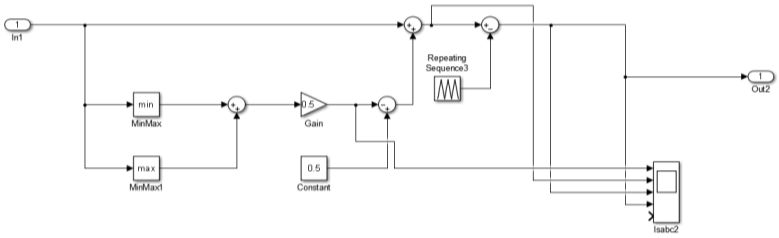

Fig.2.Block diagram of CBSVPWM

4. Mathematical model of PMSM

The mathematical model of a Permanent magnet synchronous motor is identical to that of cylindrical rotor synchronous motor. The rotor of synchronous motor is replaced with high resistivity PM material. Hence, induced current in the rotor are nearly equal to zero. The permanent magnets on the rotor are shaped in such a way as to produce sinusoidal back EMF in stator windings.

The PMSM model equations are:

$V_d = RI_d + L_d(dI_d/dt) - P\omega L_q I_q$ *(1)*
$V_q = RI_q + L_q(dI_q/dt) + P\omega L_d I_d + P\omega\lambda_f$ *(2)*
$T_e = T_L + B\omega + J_m(d\omega/dt)$ *(3)*
$T_e = K_t I_q + (3/2)P\,(L_d - L_q) I_d I_q$ *(4)*
For SMPM, the direct & quadrature components of the inductances are the same.
Hence $Te = K_t I_q$ *(5)*
$K_t = (3/2)P\,\lambda_f$ *(6)*

From the above equation (5) the torque producing current is along the quadrature-axis. To reach maximum efficiency, the torque per ampere relationship should be maximum. This can be easily obtained by keeping the direct-axis current to zero at all times.
Where
R is the stator resistance. ,V_{d-} direct axis voltage.,Vq- quadrature-axis voltage.,,I_{d-} direct axis current. ,I_{q-} quadrature-axis current.,,L_{d--} direct axis inductance, L_q - quadrature-axis. Inductance.,ω - rotor rotational speed ,λf- permanent magnet flux. ,T_{e-} electromagnetic torque.

5. Simulation results and analysis

The simulation of three level diode clamped IGBT inverter fed PMSM electrical drive system is investigated. Two modulation techniques have been applied to the three level diode clamped IGBT inverter. The system used was investigated for steady state. The output waveforms of SVPWM and CBSVPWM are shown in fig.5 to fig.9.The THD analysis of line voltage current of three level diode clamped inverter (DCMLI) using SVPWM& CB-SVPWM.are shown in fig.10 & fig.11.

The parameters used in this simulation are shown in below:

Ld=0.006365; Lq=0.006365; R=1.6; PM_flux=0.1852; P=2; F=0.00005396; J=0.0001854

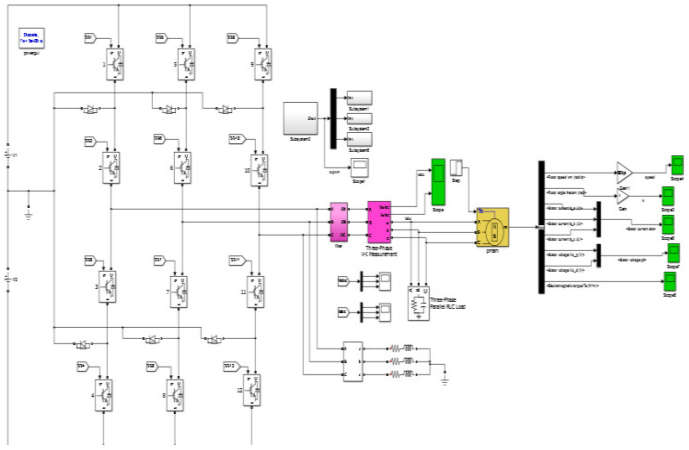

Fig.3. Simulation model of three level diode clamped inverter (DCMLI) fed PMSM drive with SVPWM.

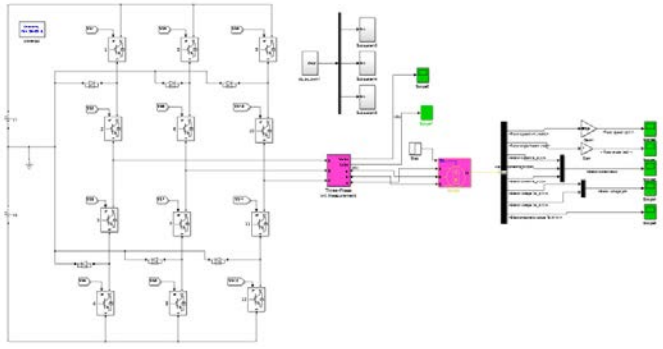

Fig.4. Simulation model of three level diode clamped inverter (DCMLI) fed PMSM drive with CB-SVPWM.

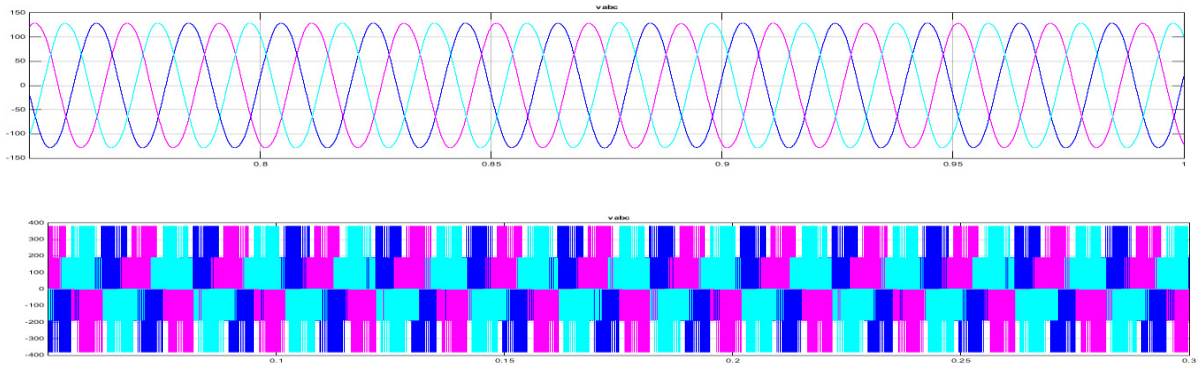

Fig.5. Output line voltage of three level diode clamped inverter (DCMLI) (a) SVPWM,(b)CB-SVPWM.

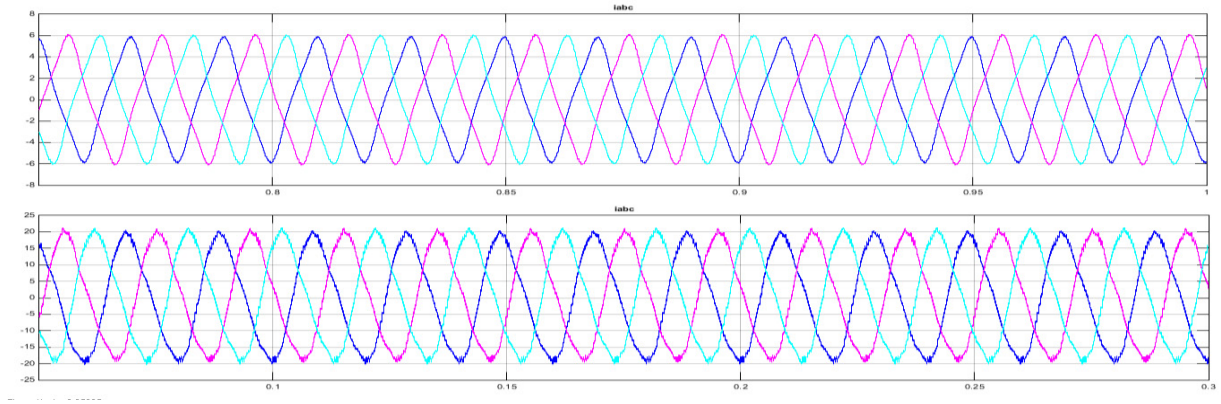

Fig.6. Output line current of three level diode clamped inverter (DCMLI) (a) SVPWM,(b)CB-SVPWM.

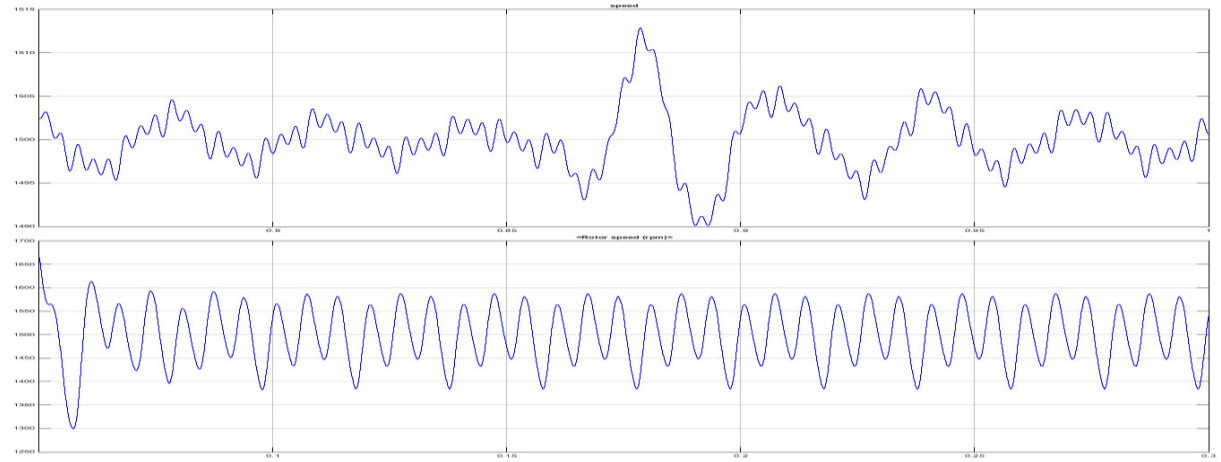

Fig.7 Output Speed of a three level diode clamped inverter (DCMLI) fed PMSM drive. (a) SVPWM,(b)CB-SVPWM.

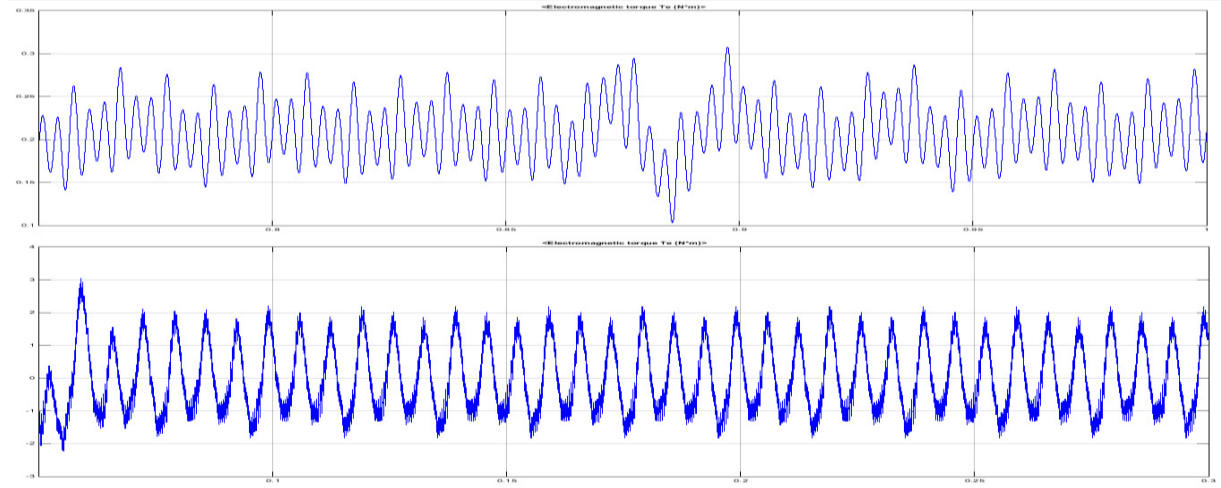

Fig.8 Output Torque of a three level diode clamped inverter (DCMLI) fed PMSM drive. (a) SVPWM,(b)CB-SVPWM.

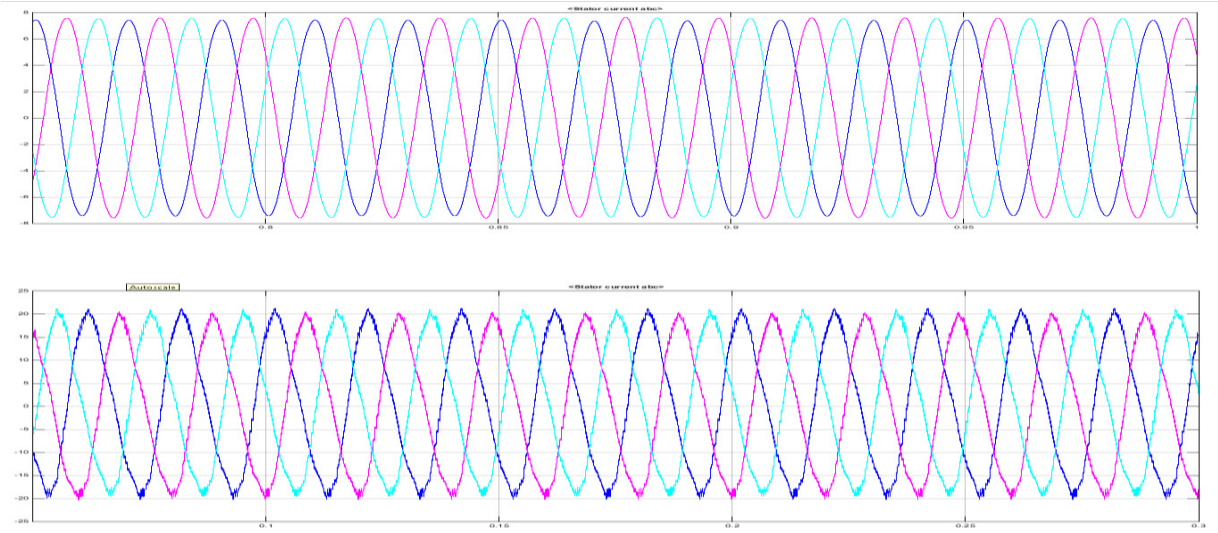

Fig.9. Three phase Stator current of three level diode clamped inverter (DCMLI) fed PMSM drive (a) SVPWM,(b)CB-SVPWM.

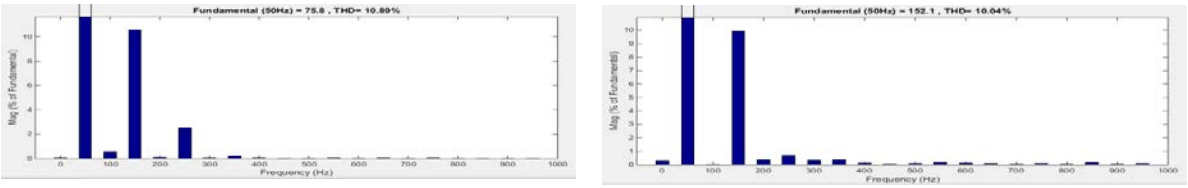

Fig .10.Determination of THD of line voltage of three level diode clamped inverter (DCMLI) (a) SVPWM,(b)CB-SVPWM.

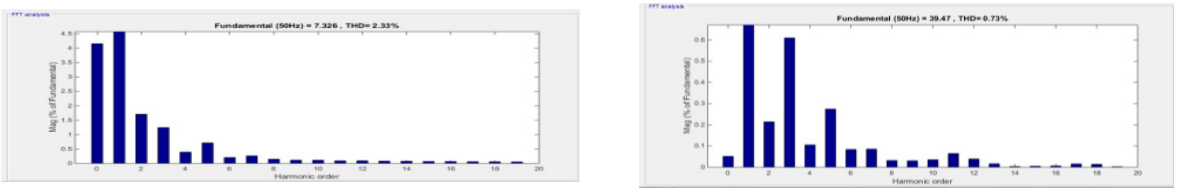

Fig .11.Determination of THD of line current of three level diode clamped inverter (DCMLI) (a) SVPWM,(b)CB-SVPWM.

Table3 Comparison of THD for voltage and currents using, SVPWM, CB-SVPWM.

THD	SVPWM	CB-SVPWM
Line Voltage	10.89%	10.04%
Line Current	2.33%	0.73%

7. Conclusion

In this paper, the simulation model of three-level diode clamped inverter fed PMSM drive using two different modulation techniques has studied. The output voltage, current of the inverter and the speed, torque and the

three-phase currents of the PMSM for SVPWM and CB-SVPWM have plotted. From the analysis we can conclude that the CBSVPWM is similar to SVPWM but much simple, easy and the fastest method without much mathematical calculations like angle and sector determination as in SVPWM. This method can be easily extended to n-level inverter. THD of voltage and current also reduces which is shown in table3.

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