Multilevel Grid-Connected Inverter Performance Under Different Modulation Strategies

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***Abstract*--In the distributed generation system, DC-DC converters and inverters are used between different sources and the loads. These inverter operation influences the power quality, stability and reliability of a given electrical network. The improvement in the performance can be achieved by using 'Multilevel Inverters' in place of conventional two level inverters. In this paper, 3-level and 5-level inverters topologies are compared under different modulation strategies with two-level inverters. When inverters are connected across the DC link to convert suitable energy available from different sources in to the grid, it is essential to utilize the DC bus to its maximum. The performance indices like THD, DC bus utilization and efficiency of an inverter solely depends on its modulation strategies. This paper also investigates the different carrier based modulation techniques used for the multilevel inverters. The inverter losses can be minimized to make more efficient energy conversion by proper implementation of these control strategies.**

***Index Terms*—Space vector pulse width modulation, pulse width modulation inverters, total harmonic distortion.**

I. Introduction

THE inherent advantages of the Multi-level inverters are already reported [1]-[2]. These inverters are having distinct advantage when interfaced with the grid. The interfaced system is shown in the figure 1. In distributed generation, the interface of DC bus to ac side requires high performance indices like lower THD and no harmonic injection within the power quality norms [5]. The conventional SPWM (Sinusoidal Pulse Width Modulation) with the in phase disposition (PD) carriers are used for the Multilevel Inverters [4]. This can be further improved to get 15.5% more DC bus utilization by using SVPWM (Space Vector Pulse Width Modulation) [5] and THIPWM (Third Harmonic Injection Pulse Width Modulation) [5][14]. The waveform quality and the harmonic content are the major issues with attainable rms output voltage. The proposed DPWM1 (Discontinuous Pulse Width Modulation) has capability to get more rms voltage and also the minimization of the inverter loss. This modulation strategy is proposed for the three level and five-level inverters. The performances of these inverters are compared with the two level inverters. This simulation work is carried out with actual device model using PSIM 0.9 software.

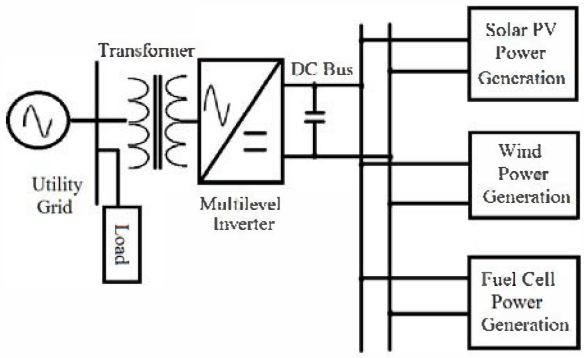

Fig.1. A Schematic diagram showing the distributed generation and its connection to grid through multilevel inverter.

Diode clamped multilevel inverter topology is used for the simulation. Advantages of diode clamped topology are already reported [1]. Generalized theory of multilevel inverters up to m-level is explained in [2], different topologies are discussed in [6]. If we go for higher levels THD is lower but the number of switches are more, control is complex and conduction losses also increases. The line voltage in three levels and five levels inverter has less than 5% THD for modulation indices Ma > 0.5. The SVPWM is a popular for two level inverters and multilevel inverters [3], [10]. Most popular carrier based modulation strategies for two level and multilevel inverter are discussed [4], [5], [8]-[12]. In this paper the results with the DPWM1 are presented and compared with the SPWM and SVPWM on the basis of THD and rms value of the line voltage.

II. Multilevel Inverters

A. Three level Diode Clamped Inverter.

The power circuit of three level inverter is shown in Fig. 2(a). An m-level diode-clamp converter typically consists of (m – 1) capacitors on the DC bus and produce m levels of the phase voltage. The DC bus consists of two capacitors, (C1 and C2). For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/2$ and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/2$, through clamping diodes (D1 and D1').

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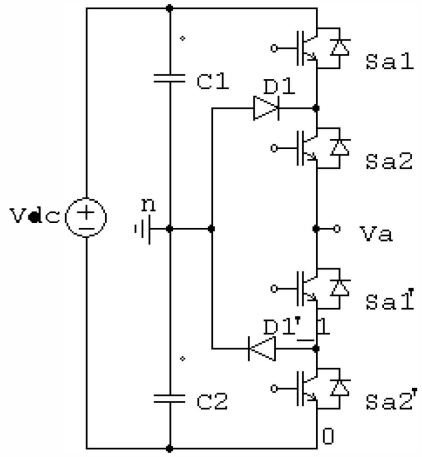
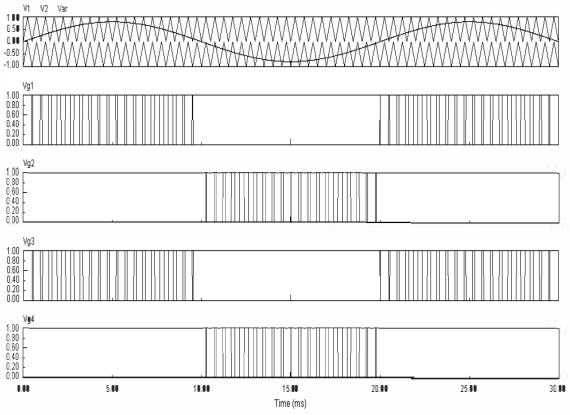
To explain how the staircase voltage is synthesized, the negative D.C. rail, '0', is considered as the output phase voltage reference point. Using the 3-level converter shown in Fig. 2 (a) as an example, there are three switch combinations to synthesize three level voltages across *a* and 0.

1) For voltage level Va0 = V_{dc}, turn on all upper switches, Sa1and Sa2.
2) For voltage level Va0 = $V_{dc}/2$, turn on one upper switch Sa2 and one lower switch Sa1'.
3) For voltage level Va0 = 0, turn on two lower switches Sa1' and Sa2'.



(a)



(b)

Fig. 2. (a) Diode Clamped Three-level inverter. (b) Modulation signal, carrier signal, Gate pulses generated with SPWM (M_a=0.8, f_s=2kHz) for Three-level inverter.

Table I lists the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and 0 means the switch is off. Each switch is switched once in a cycle. There exist two complimentary switch pairs in each phase. The complimentary switch pairs are (Sa1, Sa1') and (Sa2, Sa2'). Generation of PWM for three levels can be expressed as

$$V_{\chi n} = \begin{cases} V_{dc} & \text{for } V_{\chi r} > V_1 \\ 0 & \text{for } V_1 > V_{\chi r} > V_2 \\ -V_{dc} & \text{for } V_2 > V_{\chi r} \end{cases}$$

Where χ = a, b, c

Fig. 2. (b) Shows modulation signal, carrier signals and gate pulses generated with SPWM (M_a=0.8, f_s=2 kHz) for Three-level inverter.

B. Five level Diode Clamped Inverter.

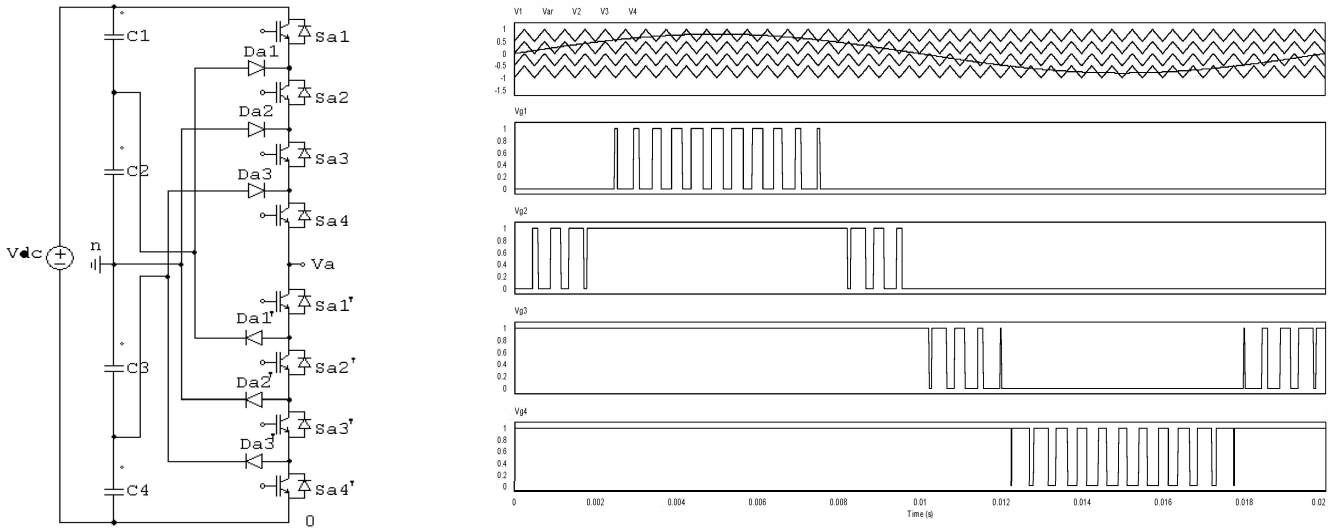
Five level inverter power circuit is shown in the Fig. 3(a). It consists of four D.C. link capacitors (C1, C2, C3 and C4). Voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes.

On the similar ground as that of three levels, the staircase voltage is synthesized as follows.

1) For voltage level Va0 = - V_{dc}, turn on all upper switches Sal through Sa4.
2) For voltage level Va0 = $3V_{dc}/4$, turn on three upper switches Sa2 through Sa4 and one lower switch Sa1'.
3) For voltage level Va0 = $V_{dc}/2$, turn on two upper switches Sa3 and Sa4 and two lower switches Sa1'and Sa2'.
4) For voltage level Va0 = $V_{dc}/4$, turn on one upper switches Sa4 and three lower switches Sal' through Sa3'.
5) For voltage level Va0 = 0, turn on all lower half switches Sa1' through Sa4'.

TABLE I
DIODE-CLAMPED THREE-LEVEL CONVERTER VOLTAGE LEVELS AND THEIR SWITCH STATES

Switch State				Output Voltage (Va0)	Output Voltage (Van)
Sa1	Sa2	Sa1'	Sa2'		
1	1	0	0	V_{dc}	$V_{dc}/2$
0	1	1	0	$V_{dc}/2$	0
0	0	1	1	0	$-V_{dc}/2$



(a) (b)

Fig. 3. (a) Diode Clamped Five-level inverter. (b) Modulation signal, carrier signal, Gate pulses generated with SPWM (M_a=0.8, f_s=2 kHz) for Five-level inverter.

Table II lists the voltage levels and their corresponding switch states. There exist four complimentary switch pairs in each phase the four complementary pairs are (Sal, Sa1'), (Sa2, Sa2'), (Sa3, Sa3') and (Sa4, Sa4'). Generation of PWM for Five level can be expressed as

$$V_{\chi n}= \begin{cases} V_{dc}/2 \text{ for } V_{\chi r} > V_1 \\ V_{dc}/4 \text{ for } V_1 > V_{\chi r} > V_2 \\ 0 \text{ for } V_2 > V_{\chi r} > V_3 \\ -V_{dc}/4 \text{ for } V_3 > V_{\chi r} > V_4 \\ -V_{dc}/2 \text{ for } V_{cr4} > V_{\chi r} \end{cases}$$

Where χ = a, b, c

Fig. 3 (b) shows modulation signal, carrier signal, Gate pulses generated with SPWM (M_a=0.8, f_s=2 kHz) for Five-level inverter.

TABLE II
DIODE-CLAMPED FIVE-LEVEL CONVERTER VOLTAGE LEVELS AND THEIR SWITCH STATES.

Switch State								Output Volt (Va0)	Output Volt (Van)
Sal	Sa2	Sa3	Sa4	Sa1'	Sa2'	Sa3'	Sa4'		
1	1	1	1	0	0	0	0	V_{dc}	$V_{dc}/2$
0	1	1	1	1	0	0	0	$3V_{dc}/4$	$V_{dc}/4$
0	0	1	1	1	1	0	0	$V_{dc}/4$	0
0	0	0	1	1	1	1	0	$V_{dc}/2$	$-V_{dc}/4$
0	0	0	0	1	1	1	1	0	$-V_{dc}/2$

Some important points to be noticed are as follows. Phase voltages have five levels and line voltage will have nine levels. There is no need to use any filter at output terminals. Blocking Voltage for the clamping diodes is very high ($3V_{dc}/4$, $V_{dc}/2$ and $V_{dc}/4$). Conduction period of each switch is different so rating of each switch is different. Each switch is controlled independently. The voltage across non-conducting switches is clamped by clamping diode and a string of series connected capacitors. This series capacitors string is shared by all the phase legs and usually serves as the dc bus or bulk capacitor. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. A proper method should be used to avoid capacitor voltage unbalance.

III. PULSE WIDTH MODULATION METHODS

A. SPWM (Sinusoidal Pulse Width Modulation)

This modulation signal consists of three sinusoidal signals displaced at mutually 120^0. This is now a very well known technique.

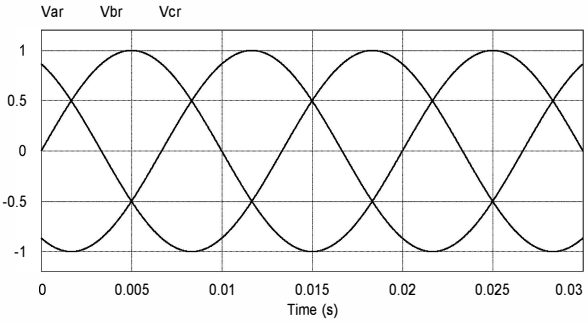


Fig. 4. Three phase sinusoidal pulse width modulation signal.

B. SVPWM (Space Vector Pulse Width Modulation)

To generate SVPWM modulation signal one of the three sinusoidal modulation waves, multiplied by a coefficient ½ of to generate the zero-sequence signal. Adding this signal to all the reference wave results in a modulation wave which is very similar to THIPWM modulation wave. The zero sequence signal is given by equation below,

$$\upsilon_o = 1/6.\ V_{am}.\ \mathrm{Sin}\ (3\omega t) \qquad (1)$$

Even though Zero sequence signals are being injected, in three phase scheme Zero sequence signal will not be present in the line voltages due to cancellation.

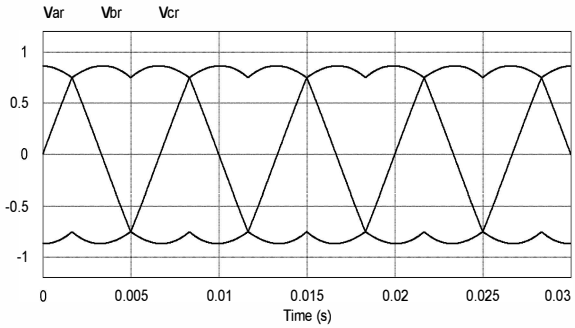


Fig. 5. Three phase space vector pulse width modulation signal.

C. DPWM1 (Depenbrock's Discontinuous Pulse Width Modulation)

Out of the three reference sinusoidal modulation waves, the one with the largest magnitude determines the zero sequence. The difference between the D.C.-bus rail with the same polarity as this modulation wave and the modulation wave is equal to the zero-sequence signal. The zero sequence signals are given by equation below.

$$\upsilon_0 = (\mathrm{sign}\ (\upsilon_a))\ Vdc/2 - \upsilon_a \qquad (2)$$

Adding such a zero sequence to the reference signals, is continuous modulation waves with two 60^0 saturated segments
results in a modulation signal called as DPWM1.

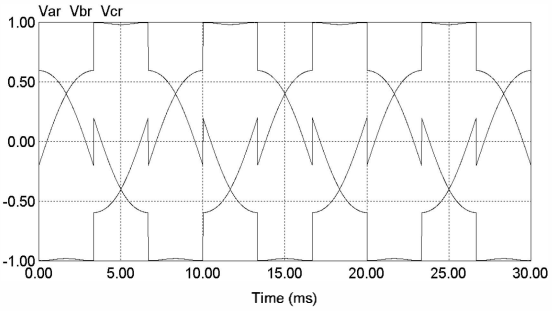


Fig. 6. Three phase Depenbrock's pulse width modulation signal.

IV. Simulation Results

These inverters are simulated using PSIM 9.0 software. The simulation parameters are as shown in the Table III. All the IGBTs and diodes used in the circuit are considered as ideal devices. When the frequency index m_f (ratio of carrier frequency to reference waveform frequency) is high, there are no substantial differences among the three carrier dispositions. This is because all the harmonics are shifted to high frequencies which can be easily filtered. The comparison becomes significant when m_f is not sufficient high. Total harmonic distortion is calculated at 50 Hz fundamental frequency. The rms value is calculated for the output line voltage which includes fundamental component and all other harmonic components.

The proposed DPWM1 can be easily implemented using analog circuit components. In some applications system cost can be reduced by using Digital Signal Processors (DSP). The proposed DPWM1 reduces switching losses at around unity power factor. Many more complex modulation signals can be generated using DSP and performance of three levels and five levels inverter can be enhanced.

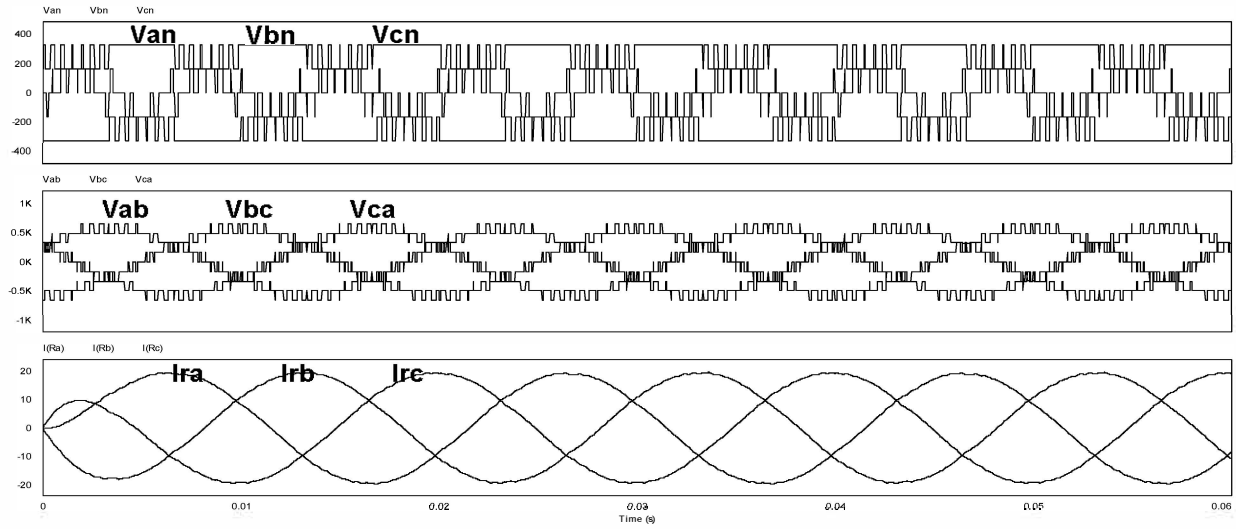


Fig. 7. Simulation wave forms (from top - Phase voltages, line voltages and line currents) with DPWM1 for five levels inverter. (M_a = 0.8, f_s=2 kHz, 3-phase star-connected load with power factor 0.8).

TABLE III
PARAMETERS OF SIMULATION

Parameter	Symbol	Value
DC Link voltage	V_{dc}	650 Volt
DC Link capacitors	C1, C2, C3, C4	2200 µF
Switching frequency	f_s	2 kHz
IGBTs	San	Ideal
Diodes	Dan	Ideal
Star connected three phase R-L load		
Load Resistance/phase	R_L	12 Ω
Load Inductance/phase	L	28.66 mH
Load Power Factor	cos Ø	0.8

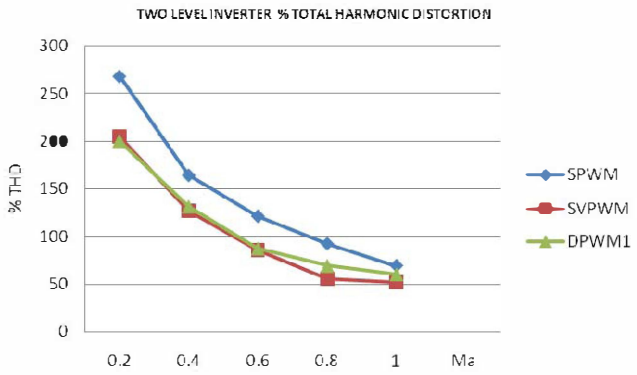


Fig. 8. % Total harmonic distortion as a fuction of modulation index for Two level inverter with SPWM, SVPWM and DPWM1.

Fig. 9. Normalised line voltage as a fuction of modulation index for Two level inverter with SPWM, SVPWM and DPWM1.

In the Fig. 8, it is observed that the THD is higher in SPWM as compred to SVPWM and DPWM1. The THD With SVPWM and DPWM1 methods are almost same for the range of Ma=0.2 to 0.6. The SVPWM fairs better for the range 0.6 to 1 range of modulation index over the DPWM1. The THD imrovement in SVPWM and DPWM1 is around 50% over the SPWM in two level inverter at Ma=1.

The rms value of output line voltage is normalized by DC bus voltage for two levels inverter in SPWM, SVPWM and DPWM1 is shown in Fig. 9. In case of SVPWM and DPWM1, there is a linear relation between output line voltage and modulation index in the range of Ma= 0.2 to 0.6. In the SVPWM and DPWM1 control technique the amplitude of fundamental output voltage is 15.5% more as compared to that of SPWM.

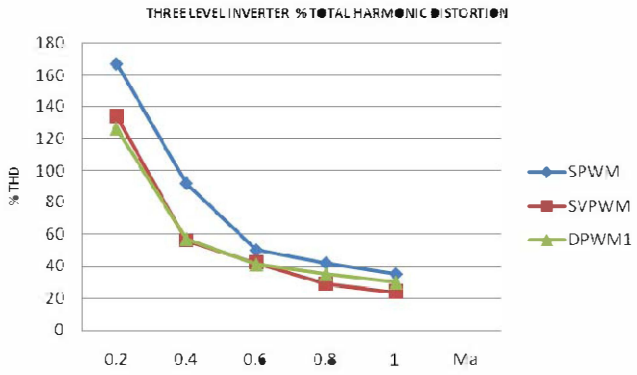


Fig. 10. % Total harmonic distortion as a fuction of modulation index for Three level inverter with SPWM, SVPWM and DPWM1.

The results presented in Fig. 10 for the total harmonic distortion gives similer picture as that of Fig. 8 when three modulation techniques are compared with each other with three level inverter. From Fig. 8 and Fig. 10 it is clear that total harmonic distortion in case of three level inverter is far better than two level inverter in all types of modulation signals used.

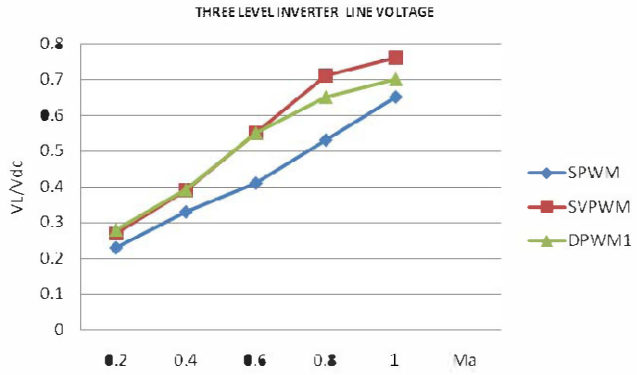


Fig. 11. Normalised line voltage as a fuction of modulation index for Three levels inverter with SPWM, SVPWM and DPWM1.

The rms value of output line voltage normalized by DC bus voltage for three levels inverter with SPWM, SVPWM and DPWM1 is shown in Fig. 11. The voltages with SVPWM and DPWM1 are almost same when modulation index is in the range of 0.2 to 0.6.When modulation index it is further increased the output voltage with SVPWM is more than DPWM1 and SPWM. With SVPWM output voltage increases linearly with modulation index up to Ma=0.8, with DPWM1 this linear relation is up to Ma=0.6.

Total harmonic distortion as a fuction of modulation index for Five level inverter with SPWM, SVPWM and DPWM1 is shown in the Fig. 12. When modulation index is between 0.2 to 0.6, THD with DPWM1 alost same as SVPWM. Near Ma=1 THD with SPWM and DPWM1 is same and with SVPWM is 5% less than others.

The rms value of output line voltage normalized by DC bus voltage for five levels inverter with SPWM, SVPWM and DPWM1 is shown in Fig. 13. Output voltages with SVPWM and DPWM1 are almost same when modulation index is 0.2 to 0.6 but when it is further increased the output voltage with SVPWM is more than DPWM1 and SPWM. With SVPWM output voltage increases linearly with modulation index up to Ma=0.8, with DPWM1 this linear relation is up to Ma=0.6. For particular modulation signal, modulation index, value of line voltage in less than that of three level inverter.

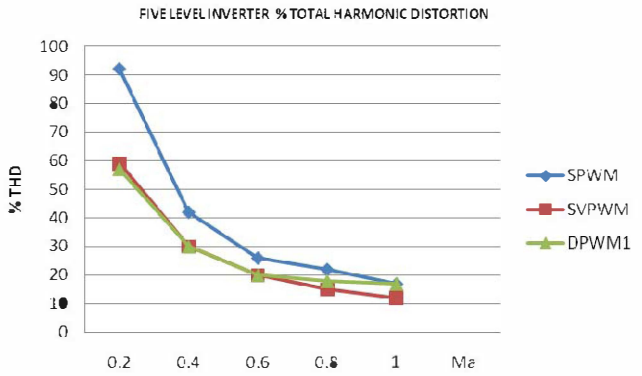


Fig. 12. % Total harmonic distortion as a fuction of modulation index for Five level inverter with SPWM, SVPWM and DPWM1.

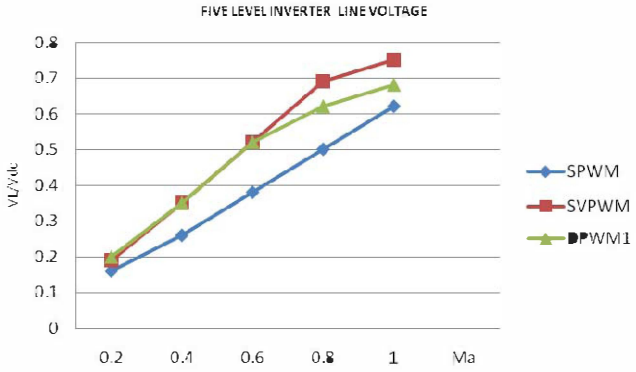


Fig. 13. Normalised line voltage as a fuction of modulation index for Five level inverter with SPWM, SVPWM and DPWM1.

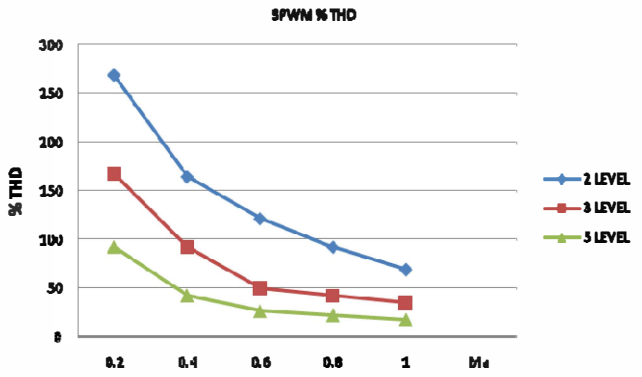


Fig. 14. % Total harmonic distortion as a fuction of modulation for two level, three level and five level inverter (SPWM).

THD as a function of modulation index is shown is shown in the Figs. 14, 15 and 16. From the figures it is clear that for any value of modulation, three level inverter THD is almost half as that of the two level inverter and five level THD is almost half as that of the three level.

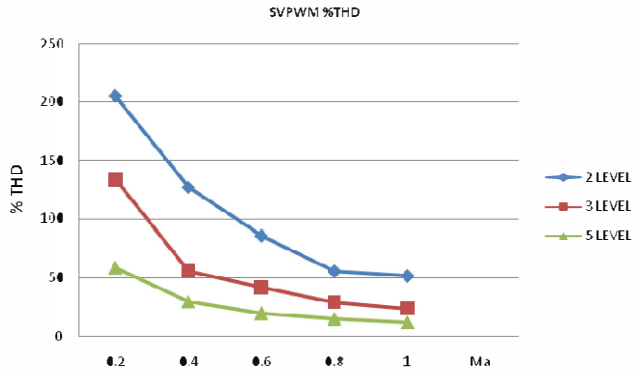


Fig. 15. % Total harmonic distortion as a fuction of modulation index for two level, three level and five level inverter (SVPWM).

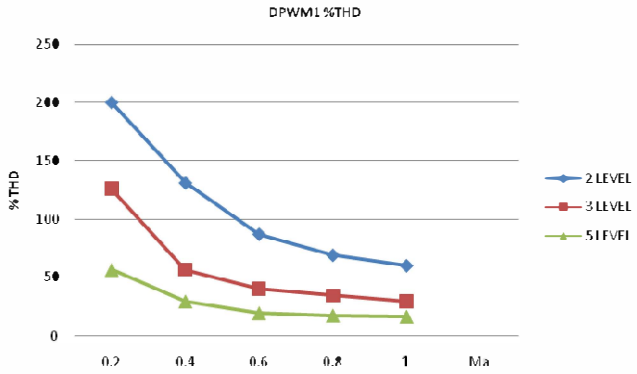


Fig. 16. % Total harmonic distortion as a fuction of modulation index for two level, three level and five level inverter (DPWM1).

From Fig.17, 18, 19 it is clear that two level inverter gives more output voltage than three level inverter and three level inverter gives slightly greater output than five level inverter. When modulation index, Ma=1, output with SVPWM and DPWM1 is almost same. For modulation index, Ma=0.2 to 0.4 three level inverter gives fairly more voltage than five level inverter.

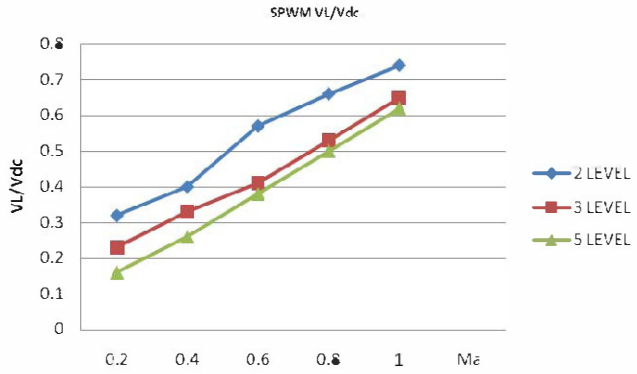


Fig. 17. Normalised line voltage as a fuction of modulation index for two level, three level and five level inverter(SPWM).

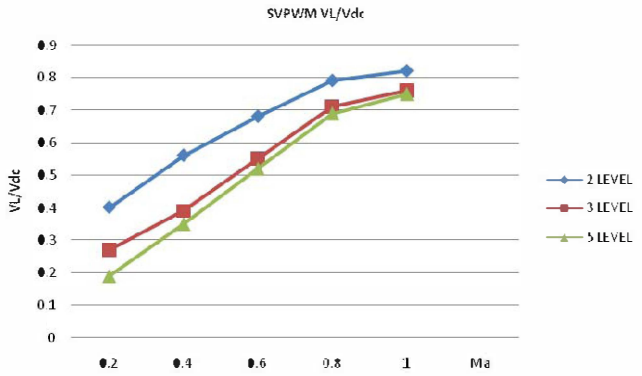


Fig. 18. Normalised line voltage as a fuction of modulation index for two level, three level and five level inverter(SVPWM).

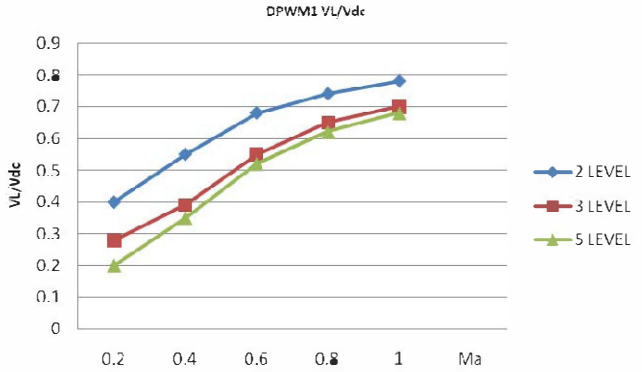


Fig. 19. Normalised line voltage as a fuction of modulation index for two level, three level and five level inverter(DPWM1).

V. Conclusion

The comparison between Two-level, Three-level and Five-level three phase inverter performance is carried out on the basis of parameters like THD and rms value of line voltage or DC bus voltage utilization. The basic control, generally employed for the inverters having SPWM with carrier based is compared with the modified SVPWM and DPWM1. The SVPWM control is observed to be a better with respect to other two control strategies. The THD in three level and five level inverters are 24% and 12% as compared to 52% in two level for a SVPWM control strategy. The results are presented with various values of modulation index under different control methods used in three level and five level inverters.

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