#### **CSE 331 – COMPUTER ORGANIZATION HOMEWORK 2 REPORT**

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# **REQUESTED:**

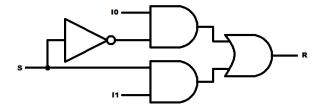
In this project, we are asked to design the same ALU as in the course notes. This ALU must support AND, OR, ADD, SUBTRACT and SET ON LESS THAN operations.

## **MODULES:**

First of all, I designed the mux module which is necessary for selection in 1 bit ALU. I need a 4x1 mux module. Firstly, I designed a 2x1 mux module to use when designing 4x1 mux module.

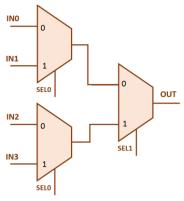
### 1.) Mux\_2:

This module is 2x1 MUX module. It takes 2 bits as input and 1 bit as select bits. Selects one of the input bits according to the select bit as output bit. In this module 2 AND, 1 OR, 1 NOT gates is used. The design is as follows:



### 2.) Mux\_4:

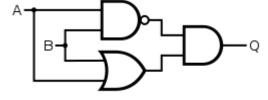
This module is 4x1 MUX module. It takes 4 bits as input and 2 bit as select bits. Selects one of the input bits according to the select bits as output bit. In this module 3 2x1 MUX modules is used. The design is as follows:



Then, I designed the xor module which is necessary in 1 bit ALU.

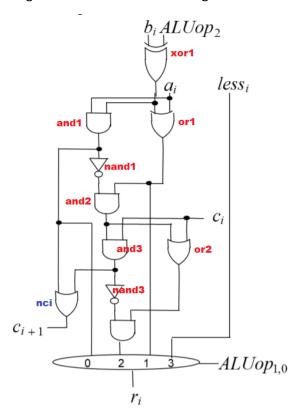
## 3.) Xor\_:

This module is XOR module. It takes 2 bits as input. After logic operations, xor result is given as output bit. In this module 2 AND, 1 OR, 1 NOT gates is used. The design is as follows:



## 4.) Alu\_1:

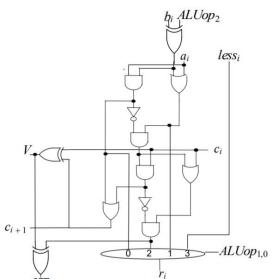
This module is 1 bit ALU module. This module is designed as given in the homework's pdf. This module takes 2 bits (as a and b), 3 bit opcode, carry bit, lessi bit as input. According to the opcode, the necessary logical operations are applied to these 2 bits (a and b) and result bit and carry bit are given as output. In this module 3 OR, 4 AND, 2 NOT gates is used. Also, in this module XOR\_ module and MUX\_4 module is used. This picture contains the names I used for the gates in the module. The design is as follows:



I needed a separate module for the set less than operation. For slt operation, we can find the result by giving the set bit of 32. bit as the less bit of the first bit. I needed this module to find the set bit of bit 32.

# 5.) Set\_alu\_1:

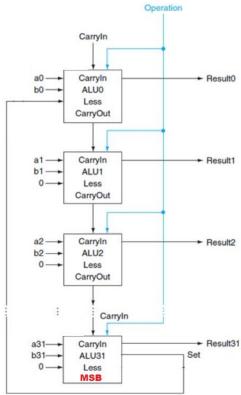
This module is 1 bit MSB ALU module. It will only be used for 32. bit. This module is designed as given in the lecture's slide. This module takes 2 bits (as a and b), 3 bit opcode, carry bit, lessi bit as input. According to the opcode, the necessary logical operations are applied to these 2 bits (a and b) and result bit, carry bit, SET bit are given as output. In this module 3 OR, 4 AND, 2 NOT gates is used. Also, in this module 2 XOR\_ module and MUX\_4 module is used. This picture contains the names I used for the gates in the module. The design is as follows:



For the SLT operation only the first bit is calculated and the other bits are 0. Therefore, the lessi bit is set to 0 when the alu modules are running. To find the lessi bit of the first module, the 32.bit 1 bit is executed in the msb module.

## 6.) Alu\_32:

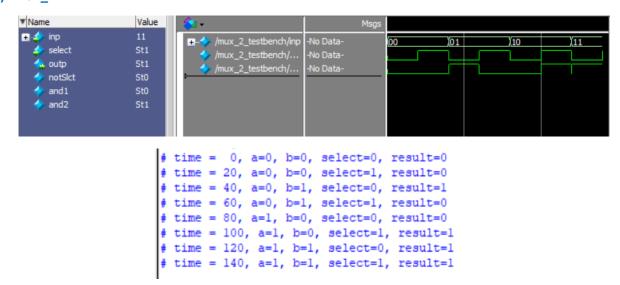
This module is 32 bit ALU module. This module takes 2 32-bit numbers (as a and b) and 3 bit opcode as input. It takes 2 32-bit numbers. According to the opcode given as input, logic operations are applied for these numbers and the output is given as 32-bit. First of all, if the opcode is 110, the initial value of carry in is set to 1, otherwise 0. Because these numbers are two's complement, the initial value of carry in must be 1 for subtraction. 1 bit alu module is executed for each bit in sequence. The carry bit of each bit is given as the carry in bit of the next bit. Unlike the other 31 bits, we run bit 32 in the module set\_alu\_1. Because we need to get the set bit from here. After receiving the set bit, we run the 1 bit alu module again for the first bit and give this set bit to as lessi bit of first module. This completes the 32-bit alu design. In this module 3 AND, 1 NOT gates is used. Also, in this module XOR\_ module and 32 ALU\_1 modules and 1 SET\_ALU\_1 module is used. The design is as follows:



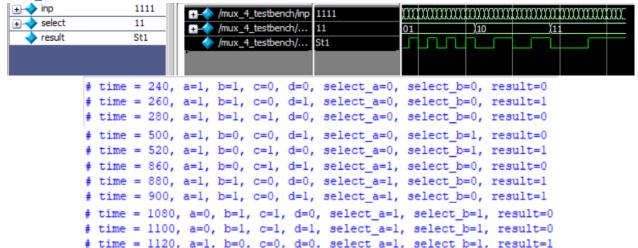
#### **TEST BENCHS:**

I added a screen shoot of only a short part of the outputs on the test bench. You can see the full part of test benches on ModelSim.

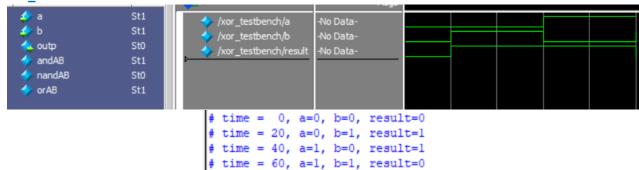
## 1.) Mux\_2:







# 3.) Xor\_:



# 4.) Alu\_1:



### 5.) Set\_alu\_1:

				/SEL_all	u_1_testb	CHILL								
-	b		1		u_1_testb								币	
-	d	1		<pre>/set_ali</pre>	u_1_testb	en 1								
-	lessi	1		/set_al	u_1_testb	en 1			Πī	$\overline{\mathbf{M}}$	mmm	MMM	MM	$\overline{\mathbf{u}}$
<u>+</u> -	opCode		11 +	⊢� /set_alı	u_1_testb	en 11	1		0	10	(110	(11)		
-	result		t1	/set_ali			1						MMM	M
- 9	nci		t1	<pre>/set_ali</pre>	u_1_testb	en St	1							
-	set	S	t0	<pre>/set_al</pre>	u_1_testb	en Sto	)			┸┸				$\Box$
a=0,	b=0, ci=1,	lessi=1,	opCode=000,	result=0,	ci+l=0,	set=0	# a=1,	b=1,	ci=0,	lessi=0,	opCode=010,	result=0,	ci+l=1,	set=
a=0,	b=1, ci=0,	lessi=0,	opCode=000,	result=0,	ci+l=0,	set=1	# # a=1,	b=1,	ci=0,	lessi=1,	opCode=010,	result=0,	ci+l=1,	set=
					-4.1						opCode=110,			
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- 0	N-1 -4-1	1			-4.1-1	0	# # a=0,	b=1,	ci=1,	lessi=1,	opCode=110,	result=1,	ci+l=0,	set=
a=0,	D=1, C1=1,	lessi=1,	opCode=000,	result=0,	C1+1=1,	set=U	#							
a=1,	b=0, ci=0,	lessi=0,	opCode=000,	result=0,	ci+l=0,	set=1	# a=1,	b=0,	ci=0,	lessi=0,	opCode=110,	result=0,	ci+l=1,	set=
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							#							
a=1,	D=0, C1=1,	lessi=0,	opCode=001,	result=1,	C1+1=1,	set=U	# a=1, #	b=0,	ci=1,	lessi=0,	opCode=110,	result=1,	ci+l=1,	set=
a=1,	b=0, ci=1,	lessi=1,	opCode=001,	result=1,	ci+l=1,	set=0	* # a=1,	b=0,	ci=1,	lessi=1,	opCode=110,	result=1,	ci+l=1,	set=
							a=0,	b=1,	ci=1,	lessi=0,	opCode=111,	result=0,	ci+l=0,	set=
a=1,	b=1, c1=0,	lessi=0,	opCode=001,	result=1,	c1+1=1,	set=1	•							
a=1,	b=1, ci=0,	lessi=1,	opCode=001,	result=1,	ci+l=1,	set=1	a=0,	b=1,	ci=1,	lessi=1,	opCode=111,	result=1,	ci+l=0,	set=
							a=1,	b=0,	ci=0,	lessi=0,	opCode=111,	result=0,	ci+l=l,	set=
a=1,	b=1, ci=1,	lessi=0,	opCode=001,	result=1,	ci+l=l,	set=l	•							
a=1,	b=1, ci=1,	lessi=1,	opCode=001,	result=1,	ci+l=1,	set=1	a=1,	b=0,	ci=0,	lessi=1,	opCode=111,	result=1,	ci+l=l,	set=
							a=1.	b=0.	ci=1.	lessi=0.	opCode=111,	result=0.	ci+l=1.	set=
a=0,	b=0, ci=0,	lessi=0,	opCode=010,	result=0,	ci+l=0,	set=0	•							
a=0,	b=0, ci=0,	lessi=1,	opCode=010,	result=0,	ci+l=0,	set=0	a=1,	b=0,	ci=1,	lessi=1,	opCode=111,	result=1,	ci+l=1,	set=
			opCode=010,	-		•	F ≜ a=1.	b=1.	ci=0.	lessi=0.	opCode=111,	result=0.	ci+1=0.	set=
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a=1,	b=0, ci=1,	lessi=0,	opCode=010,	result=0,	ci+l=l,	set=0 #	a=1,	b=1,	ci=0,	lessi=1,	opCode=111,	result=1,	ci+l=0,	set=

## 6.) Alu\_32:



# a = 10110011100100011011000001000100, decimal a=-1282297788, b = 0010110011100101101101100100110, decimal b= 753120834. OPCODE = 000, result = 0010000010000001011000001000000, decimal result= 545370176 a = 000100111100101100000100011011, decimal a= 332072043, b = 101011001001001010101010101010101010, decimal b=-1399671462, OPCODE = 000, result = 0000000010000010000010010, decimal result= 8520778 a = 001011110001010000011001101101, decimal a= 789846454, b = 0011101101111101011111100011111110, decimal b= 1002305790, OPCODE = 000, result = 001010110001010000011001101101, decimal result= 722737334 a = 000100111100101100001000110111, decimal a= 332072043, b = 101011001001010101010101010101010101, decimal b=-1399671462, OPCODE = 001, result = 101111111101101101101110111011, decimal result=-1076120197 a = 000100111100101100000100110111, decimal a= 332072043, b = 101011001001010101010101010101010. decimal b=-1399671462. OPCODE = 010. result = 1100000001011101110111100111001110. decimal result=-1067599419 a = 00101111000101000001100110110110, decimal a= 789846454, b = 001110111011111011111100011111110, decimal b= 1002305790, OPCODE = 010, result = 0110101011010010000100101010100, decimal result= 1792152244 11100100101111001101010101000010, decimal a= -457386686, b = 10101001001010101010101101010101, decimal b=-1456299063, OPCODE = 010, result = 10001101111011110111101111001100001011, decimal result=-1913685749 1011001110010001101100000100010, decimal a=-1282297788, b = 0010110011101011010110101000010, decimal b= 753120834, OPCODE = 110, result = 10000110101111111101000000010, decimal result=-2035418622 a = 0001001111001011000010001101011, decimal a= 332072043, b = 10101100100100101011010101010101010, decimal b=-1399671462, OPCODE = 110, result = 011001110011100011010010111100010001, decimal result= 1731743505 a = 00101111000101000001100110110, decimal a= 789846454, b = 001110111011111100011111110, decimal b= 1002305790, OPCODE = 110, result = 111100110101101101010100000010111000, decimal result= -212459336 a = 11100100101111001101010101000010, decimal a= -457386886, b = 101010010011001010110010101, decimal b=-1456299063, OPCODE = 110, result = 001110111000101001010111001, decimal result= 998912377 = 01011101011011011011111000101100101, decimal a= 1566962018, b = 001001001111011011101110111, decimal b= 619861739, OPCODE = 110, result = 00111000011100111011101110111, decimal result= 947100279 a = 1110010010111100110101010101000010, decimal a= -457386686, b = 1010100100101010101010101010101, decimal b=-1456299063, OPCODE = 111, result = 0000000000000000000000000000000, decimal result=